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INST 125
20FEB2018

Three Stage Signal Amplifier

Introduction:

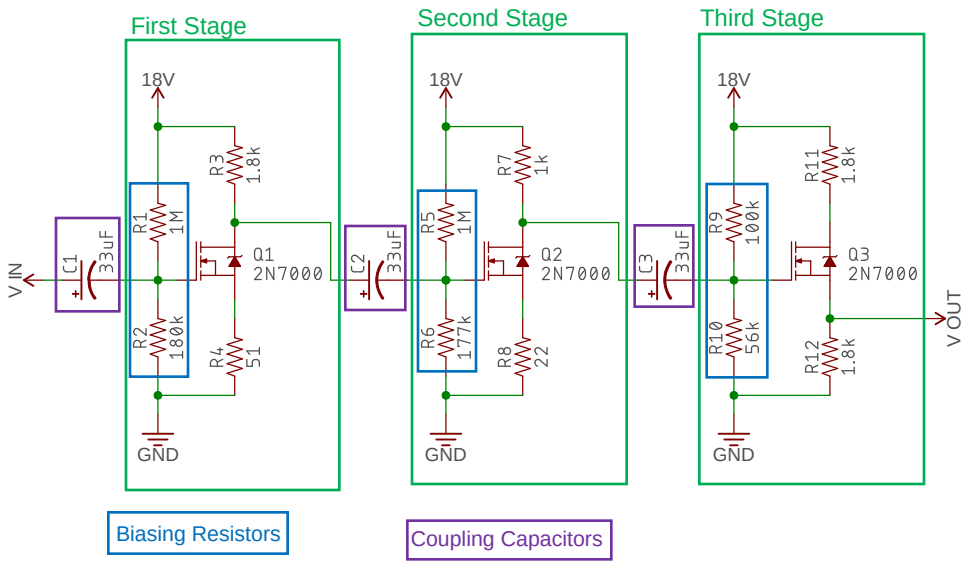
Our project this class was to build and test a three stage signal amplifier with a voltage gain of at least three hundred. This report details and diagrams the finished circuit and its operation.

Contents:

Objectives:

Design, assemble, and troubleshoot a three stage signal amplifier.
This amplifier should:

- Have a voltage gain of at least three hundred
- Produce an output signal without distortion
- Earn a high grade on this project



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Circuit Description:

The Coupling Capacitors block DC current from traveling between the circuits they are coupling, while still allowing the AC signal to pass through. There are three of them in this amplifier, two coupling amplfier stages together, and one coupling the input signal to the first stage. They are sized so that their impedance is =< 1 ohm.

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a voltage controlled transistor that acts as a good amplifier when the current through the transistor is only significantly affected by the voltage applied to the transistor's gate, and not significantly affected by the voltage across the transistor. The region where this occurs is know as the transistor's Active Region.

The DC Biasing Resistors in each stage form voltage dividers that bias the transistors' gates. They are sized such that the transistors remain in their active regions over the entire input signal waveform for their stage. Since the MOSFETs have an insulated gate and no gate current, the input impedance of each stage is the parallel equivalent of its two biasing resistors. While their size ratio must be maintained, the sizes of the biasing resistors can be increased to extremely large values. Increasing the biasing resistors also increases the RC time constant for the coupling capacitors, which increases the start-up time till the amplifier reaches its quiescent state and is ready to amplify.

Up to this point, all three stages had similar constructions and could be discussed together, that changes with the stage configurations and the selection of drain and source resistors. The first two stages are in a common-source configuration, and their drain and source resistors are selected to give them similar gains. The gain of a common-source amplifier can be calculated with the equation $A_v = gm \cdot R_D / (gm \cdot R_S + 1)$, where R_D is the Drain Resistor, R_S is the Source Resistor and gm is the MOSFET's Trans-Conductance. For both stages gain could be increased by shorting or bypassing the source resistors, however taking the source resistor out of the equation results in the MOSFETs' trans-conductance being a significant factor in determining its gain. With MOSFETs, like most FETs, the trans-conductance can be unstable and unpredictable, not desirable qualities for an amplifier's gain.

The third stage is in a common-drain configuration, whose gain is approximately one regardless of the values of the drain and source resistors. Typically in a common-drain amplifier the drain resistor is omitted, however, doing so resulted in an unstable output signal in this case. Both resistors were sized so that the output was stable, and that the output impedance is low.

Testing Results:

Input Signal:	10 mV
First Stage Output:	210 mV
First Stage Gain:	21
Second Stage Output:	4.4 V
Second Stage Gain:	21
Third Stage Output:	4.2 V
Third Stage Gain:	0.95
Total Gain:	420

Conclusion:

In the end the amplifier produced a distortion free output signal that was more than three hundred time greater than the input signal. It will likely produce a high grade for the course.

Event Log:

30 JAN – 2FEB	Amplifier research
3FEB – 5FEB	MOSFET amplifier research
5FEB – 8FEB	Amplifier Design
8FEB – 14FEB	Amplifier construction and troubleshooting
20FEB	Project Write-up

Parts/Costs List:

Resistors		Kit
Capacitors		Kit
Breadboard		Kit
2n7000 MOSFETs	(x3)	$0.60/$1.80

2N7000G

Small Signal MOSFET 200 mAmps, 60 Volts

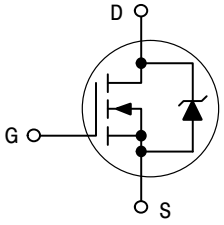
N−Channel TO−92

ON Semiconductor®

http://onsemi.com

200 mAMPS
60 VOLTS
$R_{DS(on)}$ = 5 Ω

N−Channel



Features

- AEC Qualified
- PPAP Capable
- This is a Pb−Free Device*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain Source Voltage	V_{DSS}	60	Vdc
Drain−Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate−Source Voltage − Continuous − Non−repetitive ($t_p \le 50$ μs)	 V_{GS} V_{GSM}	 ±20 ±40	 Vdc Vpk
Drain Current − Continuous − Pulsed	 I_D I_{DM}	 200 500	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

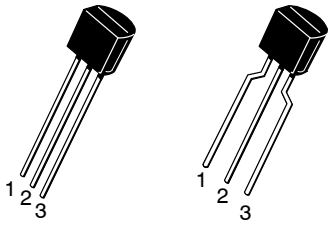
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	357	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/16″ from case for 10 seconds	T_L	300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

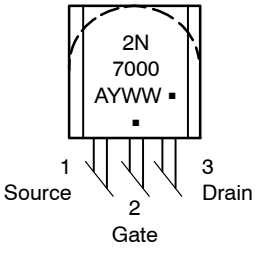
TO−92
CASE 29
STYLE 22



STRAIGHT LEAD
BULK PACK

BENT LEAD
TAPE & REEL
AMMO PACK

MARKING DIAGRAM AND PIN ASSIGNMENT



A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain−Source Breakdown Voltage	(V_{GS} = 0, I_D = 10 μAdc)	$V_{(BR)DSS}$	60	–	Vdc
Zero Gate Voltage Drain Current		I_{DSS}			
	(V_{DS} = 48 Vdc, V_{GS} = 0)		–	1.0	μAdc
	(V_{DS} = 48 Vdc, V_{GS} = 0, T_J = 125°C)		–	1.0	mAdc
Gate−Body Leakage Current, Forward	(V_{GSF} = 15 Vdc, V_{DS} = 0)	I_{GSSF}	–	−10	nAdc
ON CHARACTERISTICS (Note 1)					
Gate Threshold Voltage	(V_{DS} = V_{GS}, I_D = 1.0 mAdc)	$V_{GS(th)}$	0.8	3.0	Vdc
Static Drain−Source On−Resistance		$r_{DS(on)}$			Ω
	(V_{GS} = 10 Vdc, I_D = 0.5 Adc)		–	5.0	
	(V_{GS} = 4.5 Vdc, I_D = 75 mAdc)		–	6.0	
Drain−Source On−Voltage		$V_{DS(on)}$			Vdc
	(V_{GS} = 10 Vdc, I_D = 0.5 Adc)		–	2.5	
	(V_{GS} = 4.5 Vdc, I_D = 75 mAdc)		–	0.45	
On−State Drain Current	(V_{GS} = 4.5 Vdc, V_{DS} = 10 Vdc)	$I_{d(on)}$	75	–	mAdc
Forward Transconductance	(V_{DS} = 10 Vdc, I_D = 200 mAdc)	g_{fs}	100	–	μmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	–	60	pF
Output Capacitance		C_{oss}	–	25	
Reverse Transfer Capacitance		C_{rss}	–	5.0	
SWITCHING CHARACTERISTICS (Note 1)					
Turn−On Delay Time	(V_{DD} = 15 V, I_D = 500 mA, R_G = 25 Ω, R_L = 30 Ω, V_{gen} = 10 V)	t_{on}	–	10	ns
Turn−Off Delay Time		t_{off}	–	10	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ORDERING INFORMATION

Device	Package	Shipping†
2N7000G	TO−92 (Pb−Free)	1000 Units / Bulk
2N7000RLRAG	TO−92 (Pb−Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

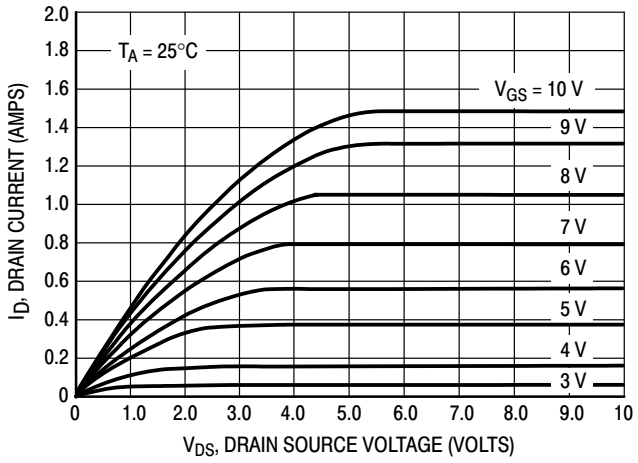


Figure 1. Ohmic Region

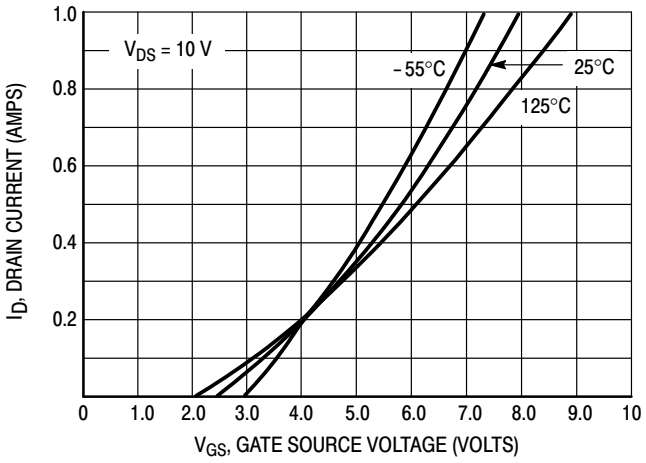


Figure 2. Transfer Characteristics

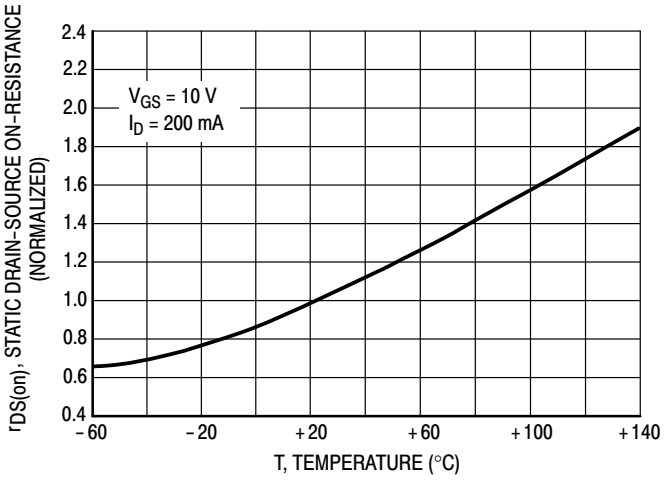


Figure 3. Temperature versus Static Drain−Source On−Resistance

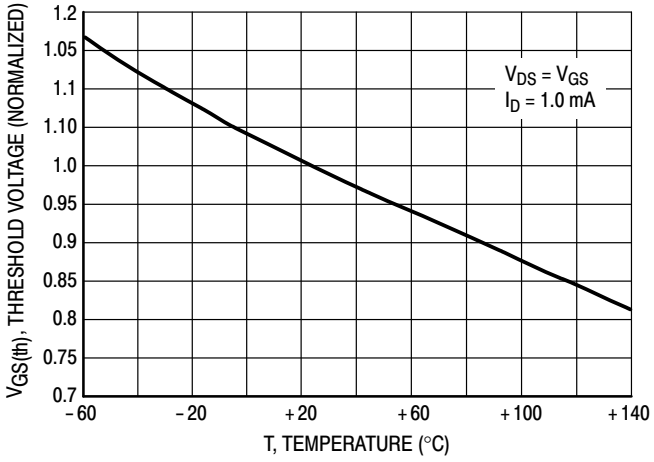


Figure 4. Temperature versus Gate Threshold Voltage