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A New Insulator for Thin-Film Transistor Backplanes and for Flexible Passivation Layers

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We describe a new flexible material that functions as a gate dielectric of amorphous-silicon thin-film transistors, as a passivation layer for plastic substrates, and as an environmental barrier for organic light-emitting diodes. The material is SiO_2 with some silicone polymer character. It is deposited, typically at room temperature, from a glow discharge in which a silicone precursor molecule, hexamethyl disiloxane, is oxidized. Films of the material can be made with a broad range of properties, which vary from those of SiO_2 to those of plasma-polymerized silicone. Many macroscopic properties of these films suggest that they are homogeneous. We call the films "hybrid."

I. Introduction

Active-matrix organic light-emitting diode (AMOLED) displays will become the dominant technology for the next generation of flexible displays, due to their light weight and flexibility. Each pixel of an AMOLED needs a thin-film transistor (TFT) to drive the OLED. The large experience and manufacturing base of a-Si:H TFTs make their upgrade to AMOLED displays very desirable. AMOLED displays require diving TFTs that can source enough current to the OLED and must be stable enough for an OLED brightness half-life of 10 years. The TFT stability at low gate electric fields has been extended to a projected drive-current half-life of 1,000 years, by modifying the a-Si:H process [1], [2].The TFT stability at high gate fields has been raised by modifying the SiN_x gate dielectric [3, 4]. A new gate dielectric material also has been found to be particularly stable against threshold voltage shift at high gate fields [5]. However, conventional a-Si:H/SiN_x TFTs have electron field-effect mobility μ of ≤1 $cm^2/V{\cdot}s$ [6]. Moreover, the deposition temperature of high quality SiN_x is over 250 ^oC, which limits its use to special plastic substrates [7]. We advance the art by introducing a new SiO_2-silicone hybrid gate dielectric deposited at room temperature for a-Si:H TFTs that raises the electron field-effect mobility μ_e to ~ 2.0 $cm^2/V{\cdot}s$ and the hole field-effect mobility μ_h to 0.1 $cm^2/V{\cdot}s$ [8].

We also are seeking to raise the flexibility of a-Si:H TFTs for use in roll-out displays. The failure of TFTs under mechanical strain depends on the stiffness of the materials used in a-Si:H TFTs, especially the dielectric material because it covers most of the foil substrate. The conventional dielectric material used in a-Si:H TFTs is brittle SiN_x, which limits the maximum applied tensile strain of a-Si:H TFTs to ~0.5% [9]. When the new, flexible SiO_2-silicone hybrid material replaces the brittle $SiN_x$the a-Si:H TFTs remain functional up to a tensile strain of 5% [10].

The resilient hybrid dielectric is deposited at nominal room temperature by plasma-enhance chemical vapor deposition (PE-CVD) from a gaseous mixture of hexamethyl disiloxane (HMDSO) and O_2. As the HMDSO/O_2 flow ratio and the power of the plasma-exciting radio frequency (rf) 13.56 MHz are varied, films are deposited with a range of properties. The properties of the hybrid films lie between those of thermal oxide and plasma-polymerized HMDSO [11].

II. Experiments

We first describe the deposition of the hybrid material, then the evaluation of its electrical and mechanical properties, and finally the fabrication of a-Si:H thin film transistors (TFTs) that use the hybrid as gate dielectric. HMDSO vapor and O_2 gas are fed into a single-chamber PE-CVD system. The liquid HMDSO source is kept at 33ºC, where the HMDSO vapor pressure is 70 Torr (9,200 Pa). The flow rates of the HMDSO vapor through heated lines, and of the oxygen gas, into a plenum in the PE-CVD chamber are metered with mass flow controllers. The stainless steel plenum is covered with a stainless steel diffuser grid and forms the bottom grounded, electrode for the capacitive glow discharge. On it rests a glass ring that confines the gas, and functions as a stand-off insulator for the radio-frequency powered (RF, 13.56 MHz) stainless steel screen electrode. The substrates are held on a copper holder of 450 cm^2 surface area, which is grounded and forms a third, top, electrode that faces down into the discharge. Substrates of silicon wafer, glass slide or polyimide foil are kept at nominal room temperature.

The electrical properties of the hybrid were calculated from measurements on the capacitor structures prepared on a p-type Si wafer, as shown in Fig. 1. The p-type Si wafer had a resistivity of 0.01-0.09 Ω·cm, diameter of 2 inch, and thickness of 280 µm. The capacitance was measured in accumulation on 0.01 cm^2 Cr dots / ~100 nm thick hybrid layer / *p*-type Si structures at 1 MHz frequency with an HP 4275A LCR meter. The leakage current and breakdown field were measured with an HP 4155A parameter analyzer. The critical tensile strain of the hybrid was measured on a sample that had a 0.6 µm thick layer deposited on a 50 µm thick polyimide foil substrate. This sample was bent successively over the shafts of drill bits with decreasing radii for 1 minute each, and then inspected for cracks under an optical microscope.

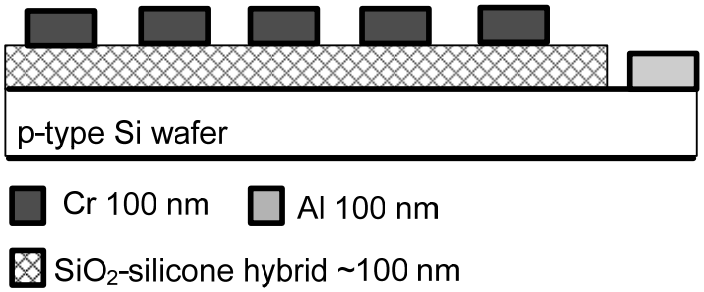

Figure 1 Schematic cross section of hybrid capacitor structure on

a-Si:H TFT with the hybrid gate dielectric were fabricated in the conventional inverted-staggered back channel-cut geometry. The TFT cross sections, layer thicknesses, and process temperatures are shown in Fig. 2(a) on Corning 1737 glass and Fig. 2(b) on 50-µm DuPont Kapton E polyimide foil. Standard Corning 1737 glass substrates were passivated with a layer of SiN_x deposited by plasma-enhanced chemical vapor deposition

(PE-CVD), while the polyimide foils were coated first with a 15-nm SiN_x adhesion layer and then 300-nm hybrid. Then Cr or Cr/Al/Cr metal was thermally evaporated and patterned with mask 1 to form the gate electrodes. Next, the hybrid gate dielectric was deposited at room temperature in a single-chamber PE-CVD system. After this deposition step the sample was transferred in air to a four-chamber PE-CVD system for deposition of the *i* a-Si:H channel layer and the highly-*n* doped a-Si:H source/drain (S/D) layers. Finally, Cr or Cr/Al/Cr was thermally evaporated and wet-etched to form the S/D electrodes (mask 2). These patterned S/D electrodes served as mask for the dry etching of the n^+ layer. The a-Si:H islands were patterned (mask 3) to separate the devices. Finally gate vias were opened (mask 4) to the gate electrodes.

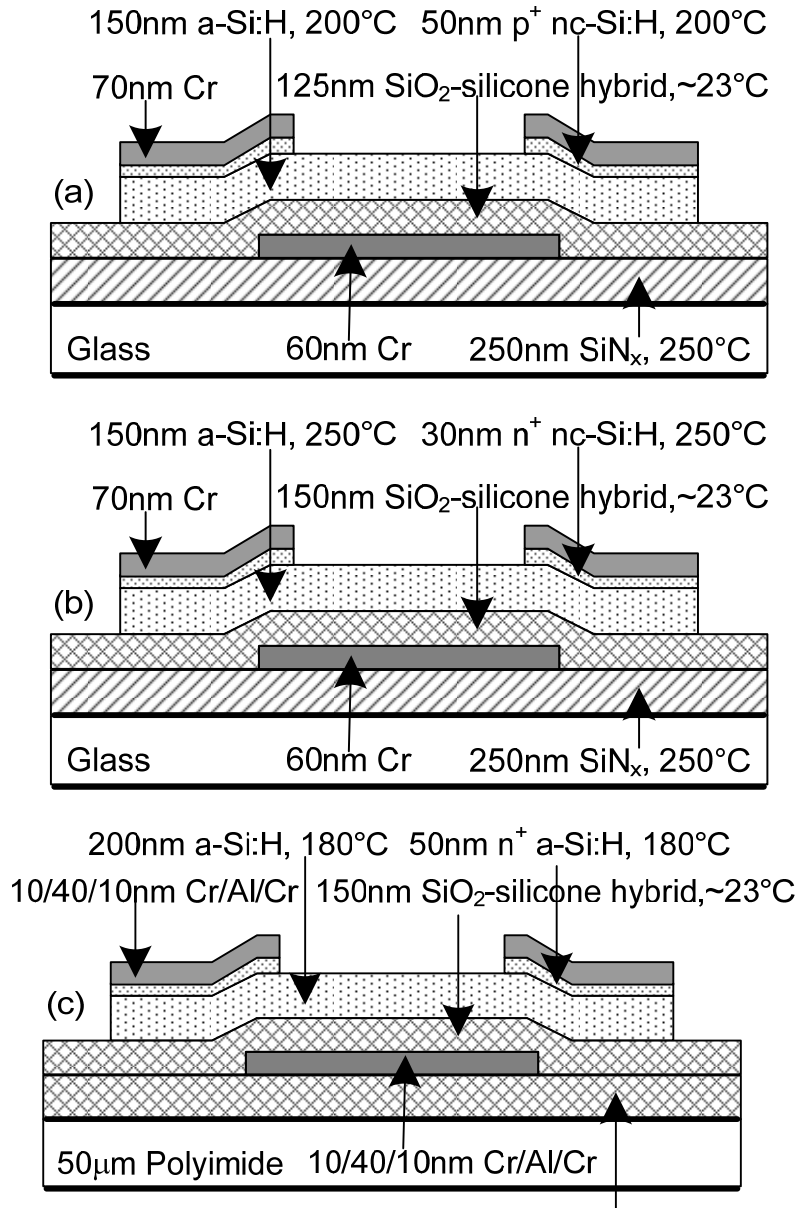

Figure 2 Schematic cross sections of (a) n-type and (b) p-type TFT on glass, and (c) n-type TFT on polyimide foil. The figures describe substrate and layer materials, thickness, and deposition temperature. (From ref. 8 and 10)Si wafer

III. Properties of the hybrid

The relative dielectric constant of the layer deposited at the highest oxygen flow rate is 3.9, equal to the value of SiO_2 grown by thermal oxidation of Si. As the oxygen flow rate is reduced the dielectric constant first rises to about 4.5 and then falls to 2 (Fig. 3a). The same range of dielectric constant is covered when the RF deposition power is varied, from a value of 2 at the low end to a value of about 4.5 at the high end of the power range (Fig. 3b).

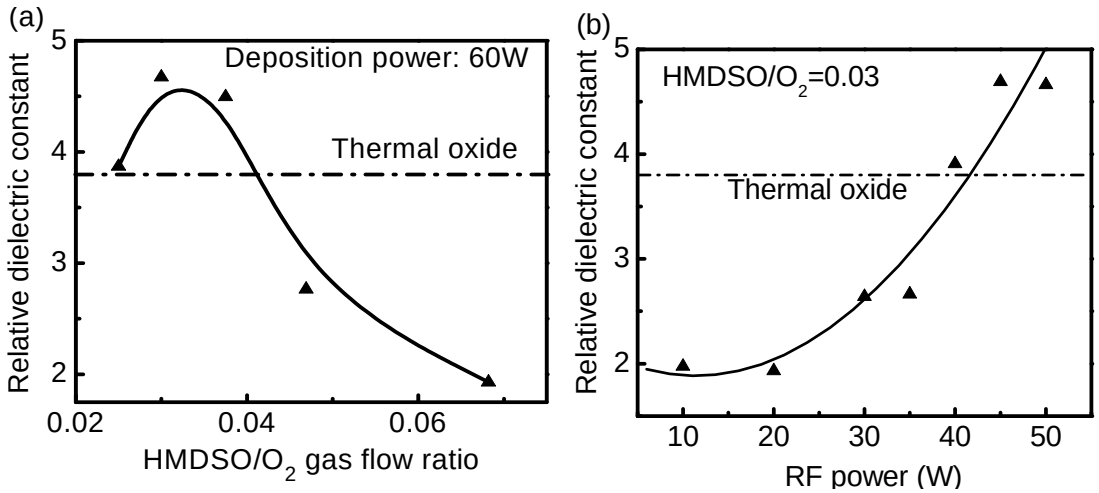

Figure 3 Dielectric constants of hybrid in function of (a) $HMDSO/O_2$ flow ratio and of (b) RF deposition power. (From ref. 11)

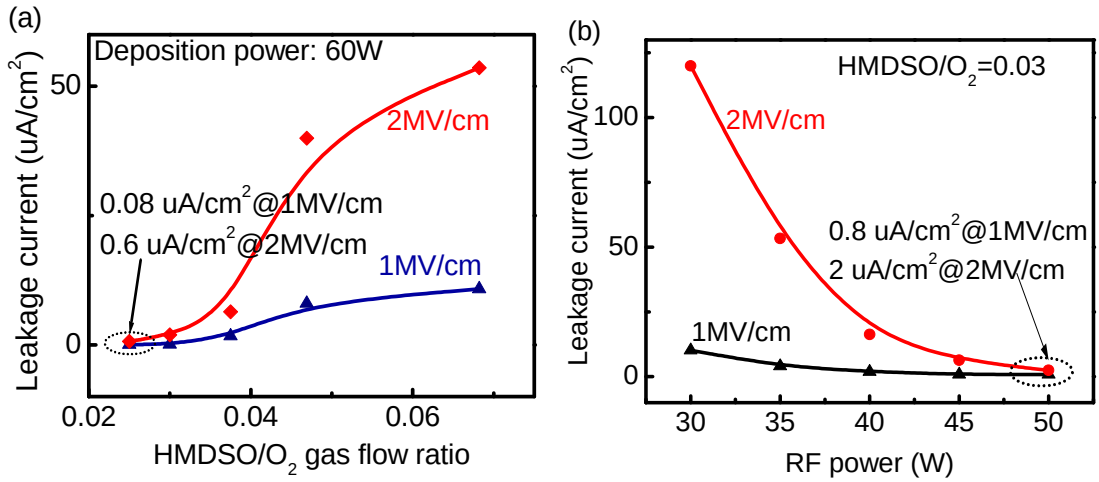

Figure 4 Current densities through Cr (+) / ~100 nm hybrid layer / *p*-type Si structures measured at electric field strengths of 1 and 2 MV/cm, in function of (a) $HMDSO/O_2$ flow ratio and of (b) RF deposition power. (From ref. 11)

The leakage current densities through the Cr (positive electrode) / 100-nm hybrid layer / *p*-type Si (ground) structures are shown in Fig. 4a and Fig. 4b. Over the range of $HMDSO/O_2$ flow ratios the leakage current at the electrical field of 1 MV/cm rises from 0.08 $\mu A/cm^2$ at high O_2 flow to ~10 $\mu A/cm^2$ at low O_2 flow. The leakage current drops from 15 $\mu A/cm^2$ at low power to 0.8 $\mu A/cm$ at high power. Figure 5a and Fig. 5b show the breakdown field strength. At dielectric breakdown the current in all layers rose sharply, with only a small spread between the breakdown voltages of layers made at any

given set of PE-CVD conditions. The lowest breakdown field is about 5MV/cm in layers deposited at high HMDSO/O_2 ratio and low RF power. Raising the O_2 flow brings the breakdown field strength to above 8 MV/cm (Fig. 5a). Raising the RF power also raises the breakdown field (Fig. 5b).

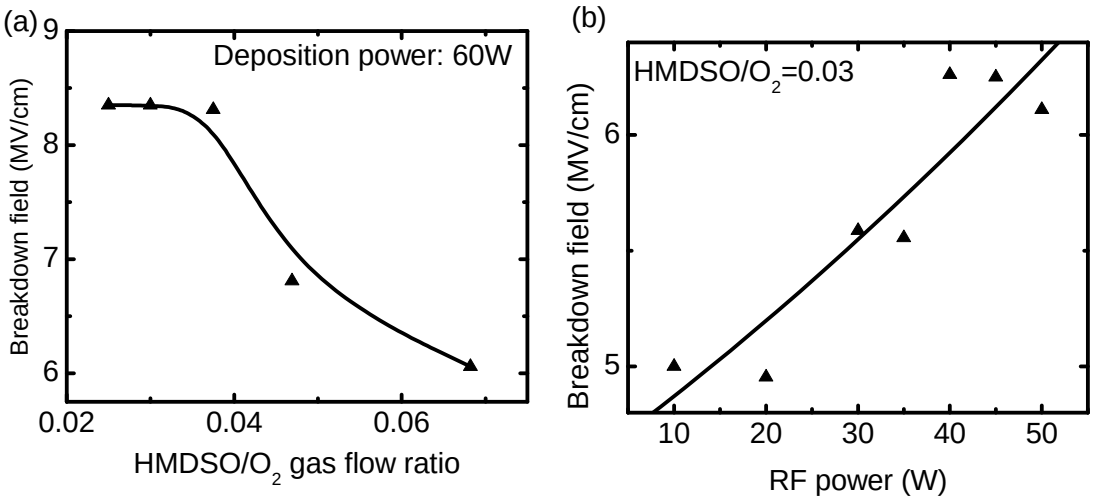

Figure 5 Dielectric breakdown strength of the capacitors measured in (a) Fig. 4a, and in (b) Fig. 4b. (From ref. 11)

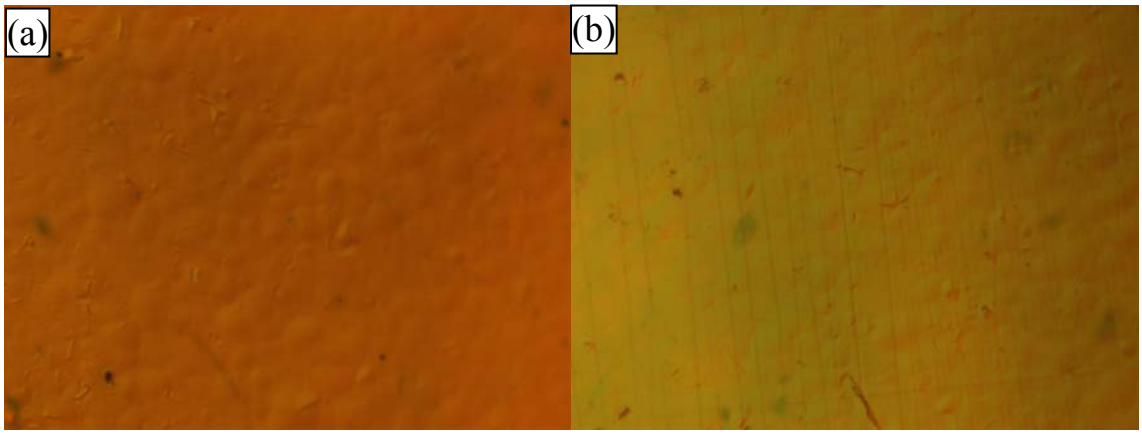

Figure 6 (a) Optical micrograph of 600 nm thick hybrid film deposited on 50-µm thick polyimide film before bending, and (b) after bending to tensile strain of 3.3%

Figure 6a is an optical micrograph of a 600-nm thick hybrid layer deposited at HMDSO/O_2 = 0.035 and 70 W RF power on polyimide foil before bending, and Fig. 6b is the micrograph after outward bending to a radius of curvature of 0.75 mm, which produced a tensile strain of 3.3% in the hybrid layer. Fig. 6b shows cracks in the layer that run parallel to the axis of bending.

IV. Hole and electron field-effect mobilities in a-Si:H TFTs

The TFT I_{DS}-V_{GS} transfer characteristics and I_{DS}-V_{DS} output characteristics are measured with an HP 4155A parameter analyzer. For the transfer characteristics V_{GS} is swept from -30 to 0 V at V_{DS} of -10 V (*p*-channel), and V_{GS} from +20 to -10 V at V_{DS} of +0.1 V or +10 V (*n*-channel). The V_{GS} sweep takes 30 s, and on the 30-s return sweeps the n-

channel TFTs show hysteresis of 0.1 V to 0.2 V. For output characteristics V_{DS} is swept from 0 to -20V while stepping V_{GS} from -10 to -22 V in increments of -2 V (*p*-channel), and V_{DS} is swept from 0 to +20 V while stepping a V_{GS} from 10 to 22 V in increments of 2 V (*n*-channel). The p-channel data are not definitive as we observe considerable V_{GS} shifts between different measurement protocols. The dc transfer ($\log_{10}I_{DS}$ - V_{GS}) characteristics of a *p*-channel and an *n*-channel TFT are plotted in Figs. 7(a) and 7(b), and their output (I_{DS} - V_{DS}) characteristics in Figs. 7(c) and 7(d). The *p*-channel TFT has an ON/OFF current ratio of ~ 10^5, a subthreshold slope $S \cong 1.5$ V/decade, and OFF and gate leakage currents I_{GS} of ~ 10 pA. From the least-squares fit of Fig. 8(a) we extract a saturated hole mobility $\mu_{eff,h,sat} \cong 0.1$ cm^2/V·s. We did not extract the linear hole mobility since I_{DS} was too noisy at V_{DS} of -0.1V. The *n*-channel TFT has an ON/OFF current ratio of ~ 10^7, S = 300 mV/decade, an OFF current of ~ 0.5 pA, and a gate leakage current I_{GS} of ~ 0.1 pA. We extract from the least-squares fits of Fig. 8(b) to the saturated (V_{DS} = 10V) and linear (V_{DS} = 0.1V) regimes values for $\mu_{eff,e,sat}$ = 1.9 cm^2/V·s and $\mu_{eff,e,lin}$ = 2.2 cm^2/V·s, and threshold voltages of V_T = 3.8 V and 4.0V, respectively.

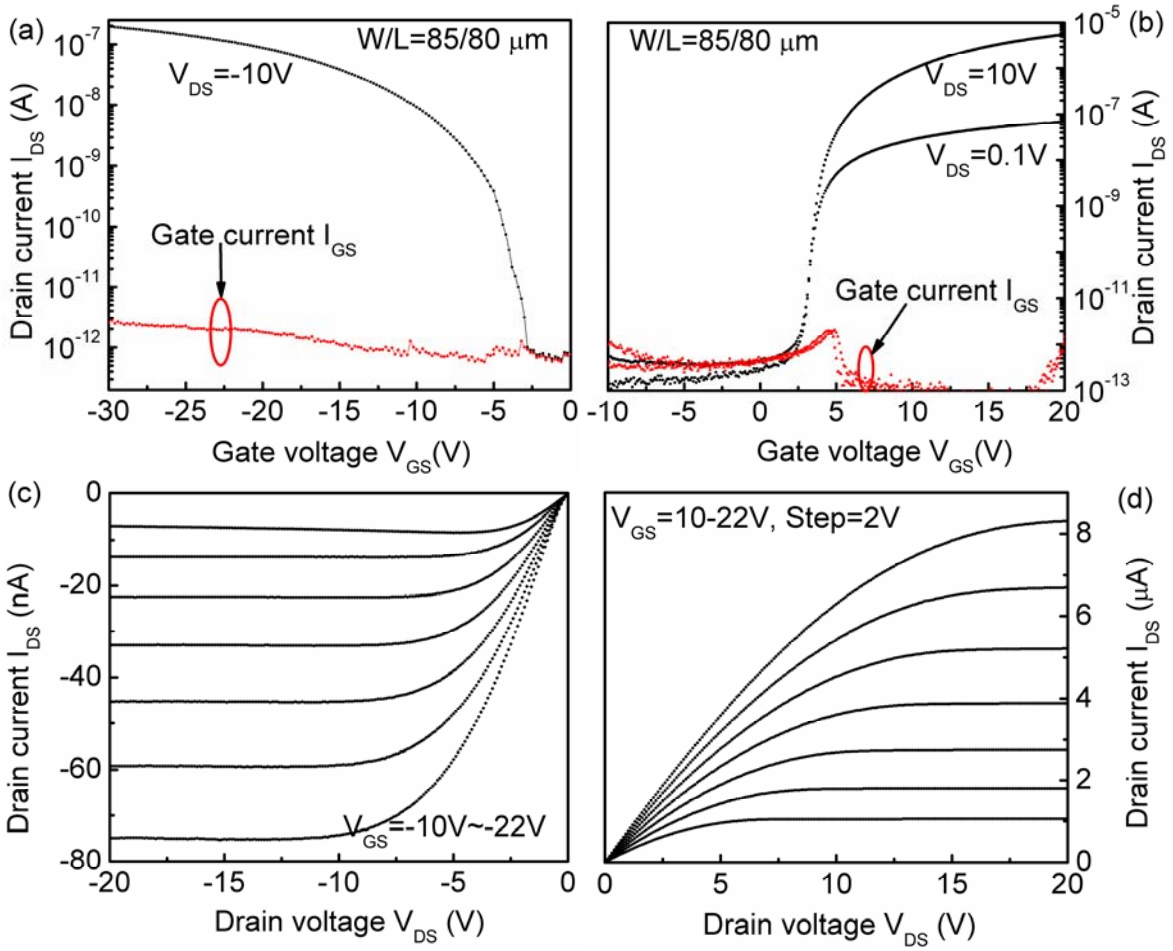

Figure 7 Transfer characteristics and gate leakage current of (a) *p*-channel and (b) *n*-channel TFTs of Fig. 2a and 2b. Output characteristics of (c) *p*-channel and (d) *n*-channel TFTs of Fig. 2a and 2b. (From ref. 8)

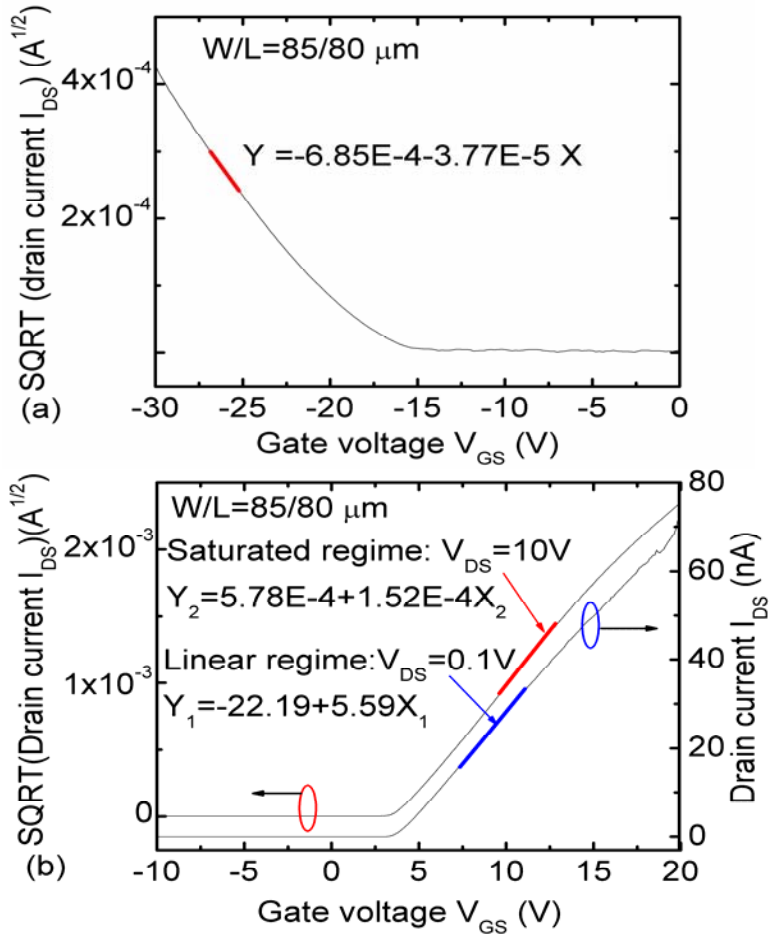

Figure 8 (a) Least-squares fits to the saturated (V_{DS}= 10 V) of the *p*-channel TFT of Fig. 2a. (b) Least-squares fits to the saturated (V_{DS}= 10 V) and linear regimes (V_{DS}= 0.1 V) of the *n*-channel TFT in Fig. 2b. (From ref. 8)

V. Mechanical flexibility of a-Si:H TFTs

The mechanical flexibility of TFTs made on the 50-μm polyimide foil substrate and with hybrid passivation and gate dielectric layers was tested by bending a given TFT around cylinders of successively smaller radii *R*. The test sequence was: electrical measurement / bending for 1 minute / flattening / electrical measurement. We monitored the changes in electrical characteristics, which turned out to be small, and electrical failure, which we translated to having surpassed a critical strain $\varepsilon_{critical}$. We measured a TFT's drain current I_{DS} – gate voltage V_{GS} transfer characteristic and gate-source leakage current I_{leak} (Fig. 9). From these we evaluated the threshold voltage V_T and $\mu_{eff,e,lin}$, I_{on} at gate voltage V_{GS} = 15V, I_{off} at V_{GS} = -5V, and the gate leakage I_{leak} current at V_{GS} = -5V (Fig. 10). The channel length *L* is the distance between the source and drain, and the channel width *W* is the width of the a-Si:H island; the photomask dimensions are only their nominal values. Theory [12] and experience confirm that the mechanical strain ε is approximated well by treating the TFT-on-substrate composite as a homogeneous sheet of thickness *h*, such that in bending to a cylinder of radius *R*, $\varepsilon = h / 2 \cdot R$. This relation captures the two approaches to raising flexibility: reducing *h*, a design parameter, and raising $\varepsilon_{critical}$, a materials property. Other important parameters that affect flexibility are device layer

thickness d, which enters *via* $\varepsilon_{critical} \propto 1/\sqrt{d}$ [13], and layer adhesion, which affects $\varepsilon_{critical}$ in compression [9].

Representative transfer characteristics of hybrid TFTs are shown before and after bending to the maximum tensile strain of +5% (Fig. 9a) and maximum compressive strain of -2.5% (Fig.9b). These transistors remained functional. Fig. 10 shows strain-point by strain-point data for the TFTs of Fig. 9; the points correspond to R = 3, 2.5, 2, 1.5, 1, 0.75, and 0.5 mm. 20 hybrid TFTs each were tested in tension and in compression. In tension, 3 TFTs failed during manipulation, 17 withstood bending to R = 0.75mm (ε = 3.3%), and 2 bending to R = 0.5mm (ε = 5%). In compression, 17 of 20 TFTs withstood bending to R = 1.25mm (ε = 2%), and 5 of 20 bending to R = 1.0 mm (ε = 2.5%). During outward (tensile) bending cracks appeared first in the source/drain and gate contact pads and eventually in the channel, where cracks developed preferentially at the edge of the source/drain metal. During inward (compressive) bending, the TFTs peeled off first at the source/drain and in the channel.

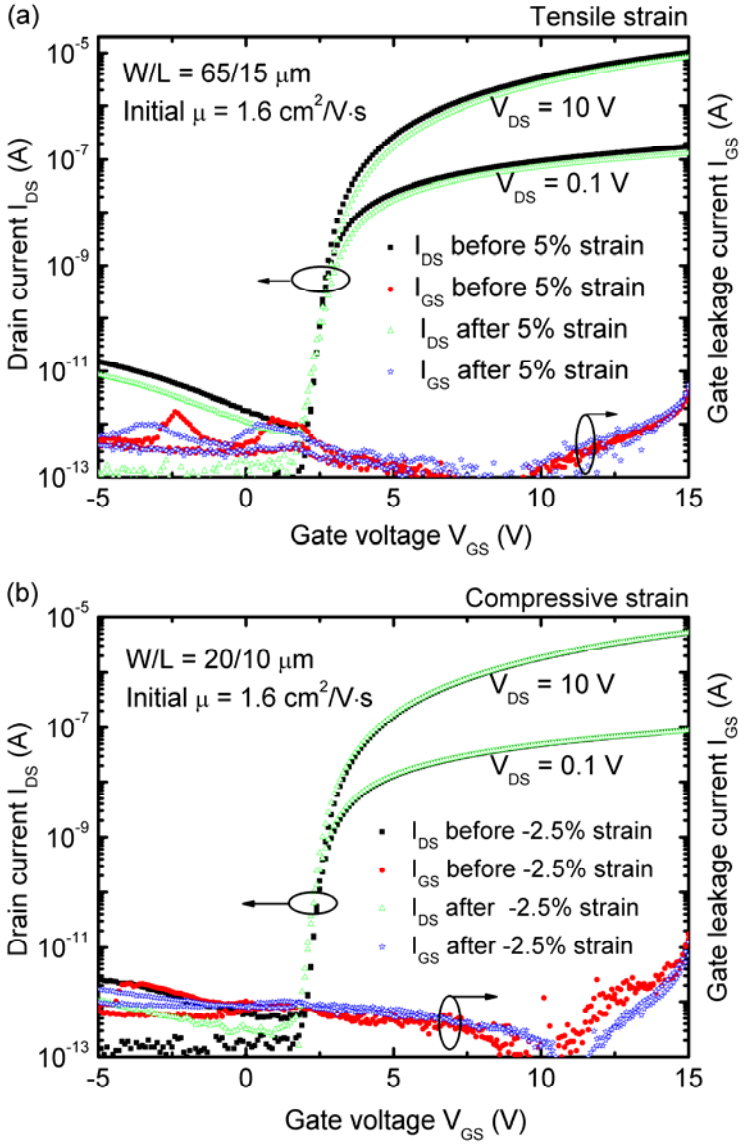

Figure 9 Transfer characteristics of the two hybrid TFTs of Fig. 2c. (a) TFT bent to tensile strain. (b) TFT bent to compressive strain. TFTs were evaluated while reflattened after each bending step. (From ref. 10)

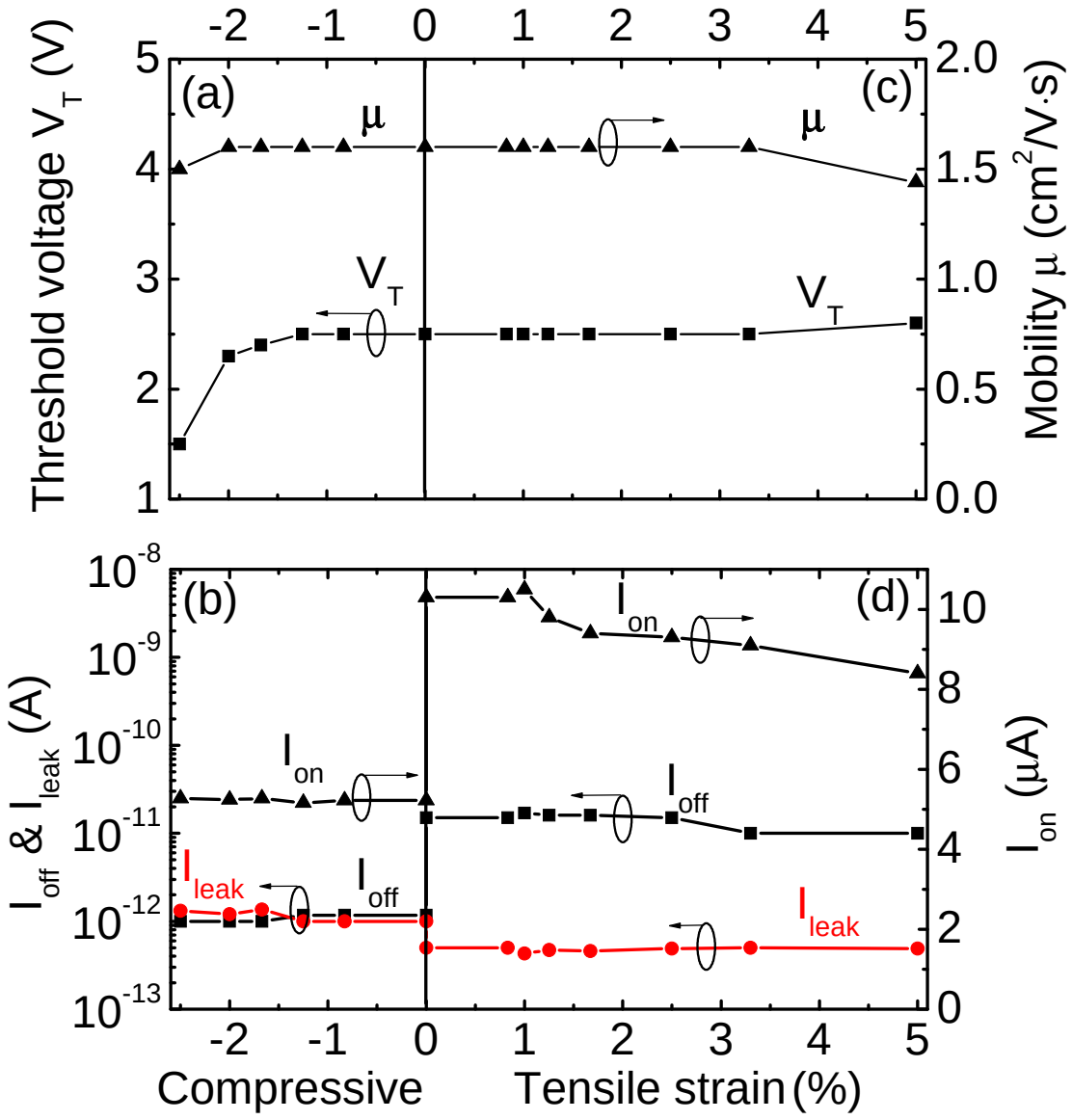

Figure 10 Performance parameters of the TFTs of Fig. 2c, evaluated after each bending step and plotted against (a), (b) compressive, and (c), (d) tensile strain. (a), (b): W/L = 20/10 μm; (c), (d): W/L = 65/15 μm. (From ref. 10)

The maximum *tensile* $\varepsilon_{critical}$ of the hybrid TFTs of 5% is a factor of ~ 10 higher than that of SiN_x TFTs, 0.5% [9]. The maximum *compressive* $\varepsilon_{critical}$, 2.5%, lies a bit higher than the already high value observed in SiN_x TFTs, 2%. The difference between tensile and compressive $\varepsilon_{critical}$ arises from the different mechanisms that cause failure in tension and compression. In tension a device layer develops channel cracks, while in compression it breaks after the buckling that is coupled with delamination [9].

VI. Discussion

The room-temperature deposition makes the hybrid especially promising for the fabrication of a-Si:H TFTs on common plastic substrates. The hybrid is free of stress, which facilitates device processing. The high electron field-effect mobility and sharp subthreshold slope of *n* channel TFTs suggests that the interface between the hybrid

dielectric and the a-Si:H channel layer has an unusually low density of traps. At high bias stress fields, the electrical stability of hybrid a-Si:H TFTs is comparable to those of SiN_x a-Si:H TFTs processed at 300 ^oC. At high bias stress fields, ΔV_T is dominated by electron injection into the gate dielectric [14], [15]. The low shift that we observe suggests that the hybrid dielectric is less susceptible to electron injection from the channel than SiN_x. The new hybrid TFTs can be bent down to 0.5 mm radius (5% strain) in tension, which is ten times that of conventional a-Si:H/SiN_x TFTs. These hybrid TFTs therefore qualify for use in roll-out screens of hand-held devices. The low deposition temperature, low-trap interface with a-Si:H, and high flexibility qualify the hybrid material as a dielectric for large-are flexible electronic surfaces.

VI. Summary

The new SiO_2-silicone hybrid material is an excellent dielectric which substantially raises the mechanical flexibility and field-effect mobilities of both electrons and holes in a-Si:H TFTs, and brings their performance to the level needed for driving roll-up OLED displays for handheld devices.

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