17.3: a-Si:H Thin-film Transistors with a New Hybrid Dielectric Highly Stable under Mechanical and Electrical Stress

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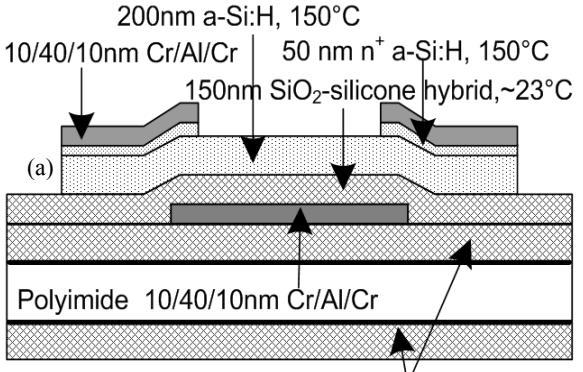
Abstract

A resilient, homogeneous, hybrid of silicon dioxide and silicone polymer deposited at room-temperature replaces the conventional, brittle, silicon nitride barrier layer and gate insulator in amorphous silicon thin-film transistors(a-Si:H TFTs) on flexible polyimide foil. The electron field-effect mobility is high at 1.6 $cm^2/V{\cdot}s$, and the threshold voltage shift under high gate bias is comparable to that in conventional a-Si:H/SiN_x TFTs fabricated at 300°C. The substhreshold slope is 290 mV/decade. The new transistors are highly flexible, as they can be bent down to 0.5 mm radius (5% strain) in tension and down to 1mm radius (2.5% strain) in compression. These TFTs qualify for roll-out screens of hand-held devices.

1. Introduction

Active-matrix organic light-emitting diode (AMOLED) displays promise to become the dominant technology for flexible displays, because of their brilliance, light weight, and inherent flexibility. Each pixel of an AMOLED needs two thin-film transistors (TFTs) to switch and drive the OLED. The large experience and manufacturing base of a-Si:H TFTs make their upgrade to circuits for AMOLED displays very desirable. The drive TFT must source enough current to the OLED and be sufficiently stable to ensure an OLED brightness half-life of at least ten years. Conventional a-Si:H TFT relies on silicon nitride (SiN_x) as the gate dielectric. By modifying the fabrication process for such a-Si:H/SiNx TFTs, their stability at low gate bias has been extended to a projected drive-current half-life of 1000 years [1], [2], Their stability at high gate bias has been raised by keeping the deposition temperature for the SiN_x gate dielectric high, and modifying the post-deposition process [3], [4]. We also have been focusing on enhancing the rollability of a-Si:H TFTs on plastic substrates to values that are needed for roll-out displays of hand-held devices.

Therefore we developed high-performance a-Si:H TFTs in which the conventional SiN_x is replaced with a new hybrid dielectric. The hybrid is deposited by plasma-enhance chemical vapor deposition (PE-CVD), and is part-SiO_2 and part-silicone polymer [5], [6], such that it has the electrical properties of SiO_2, but is not brittle like SiO_2 or SiN_x. When fabricated on 50-µm Kapton E polyimide foil, the "hybrid" a-Si:H TFT has an electron field-effect mobility of 1.6 $cm^2/V{\cdot}s$. At high gate field, its stability is comparable to that of a-Si:H/SiN_x TFTs processed at 300 °C. Most important for the present work is that the new a-Si:H TFT has a critical tensile strain of +5%, which is 10 times of that of a-Si:H/SiN_x TFTs, and critical compressive strain of -2.5%, and which is similar to that of a-Si:H/SiN_x TFT [7].



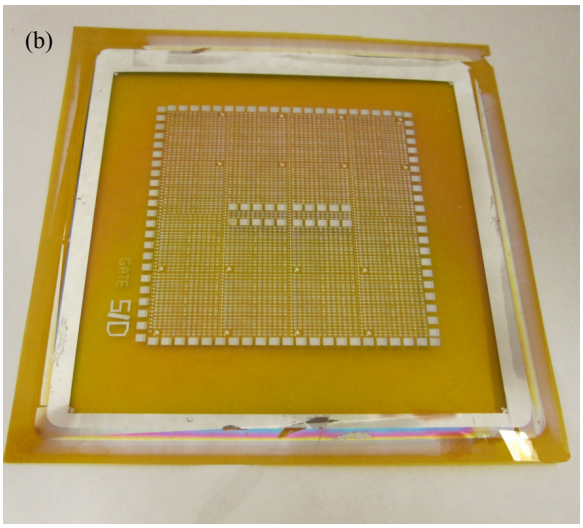


Fig. 1(a) Schematic cross section of the TFT with substrate and layer thickness, material, and process temperatures. (b) Optical micrograph of completed hybrid TFTs on a polyimide foil substrate.

2. Transistor fabrication and evaluation

A schematic cross section of the hybrid TFT on polyimide foil is shown in Fig. 1(a). The polyimide foil substrate is pre-shrunk for one hour at 150 °C before a 15-nm thick SiN_x adhesion layer is deposited at 150°C on both faces. Then, on both faces of the substrate 300-nm thick hybrid layers for substrate passivation are deposited at nominal room temperature. The 15-nm SiN_x serves to make the hybrid layers adhere to the substrate. Tri-layer Cr/Al/Cr (10/40/10nm) gate metal is thermally evaporated and patterned to gate electrodes. Then at nominal room temperature, a 150-nm thick SiO_2-silicone hybrid gate dielectric is deposited in a

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composition that has a relative dielectric constant of 4.0. Deposition of a 200-nm thick *i* a-Si:H channel layer and a 50-nm thick n^+ a-Si:H source/drain (S/D) layer at 150°C follows. Finally, another 10/40/10-nm Cr/Al/Cr tri-layer is thermally evaporated, and patterned to S/D contacts, which are then used as masks for dry etching the n^+ layer. a-Si:H islands are separated and vias to the gate contacts are opened by etching. A polyimide substrate foil covered with hybrid TFTs of varying dimensionsl is shown in Fig. 1(b). The substrate is flat after fabrication because the hybrid film is free of strain.

The TFTs are evaluated for I_{DS}-V_{DS} output characteristics, I_{DS}-V_{GS} transfer characteristics, gate-bias stress stability, and mechanical stability using an HP4155A parameter analyzer. For output characteristics V_{DS} is swept from 0 to 5V, and V_{GS} is swept from 8 to 16V in steps of 2V (Fig. 2). For transfer characteristics V_{GS} is swept from 15V to -5V at V_{DS} of 0.1V or 10V (Fig. 3). For each data point in gate-bias stressing, the source and drain of a new transistor are grounded, and a positive voltage is applied to the gate for 600s. Threshold voltage shifts are evaluated for gate-bias voltages between 5 to 30 V, i.e., at electric fields from 0.3 to 2 MV/cm. Before and after each stressing experiment the transfer characteristics are measured by sweeping the gate voltage from 20 to -10 V. ΔV_T is determined on the subthreshold slope of the transfer curve at the drain-current value of 1×10^{-10} A (Fig.4).

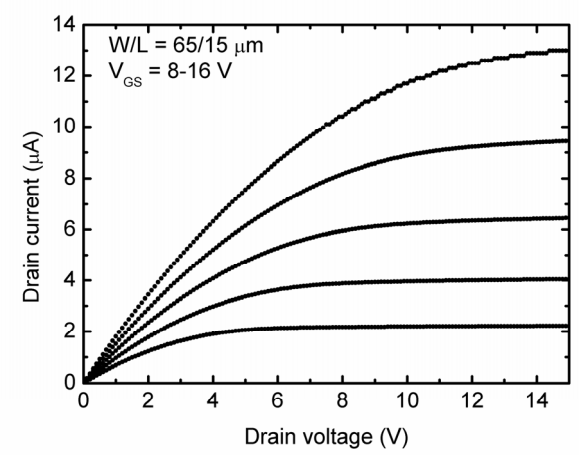
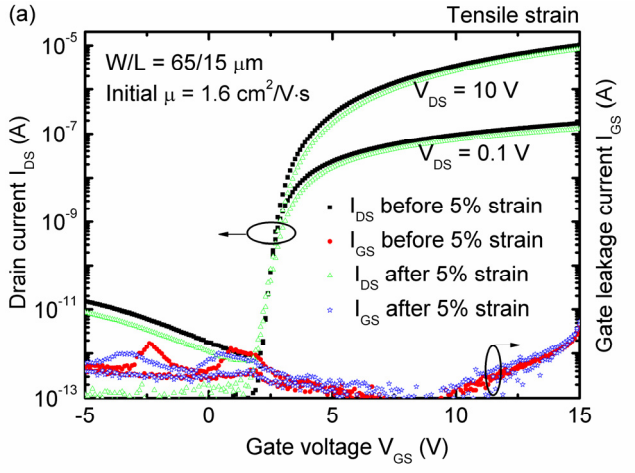


Fig. 2 Output characteristics of an a-Si:H TFT with the new hybrid gate dielectric.



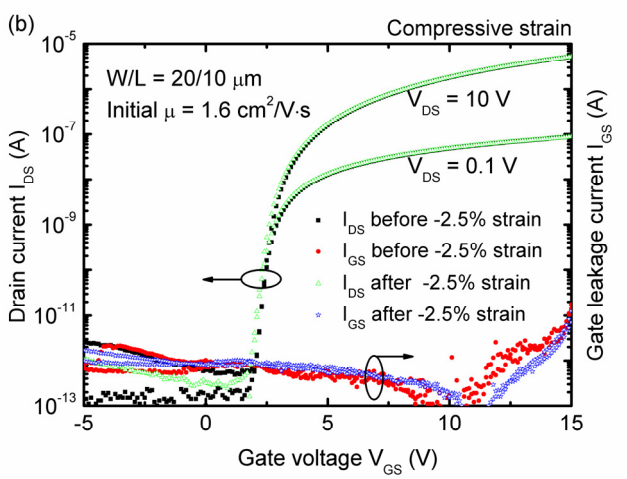


Fig. 3 Transfer characteristics of two hybrid TFTs before and after bending. (a) TFT bent to tensile strain. (b) TFT bent to compressive strain. TFTs were evaluated while re-flattened after each bending step.

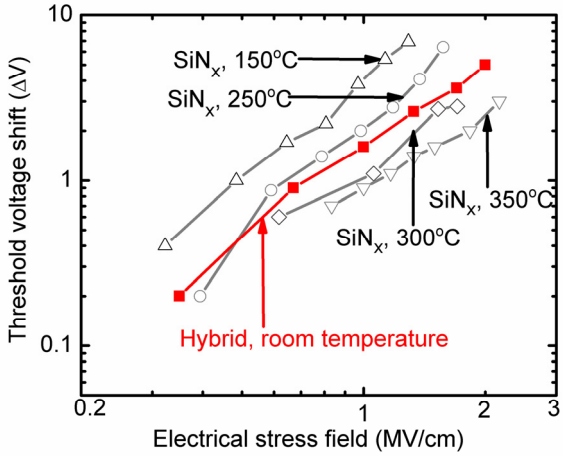


Fig. 4 Threshold voltage shift ΔV_T versus gate bias field for TFTs with the new hybrid gate dielectric, and for TFTs with the conventional SiN_x gate dielectric fabricated at 150 °C, 250 °C [3], 300 °C [8], and 350 °C [9]. Gate bias stress was applied for 600 s to all TFTs

We evaluated the electro-mechanical stability by bending a given TFT around cylinders of successively smaller radii *R*, around an axis perpendicular to the channel length. The test sequence was: electrical measurement / bending for 1 minute / flattening / electrical measurement. We monitored the changes in electrical characteristics, which turned out to be small and eventually logged electrical failure, which we translated to having surpassed a critical strain $\varepsilon_{critical}$. To capture the results of these flexibility tests we measured the transfer characteristics and the gate-source leakage current I_{leak} for each value of mechanical strain. Two examples are shown in Fig. 3.

3. Results

The output (I_{DS}-V_{DS}) characteristics of a TFT with gate width W = 65 μm (width of the a-Si:H island) and length L = 15 μm are shown in Fig. 2. Figure 4 is a log-log plot of ΔV_T versus gate-bias

field. For comparison, we show representative high-field stability data for our standard-process TFTs, made without breaking vacuum, with the SiN_x gate dielectric deposited at 150 ^oC, 250 ^oC [3], and 300 ^oC [8], and for a TFT with 350 ^oC SiN_x [9].

Representative transfer characteristics of hybrid TFTs are shown before and after bending to the maximum tensile strain of +5% (Fig. 3(a)) and maximum compressive strain of -2.5% (Fig. 3(b)). These transistors remained functional. The transfer characteristics of Fig. 3 reflects the high electron field-effect mobility of 1.6 $cm^2/V{\cdot}s$, an on/off current ratio of $\sim 10^7$, a subthreshold slope S = 290 mV/decade, and off and gate leakage currents I_{GS} of ~1pA.

4. Discussion

Room-temperature deposition makes the hybrid especially promising for the fabrication of a-Si:H TFTs on common plastic substrates. The hybrid is free of stress, which facilitates device processing. The high electron field-effect mobility and sharp subthreshold slope suggests that the interface between the hybrid dielectric and the a-Si:H channel has an unusually low density of traps. At high bias stress fields, the electrical stability of hybrid a-Si:H TFTs is comparable to those of SiN_x a-Si:H TFTs processed at 300 ^oC. At high bias stress fields, ΔV_T dominated by electron injection into the gate dielectric [10], [11]. The low shift that we observe suggests that the hybrid dielectric is less susceptible to electron injection from the channel than SiN_x. The new hybrid TFTs can be bent down to 0.5 mm radius (5% strain) in tension, which is ten times that of traditional a-Si:H/SiN_x TFTs. These hybrid TFTs therefore qualify for use in roll-out screens of hand-held devices. The low deposition temperature, low-trap interface with a-Si:H, and high flexibility qualify the hybrid material as a dielectric for large-area flexible electronic surfaces.

5. Acknowledgements

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