5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input terminal pin assignment (LVDS, Connector : 20455-040E-0 by I-PEX or equivalent)

No.	Signal	Description
1	NC	No Connection
2~3	AVDD	Power Supply, 3.3V (typical)
4	DVDD	DDC 3.3V power
5	NC	No Connection
6	SCL	DDC Clock
7	SDA	DDC Data
8	Rin0-	-LVDS differential data input (R0-R5, G0)
9	Rin0+	+LVDS differential data input (R0-R5, G0)
10	GND	Ground
11	Rin1-	-LVDS differential data input (G1-G5, B0-B1)
12	Rin1+	+LVDS differential data input (G1-G5, B0-B1)
13	GND	Ground
14	Rin2-	-LVDS differential data input (B2-B5, HS, VS, DE)
15	Rin2+	+LVDS differential data input (B2-B5, HS, VS, DE)
16	GND	Ground
17	ClkIN-	-LVDS differential clock input
18	ClkIN+	+LVDS differential clock input
19	GND	Ground
20~21	NC	No Connection
22	GND	Ground
23~24	NC	No Connection
25	GND	Ground
26~27	NC	No Connection
28	GND	Ground
29~30	NC	No Connection
31~33	VBL-	LED Ground
34	NC	No Connection
35	BLIM	PWM for luminance control (200~1KHz, 3.3V, 10~100%)
36	BL_Enable	BL On/Off (On:2.0~3.3V, Off: 0~0.5V)
37	NC	No Connection
38~40	VBL+	LED Power Supply 6V~20V