COMP 2004
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Assignment 7

1. (20%) Given six memory partitions of 100 MB, 170 MB, 40 MB, 205 MB, 300 MB, and 185 MB (in order), how would the first-fit, best-fit, and worst-fit algorithms place processes of size 200 MB, 15 MB, 185 MB, 75 MB, 175 MB, and 80 MB (in order)?

   Indicate which—if any—requests cannot be satisfied. Comment on how efficiently each of the algorithms manages memory.

2. (5%) Assuming a 1-KB page size, what are the page numbers and offsets for the following address references (provided here as decimal numbers)?

   a. 21205

   b. 164250

   c. 121357

   d. 16479315

   e. 27253187

3. (30%) Apply the (1) FIFO, (2) LRU, and (3) optimal (OPT) replacement algorithms for the following page-reference strings:

   a. 2,6,9,2,4,2,1,7,3,0,5,2,1,2,9,5,7,3,8,5
   b. 0,6,3,0,2,6,3,5,2,4,1,3,0,6,1,4,2,3,5,7
   c. 3,1,4,2,5,4,1,3,5,2,0,1,1,0,2,3,4,5,0,1
   d. 4,2,1,7,9,8,3,5,2,6,8,1,0,7,2,4,1,3,5,8
   e. 0,1,2,3,4,4,3,2,1,0,0,1,2,3,4,4,3,2,1,0

   Indicate the number of page faults for each algorithm assuming demand paging with three frames.

4. (15%) Consider the page table for a system with 16-bit virtual and physical addresses and 4,096-byte pages.

Page	Page Frame	Reference bit
0	9	0
1	-	0
2	10	0
3	15	0

4	6	0
5	13	0
6	8	0
7	12	0
8	7	0
9	-	0
10	5	0
11	4	0
12	1	0
13	0	0
14	-	0
15	2	0

The reference bit for a page is set to 1 when the page has been referenced. Periodically, a thread zeroes out all values of the reference bit. A dash for a page frame indicates that the page is not in memory. The page-replacement algorithm is localized LRU, and all numbers are provided in decimal.

a. Convert the following virtual addresses (in hexadecimal) to the equivalent physical addresses. You may provide answers in either hexadecimal or decimal. Also, update the reference bit for the appropriate entry in the page table.

   i. 0x621C
   ii. 0xF0A3
   iii. 0xBC1A
   iv. 0x5BAA
   v. 0x0BA1

b. Using the above addresses as a guide, provide an example of a logical address (in hexadecimal) that results in a page fault.
c. From what set of page frames will the LRU page-replacement algorithm choose n resolve a page fault?

5. (5%) Consider a demand-paging system with a paging disk that has average access and transfers time of 20 milliseconds. Addresses are translated through a page table in the main memory, with an access time of 1 microsecond per memory access. Thus, each memory reference through the page table takes two accesses. To improve this time, we have added an associative memory that reduces access time to one memory reference if the page-table entry is in the associative memory.

   Assume that 80 percent of the accesses are in the associative memory and that, of those remaining, 10 percent (or 2 percent of the total) cause page faults. What is the effective memory access time?

6. (15%) What is the cause of thrashing? How does the system detect thrashing? Once it detects thrashing, what can the system do to eliminate this problem?

7. (10%) How does DMA increase system concurrency? How does it complicate hardware design?