Comparison with prior works					
	Proposed RTB	ABC Retiming	[2]	[3]	[10]
FPGA/ASIC	FPGA	FPGA	ASIC	FPGA	ASIC
Time Borrowing	✓	✗	✗	✗	✓
Support latch-based design	✓	✗	✗	✗	✓
Retiming Stage	Post STA	Before mapping	Post placement	Post routing	Gate-level
Delay in Retiming	STA	Logic Depth	Roughly Estimation	Simple timing model	STA