Retiming	
v	a vertex of the graph
e	an interconnection betweenfunctional elements
V	set of vertices
E	set of edges
d(v)	fixed propagation delay of vertex v
w_uv	s the number of the registers along the connection
W(u, v)	the minimum number of registers on any path p from vertex u to v
D(u, v)	the maximum propagation delay on a critical path from vertex u to v
W(e)	the initial register number of edge e
r(u)	registers need to be moved onto edge e
r(v)	registers need to be removed from edge e

Minimum Cost-to-time Ratio Problem	
c	a cycle in graph G
C	set of all cycles in G
ω(c)	sum of costs associated with all edges on cycle
τ(c)	the sum of transit times for edges on cycle
ρ(c)	ratio of ω(c) and τ(c)
r	a modified weight function

Timing constraints of latch	
W	pulse width of latch
Tcq	Clock-to-Q Delay
Tdq	Data-to-Q Delay
Tsu	Setup Time
Th	Hold Time
ti	clock skew of latch i
Di	inpur port of latch i
Dij	maximum delay of combinational logic between latch i and j
dij	minimum delay of combinational logic between latch i and j

Timing analysis of latch-based circuit	
di	earliest departure time
Di	latese departure time
aj	earliest arrival time
Aj	latese arrival time