Retiming	
v	a vertex of the graph
e	an interconnection between functional elements
V	set of vertices
E	set of edges
$d(v)$	fixed propagation delay of vertex v
w_{uv}	s the number of the registers along the connection
$W(u,v)$	the minimum number of registers on any path p from vertex u to v
$D(u,v)$	the maximum propagation delay on a critical path from vertex u to v
$W(e)$	the initial register number of edge e
$r(u)$	registers need to be moved onto edge e
$r(v)$	registers need to be removed from edge e

Minimum Cost-to-time Ratio Problem	
c	a cycle in graph G
C	set of all cycles in G
$\omega(c)$	sum of costs associated with all edges on cycle
$\tau(c)$	the sum of transit times for edges on cycle
$\rho(c)$	ratio of $\omega(c)$ and $\tau(c)$
r	a modified weight function

Timing constraints of latch	
W	pulse width of latch
T_{cq}	Clock-to-Q Delay
T_{dq}	Data-to-Q Delay
T_{su}	Setup Time
T_h	Hold Time
t_i	clock skew of latch i
D_i	input port of latch i
D_{ij}	maximum delay of combinational logic between latch i and j
d_{ij}	minimum delay of combinational logic between latch i and j

Timing analysis of latch-based circuit	
d_i	earliest departure time
D_i	latese departure time
a_j	earliest arrival time
A_j	latest arrival time