CSE1400 - Computer Organisation

Self-Study: Week 7
I/O & Memory

Delft University of Technology

2022/2023 Q1

Special thanks to Sára Juhošová and Alexandra Marcu
for helping with the compilation of this set of questions.

Important information:

1. If any question is unclear please consult Answers EWI. For more specific questions, you can use the Queue during lab hours.
2. The average time for solving this self study is **3** hours, and **1** hour is allocated to giving feedback. Timings are included for each exercise to give you a more clear overview of how much time you should be spending on them.
3. The maximum amount of points for this self study is 200 points. To get the points you should submit a serious attempt on Peer and **properly review** your peers' submissions (100 points per serious review).
4. Answers will be provided during the weekly tutorial sessions.

1. (5 mins) Fill in **T** if the claim is true and **F** if it is false. Correct the claim if it is false.
   (a) F A pro of single-bus architecture is that it is very scalable.

   Single-bus architecture is not scalable.

   (b) T A dual-bus architecture is fast and quite cheap.

   (c) T Passive signalling (or polling) is the synchronization between the CPU and I/O device by programmed interrogation by CPU.

   (d) F An interrupt occurs when an I/O device alerts the CPU by using a software signal.

   An interrupt occurs when an I/O device alerts the CPU by a hardware signal.

   (e) T The DMA controller is a block based, independent entity which specializes in data transfer.

2. (5 mins) Write down the Interrupts execution flow:
   1. I/O device alerts CPU by hardware signal.
   2. CPU stops program execution.
   3. Interrupts are disabled.
   4. Device is informed of acceptance and clears IRQ.
   5. ISR is invoked to handle device's request.
   6. Interrupts are enabled.
   7. Execution of program resumes.

3. (10 mins) You have a 32 MiB **word addressable** memory chip. How many adress lines are needed for the following word sizes? *Show your work.*
   (a) 128-bit words

   $\log_2(2^{28} \times 2^{-7}) = 21$

   (b) 64-bit words

   $\log_2(2^{28} \times 2^{-6}) = 22$

   (c) 32-bit words

   $\log_2(2^{28} \times 2^{-5}) = 23$

   (d) 16-bit words

   $\log_2(2^{28} \times 2^{-4}) = 24$

32 MiB $= 2^{25}$ B $= 2^{28}$ b

4. (10 mins) The memory display in Figure 1 has a `2048xA` memory organisation. The word size is two bytes. There are 7 address lines at C.

2048x16

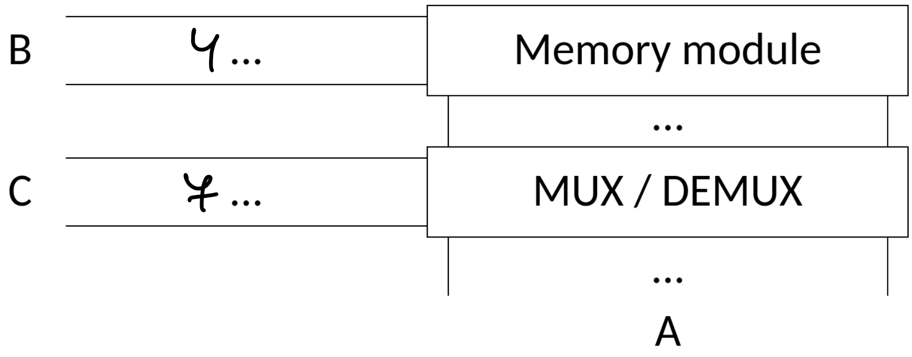


Figure 1: Memory Organisation

Show your work for the following questions.

(a) How many address lines are there at B?

(b) How many data lines are there at A?

(c) Unfortunately, you realise that the least significant data line is broken and can only carry a zero. What values will the MUX / DEMUX never be able to output correctly?

a) $2048 = 2^{11} \Rightarrow 11$ address lines

$C = 7 \quad B + C = 11 \Rightarrow B = 4$ address lines

b) word size is two bytes ($2B = 16b$), therefore $A = 16$ data lines.

c) MUX/DEMUX cannot output odd values.

5. (8 mins) A computer is required to accept characters from the keyboard input of **40 terminals**. Input data must be collected from the terminals while another program is running. This can be done in two ways:

- Every **T** seconds, call a polling subroutine POLL. This subroutine checks the status of **each terminal** in sequence and transfers any input to memory. Assume the typing rate is between 0 and 200 cps and that **POLL takes 1000 ns** in total to check all the terminals.
- Whenever a character is ready in any of the terminals, an interrupt request is generated. This causes the INT routine to be executed which polls the status registers to find the first ready character, transfers it and then returns. Assume INT takes 100 ns.

(a) What is the maximum value of **T** in method 1 that guarantees that no characters will be lost?

$V_{max} = 200$ cps $\Rightarrow \frac{1}{200}$ s $= 5$ ms per typing a character

POLL takes 1000ns $= 1\mu s \ll 5$ ms $\Rightarrow T = 5$ ms

$5ms - 1\mu s = 4.999$ ms

(b) Let **C** be the average cps of a terminal. For what values of **C** is method 2 the least time-consuming?

INT takes 100ns $= 10^{-7}$s

10^{-7}s to execute an interrupt $\Rightarrow \frac{1}{10^{-7}}$ cps $= 10^{7}$ cps

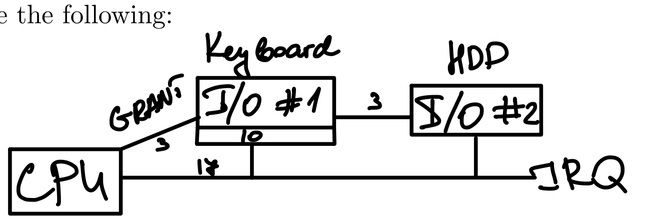
$C = \frac{10^7 \text{ cps}}{40 \text{ terminals}} = 2.5 \times 10^5$ average cps

$C \times 40 \times 100 < 200 \times 1000$

$C < 50$

6. (8 mins) You would like to connect 2 I/O devices to a CPU using daisy-chaining. The device closest to the CPU is a keyboard, next in line is a HDD. Assume the following:

- we are using Programmed-I/O
- there is only one I/O bus
- reaction to an interrupt takes 17 ms
- it takes $3 \cdot i$ ms for the grant to reach the i_{th} device
- it takes 10 ms to handle the keyboard interrupt.



How fast should you type to prevent the CPU from accessing the disk?

keyboard → 1st device next to CPU ⇒ 3ms for the grant to reach it.

$\Rightarrow 3 + 17 + 10 = 30$ ms per keyboard interrupt

$\Rightarrow \frac{1}{30ms} = \frac{1}{3 \times 10^{-2} s} = 33.33....$ cps rounded to 34 cps to not be able to access disk

7. (5 mins) The address bus of a computer has 16 address lines: A_{15-0}. If the hexadecimal address assigned to one device is `0x90BA` and the address decoder for that device ignores lines A_2 and A_{13}, what are all the addresses (in hexadecimal notation) to which this device will respond?

9 0 B 11 A 10

A_0 A_2 A_{13} A_{15}

1001 0000 1011 1010

$A_2 = 1$ 9 -> B

$A_{13} = 1$ A -> E

9 0 B 11 A 10

A_{15} A_{13} A_2 A_0

1001 0000 1011 1010

$A_2 = 1$ A -> E

$A_{13} = 1$ 9 -> B

=> 0x 90BA

0x B0BA

0x 90BE

0x B0BE

8. (10 mins) The Coati are playing an online game called "Among them" with Taico. The purpose of this game is to find the impostor IO device on a bus with many devices. All normal devices respond to a 16-bit address ignoring two address lines; which 2 lines differs per device. The imposter tries to steal secret data and thus listens to more addresses (ignores more address lines).

- The following address appears on the bus: `0xBABF`
  The following devices respond: **A** , **B**
- The next address that appears on the bus is: `0xBABE`
  The following devices respond: **B** , **C**
- The next address that appears on the bus is: `0xBACE`
  The following devices respond: **C** , **D**
- The next address that appears on the bus is: `0xBACF`
  The following devices respond: **D**

Taico now calls for an emergency meeting. Which device do you think is the imposter and why?

0x BABF

$A_7 A_6 A_5 A_4$ $A_3 A_2 A_1 A_0$

1011 1010 1011 1111 } A & B

B - ignores A_0

0x BABE

1011 1010 1011 1110 } B & C

C - ignores A_4, A_5, A_6 => is imposter I/O.

0x BACE

1011 1010 1100 1110 } C & D

D - ignores A_0

0x BACF

1011 1010 1100 1111 } D