CSE1400 - Computer Organisation

Self-Study: Week 4 - Instruction Set Architecture

Delft University of Technology

2021/2022 Q1

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Important information:

1. If any question is unclear please consult Answers EWI. For more specific questions, you can use the Queue during lab hours.
2. The average time for solving this self study is **2** hours, and **1** hour is allocated to giving feedback. Timings are included for each exercise to give you a more clear overview of how much time you should be spending on them.
3. The maximum amount of points for this self study is 200 points. To get the points you should submit a serious attempt on Peer and **properly review** your peers' submissions (100 points per full cycle, including review evaluation).
4. Answers will be provided during the weekly tutorial sessions.

Show your work for all assignments. Make sure to highlight your final answer.

1. (3 mins) Name the components of the following Von Neumann Architecture:

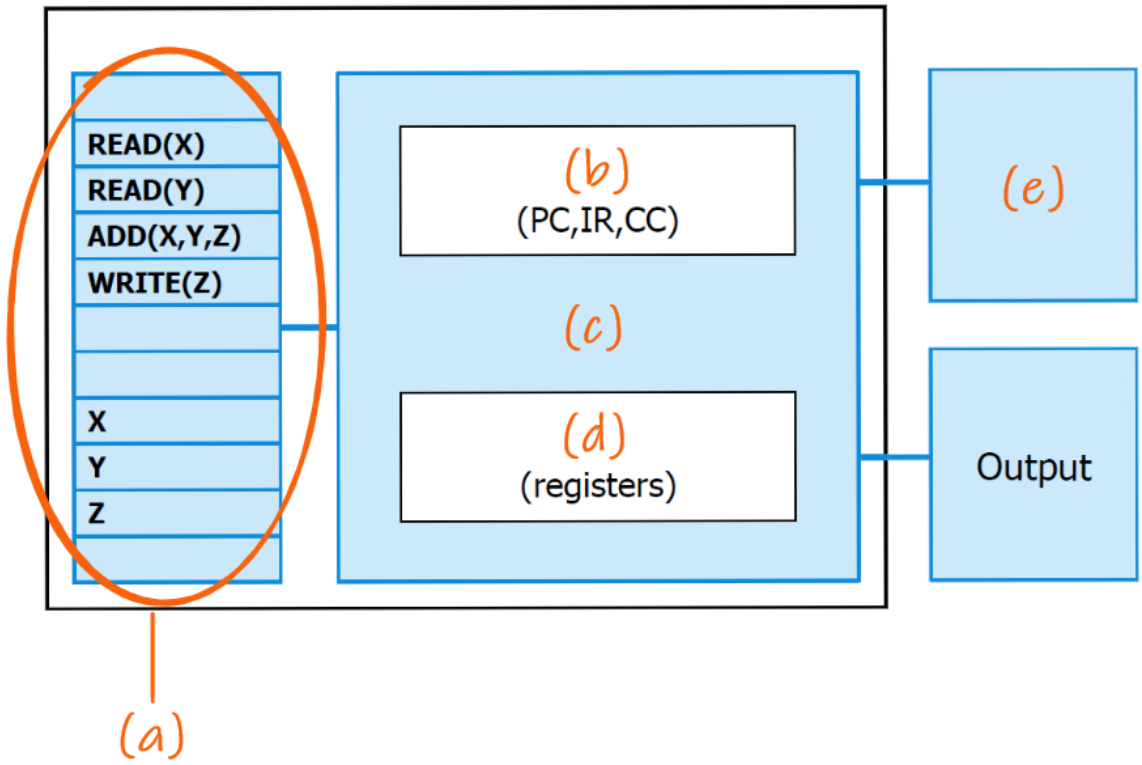

Figure 1: Von Neumann Architecture

(a) memory
(b) control unit
(c) CPU
(d) arithmetic/logic unit
(e) input

2. (5 mins) You have a 24-bit word addressable memory and you want to store "**COMPUTER ORGANISATION**" in memory. Show how it will be saved in memory if it is little or big endian. You can assume every character takes 8 bits, the empty space between the words is also a character, and that your memory position starts at 0:

   (a) little endian:

Characters	ION	SAT	ANI	ORG	ER␣	PUT	COM
Position in memory	0	24	48	72	96	120	144

   (b) big endian:

Characters	COM	PUT	ER␣	ORG	ANI	SAT	ION
Position in memory	0	24	48	72	96	120	144

3. (8 mins) Consider a 32 MiB main memory. How many bits are required to be able to individually address each of the following.

   (a) every bit

$32\,MiB = 2^5\,MiB = 2^5 \cdot 2^{10}\,KiB = 2^5 \cdot 2^{10} \cdot 2^{10}\,B = 2^5 \cdot 2^{10} \cdot 2^{10} \cdot 2^3\,b = 2^{28}\,b$

$\Rightarrow$ 28 bits required to access every bit.

   (b) every byte

$1B = 8\,b$

$32\,MiB = 2^{28}\,b = \frac{2^{28}}{2^3}\,B = 2^{25}\,B$

$\Rightarrow$ 25 bits are required to access every byte.

   (c) every 64-bit quadword

$1q = 64b = \frac{64}{8}\,B = 8B$

$32\,MiB = 2^{25}\,B = \frac{2^{25}}{2^3}\,q = 2^{22}\,q$

$\Rightarrow$ 22 bits are required to access every 64-bit quadword.

4. (3 mins) How many bits are required to address 42 registers?

$2^0 = 1 < 42$
$2^1 = 2 < 42$
$2^2 = 4 < 42$
$2^3 = 8 < 42$
$2^4 = 16 < 42$
$2^5 = 32 < 42$
$2^6 = 64 > 42$

$\Rightarrow$ 6 bits are required to address 42 registers.

5. (3 mins) How many different instructions can an ISA have if its opcode size is 10 bits?

If an ISA has opcode size of 10 bits, then it can have $2^{10} = 1024$ instructions.

6. (15 mins) Consider an ISA with 128 possible instructions, 32 registers and 64-bit instructions. Each instruction consists of an opcode, one register operand and two direct memory access operands. How much memory (in MiB) can it address if the memory is of the following type:

   (a) bit addressable memory

128 instructions $= 2^7 \rightarrow$ 7 bits for OP code
32 registers $= 2^5 \rightarrow$ 5 bits for a register operand
64-bit instructions [OP, reg, dir, dir] $\Rightarrow 64 = 7+5+2\text{dir} \Rightarrow \text{dir} = 26$ bits for addressing memory
bit addressable $\Rightarrow 2^3$ b in B $\Rightarrow 2^3 \cdot 2^{10}$ b in KiB $= 2^3 \cdot 2^{10} \cdot 2^{10}$ b in MiB
$\Rightarrow$ 23 bits for addressing 1 MiB memory.
$\Rightarrow 26 - 23 = 3 \Rightarrow 2^3 =$ 8 MiB memory

   (b) byte addressable memory

26 bits for addressing memory
1B $\Rightarrow 2^{10}$ B in KiB $\Rightarrow 2^{10} \cdot 2^{10}$ B in MiB
$\Rightarrow$ 20 bits for addressing 1 MiB memory
$\Rightarrow 26 - 20 = 6 \Rightarrow 2^6 =$ 64 MiB memory

   (c) 32-bit word addressable memory

26 bits for addressing memory
1w = 4B $\Rightarrow \frac{2^{10}}{4} = 2^8$ w in KiB $\Rightarrow 2^{10} \cdot 2^8$ w in MiB
$\Rightarrow$ 18 bits for addressing 1 MiB memory.
$\Rightarrow 26 - 18 = 8 \Rightarrow 2^8 =$ 256 MiB memory

7. (4 mins) Consider an ISA that has 64 registers and 15 different instructions which are all composed of an opcode and two register operands. How many bits are used for each instruction?

64 registers $= 2^6 \rightarrow$ 6 bits for a register operand
15 instructions $\rightarrow 2^4 \rightarrow$ 4 bits for OP
$\Rightarrow$ OP + 2 reg. $= 4 + 2 \times 6 =$ 16-bit instructions

8. (6 mins) Consider an ISA with 32 registers and instructions which are each 2-byte-word long. Each instruction has an opcode and two register operands. How many bits does the opcode have?

32 registers $= 2^5 \rightarrow$ 5 bits for a register operand
2-byte-word instructions = 16 bits
$16 =$ OP + 2 reg. $=$ OP $+ 2 \times 5 \Rightarrow$ OP $=$ 6 bits

9. (7 mins) Consider an ISA with 64-bit instructions, 64 registers, and a 32 MiB byte-addressable main memory. 42 of these instructions have two direct memory addresses and one register operand. Considering all instructions have the same opcode length, how many other instructions can be created within the same ISA?

64 registers $= 2^6 \rightarrow$ 6 bits for addressing a register operand
$32\,\text{MiB} = 2^5\,\text{MiB} = 2^5 \cdot 2^{10}\,\text{KiB} = 2^5 \cdot 2^{10} \cdot 2^{10}\,\text{B} = 2^{25}\,\text{B} \rightarrow$ 25 bits for addressing a byte in memory

OP + 2 dir + 1 reg = 64
OP + 2(25) + 1(6) = 64
OP = 8 bits $\Rightarrow 2^8 = 256$ instructions
$-$ 42 known
214 other

10. (7 mins) Consider a 64-bit processor with 36 registers and three addressing modes (immediate, direct and register). This processor supports 144 instructions and a byte addressable memory of up to 2 TiB. Every instruction has the following operands: two registers, one direct memory access and one immediate value. If all of the instructions are 128 bits long, how many bits does the immediate value operand have?

36 registers → 2^6 → 6 bits for addressing a register operand
144 instructions → 2^8 → 8 bits for OP
2 TiB = 2^{11} GiB = 2^{21} MiB = 2^{31} KiB = 2^{41} B → 41 bits for addressing a byte in memory
128 bit instructions → operands: 2 registers, 1 direct, 1 immediate
128 = OP + 2reg + 1 dir + 1 imm
= 8 + 2(6) + 1(41) + 1 imm
= 61 + imm => 128 − 61 = 67 bits for immediate

11. (7 mins) Consider an ISA with 102 bits per instruction and a total number of 256 possible instructions. This ISA supports 42 registers and can access 32 MiB of byte-addressable main memory. Each instruction has an opcode, two register operands, two direct memory access operands and one immediate value. How many bits does the immediate value operand have?

256 instructions = 2^8 → 8 bits for OP
42 registers → 2^6 → 6 bits for addressing a register operand
32 MiB = 2^5 MiB = 2^{25} KiB = 2^{25} B → 25 bits for addressing a byte in memory
102 bit instructions → operands: 2 registers, 2 direct, 1 immediate
102 = OP + 2reg + 2dir + 1 imm
= 8 + 2(6) + 2(25) + 1 imm
= 70 + imm => 102 − 70 = 32 bits for immediate

12. (8 mins) Consider having an ISA that takes zero-address instructions that uses implicit reference to the stack for ALU operations. You are asked to write a program that calculates the following expression: $(A \cdot (B + C)) \cdot (A + B) \cdot C$