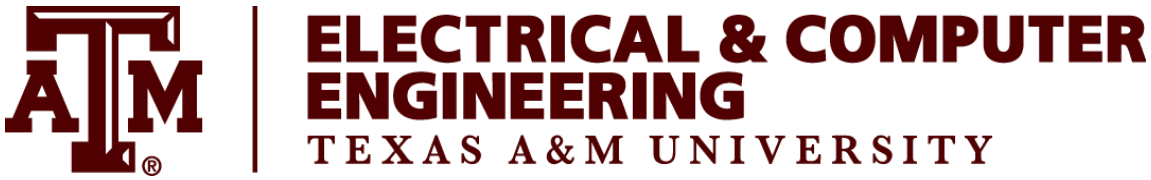

ECEN 325 Final Project:

Preliminary Report

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ECEN 325 - 502

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Introduction

The purpose of this project is to familiarize and test our understanding of a CMOS amplifier.

Design Requirements: Design a three-stage amplifier with Bipolar and CMOS transistors to satisfy the following constraints. Note, the design should use standard value resistors (no potentiometers).

- $|A_V| \geq 25$
- $R_{in} \geq 200k\Omega$
- 3 dB Bandwidth > 200kHz
- Harmonic distortion below -30dB with vimax = 5mVpk (10mVpp) measured at 10kHz input sine signal VCC = 5V (referred to a ground voltage of 0V)
- Output large-signal voltage swing of 2V peak.
- Rload = 8Ω. Note, you may have to use multiple transistors in parallel in the output stage to drive this load. Check the power ratings of the transistors.
- Use a minimum of 3 MOSFETs in your design. Note, if desired you can use more and also BJTS, but the intent is that MOSFETs are a key part of your design.

Design & Procedure

First Stage Values:

$$A_{V_1} = 10$$

$$V_{RS} = 1\ V,\ R_{Load} = 8\ \Omega$$

$$V_{RD} = \frac{\left(V_{DD} - V_O - V_{RS} \right)}{\left(1 + \left(\frac{2}{A_{V_1}} \right) \right)} = \frac{5 - 1 - 1}{\left(1 + \left(\frac{2}{10} \right) \right)} = 2.5\ V$$

$$Let\ V_{RD} = 2.25\ to\ avoid\ clipping,$$

$$V_O = \frac{2 \cdot V_{RD}}{|A_{V_1}|} = 0.5\ V$$

$$I_D = \frac{\beta}{2} \cdot V_O = 7.19\ mA$$

$$R_D = \frac{V_{RD}}{I_D} = 313\ \Omega$$

$$R_{G1} = \frac{200\ k\Omega \cdot 5}{(1 + 2.2 + 0.45)} = 274\ k\Omega$$

$$R_{G2} = 740.75\ k\Omega$$

Second and Third Stage Values :

$$A_{V_2} \cdot Av_3 = 19.4$$

$$I_X = \frac{V_O}{R_{Load}} = \frac{1}{8} = 0.125\ A$$

$$V_d = \frac{V_O}{A_{V_3}} = 1.93$$

$$V_{O(Vx)} = 1.876\ V$$

$$V_{RD} \leq \frac{\left(10 - 1.93 - 0.5 - 0.5 - 2 \cdot V_{RD}\right)}{19.4}$$

$$V_{RD} \leq 6.4 \approx 6$$

$$I_D = 5.37\ \mu A$$

$$V_{O(V2)} = \frac{226}{19.4} = 0.158$$

$$Hence,\ R_D = 1.1178\ M\Omega$$

$$R_{G1} = \frac{(10k \cdot 10)}{(0.5 + 1.5 + 0.158)} = 46.34\ k\Omega$$

$$R_{G2} = 12.75\ k\Omega$$

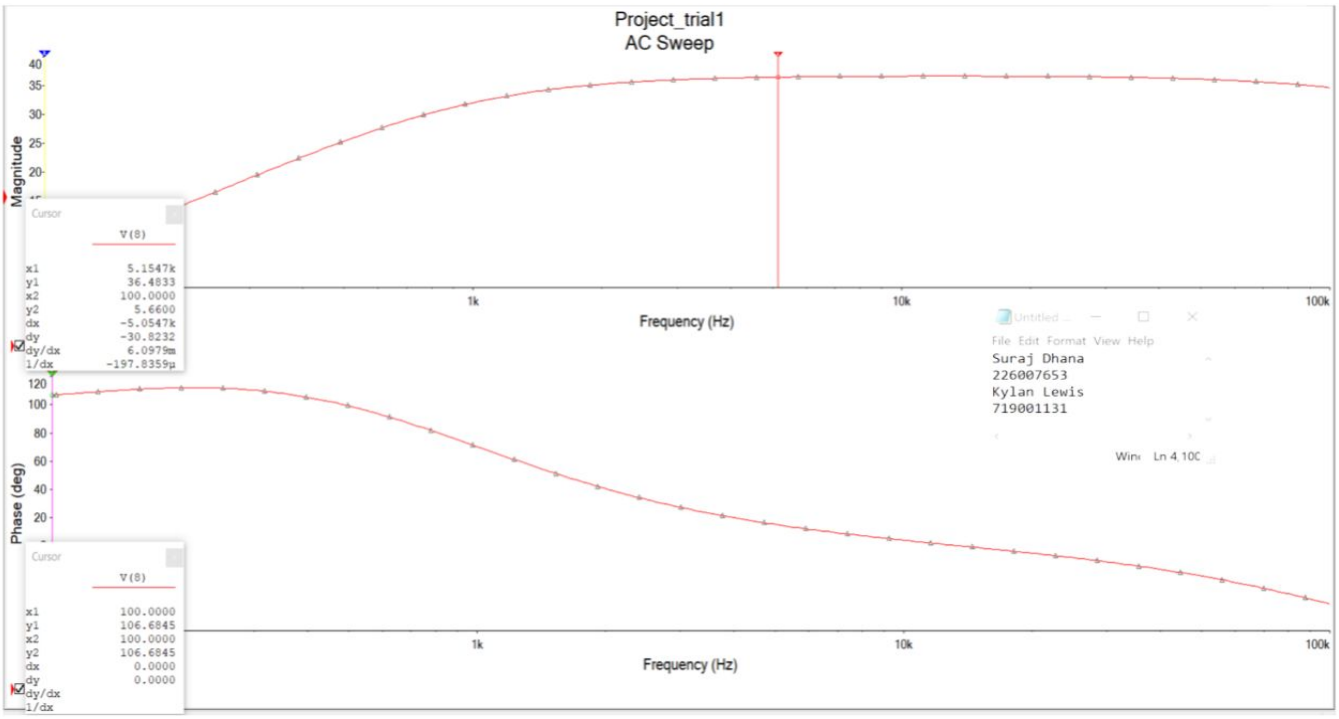
$$R_S = 93.157$$

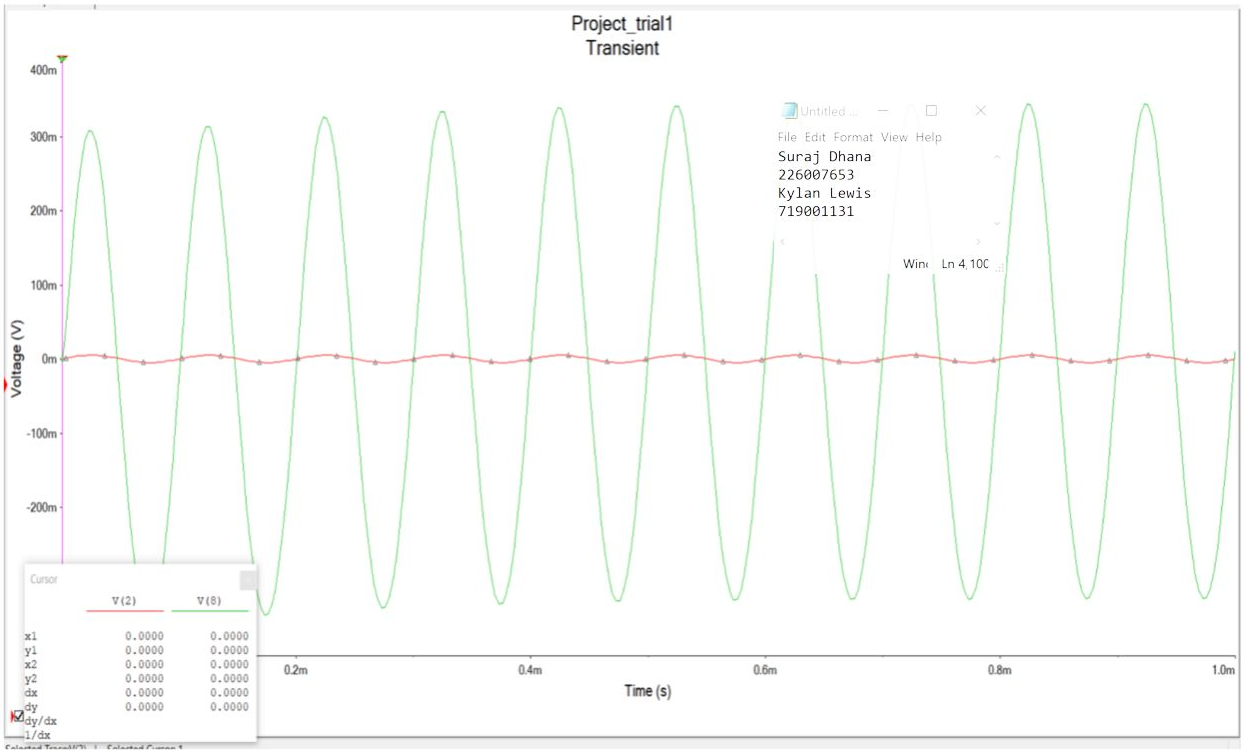
$$VR_{G4} = 1.25 + 2.2 + 1.876\ ;\ VR_{G4} = 5.33\ V$$

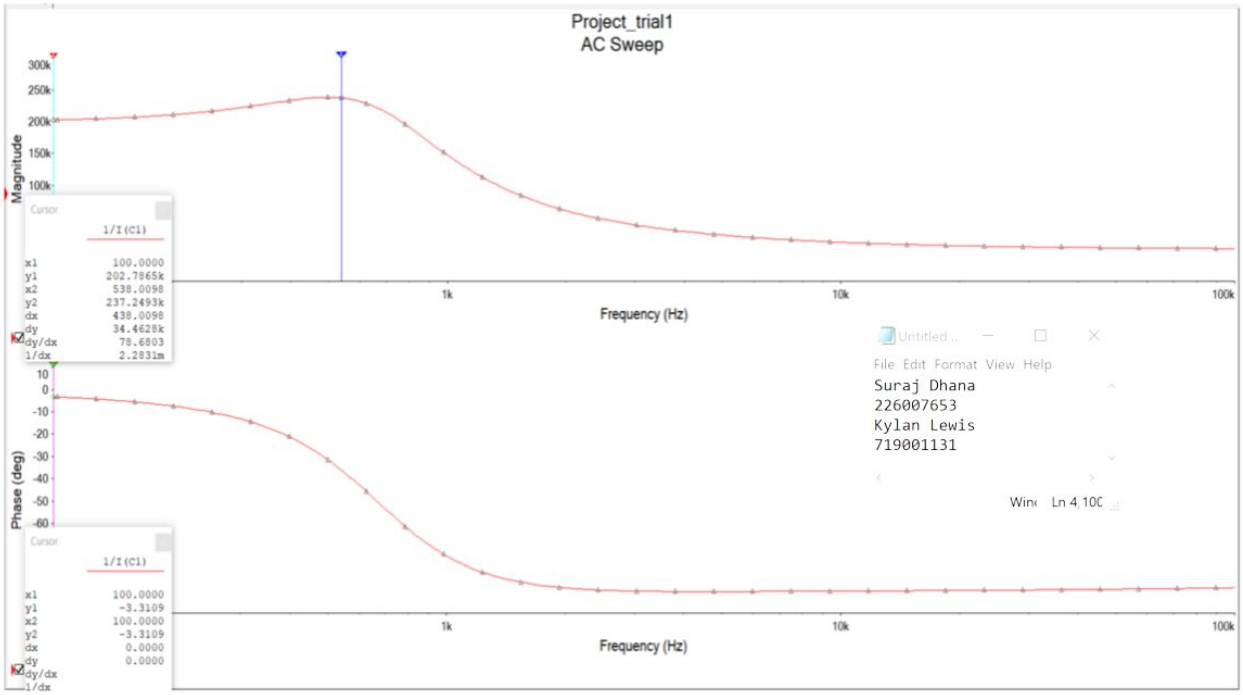
$$R_{G4} = 5.33\ k\Omega$$

$$R_{G3} = 4.67\ k\Omega$$

Simulation Results






Project_trial1
AC Sweep
Magnitude
Cursor
1/I(C1)
x1 100.0000
y1 202.7865k
x2 538.0098
y2 237.2493k
dx 438.0098
dy 34.4628k
dy/dx 78.6803
1/dx 2.2831m
Frequency (Hz)
Phase (deg)
Cursor
1/I(C1)
x1 100.0000
y1 -3.3109
x2 100.0000
y2 -3.3109
dx 0.0000
dy 0.0000
dy/dx
1/dx
Frequency (Hz)
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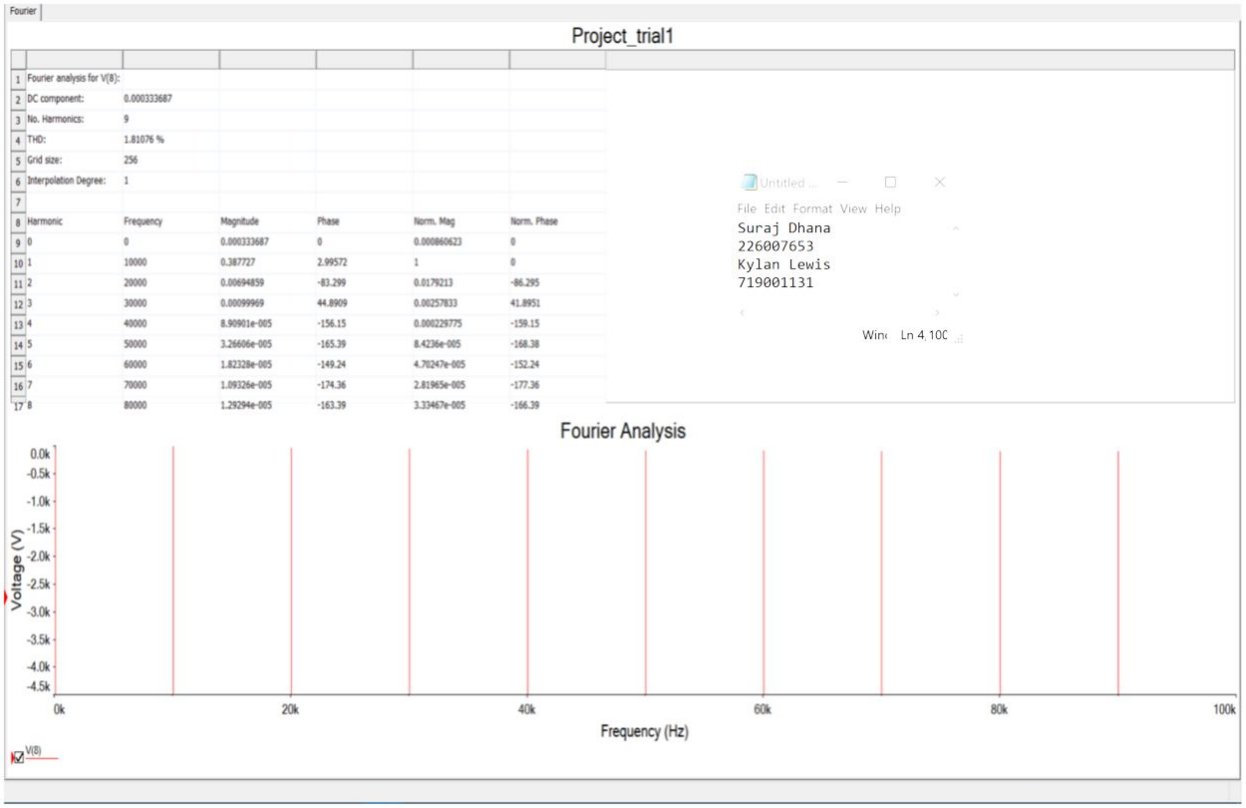
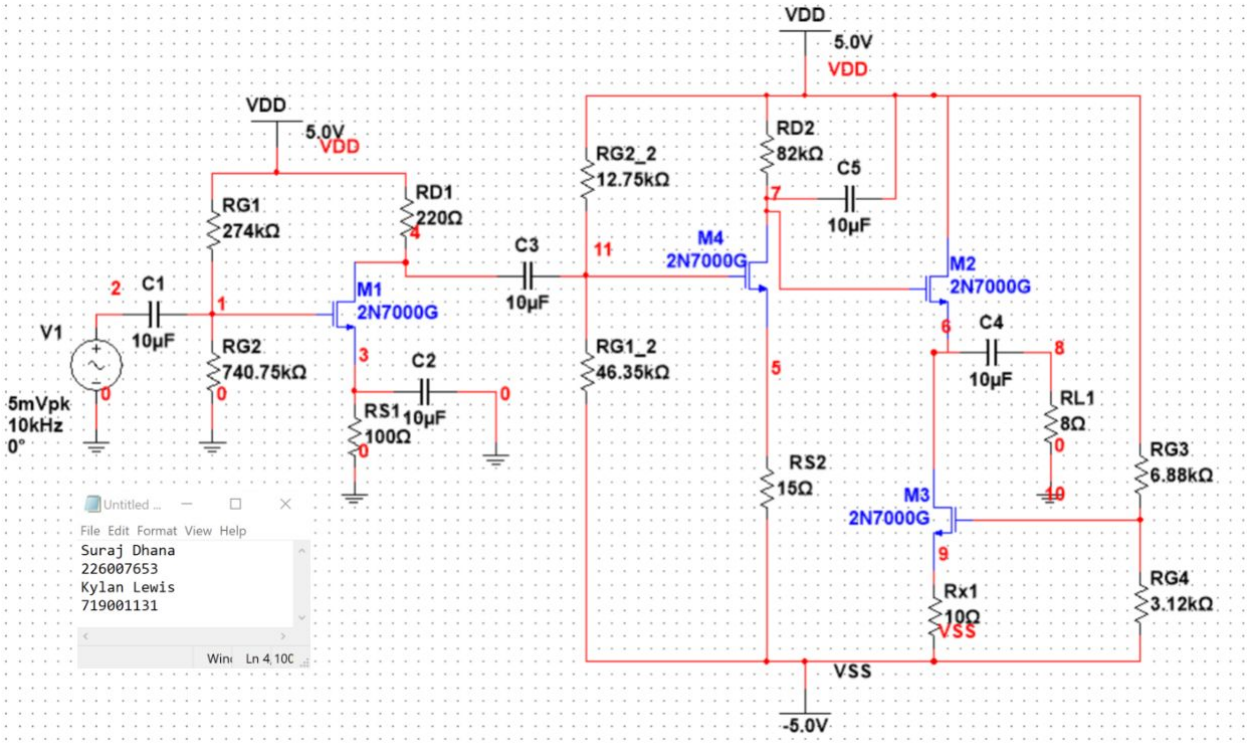
File Edit Format View Help
Suraj Dhana
226007653
Kylan Lewis
719001131
Ln 4, 10C


Fourier
Project_trial1
Fourier analysis for V(8):
DC component: 0.000333687
No. Harmonics: 9
THD: 1.81076 %
Grid size: 256
Interpolation Degree: 1
Harmonic | Frequency | Magnitude | Phase | Norm. Mag | Norm. Phase
0 | 0 | 0.000333687 | 0 | 0.000860623 | 0
1 | 10000 | 0.387727 | 2.99572 | 1 | 0
2 | 20000 | 0.00694859 | -83.299 | 0.0179213 | -86.295
3 | 30000 | 0.00099969 | 44.8909 | 0.00257833 | 41.8951
4 | 40000 | 8.90901e-005 | -156.15 | 0.000229775 | -159.15
5 | 50000 | 3.26606e-005 | -165.39 | 8.4236e-005 | -168.38
6 | 60000 | 1.82328e-005 | -149.24 | 4.70247e-005 | -152.24
7 | 70000 | 1.09326e-005 | -174.36 | 2.81965e-005 | -177.36
8 | 80000 | 1.29294e-005 | -163.39 | 3.33467e-005 | -166.39
Untitled ...
File Edit Format View Help
Suraj Dhana
226007653
Kylan Lewis
719001131
Ln 4, 10C
Fourier Analysis
Voltage (V)
Frequency (Hz)
V(8)

Final Design



Results

Specifications	Simulated Results
$\|A_V\| \geq 25$	36.48 dB = 66.71 Gain
Rin ≥ 200kOhms	202.7865 kOhms
3-dB Freq. ≥ 200kHz	210 kHz
THD < -30dBc	1.81076% = 34.83 dB
Total Power Dissipation	≈ 1200 mW
VDD & VSS	5 V and -5 V
MOSFETS Used (min 3)	4