ECEN 449/749 --- Microprocessor System Design

Fall 2020

Instructor:

- Sunil P Khatri, email:i r t a h k l i n u s (spell backwards, drop spaces) at tamu dot edu
- Phone:979-845-8371
- Zoom: https://tamu.zoom.us/j/9516377116?pwd=NVdkVks4WEhLYVFXMWpxNFZpOTVZdz09
- Office: Wisenbaker 333F

Class Hours:

Monday, Wednesday 04:15 pm - 05:10 pm, or
Lecture video will be posted shortly after each lecture

Lab Hours:

Labs can be done at home. Optionally you can go to the lab physically for 1/2 of a lab session, every other week.
Section 200/501/601: Thu, 8 AM - 9:50 AM, ZACH 333
Section 502/602: Thu, 11:10 AM - 1:00 PM, ZACH 333
Section 503/603: Thu, 2:20 PM - 4:10 PM, ZACH 333
Section 504/604: Fri, 8:00 AM - 9:50 AM, ZACH 333.
Section 505/605: Fri, 10:20 AM - 12:10 PM, ZACH 333.
Section 506/606: Fri, 12:40 PM - 2:30 PM, ZACH 333

Office hours (on zoom)

Mon 3:00pm - 4:00pm
Wed 3:00pm - 4:00pm

TA Information:

1. Name: Kyler Scott
   Sections: TBA
   Zoom: TBA
   E-mail: kylerrscott@tamu.edu
   Office Hours: TBA
2. Name: Ashwin Ashokan
   Sections: TBA
   Office: TBA
   E-mail: ash_win@tamu.edu
   Office Hours: TBA

Graders (all sections):

449and749graders@gmail.com

Class conscience:

TBA

2nd week : lab discussion zoom
3rd week : actual lab
"h/w s/w co-design"
"embedded system design"
sunilkhatri@tamu.edu
my zoom → 951 637 7116 449
10 - 515
Lec, OH = zoom
lab
zach
[ore name] 16 ppl
A B C D
12:40 - 1:30
1:30 - 2:20
2 Emails - received?
• web + ecampus
• chat/log in to zoom
• +/- 5m
you
me
Gaurav Bhalla (gauravbhalla@tamu.edu)

Resources:

1. Zybo Development Platform
   - Online Reference Manual
   - MicroBlaze Processor Reference
   - Zybo Board Reference Manual
   - FPGA Board Schematics
2. Logic Analyzer and Oscilloscope
   - Agilent 1673G Logic Analyzer
   - Agilent 54622D Mixed Signal Oscilloscope
3. Linux Documentation
   - Linux basics, command line interface etc.
   - O'Reilly's Linux Device Drivers, 3rd Ediltion
   - Linux on MicroBlaze Information
   - Man pages for internal Linux kernel functions
4. Verilog Documentation
   - Verilog Quick Reference
   - Verilog Reference Card
   - Longer Verilog Reference
   - Nonblocking and Blocking Assignments in Synthesizable Verilog
   - Designing FSM in Verilog

Class Notes:

Posted here on this web page. The notes are either developed by the course instructors or derived from other original copyrighted classnotes.

Grading policy:

- Homeworks 20%.
  - I will assign homework assignments on Wednesday, and you will have one week to turn in your solution via Ecampus. 50% credit will be given for homework that is late by a week. 0% credit will be given for homework that is late by more than a week.
  - Upload your homework solution to ecampus as a **single PDF** file.
  - Your homework solution should include a listing of any C code or Verilog code, along with any output obtained when the code is run. **DO NOT** include pictures of your code in your homework solution file, instead, copy the text of your C or Verilog code into your homework solution file.
  - **DO NOT** upload a zip file.
  - You will have only **ONE** attempt to upload your homework solution.
  - In addition, your source code (any C code or Verilog code or testbenches) should be sent via email to 449and749graders@gmail.com. Your email title should state your NAME, SECTION NUMBER and HOMEWORK NUMBER. Name your files in a way that identifies the homework number and the question (e.g. hw1-Q1b.v). For all the code that you write, please provide comments for full credit. Your code will be compiled and tested by the graders.
- Lab 30%
  - The lab grade will be equally divided among the number of lab sessions. You will be paired up based on the TA's discretion.
  - Lab reports must be turned in individually. Lab reports for week i should be turned in at the start of the lab of week i+1.
  - 50% credit will be given for reports that are late by a week. 0% credit will be given for reports that are late by more than a week.
  - For full credit, you should include comments in any code (Verilog or C) that you include in the lab report.

    - If any student misses a lab session, they will receive no credit at all for the lab session, even if they turn in the lab report for that lab session.
- Two tests 50%
    - Test1 (2 hours) 25%, Test2 (2 hours) 25%. Both tests will be open notes, and may include lab related questions. Test2 will be cumulative.
    - TEST 1: Wed March 6, 8pm to 10pm. Location TBA
    - TEST 2: Fri April 26, 8pm to 10pm. Location TBA
    - Extended office hours will be held in my office before each test. The times for these office hours will be announced closer to the time of the test.
- EE449 and EE749 will be graded on a separate curve. Graduate (EE749) students will have additional "G" questions on homework assignments and exams. These questions will be numbered "G1", "G2" etc. These questions are mandatory for students registered for ECEN 749, and will count towards the grade. If an ECEN 449 student attempts these questions, they will be graded, but will NOT count towards the grade.

Course Objective:

- The goal of this course is to provide the student with an in-depth knowledge of digital circuit design using an embedded platform as an implementation method. We will cover hardware and software co-design, using a commercial FPGA with an embedded on-chip microprocessor.
- At the end of the course the student should be able to view the design of digital systems from a embedded hardware/software perspective and obtain a set of fundamental concepts and design skills that can be applied to a wide variety of digital design problems.

Important Logistical Issues:

- As indicated in the first week of class, you are responsible to read this page and familiarize yourself with the important logistical information on it.
- *Excused absences:* Rules concerning excused absences may be found at http://student-rules.tamu.edu/rule7.htm. In particular, except for absences due to religious obligations, the student must notify his or her instructor in writing (acknowledged e-mail message is acceptable) prior to the date of absence if such notification is feasible. In cases where advance notification is not feasible (e.g., accident, or emergency) the student must provide notification by the end of the second working day after the absence. This notification should include an explanation of why notice could not be sent prior to the class. If the absence is excused, the instructor must either provide the student with an opportunity to make up any quiz, exam or other graded activities or provide a satisfactory alternative to be completed within 30 calendar days from the last day of the absence.
- *Days of religious observance:* By state law, if a student misses class due to an obligation of his or her religion, the absence is excused. A list of days of religious obligation for the coming semester may be found at http://dof.tamu.edu/faculty/policies/religiousobservance.php.
- *Disruptive behavior:* If a student's behavior in class is sufficiently disruptive to warrant immediate action, the instructor is entitled to remove a student on an interim basis, pending an informal hearing with the Head of the Department offering the course. This hearing must take place within three working days of the student's removal. This rule and supporting information may be found at http://studentrules.tamu.edu/rule21.htm.
- *Accommodations for students with disabilities:* It is the responsibility of the student to provide instructors with documentation showing they have registered with Disability Services and requested accommodation. Instructors then have the responsibility to work with Disability Services to provide reasonable accommodations. If a student who has not registered with Disability Services requests an accommodation, they should be referred to Disability Services at http://disability.tamu.edu .
- *Email Policy:* Please remember that your official TAMU email will be used as an official means of communicating class information to you.
- *Academic Honesty:* Remember that plagiarism will not be tolerated and will be dealt with under the Aggie Honor System Office guidelines. Upon discovering a suspected violation of the Aggie Honor code, I will contact the Aggie Honor System office http://www.tamu.edu/aggiehonor/.

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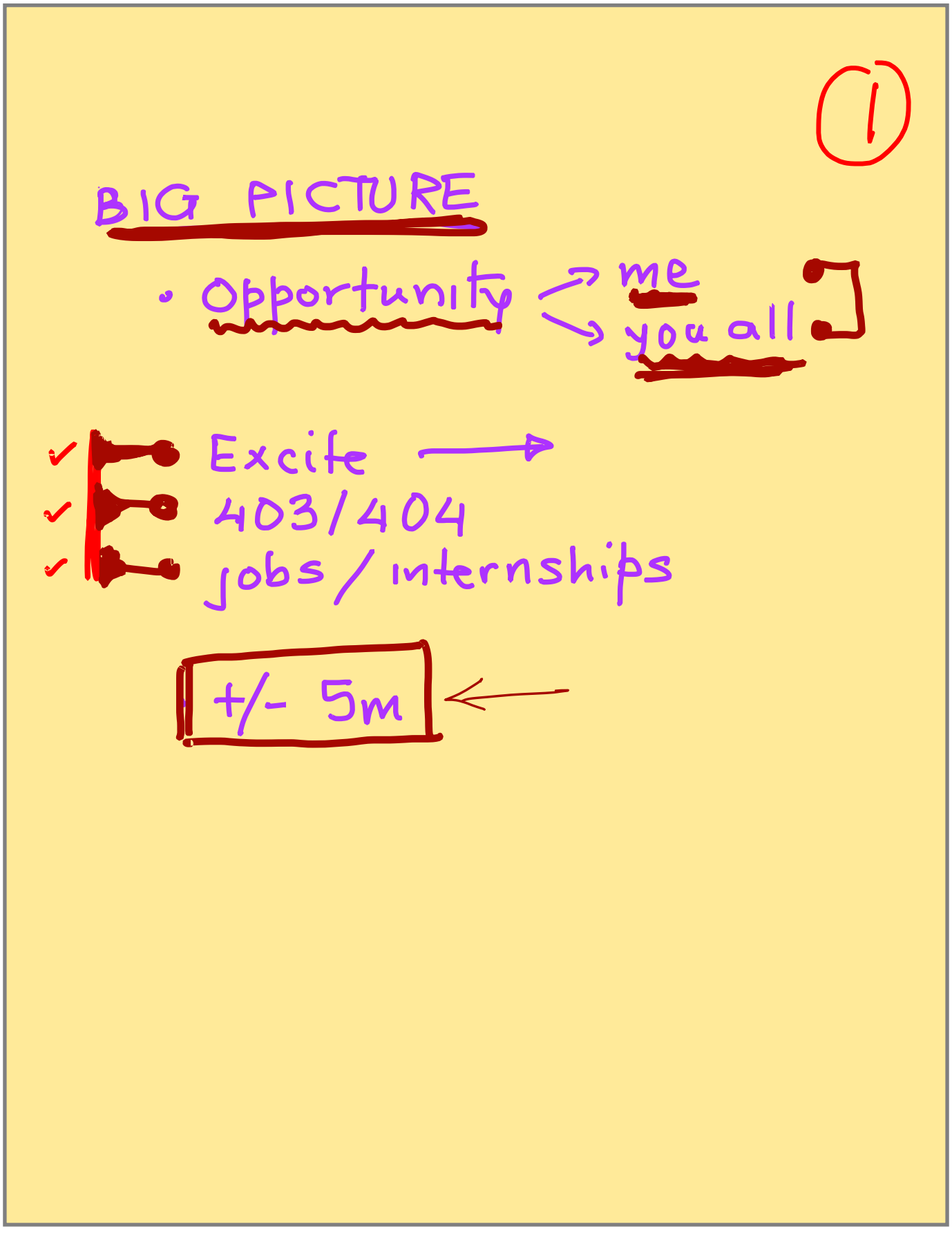
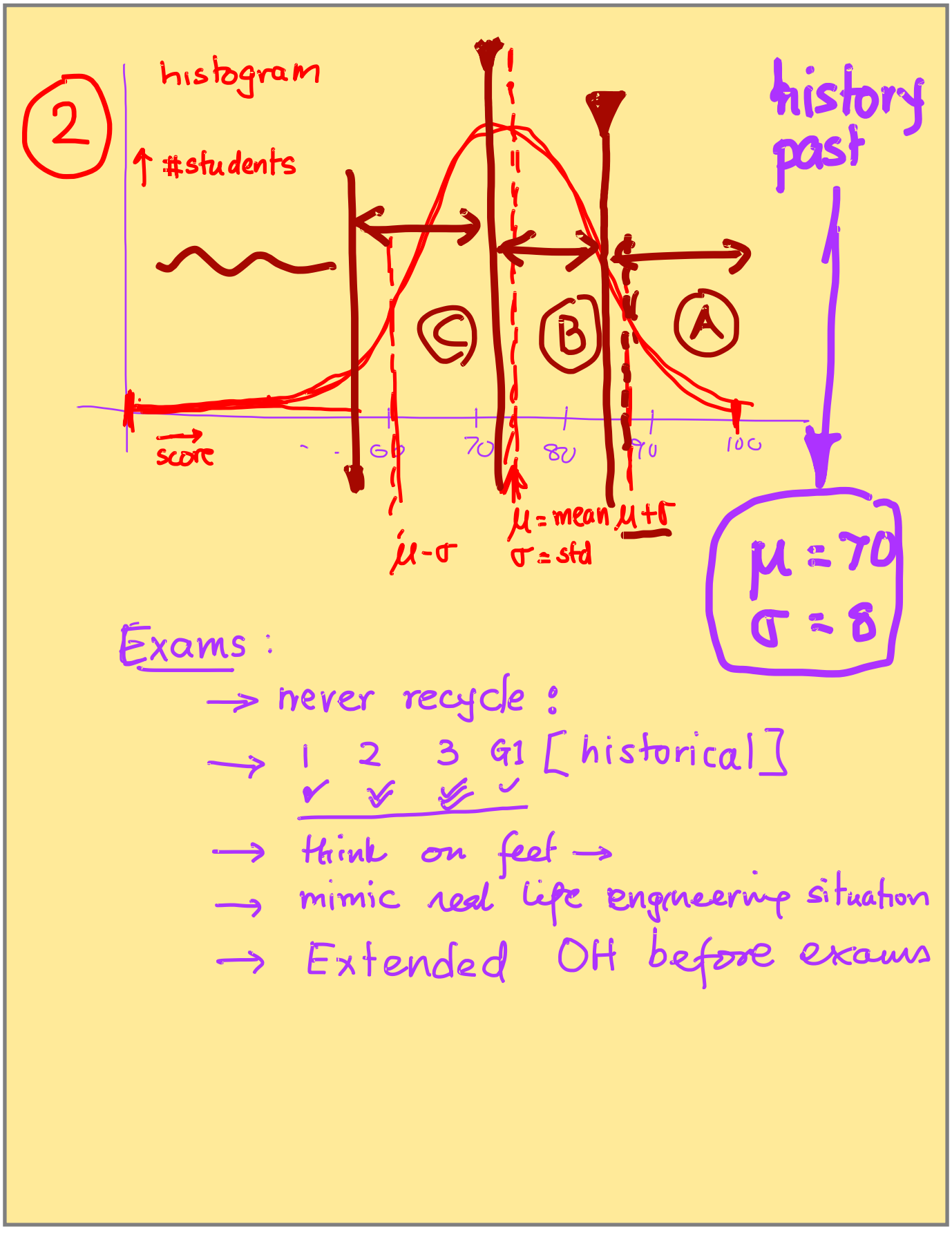
Tentative Schedule -subject to change

Week	Monday Topic	Wednesday Topic	Laboratory	Comments
1 (8/17, 8/19)	-	Class overview	No Lab this week!!! FPGA Board Reference Manual FPGA Board Schematics	Homework and Lab - Policy and Tips - PDF
2 (8/24, 8/26)	Verilog	Verilog	Lab1 - Vivado	
3 (8/31, 9/2)	Verilog	Verilog	Lab2 - SDK	
4 (9/07,9/09)	Verilog	C Programming	Lab3 - Hardware and Software	
5 (9/14, 9/16)	C Programming	Tips on C Programming	Lab4 - Booting Linux	
6 (9/21, 9/23)	FPGAs (User Aspects)	FPGAs (User Aspects)	Lab5 - Simple Kernel Module	
7 (9/28, 9/30)	Linux Introduction	Linux Introduction	Lab6 - Device Drivers	
8 (10/5, 10/7)	Linux Introduction	Linux Introduction	Lab7 -IR Remote HW	TEST 1 on Wed 10/7 8pm to 10pm. Location online.
9 (10/12, 10/14)	Exam discussion	Pulse Modulation	Continue with Lab 7	
10 (10/19,10/21)	Pulse modulation	Pulse modulation	Lab8 - Interrupt Driven IR Remote Device Driver	
11 (10/26, 10/28)	AC97 CODEC	Hardware-software Communication	Continue with Lab 8	
12 (11/2, 11/4)	Hardware-software Communication	FPGAs and reconfigurable computing	Lab9 - Linux built-in Kernel Modules	
13 (11/9, 11/13)	FPGAs and reconfigurable computing	FPGAs and reconfigurable computing	Complete Lab 9	
14 (11/16, 11/18)	Transmission Lines	Memories		
15 (11/23, 11/25)	Transmission Lines	---	---	
16 (11/30, 12/2)	---	---	---	TEST 2 on Thu 12/3 from 11am to 12:30pm. Location online


1
BIG PICTURE
• opportunity
me
you all
Excite
403/404
jobs / internships
+/- 5m



Exams :

→ never recycle !

→ 1 2 3 G1 [historical]

→ think on feet →

→ mimic real life engineering situation

→ Extended OH before exams

My appeal to you

(3)

(1) attend office hours

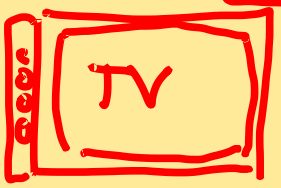
(2) do you HW - its 5% of grade for each HW!

- 48% 2 exams (4)
- 2% participation
- webpage up
- exam date →
- board purchased?
- honors "200"
- Lab — { no lab this week
  will meet in zoom
  to discuss logistics
  — { real labs next
  week

What is 449 about? 5

How we design digital systems today

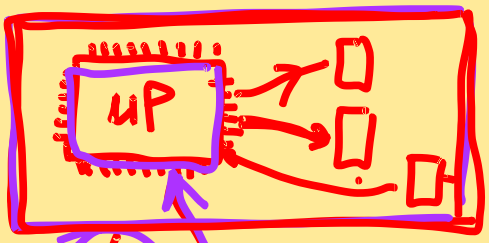
OLD



- all h/w custom built

☹ couldn't upgrade
☹ hard to design
☹ no forced obsolescence

NEW



s/w

☺ upgrade features
☺ easier to design
- faster to market
- share design across prod.

☹ forced obsolesc.