Kyle Patrick **May**

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Summary

Computer Systems Researcher

Strongly interested and involved with computer architecture research

- Primarily interested in, but not limited to, general purpose hardware accelerators, microarchitecture, hardware-software co-design, heterogeneous architectures, and resource-constrained computing
- Currently in final year of undergraduate degree
- Pursuing a PhD program that encourages the exploration of computer architecture, motivated by my drive to do research in industry and eventually return to academia to become a professor

Education

University of Michigan

Ann Arbor, MI

B.S.E. in Computer Engineering

Sept. 2015 - Exp. Apr. 2019

- **Current Research Area:** 'Reconfigurable Software-Defined Hardware Architectures'
- **Mentor:** Dr. Trevor Mudge
- **GPA:** 3.965 / 4.000
- **Relevant Coursework:** Advanced Topics in Computer Architecture (EECS 573), Computer Architecture (EECS 470), Introduction to Operating Systems (EECS 482), Data Structures and Algorithms (EECS 281)

Research Experience

University of Michigan - College of Engineering

Ann Arbor

Undergraduate Research Assistant : Dr. Trevor Mudge

Feb. 2018 - Present

- Developing a flexible, reconfigurable hardware architecture capable of supporting irregular workloads
- Tailoring an existing architectural simulator to model our proposed architecture
- Leading development of a flexible hardware prefetcher for the architecture in order to support both regular and irregular workloads
- Conducting literature surveys in order to fully understand prior work, in order to develop a novel prefetching framework
- Leveraging architectural simulator frameworks to quickly validate underlying assumptions and to further hone in on creating a high performance design
- Gaining experience working with popular benchmark suites and adapting the suites to work with our development environment, like the Lonestar benchmark suite
- Analyzing irregular workloads and their memory characteristics to fully understand what is required from the memory system to deliver high performance

University of Michigan - College of Engineering

Ann Arbor

Undergraduate Research Assistant : Dr. Trevor Mudge

May 2018 - June 2018

- Explored novel compiler techniques to efficiently execute sparse matrix-matrix and sparse matrix-vector operations on CPU architectures, trading off memory usage for simpler control flow
- Analyzed the compiler techniques on real hardware and an architectural simulator to determine implications of the compiler technique on the memory system and to analyze our solution
- Developed the compiler framework in order to generate efficient linear algebra operations
- Examined the scalability of the compiler technique on multi-core systems, modeling the interactions of multiple cores and their shared caches
- Learned about the gem5 architectural simulator, experimenting with the simulator while working on this project

University of Michigan - College of Engineering

Ann Arbor

Undergraduate Research Assistant : Dr. Robert Dick

Feb. 2017 - Present

- Creating a sensing module that can interface with both analog and digital sensors, provide signal processing capabilities, and transmit data to the cloud to further research in remote, battery-powered sensing applications
- Designed and prototyped analog signal conditioning circuitry to provide high levels of accuracy and precision in sensing applications
- Developed and debugged C and C++ code for interfacing with the data acquisition system, utilizing serial protocols such as SPI and I2C, to provide an intuitive and efficient interface between the hardware and software
- Produced a printed circuit board design that preserves the integrity of sensitive analog signal paths, as well as a board design that could be developed at scale
- Created and tested calibration algorithms to compensate for errors introduced by signal conditioning circuitry to improve the absolute accuracy of the data acquisition system
- Worked in an extremely independent capacity, while still collaborating with other students to solve major design issues
- Currently, mentoring students that continued the project after me, helping them overcome design and implementation obstacles and become comfortable with the uncertainty that comes with the research environment

Notable Projects

University of Michigan - College of Engineering

EECS 470

Out of Order Processor Design and Implementation

Winter 2018

- Tasked with the design of a fully out of order processor microarchitecture implementing a subset of the Alpha ISA
- Heavily involved with design and verification of all major components of the processor (front-end, back-end, memory hierarchy, etc.), gaining valuable insight into the intricate details of implementing a processor design in SystemVerilog
- Constrained by physical implications by synthesizing our design, ensuring that our design worked at an aggressive clock period (9.1ns)
- Implemented advanced features in our design, including (almost) arbitrary way superscalar execution, non-blocking data caches, an advanced load-store unit, and non-trivial branch prediction algorithms
- Optimized critical execution loop, allowing for a pipelined wake-up, select, issue logic to the functional units without losing the ability to issue dependent instructions back-to-back
- Acted in a leadership role to organize a team of 5 to meet deadlines and to efficiently produce the design and verification results needed

University of Michigan - College of Engineering

EECS 573

General Purpose Programmable Prefetcher

Fall 2018

- Tasked with a semester long, novel computer architecture research project
- Conducted in-depth surveys of recent literature in data and instruction prefetching to find a unexplored idea within the problem space
- Created simple experiments to test initial assumptions to quickly validate the basis of the project
- Gained experience with useful, common resources like gem5, Intel Pin, and benchmark suites like Lonestar, and used these tools throughout the project
- Currently designing and developing an architectural model of the proposed prefetching system, using the gem5 architectural simulator framework

University of Michigan - College of Engineering

EECS 482

Design and Implementation of Core Components of an Operating System

Fall 2018

- Designed and implemented a multi-threaded disk scheduler in C++ to gain experience in standard monitor-style multi-threaded programming
- From simple primitives like spin locks, created a user-level thread library that implemented mutual exclusion locks, condition variables, and a POSIX-style thread interface
- Learned how to use modern language constructs to efficiently implement kernel-level multi-threaded code
- Designed and developed a virtual memory pager, capable of implementing Linux-like system calls, such as fork and map
- Constructed a concurrent distributed file server application, focusing on concurrency and reliability

Skills

Programming Languages and Tools C/C++, Verilog/SystemVerilog, gem5, Intel Pin, git, Python, Matlab

Operating Systems Linux, MacOS, Windows

Miscellaneous SMT Soldering, Arduino-based prototyping, Mixed-signal circuit design, PCB design

Honors & Awards

University of Michigan

James B. Angell Scholar, 2017, 2018

University Honors, 2016, 2017, 2018

Dean's List, 2015, 2016, 2017, 2018

Most Active Electee : HKN-IEEE, 2017

Extracurriculars

Eta Kappa Nu - Beta Epsilon

EECS Honor Society

Sept. 2017 - PRESENT

- Joined a volunteering- and professional-orient student organization to become more involved in the University of Michigan community.
- Participated in mentor-ship opportunities, holding office hours for introductory electrical engineering and computer science courses.
- Volunteered at the local nature preserves to help remove invasive species that were threatening local species.