# Two Bit Adder Circuit

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## Goals of the Experiment

To continue with lab 1 by combining a two bit adder circuit to the full adder circuit using MAX7008 family in Quartus 9. The full adder circuit has been created into a symbol to minimize the complexity of the circuit.

## Theory of Operation

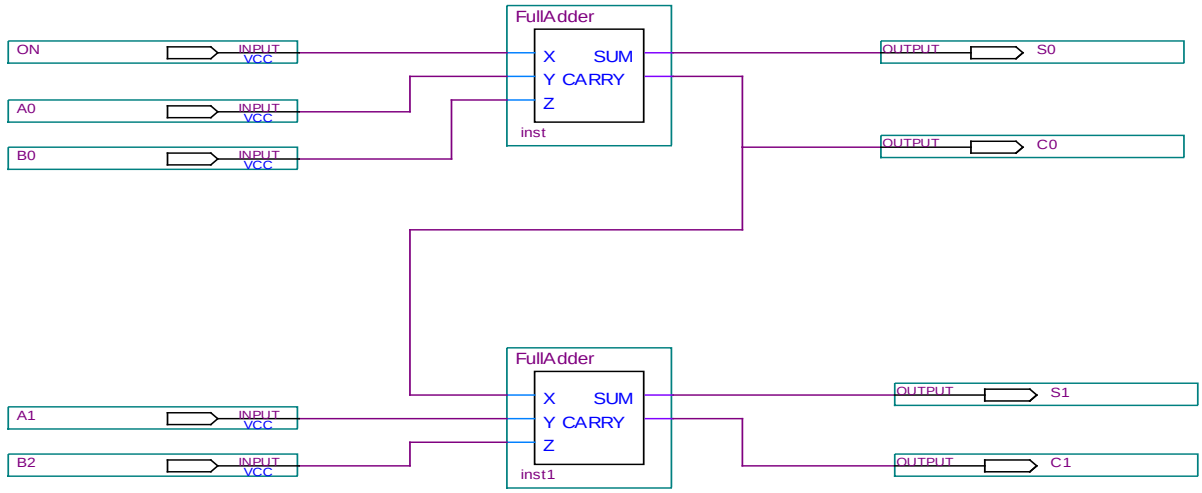
A two-bit adder can add two binary bits together by taking a carry from the next lower order of magnitude and sending a carry to the next higher order of magnitude. For a multi-bit operation, each bit must be represented by a full adder and must be added simultaneously.

### *Truth Table*

| INPUTS | | | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|
| A0 | A1 | B0 | B1 | Ci | S0 | S1 | Co |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## Schematics of the Circuit

The graphic schematic below shows the two bit adder connected by inputs to the black box or the full adder.



## Experimental Results

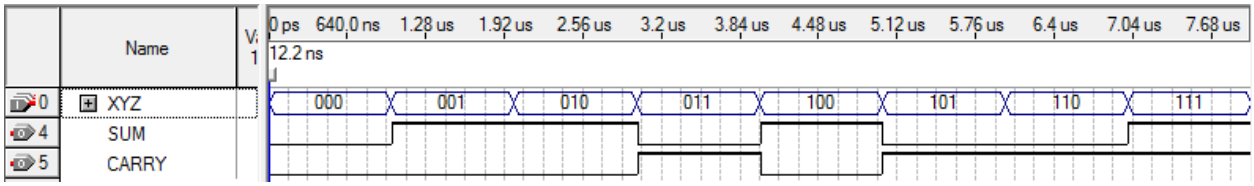
The schematic has been compiled below in order to prepare for the simulation of the circuit. Then, the values are specified in the Waveform editor for the input and for the time intervals.

### *Compilation Results*

| | |
|---|---|
| Flow Status | Successful - Mon Feb 05 11:43:07 2018 |
| Quartus II Version | 9.1 Build 350 03/24/2010 SP 2 SJ Web Edition |
| Revision Name | FullAdder |
| Top-level Entity Name | FullAdder |
| Family | MAX7000S |
| Device | EPM7128SLC84-7 |
| Timing Models | Final |
| Met timing requirements | Yes |
| Total macrocells | 2 / 128 ( 2 % ) |
| Total pins | 9 / 68 ( 13 % ) |

### *Simulation Results*

Below are the Compilation and Waveform chart for the two-bit adder circuit. The outputs for the addition and subtraction are correct. The simulation is based on an 8 micro-second end time with a 1 micro-second count time.




## Conclusion

The Truth table, schematic, compilation, and simulation for the two bit adder were successful. There were no errors to document in the compilation or simulation. The simulations success is documented below. The circuit will be suitable to proceed to Lab 3.

```
Info: Using vector source file "E:/Wayne State U/EET 3100/NEW LAB 1/FullAdder.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is      85.71 %
Info: Number of transitions in simulation is 35
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```