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EET 3100: Advanced Digital Design

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Sequence Detector Circuit

Goals of the Experiment:

Design a one-input, one-output sequence detector, that produces an output 1 every time the sequence 1111 is detected and an output 0 at all other times. The circuit is also required to recognize overlapping sequences, with the output string z that results from the following input string x using JK flip-flops.

The following input string will be used as part of the simulation x=1101111111010 and output string z=0000001111000. The sequence detector will be designed in schematic form to be compiled for simulation using the MAX7008S family on the EPM7129LS84-7 device in the Quartus 9.1 software.

Theory of Operation:

Flip Flops

A digital computer needs devices which can store information. A flip flop is a binary storage device that can store a binary bit as either 0 or 1. It has two stable states HIGH and LOW i.e. 1 and 0. It has the property to remain in one state indefinitely until it is directed by an input signal to switch over to the other state. It is also called bistable multivibrator.

The basic primary formation of a flip flop is to store data. They can be used to keep a record or what value of variable (input, output or intermediate). Flip flops are also used to exercise control over the functionality of a digital circuit i.e., change the operation of a circuit depending on the state of one or more flip flops. These devices are mainly used in situations which require one or more of the following three: Operations, storage, and sequencing.

JK Flip Flops

The JK flip flop is probably the most widely used and is considered the universal flip flop because it can be used in many ways. A JK flip flop is a modified version of an SR flip flop with no “invalid” output state. And this is achieved by the addition of a clock input circuitry with the SR flip flop which prevents the “invalid “output condition that can occur when both inputs S and R are equal to logic level “1”.

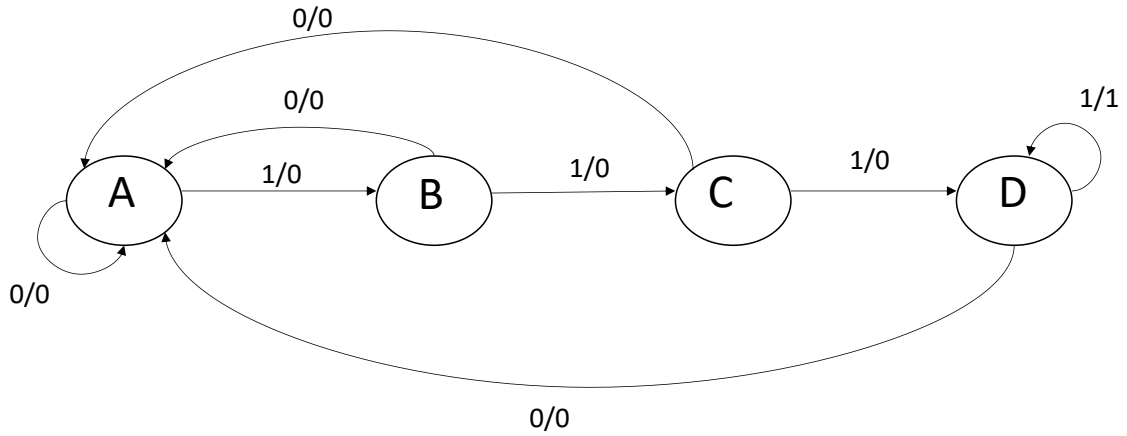
JK flip flops are bistable circuits made up of logic gates. They exist in either of two stable states indefinitely or can be made to change its state by means of some external signal.

JK Flip Flop Applications

Common applications for JK flip flops include:

- Registers.
- Counters.
- Event Detectors.
- Data Synchronizers.
- Frequency Divider.

State Diagram



Excitation Table

PS	NS	
	x=0	x=1
A	A,0	B,0
B	A,0	C,0
C	A,0	D,0
D	A,0	D,1

PS		NS	
		x=0	x=1
M	N	MN	MN
0	0	00,0	01,0
0	1	00,0	11,0
1	1	00,0	10,0
1	0	00,0	10,1

K-Map

M	N \ X	0	1
0	0	0	0
0	1	0	1
1	1	x	x
1	0	x	x

J_M= Nx

M	N \ X	0	1
0	0	0	1
0	1	x	x
1	1	x	x
1	0	0	0

J_N= M'x

M	N \ X	0	1
0	0	x	x
0	1	x	x
1	1	1	0
1	0	1	0

K_M= x'

M	N \ X	0	1
0	0	x	x
0	1	x	0
1	1	1	1
1	0	x	x

K_N= x' + M

M	N \ X	0	1
0	0	0	0
0	1	0	0
1	1	0	0
1	0	0	1

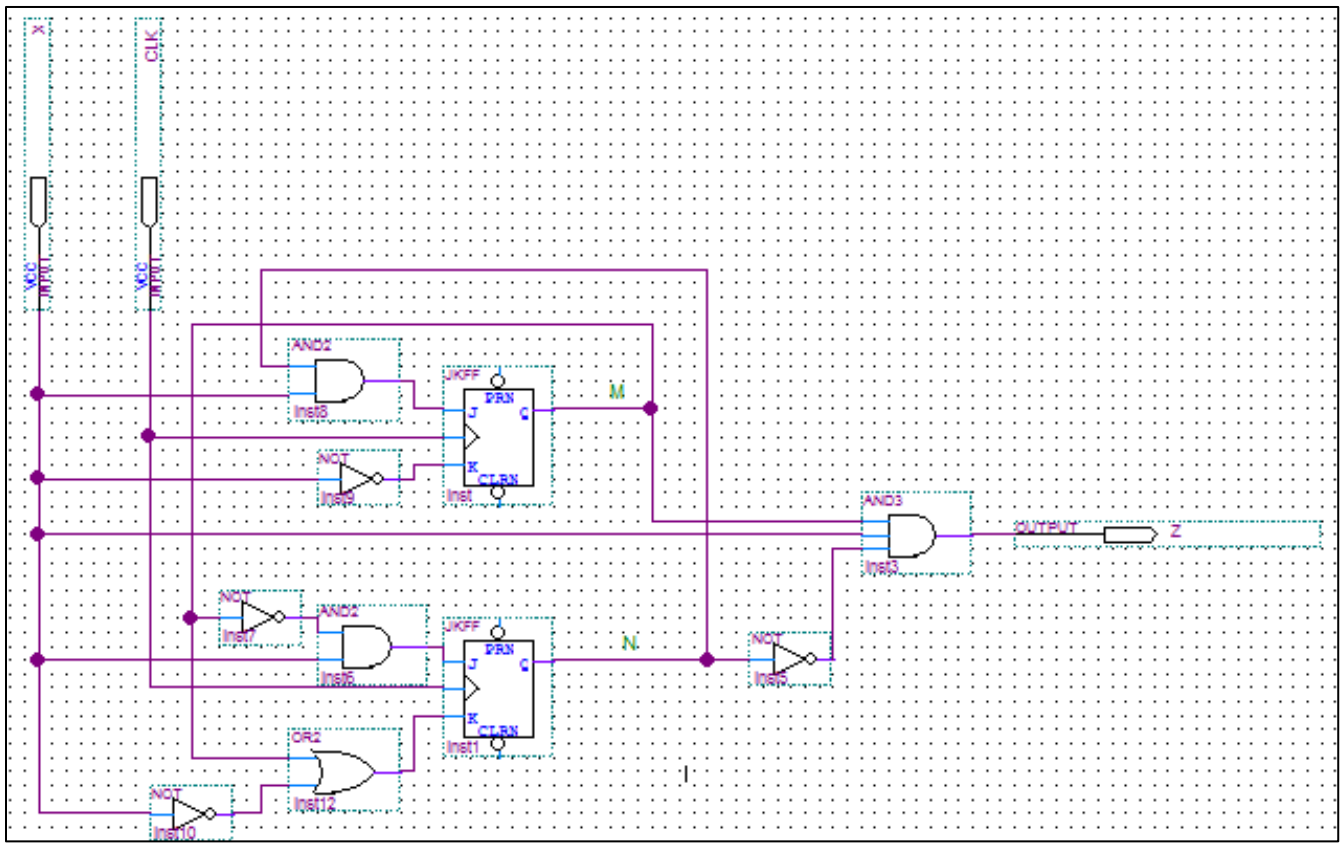
Z= MN'x

Schematics of the Circuit:

A schematic was designed from state diagram, excitation table, and k-map. If the J and K input are both at 1 and the clock pulse is applied, then the output will change state, regardless of its previous condition. If both J and K inputs are at 0 and the clock pulse is applied will result in no change in the output. There is no indeterminate condition in the operation of JK flip flop i.e. it has no ambiguous state. If J and K are different then the output Q takes the value of J at the next clock edge.

If J and K are both LOW then no change occurs. If J and K are both HIGH at the clock edge then the output will toggle from one state to the other. It can perform the functions of the SET/RESET flip-flop and has the advantage that there are no ambiguous states. It can also act as a T flip-flop to accomplish toggling action if J and K are tied together. This TOGGLE application finds extensive use in binary counters.

Schematic



Experimental Results:

The schematic was compiled to expedite synthesis of the circuit into waveform for simulation analysis. The results from the compilation were used as values for preparation of the waveform editor. The compilation and simulation success are documented below.

Compilation Results

Flow Status	Successful - Mon Feb 26 11:02:50 2018
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	Detector
Top-level Entity Name	Detector
Family	MAX7000S
Device	EPM7128SLC84-7
Timing Models	Final
Met timing requirements	Yes
Total macrocells	3 / 128 (2 %)
Total pins	7 / 68 (10 %)

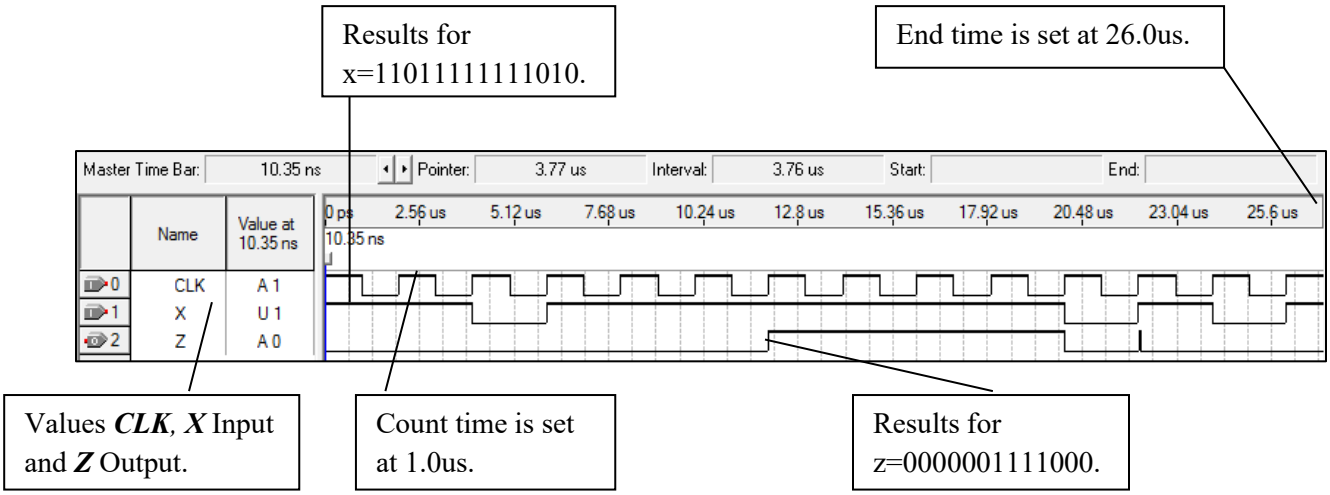
Flow: Compilation

Task	Time
Compile Design	00:00:13
Analysis & Synthesis	00:00:07
Fitter (Place & Route)	00:00:02
Assembler (Generate programming files)	00:00:02
Classic Timing Analysis	00:00:02

```
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 2 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 2 warnings
```

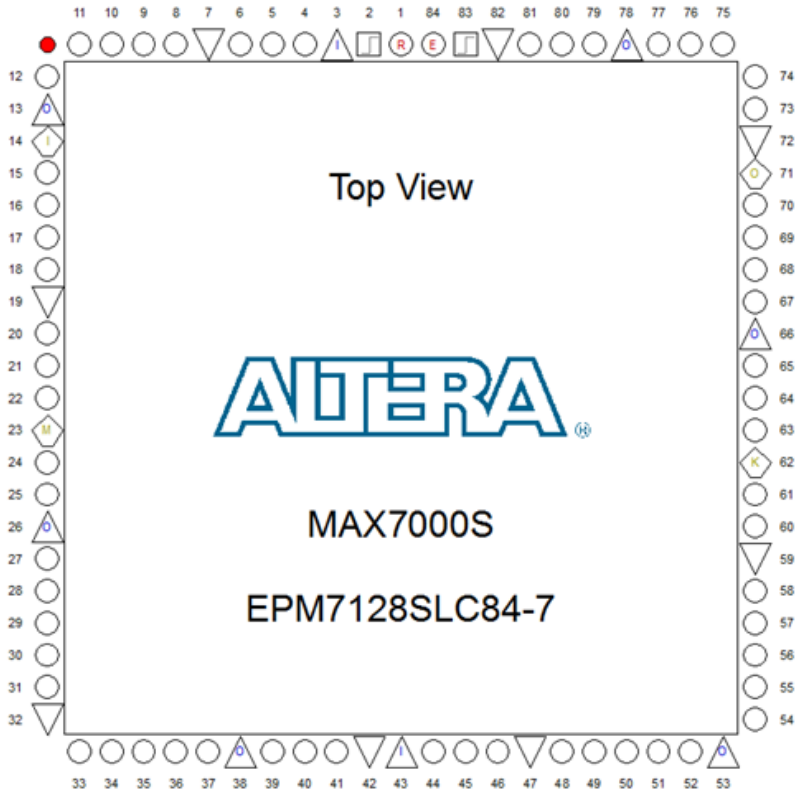
Simulation Results

Below is the Waveform for the sequence detector circuit. The simulation is based on a 26.0us end time with a 1.0us count time as denoted.




```
Info: Number of transitions in simulation is 46
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```

Pin Assignment



Conclusion

A sequence detector circuit was designed using *JK Flip Flops* with *CLK* and *X* as inputs and *Z* as the output. Based on the state diagram, excitation table, and k-map a schematic was designed for compilation and simulation that provided successful results. There were no errors to document in the compilation or simulation reports. The circuit is suitable to proceed to the next step in the design.

Reference Page

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