

# Full Adder Circuit

## Goals of the Experiment

To design a full adder circuit using MAX 10(DA/DF/DC/SA/SC) family in Quartus 17.1. The full adder circuit will be created into a symbol to minimize the complexity of the circuit.

## Theory of Operation

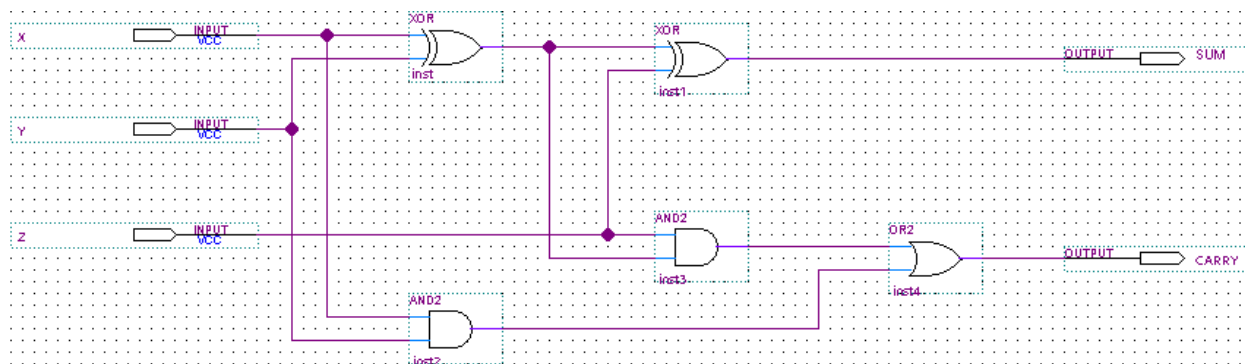
Full Adders are a circuit that will add a carry bit from another full or half adder and two operand bits to produce a sum bit and a carry bit. Full Adders can add two 1-bit numbers and accept a carry bit from a previous adder stage.

### Truth Table

X	Y	Z	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

## Schematics of the Circuit

The graphic schematic below shows the full adder connected by, XOR, OR, and AND gates.







The schematic has been compiled below in order to prepare for the simulation of the circuit. Then, the values need to be specified in the Waveform editor for the input and also the time intervals.



## Compilation Results

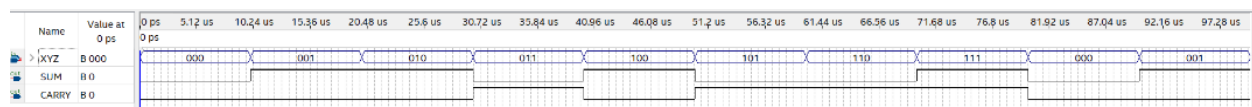
Flow Status	Successful - Mon Jan 29 11:27:38 2018
Quartus Prime Version	17.1.0 Build 590 10/25/2017 SJ Lite Edition
Revision Name	FullAdder
Top-level Entity Name	FullAdder
Family	MAX 10
Device	10M08DAF484C8G
Timing Models	Final
Total logic elements	3 / 8,064 (< 1 %)
Total registers	0
Total pins	5 / 250 (2 %)
Total virtual pins	0
Total memory bits	0 / 387,072 (0 %)
Embedded Multiplier 9-bit elements	0 / 48 (0 %)
Total PLLs	0 / 2 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 1 (0 %)



 Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 5 warnings  


 293000 Quartus Prime Full Compilation was successful. 0 errors, 13 warnings

## Experimental Results

Below are the Compilation and Waveform chart for this circuit. The outputs for the addition and subtraction are correct. This would lead to the belief that the circuit was graphically represented properly.

## Simulation Results



## Conclusion

The Truth table, schematic, compilation, and simulation were successful. There were no errors to document in the compilation or simulation. The circuit will be suitable for further development with FPGA developmental board.

