Two-Bit Binary Counter Circuit

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Goals of the Experiment

To design a two-bit counter circuit given the following state diagram listed below. The two-bit binary counter will be designed in schematic form to be compiled for simulation using the MAX7008S family on the EPM7129LS84-7 device in the Quartus 9.1 software. The circuit is required to repeat sequences when an external input X is equal to 1. When the external input X is equal 0, the circuit should remain unchanged. The circuit needs to be designed by utilizing JK flip-flops.

Theory of Operation

Counters

A counter is a digital sequential logic device that will go through certain predefined states (for example counting up or down) based on the application of the input pulses. They are utilized in almost all computers and digital electronics systems. Counters are one of the most important sequential circuits. Counter is the widest application of flip-flops. It is a group of flip-flops with a clock signal applied.

Counters are of two types:

- Asynchronous or ripple counters
- Synchronous counters

Counter Design

Synchronous Counters is a counter that's constructed with one common clock signal as the input to al the flip-flops simultaneously. Ripple counters are referred to as asynchronous counters. The output of one stage serves as the clock input to the next stage. Count Modulus (MOD**)** is the total number of states generated by the counter as it progresses through its specified sequence. The MOD is one of the most important characteristics to specify when classifying a counter since it determines the number of values in the count sequence and determines the frequency division capabilities of the counter.

A counter is a circuit that counts pulses. It is used in many circuit applications, such as event counting and sequencing, timing, frequency division, and control. A basic counter can be enhanced to incorporate functions such as synchronous or asynchronous parallel loading, synchronous or asynchronous clear, countable, directional control, and output decoding.

JK Flip Flops

The JK flip flop is probably the most widely used and is considered the universal flip flop because it can be used in many ways. A JK flip flop is a modified version of an SR flip flop with no "invalid" output state. And this is achieved by the addition of a clock input circuitry with the SR flip flop which prevents the "invalid "output condition that can occur when both inputs S and

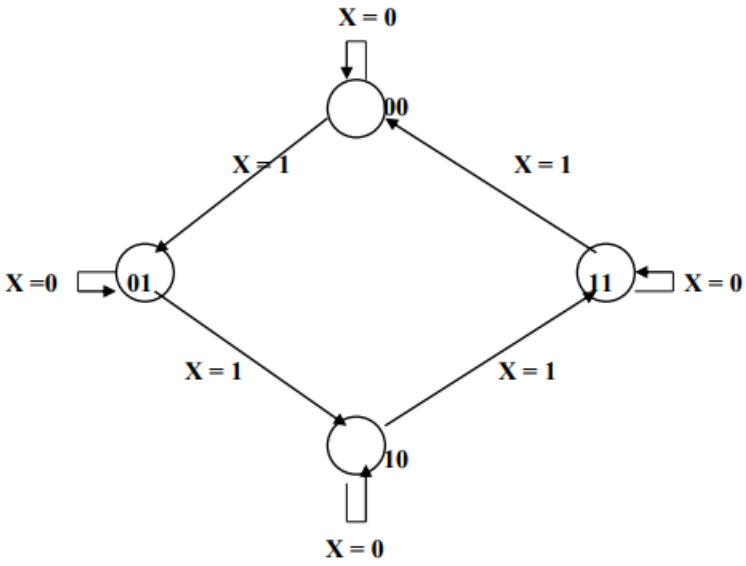
R are equal to logic level “1”. JK flip-flops are bistable circuits made up of logic gates. They exist in either of two stable states indefinitely and can be made to change its state by means of some external signal.

Counter Applications

Common applications for Counters include:

- Frequency counters
- Digital clock
- Time measurement
- A to D converter
- Frequency divider circuits
- Digital triangular wave generator

State Diagram



Excitation Table

PS		NS x=0	NS x=1
A	**B**	**AB**	**AB**
0	0	00	01
0	1	01	10
1	1	11	00
1	0	10	11

K-Map

A	B \ X	0	1
0	0	0	0
0	1	0	1
1	1	x	x
1	0	x	x

$J_A = Bx$

A	B \ X	0	1
0	0	x	x
0	1	x	x
1	1	0	1
1	0	0	0

$K_A = Bx$

A	B \ X	0	1
0	0	0	1
0	1	x	x
1	1	x	x
1	0	0	1

$J_B = x$

A	B \ X	0	1
0	0	x	x
0	1	x	1
1	1	x	1
1	0	0	x

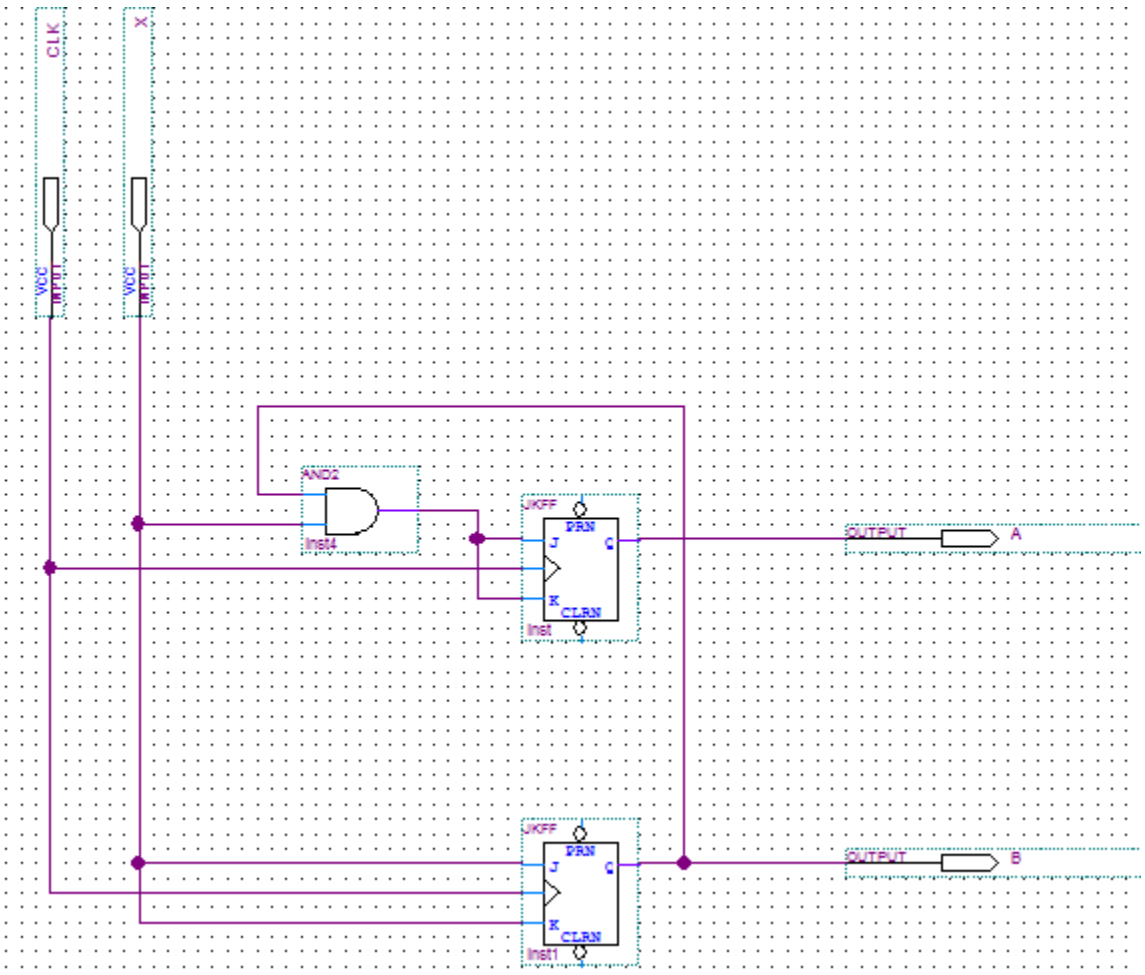
$K_B = x$

Schematics of the Circuit

A schematic was designed from state diagram, excitation table, and k-map. If the J and K input are both at 1 and the clock pulse is applied, then the output will change state, regardless of its previous condition. If both J and K inputs are at 0 and the clock pulse is applied will result in no change in the output. There is no indeterminate condition in the operation of JK flip flop i.e. it has no ambiguous state. If J and K are different then the output Q takes the value of J at the next clock edge.

If J and K are both LOW, then no change occurs. If J and K are both HIGH at the clock edge, then the output will toggle from one state to the other. It can perform the functions of the SET/RESET flip-flop and has the advantage that there are no ambiguous states. It can also act as a T flip-flop to accomplish toggling action if J and K are tied together. This TOGGLE application finds extensive use in binary counters.

Schematic



Experimental Results

The schematic was compiled to expedite synthesis of the circuit into waveform for simulation analysis. The results from the compilation were used as input values for preparation of the waveform editor. The compilation and simulation success are documented below.

Compilation Results

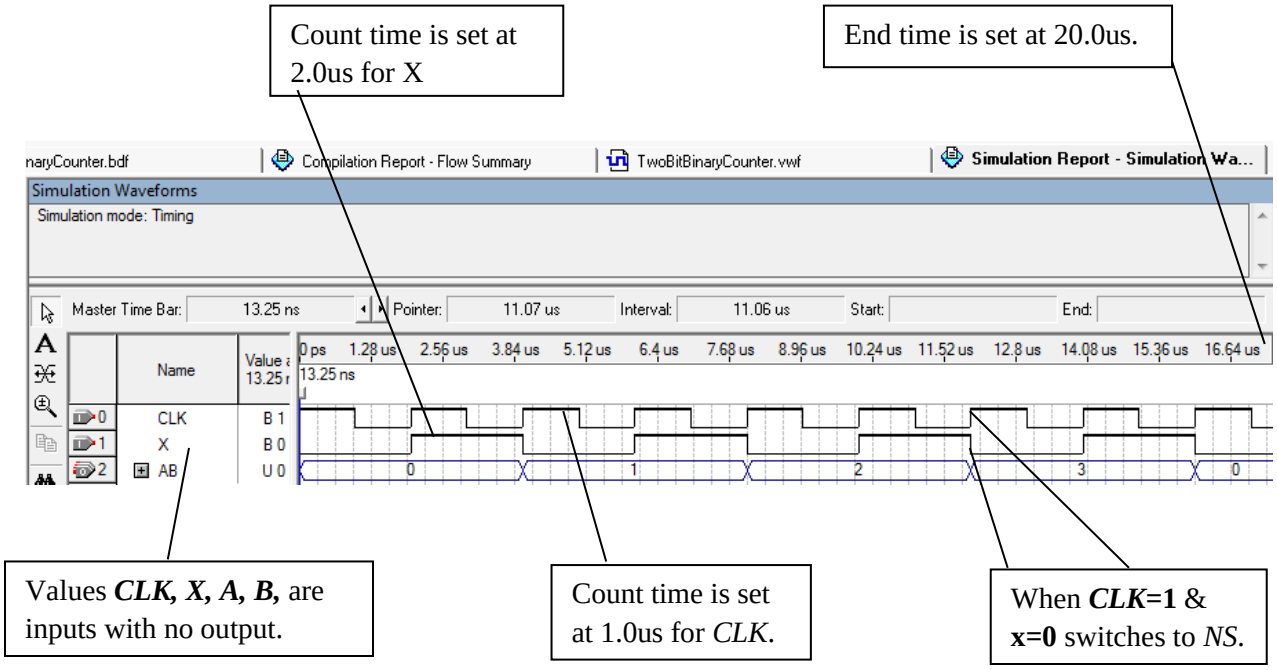
Flow Status	Successful - Mon Mar 05 11:31:55 2018
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	TwoBitBinaryCounter
Top-level Entity Name	TwoBitBinaryCounter
Family	MAX7000S
Device	EPM7128SLC84-7
Timing Models	Final
Met timing requirements	Yes
Total macrocells	2 / 128 (2 %)
Total pins	8 / 68 (12 %)

Task	Time
Compile Design	00:00:10
Analysis & Synthesis	00:00:03
Fitter (Place & Route)	00:00:02
Assembler (Generate programming files)	00:00:03
Classic Timing Analysis	00:00:02

```
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 2 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 2 warnings
```

Simulation Results

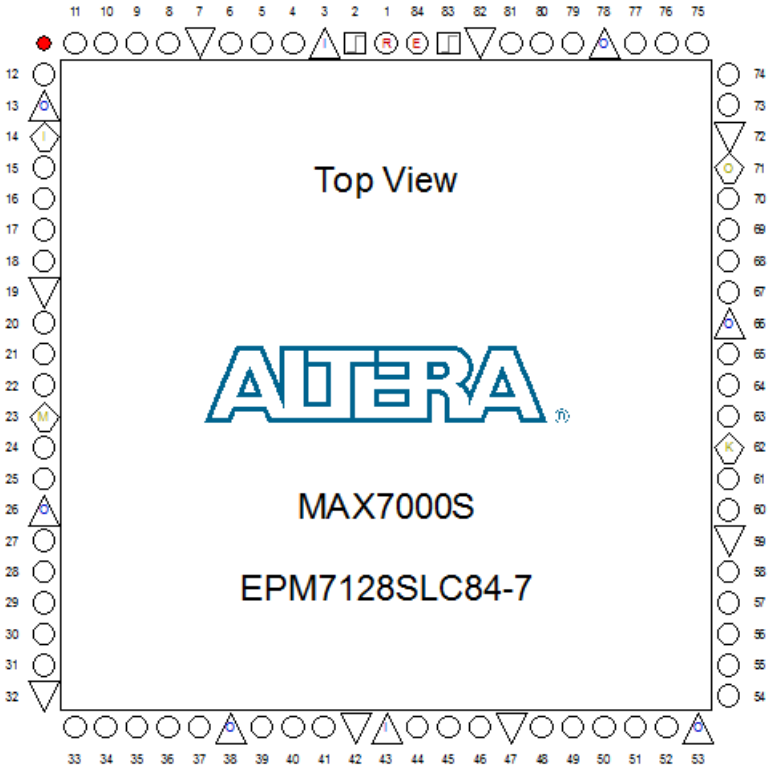
Below is the Waveform for the sequence detector circuit. The simulation is based on a 20.0us end time with a 1.0us count time as denoted.




```
Info: Simulation coverage is      100.00 %
Info: Number of transitions in simulation is 40
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```

Pin Assignment

Node Name	Direction
A	Output
B	Output
CLK	Input
TCK	Input
TDI	Input
TDO	Output
TMS	Input
X	Input



Conclusion

A two-bit counter circuit was designed using *JK Flip Flops* with *CLK*, *X*, *A*, and *B* as inputs with no outputs. From the given state diagram an excitation table and k-map were designed into a schematic for compilation and simulation that provided successful results. There were no errors to document in the compilation or simulation reports. The circuit is suitable to proceed to the next step in the design.

Reference Page

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