Bi-Directional Shift Register Design

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Goals of the Experiment

To design a bi-directional shift register circuit from lecture 9s, shift right/left example. The bi-directional shift register will be designed in schematic form to be compiled for simulation using the MAX7008S family on the EPM7129LS84-7 device in the Quartus 9.1 software.

There are two shifts needed to be performed: (1) All flip-flops are initially cleared with A1 being clocked into the shift register followed by a string of 0's (Right shift in/Left shift in). (2) A1 is clocked into the shift register, followed by a string of 1s (Right shift in/Left shift in). The circuit will be utilizing D Flip-Flops.

Theory of Operation

Shift Register

A shift register (abbreviated SRG*n* for an *n*-bit circuit) is *synchronous sequential circuit* that will store or move data. It consists of several flip-flops, which are connected so that the data is transferred into and out the flip-flops in a standard pattern. Shift registers are often used to interface digital systems situated remotely from each other. For example, suppose it is necessary to transmit an *n*-bit quantity between two points. If the distance is far, it will be expensive to use *n* lines to transmit the *n* bits in parallel. It is more economical to use a single line and transmit the information serially, one bit at a time.

The transmitter accepts the *n*-bit data in parallel into a shift register and then transmits the data serially along the common line. The receiver accepts the data serially into a shift register. When all *n* bits are received, they can be taken from the outputs of the register in parallel. Thus, the transmitter performs a parallel-to-serial conversion of data and the receiver does a serial-to-parallel conversion.

Right Shift

A right shift is a movement of data from the left to the right (towards the LSB) at a rate of one bit per clock pulse.

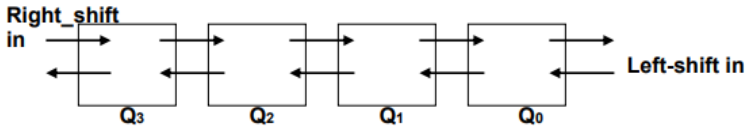
Left Shift

A left shift is a movement of data from the right to the left (towards the MSB) at a rate of one bit per clock pulse.

Bi-Directional Shift Register

A bi-directional shift register shift bit serially to the left or right according to the stat of direction control input. A four-bit bi-directional shift register consists of four D flip-flops connected in cascade and clocked synchronously. When a clock pulse is applied to the circuit, the

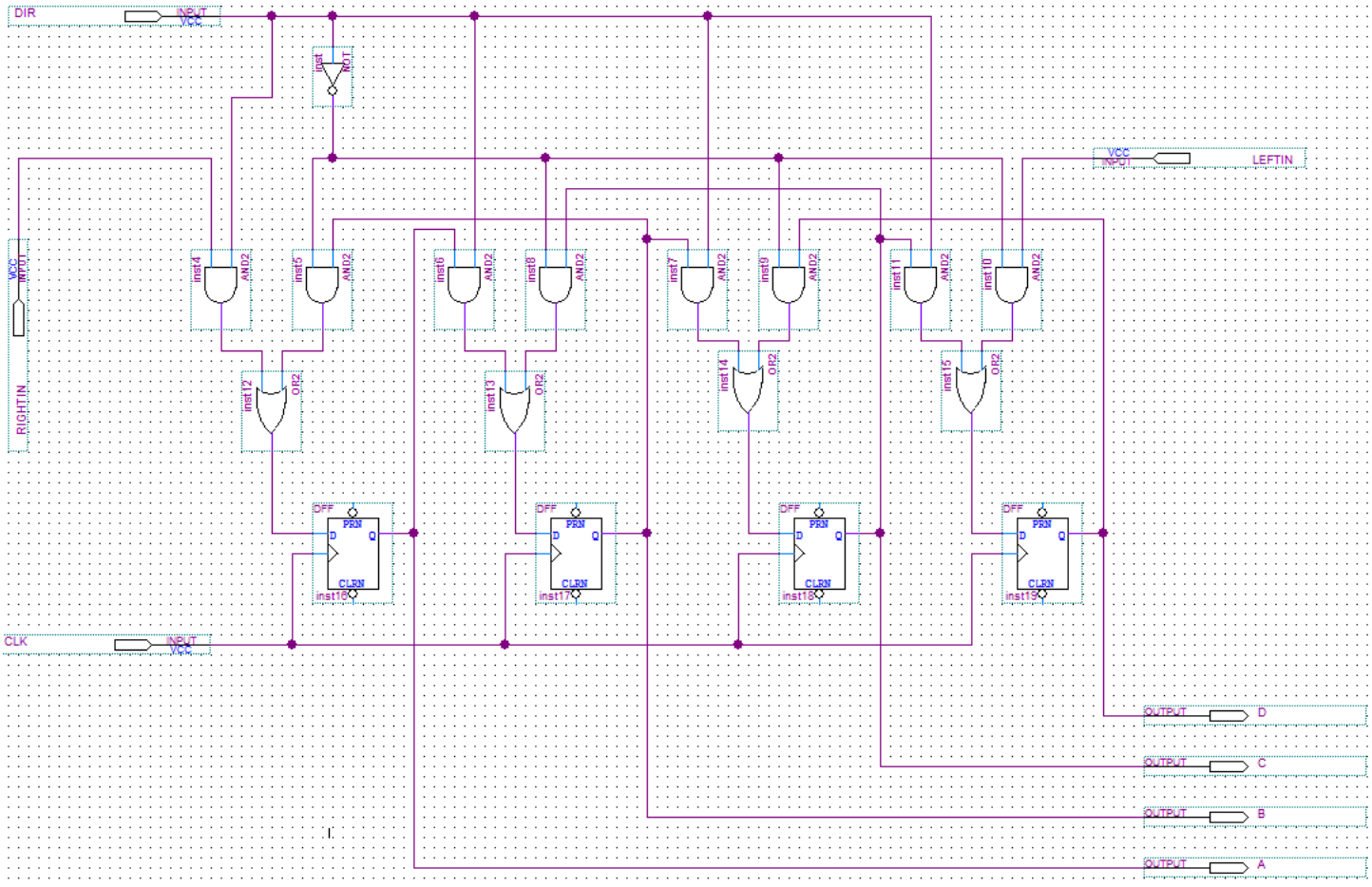
contents of the flip-flops move one position to the right/left depending on the direction control input.



Schematics of the Circuit

A schematic of the bi-directional register circuit was designed using AND-OR gates connected to D flip-flops. Each AND-OR circuit acts as multiplexer to direct one of several possible data sources to the synchronous inputs of flip-flops. The circuit can serially move data right or left, depending on the state of a control input, called *DIRECTION* or *DIR.*

Schematic

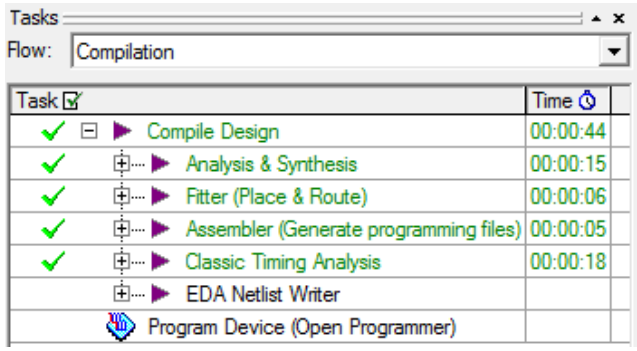


Experimental Results

The schematic was compiled to expedite synthesis of the circuit into waveform for simulation analysis. The results from the compilation were used as input values for preparation of the waveform editor. The compilation and simulation success are documented below.

Compilation Results

Flow Status	In progress - Mon Apr 02 10:48:29 2018
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	RightLeftRegister
Top-level Entity Name	RightLeftRegister
Family	MAX7000S
Device	EPM7064SLC84-7
Timing Models	Final
Met timing requirements	N/A
Total macrocells	4
Total pins	8

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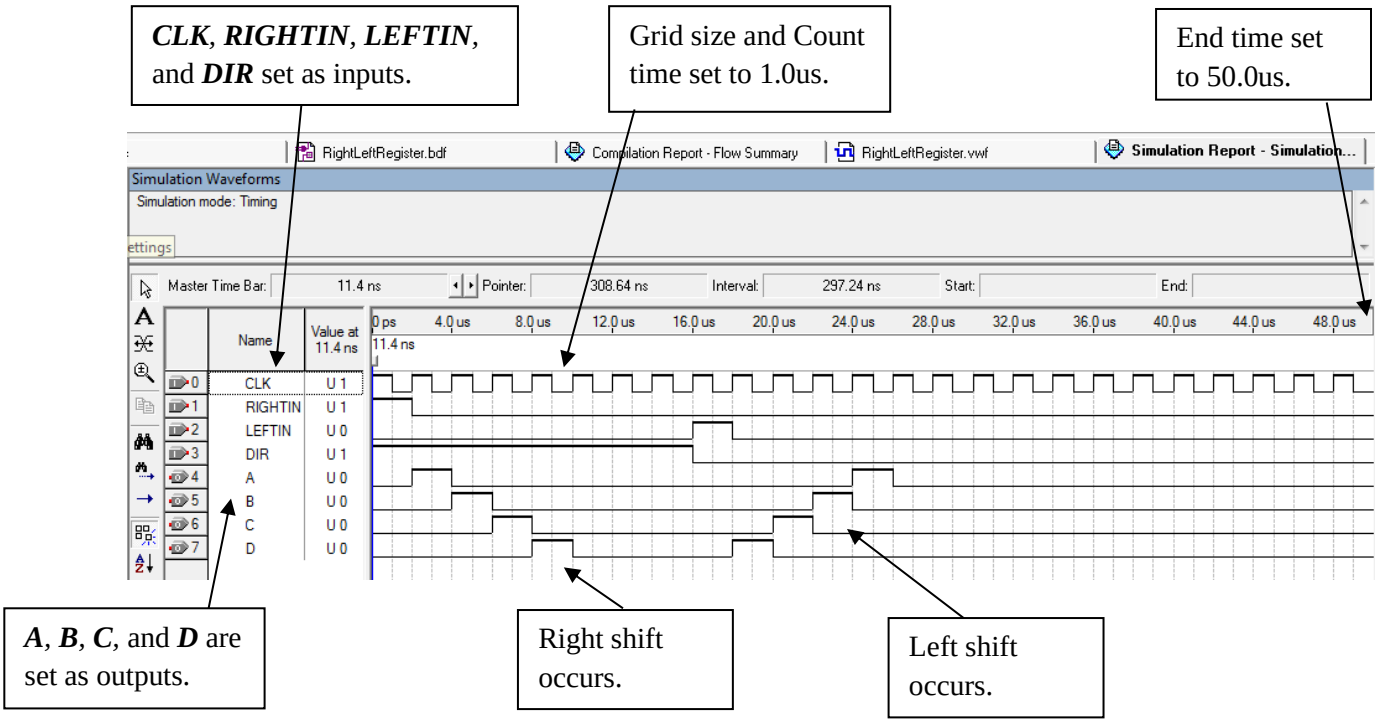
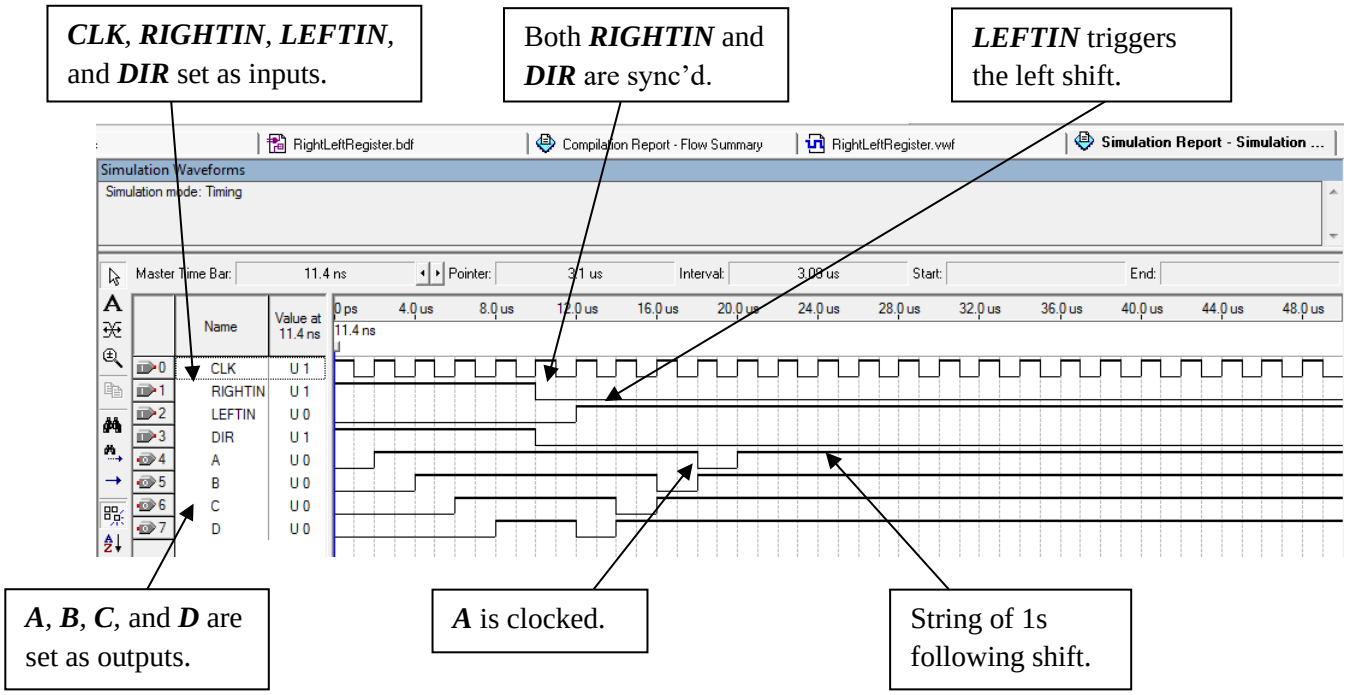
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 2 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 2 warnings
```

Simulation Results

Below is the Waveform for the bi-directional shift register circuit. The simulation is based on a 50.0us end time with a 1.0us and the count time and grid size as denoted.



The simulation shows the left shift function from 0 to 16.0us and left shift after 16.0us. Both *RIGHTIN* and *LEFTIN* are applied in both parts of the simulation, but the circuit responds only to one for each function. For the left shift function, a 1 is applied to *D* at 18.0us and shifted left as indicated. The *RIGHTIN* pulsed is ignored. Similarly, for the right shift function, a 1 is applied to *A* at 2.0us and shifted right. *LEFTIN* is ignored.



The simulation above shows *A* being clocked into the shift register, followed by a string of 1s that follow (Right shift in/Left shift in). For the left shift function, a 1 is applied to *D* at 12.0us and the shift occurred as indicated.

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Info: Number of transitions in simulation is 76
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
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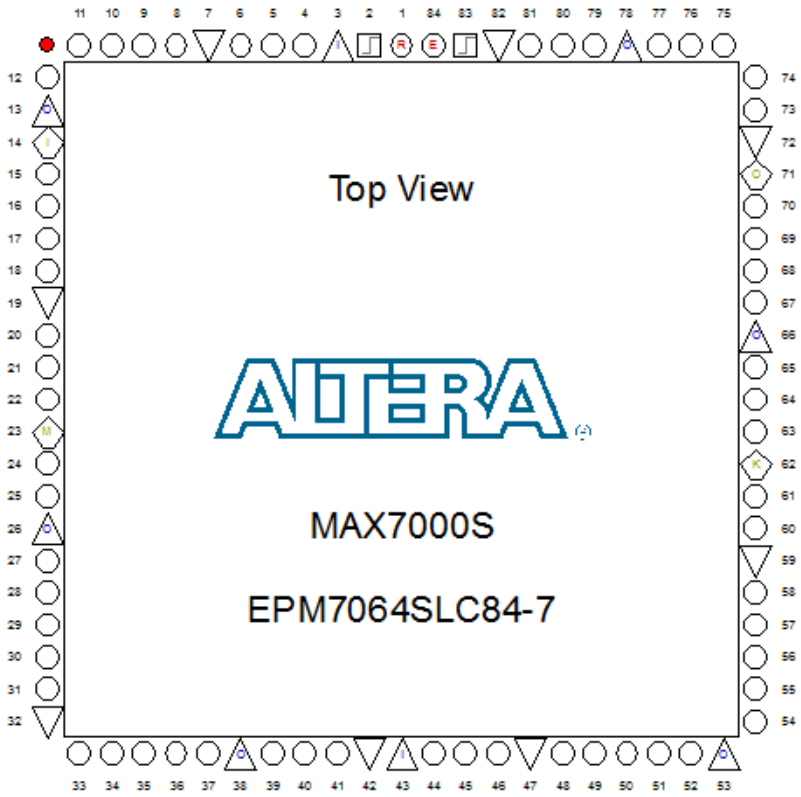
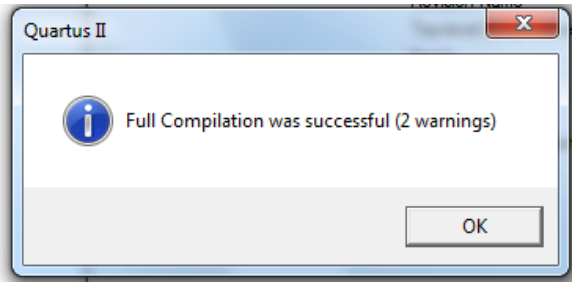
Pin Assignment

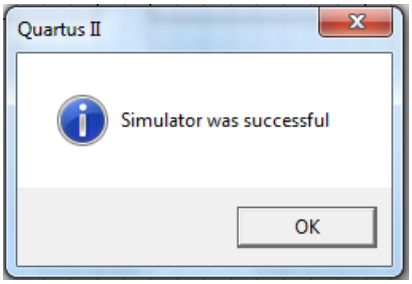
	Node Name	Direction
1	A	Output
2	B	Output
3	C	Output
4	CLK	Input
5	D	Output
6	DIR	Input
7	LEFTIN	Input
8	RIGHTIN	Input
9	TCK	Input
10	TDI	Input
11	TDO	Output
12	TMS	Input



Conclusion

A bi-directional shift register circuit was designed using *D Flip Flops* with *CLK*, *DIR*, *LEFTIN*, and *RIGHTIN* as inputs connecting to *A*, *B*, *C*, and *D* outputs. The bi-directional shift register's schematic was replicated for compilation and simulation that provided successful results. There were no errors to document in the compilation or simulation reports, as noted below. The circuit is suitable to proceed to the next step in the design process.





Reference Page

Dueck, K. *Digital Design with CPLD Applications and VHDL*. 2nd ed. Clifton Park, NY. Cengage Learning. 2005.

Mano, M. *Digital Design*. 3rd ed. New Delhi. Prentice-Hall of India. 2008.