Programming FPGA: Two-Bit Full Adder Circuit

By: Kyle W. Brown

Goals of the Experiment

To design a bi-directional shift register circuit from lecture 9s, shift right/left example. The two-bit full adder circuit will be designed in schematic form to be compiled for simulation using the MAX 10 family on the 10M50DAF484C7G device in the Quartus 17.1 software. The goal is to programming FPGA on the Altera DE10 Lite Development Board 2-bit full adder design.

There are two shifts needed to be performed: (1) All flip-flops are initially cleared with A1 being clocked into the shift register followed by a string of 0's (Right shift in/Left shift in). (2) A1 is clocked into the shift register, followed by a string of 1s (Right shift in/Left shift in). The circuit will be utilizing D Flip-Flops. Programming FPGA on the Altera DE10 Lite Development Board 2-bit Full Adder Design.

Theory of Operation

Full Adder

Full Adders are a circuit that will add a carry bit from another full or half adder and two operand bits to produce a sum bit and a carry bit. Full Adders can add two 1-bit numbers and accept a carry bit from a previous adder stage.

Two-Bit Adder

A two-bit adder can add two binary bits together by taking a carry from the next lower order of magnitude, and sending a carry to the next higher order of magnitude. For a multi-bit operation, each bit must be represented by a full adder and must be added simultaneously.

In order to take a digital design from a word description to the programmed silicon chip, you must go through a series of steps: These include:

- Design
- Compiling
- Simulation
- Programming

Programming Slide Switches

When using the switches on the DE10 there are ten slide switches connected to FGPA on the board. These switches are used as level-sensitive data inputs to a circuit. Each switch is connected directly and individually to a pin on the MAX 10 FPGA. When the switch is in the DOWN position (closest to the edge of the board), it provides a low logic level to the FPGA, and when the switch is in the UP position it provides a high logic level. Table 3-4 list the pin assignments of the user switches.

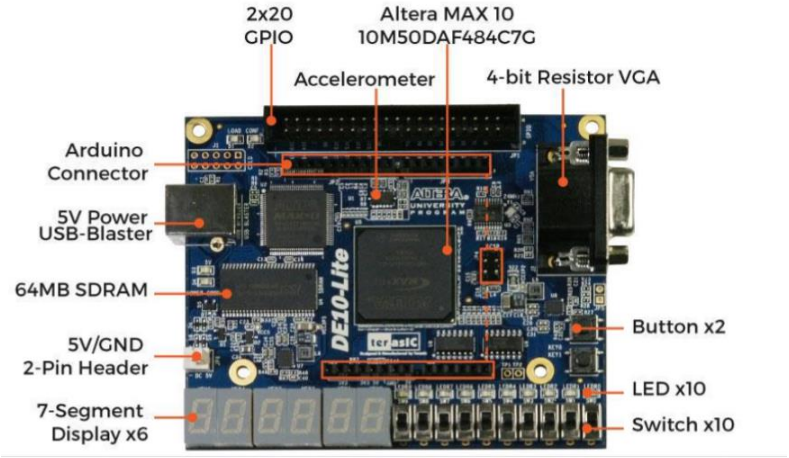
Table 3-4 Pin Assignment of Slide Switches

Signal Name	FPGA Pin No.	Description	I/O Standard
SW0	PIN_C10	Slide Switch[0]	3.3-V LVTTL
SW1	PIN_C11	Slide Switch[1]	3.3-V LVTTL
SW2	PIN_D12	Slide Switch[2]	3.3-V LVTTL
SW3	PIN_C12	Slide Switch[3]	3.3-V LVTTL
SW4	PIN_A12	Slide Switch[4]	3.3-V LVTTL
SW5	PIN_B12	Slide Switch[5]	3.3-V LVTTL
SW6	PIN_A13	Slide Switch[6]	3.3-V LVTTL
SW7	PIN_A14	Slide Switch[7]	3.3-V LVTTL
SW8	PIN_B14	Slide Switch[8]	3.3-V LVTTL
SW9	PIN_F15	Slide Switch[9]	3.3-V LVTTL

7 Segment Unit Display

The DE10 Lite board has six 7 segment displays. These displays are paired to display numbers in various sizes that connected to pins on MAX 10 FPGA. Then segment can be turned on or off by applying a low logic level or high logic level from the FPGA, respectively. Each segment in a display is indexed from 0 to 6 and DP (decimal point), with corresponding positions that shows the pin assignment of FPGA to the 7 segments displays.

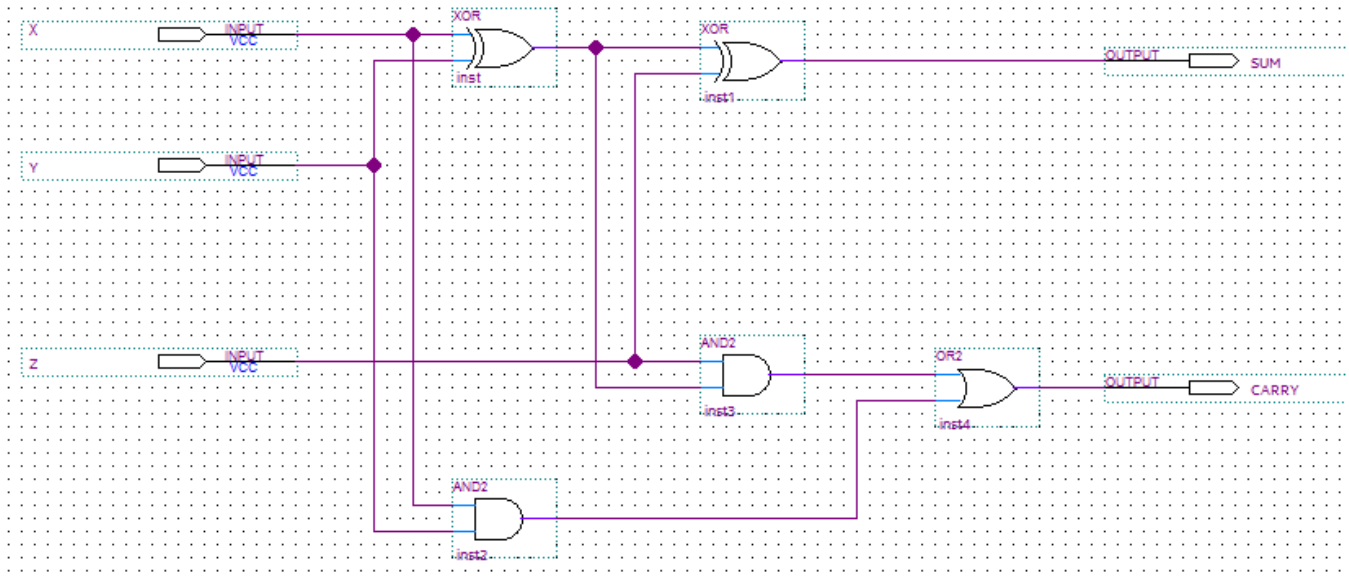
Altera DE 10-Lite



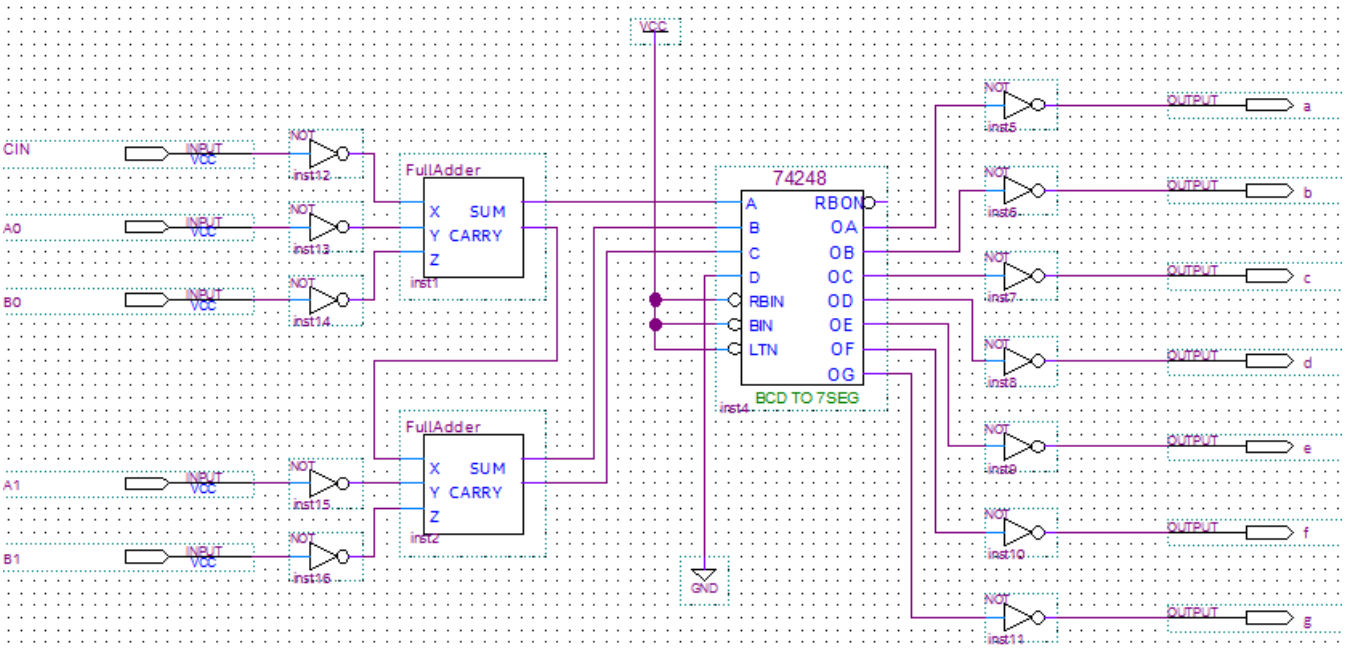
Schematics of the Circuit

A schematic of the bi-directional register circuit was designed using AND-OR gates connected to D flip-flops. Each AND-OR circuit acts as multiplexer to direct one of several possible data sources to the synchronous inputs of flip-flops. The circuit can serially move data right or left, depending on the state of a control input, called *DIRECTION* or *DIR*. The function of 74248 is that it can transform binary digits to the digits that can be displayed on the 7-segment display (7SEG). Experimentally we need NOT gates to invert the input and output signals from the board or to the board in order to get the right results.

Full Adder Schematic



2-Bit Full Adder Schematic



Experimental Results

The schematic was compiled to expedite synthesis of the circuit into waveform for simulation analysis. The results from the compilation were used as input values for preparation of the waveform editor. The compilation and simulation success are documented below.

Compilation Results

Flow Summary

<<Filter>>

Flow Status	Successful - Mon Apr 09 11:53:57 2018
Quartus Prime Version	17.1.0 Build 590 10/25/2017 SJ Lite Edition
Revision Name	2BitFullAdder
Top-level Entity Name	2BitFullAdder
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	10 / 49,760 (< 1 %)
Total registers	0
Total pins	12 / 360 (3 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

Tasks: Compilation

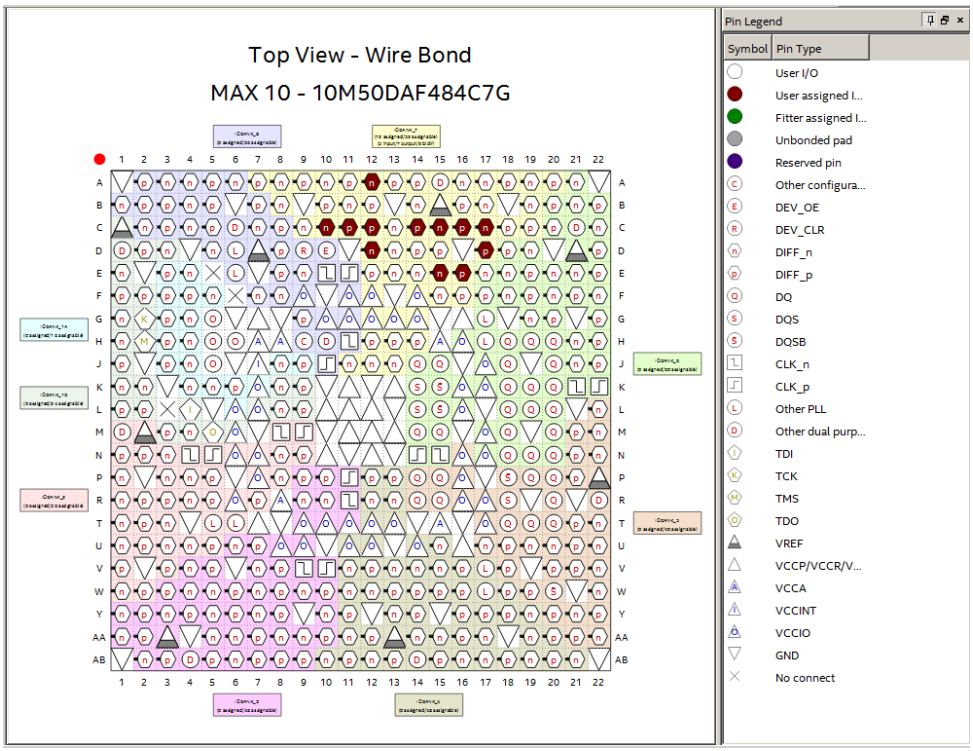
	Task	Time
✓	Compile Design	00:00:55
✓	Analysis & Synthesis	00:00:25
✓	Fitter (Place & Route)	00:00:16
✓	Assembler (Generate programming files)	00:00:06
✓	TimeQuest Timing Analysis	00:00:08

```
        Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 5 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 13 warnings
```

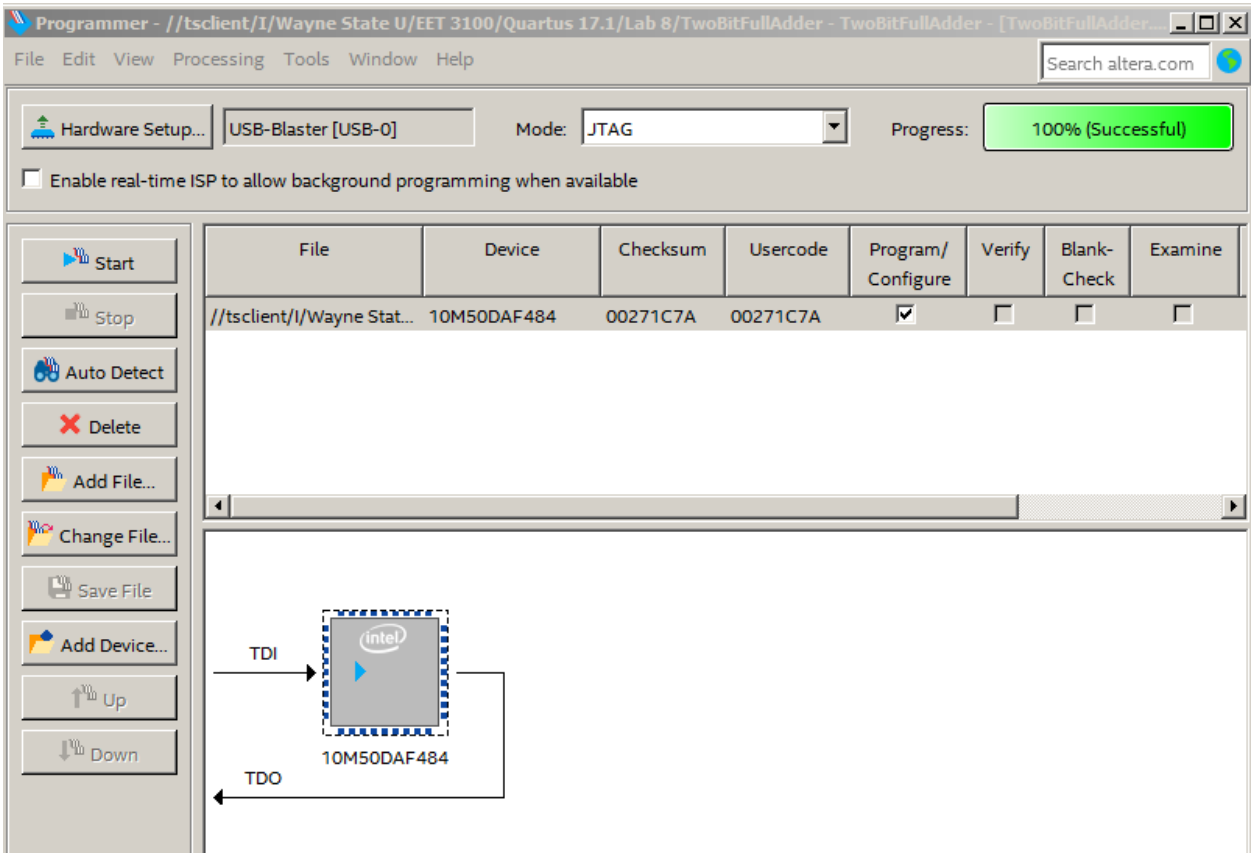
Pin Planning

Named: * Edit: PIN_C17 Filter: Pins: all

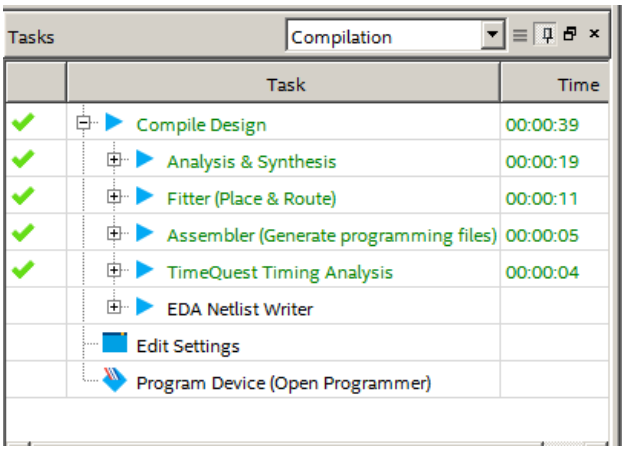
Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preserva
out a	Output	PIN_C14	7	B7_N0	PIN_W4	2.5 V (default)		12mA (default)	2 (default)		
in A0	Input	PIN_C10	7	B7_N0	PIN_V7	2.5 V (default)		12mA (default)			
in A1	Input	PIN_C11	7	B7_N0	PIN_Y8	2.5 V (default)		12mA (default)			
out b	Output	PIN_E15	7	B7_N0	PIN_W3	2.5 V (default)		12mA (default)	2 (default)		
in B0	Input	PIN_D12	7	B7_N0	PIN_V8	2.5 V (default)		12mA (default)			
in B1	Input	PIN_C12	7	B7_N0	PIN_Y7	2.5 V (default)		12mA (default)			
out c	Output	PIN_C15	7	B7_N0	PIN_Y1	2.5 V (default)		12mA (default)	2 (default)		
in CIN	Input	PIN_A12	7	B7_N0	PIN_Y6	2.5 V (default)		12mA (default)			
out d	Output	PIN_C16	7	B7_N0	PIN_W6	2.5 V (default)		12mA (default)	2 (default)		
out e	Output	PIN_E16	7	B7_N0	PIN_AA2	2.5 V (default)		12mA (default)	2 (default)		
out f	Output	PIN_D17	7	B7_N0	PIN_Y5	2.5 V (default)		12mA (default)	2 (default)		
out g	Output	PIN_C17	7	B7_N0	PIN_AA1	2.5 V (default)		12mA (default)	2 (default)		
<<new node>>											

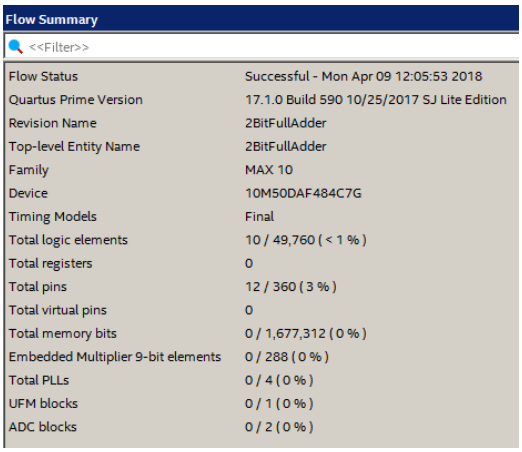


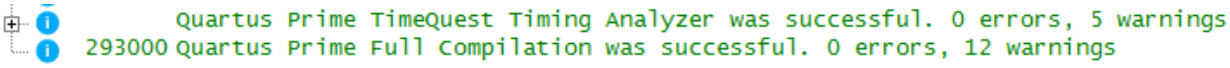
Hardware Recognized



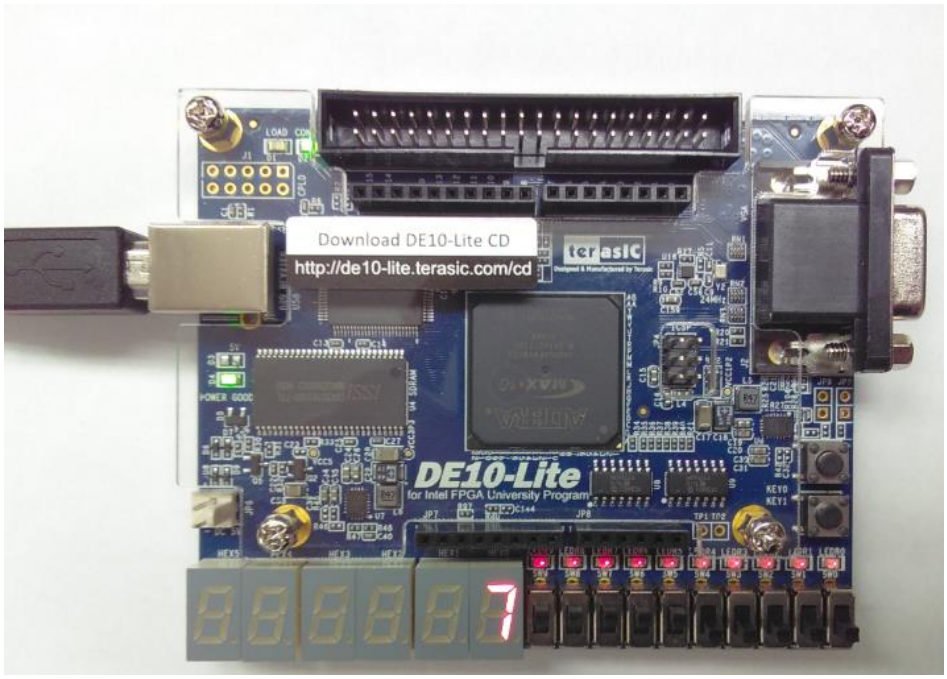
Compilation Results







Programmed Device



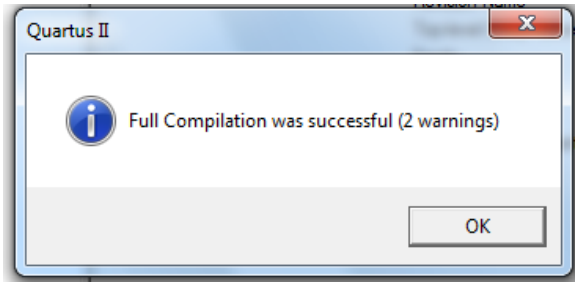
All the bits and carry turned on. 3+3=6 +1 (CARRY)

Each input for both bits is on. 3+3=6

2 bit + 2 bit = 4

Conclusion

A Two-Bit Full Adder circuit was designed by combining the Full Adder from Lab 1 into a Two-Bit Full Adder circuit. The Two-Bit Full Adder schematic was replicated for compilation to be programmed onto the DE-10 Lite device which provided successful results. There were no errors to document in either compilation reports, as noted below. The circuit is suitable to proceed to the next step in the design process.



Reference Page

Dueck, K. *Digital Design with CPLD Applications and VHDL*. 2nd ed. Clifton Park, NY. Cengage Learning. 2005.

Mano, M. *Digital Design*. 3rd ed. New Delhi. Prentice-Hall of India. 2008.