Kyle Brown

EET 3100: Advanced Digital Design

Dr. Victor Bondarenko

18 Feb. 2018

8x1 Multiplexer Circuit

Goals of the Experiment:

Design an 8x1 Multiplexer (MUX) circuit by combining previous lab circuits using the MAX7000S family, EPM7128SLC84-7 device in Quartus 9.1 software. Given F(A,B,C,D) = (A+B+D')(C+A)(B+D) to simplify. Using *A, C,* and *D* as selection lines.

Theory of Operation:

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of an input line is controlled by a set of selection lines. Normally, there are 2^n input lines and *n* selection lines whose bit combinations determine which input is selected.

Multiplexers allows multiple inputs to be connected independently to a single output, these are found in a variety of applications including data routing, logic function generators, control sequencers, and parallel-to-serial converters.

Truth Table

Dec	A	B	C	D		F
0	0	0	0	0		0
1	0	0	0	1		0
2	0	0	1	0		0
3	0	0	1	1		0
4	0	1	0	0		0
5	0	1	0	1		0
6	0	1	1	0		1
7	0	1	1	1		1
8	1	0	0	0		0
9	1	0	0	1		1
10	1	0	1	0		0
11	1	0	1	1		1
12	1	1	0	0		1
13	1	1	0	1		1
14	1	1	1	0		1

15	1	1	1	1		1

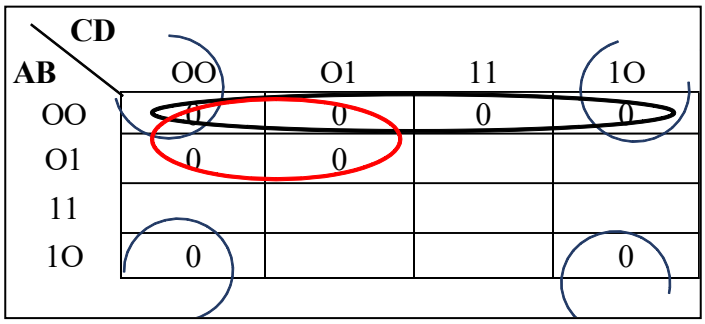
Function Table

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
B'	OOOO	OOO1	OO1O	OO11	1OOO	1OO1	1O1O	1O11
B	O1OO	O1O1	O11O	O111	11OO	11O1	11O1	1111

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
B'	O	1	2	3	8	9	1O	11
B	4	5	6	7	12	13	14	15
	Vcc	**Vcc**	**B'**	**B'**	**B'**	**GND**	**B'**	**GND**

F(A,B,C,D)=Π(0,1,2,3,4,5,8,10)

K-Map



F'=A'B'+B'D'+A'C'

F'=A'B'+B'D'+A'C'

F= (A+B)(B+D)(A+C)

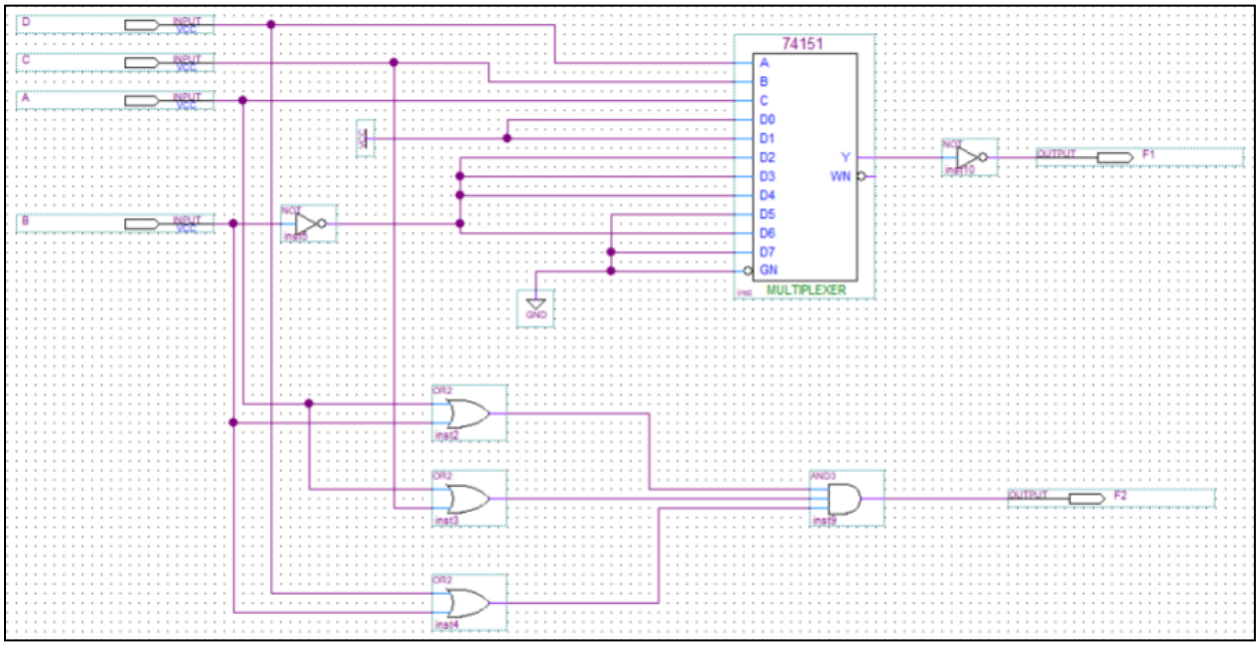
Schematics of the Circuit:

An 8x1 multiplexer consists of eight data inputs *D0* through *D7*. Three inputs select lines *A*, *B*, *C* and two output lines *F1* and *F2*. Depending on the select lines combinations, multiplexer decodes the inputs. The schematic below denotes an 8x1 multiplexer connected by 3 inputs and 1 select lines using OR gates to the Mux.

The below figure shows the block diagram of an 8x1 multiplexer with enable input that enable or disable the multiplexer. Since the number data bits given to the MUX are eight then 3 bits (23=8) are needed to select one of the eight data bits. In the circuit, when enable pin set to one, the

multiplexer will be disabled and if it is zero then select lines will select the corresponding data input to pass through the output.

Schematic



From the above Boolean equation, the logic circuit diagram of an 8x1 multiplexer can be implemented by using 3 OR gates, AND gate, and a NOT gate.

Experimental Results:

The schematic was compiled to expedite synthesis of the circuit into waveform for simulation analysis. The results from the compilation were used as values for preparation of the waveform editor. The compilation and simulation success are documented below.

Compilation Results

Flow Status	Successful - Mon Feb 12 11:55:58 2018
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	MUX
Top-level Entity Name	MUX
Family	MAX7000S
Device	EPM7128SLC84-7
Timing Models	Final
Met timing requirements	Yes
Total macrocells	2 / 128 (2 %)
Total pins	10 / 68 (15 %)

Tasks

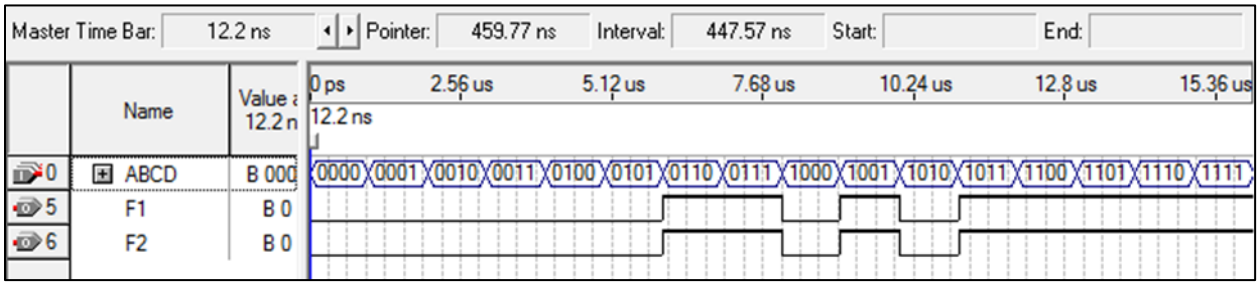
Flow: Compilation

Task	Time
Compile Design	00:00:40
Analysis & Synthesis	00:00:30
Fitter (Place & Route)	00:00:04
Assembler (Generate programming files)	00:00:04
Classic Timing Analysis	00:00:02
EDA Netlist Writer	
Program Device (Open Programmer)	

```
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 1 warning
Info: Quartus II Full Compilation was successful. 0 errors, 2 warnings
```

Simulation Results

Below is the Waveform for the 8x1 MUX circuit. The simulation is based on a 16.0us end time with a 1.0us count time. Inputs *A,B,C,D* were grouped together leaving outputs *F1* and *F2*.




```
Info: Number of transitions in simulation is 50
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```

Conclusion

An 8x1 multiplexer was designed in a schematic diagram with *A,B,C*, and *D* as inputs with *F1* and *F2* as output values. Based on the Truth table and K-Map the schematic, compilation, and simulation for the 8x1 Multiplexer circuit was successful. There were no errors to document in the compilation or simulation reports. The circuit is suitable to proceed to the next step in the design.

Reference Page

Dueck, K. *JK Flip Flop Truth Table and Circuit Diagram*. 2nd ed. Clifton Park, NY. Cengage Learning. 2005