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EET 3100: Advanced Digital Design

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# Adder/Subtractor Circuit

**Goals of the Experiment:**

Design an adder/subtractor circuit by combining lab 1 full adder circuit using MAX7008 family in Quartus 9. The full adder circuit has been created into a symbol to minimize the complexity of the circuit.

**Theory of Operation:**

Adder/Subtractor circuit is combined into one circuit with one common binary adder. This is done by including an exclusive-OR gate with each full adder. The mode input M controls the operation. When M=0, the circuit is an adder, and when M=1, the circuit becomes a subtractor. The B inputs are all complemented and a 1 is added through the input carry. The circuit performs the operation A plus the 2's complement of B.

The range of binary numbers both signed and unsigned for the adder/subtractor circuit is $2^4$ or $15_{10}$ and $-16_{10}$. An overflow occurs when two numbers of n digits each are added, and the sum occupies n+1 digit. The detection of an overflow after the addition of two binary numbers depends on whether the numbers are considered to be signed or unsigned. When two unsigned numbers are added an overflow is detected from the end carry out of the most significant position. The Exclusive-OR is for detecting an overflow.

| Use the following data (unsigned numbers) to show the proper operation of your circuit (the given numbers are in decimal): **Addition** | **Subtraction** |
|---|---|
| 5 + 2 | 5 – 2 |
| 7 + 7 | 7 - 7 |
| 10 + 8 | 11 - 6 |
| 2 + 9 | 14 - 9 |
| 11 + 5 | 5 - 0 |
| 3 + 12 | 13 - 3 |

*Truth Table*

| $A_n$ | $B_n$ | $C_{n-1}$ | $S_n$ | $C_n$ |
|-------|-------|-----------|-------|-------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

## Schematics of the Circuit:

The schematic below shows an 8x1 multiplexer with adder/subtractor connected by XOR gates to the black box or the full adder.
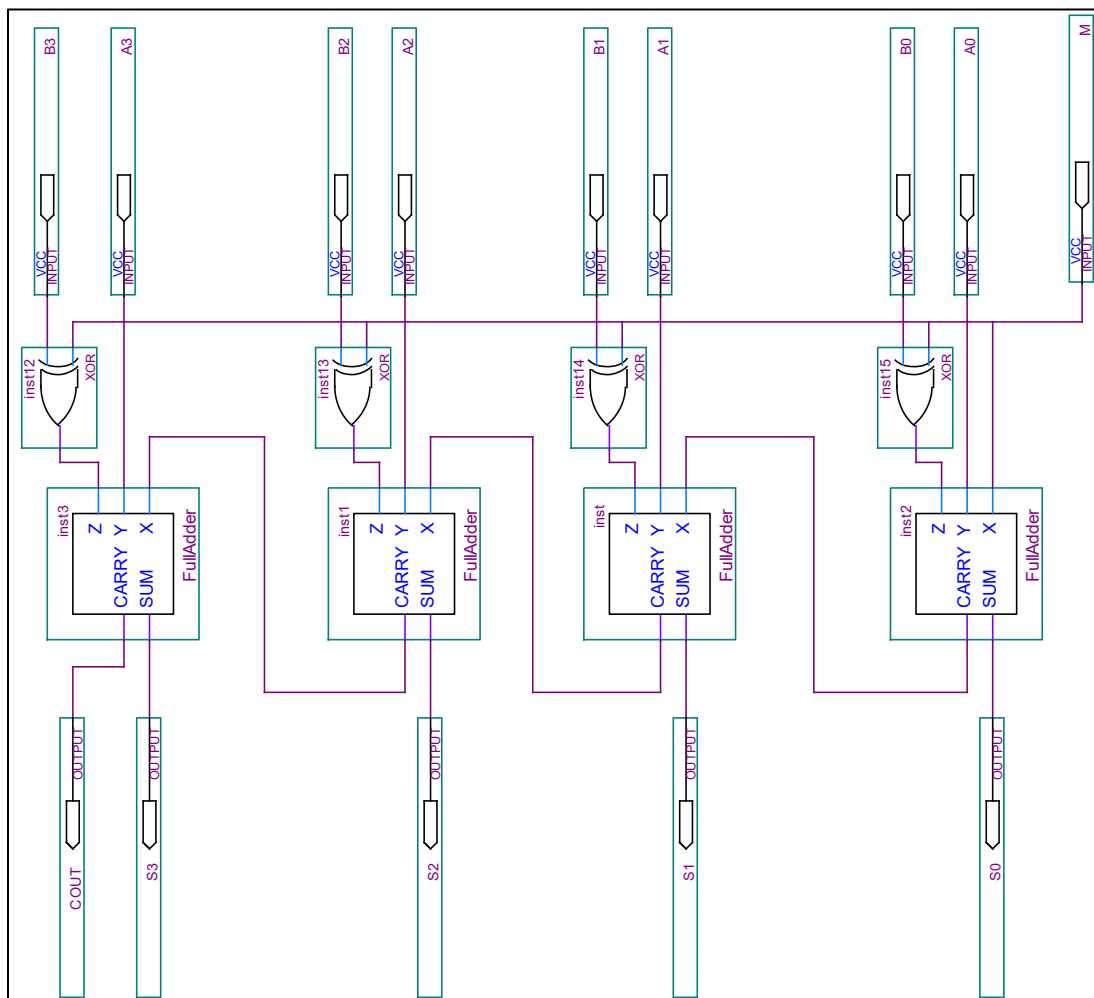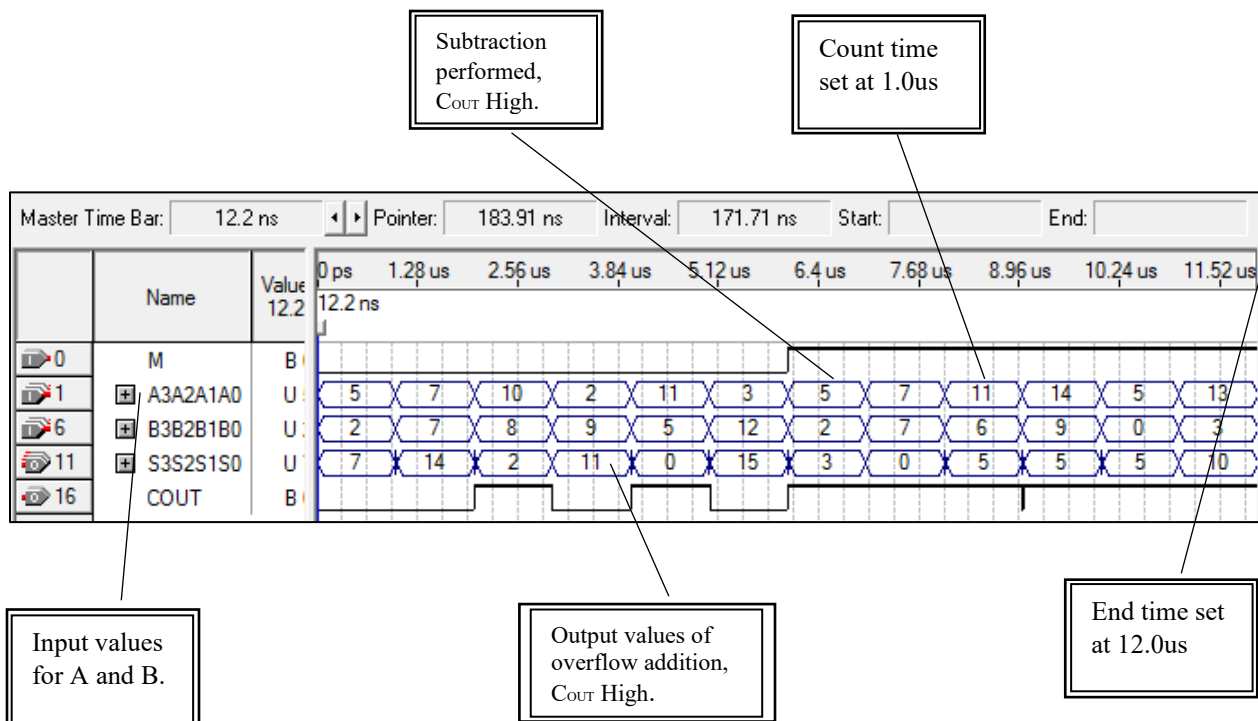
## Experimental Results:

*Compilation Results*

The schematic has been compiled below in order to expedite synthesis of the circuit. The results from the compilation were used as values for preparation of the waveform editor.

| Flow Status | Successful - Mon Feb 12 12:42:42 2018 |
|---|---|
| Quartus II Version | 9.1 Build 350 03/24/2010 SP 2 SJ Web Edition |
| Revision Name | AdderSubtractor |
| Top-level Entity Name | AdderSubtractor |
| Family | MAX7000S |
| Device | EPM7128SLC84-7 |
| Timing Models | Final |
| Met timing requirements | Yes |
| Total macrocells | 11 / 128 ( 9 % ) |
| Total pins | 18 / 68 ( 26 % ) |

Flow: Compilation

| Task ☑ | Time ⏱ |
|---|---|
| ✓ ⊟ ▶ Compile Design | 00:00:14 |
| ✓ ⊞... ▶ Analysis & Synthesis | 00:00:07 |
| ✓ ⊞... ▶ Fitter (Place & Route) | 00:00:03 |
| ✓ ⊞... ▶ Assembler (Generate programming files) | 00:00:03 |
| ✓ ⊞... ▶ Classic Timing Analysis | 00:00:01 |
| ⊞... ▶ EDA Netlist Writer | |
| ✋ Program Device (Open Programmer) | |

*Simulation Results*

Below is the Waveform for adder/subtractor circuit. The outputs for the addition and subtraction are correct. The simulation is based on a 12.0 us end time with a 1.0us count time.



Subtraction performed, $C_{OUT}$ High.

Count time set at 1.0us

Input values for A and B.

Output values of overflow addition, $C_{OUT}$ High.

End time set at 12.0us

**Conclusion**

The Truth table, schematic, compilation, and simulation for the adder/subtractor adder were successful. There were no errors to document in the compilation or simulation. The additions and subtractions were performed from the Theory of Operation table. The simulations success is documented below. The circuit will be suitable to proceed to lab 4.

```
Info: Number of transitions in simulation is 204
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```

## Reference Page

Dueck, K. *JK Flip Flop Truth Table and Circuit Diagram*. 2nd ed. Clifton Park, NY. Cengage Learning. 2005