CS 4341 Digital Logic and Computer Design

Semester Project - Arithmetic Logic Unit

Online Version

SNAKS Cohort

The University of Texas at Dallas

Department of Computer Science

CS 4141.002 – Digital Logic and Computer Design

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Description

Our cohort, SNAKS, will be working on a one-input ALU that has the capability of doing math functions such as addition, subtraction, multiplication, division. Our ALU also has the capability of doing logic functions such as AND, OR, NOT, XOR. Additionally, the ALU has support functions such as No Operation and Reset. Channels 0 through 9 on the Multiplexer will contain these 10 operations. Each operation of the ALU is its own circuit that will connect into one channel of the Multiplexer. The ALU we are creating is a memory unit that updates based on the operation code. The innermost portion is a memory register with the current value.

An Arithmetic Logic Circuit contains a 32-bit Accumulator register, that holds the current value. The 32- bit accumulator registers is made up of 32 one-bit D Flip-flops working synchronously. On each instruction, the ALU will take a 16-bit integer input and the lower 16-bits of the accumulator register and send them as inputs to 8 different modules. These modules will be a 16-bit adder, a 16-bit subtractor, a 16-bit multiplier, a 16-bit divider, a 16-bit AND, a 16-bit OR, a 16-bit NOT, and a 16-bit XOR. Each of these modules operate in parallel, and each of their outputs goes to a different input channel of a 16x32 bit multiplexer. (The output of a 16-bit multiplier can go up to 32 bits) The accumulator is updated on every clock cycle and the update is based on the operational cycle. The output of the ALU will be the current contents of the Accumulator register. The Subtractor will have an Overflow check, which will be an additional output. Also, the multiplexer has to handle the “No Operation” when no results of any module is used. And also, the D-Flip Flops must be able to be either preset to 1 or reset to 0. No-op, preset, and reset, will be handled by unused multiplexer channels.

Parts List

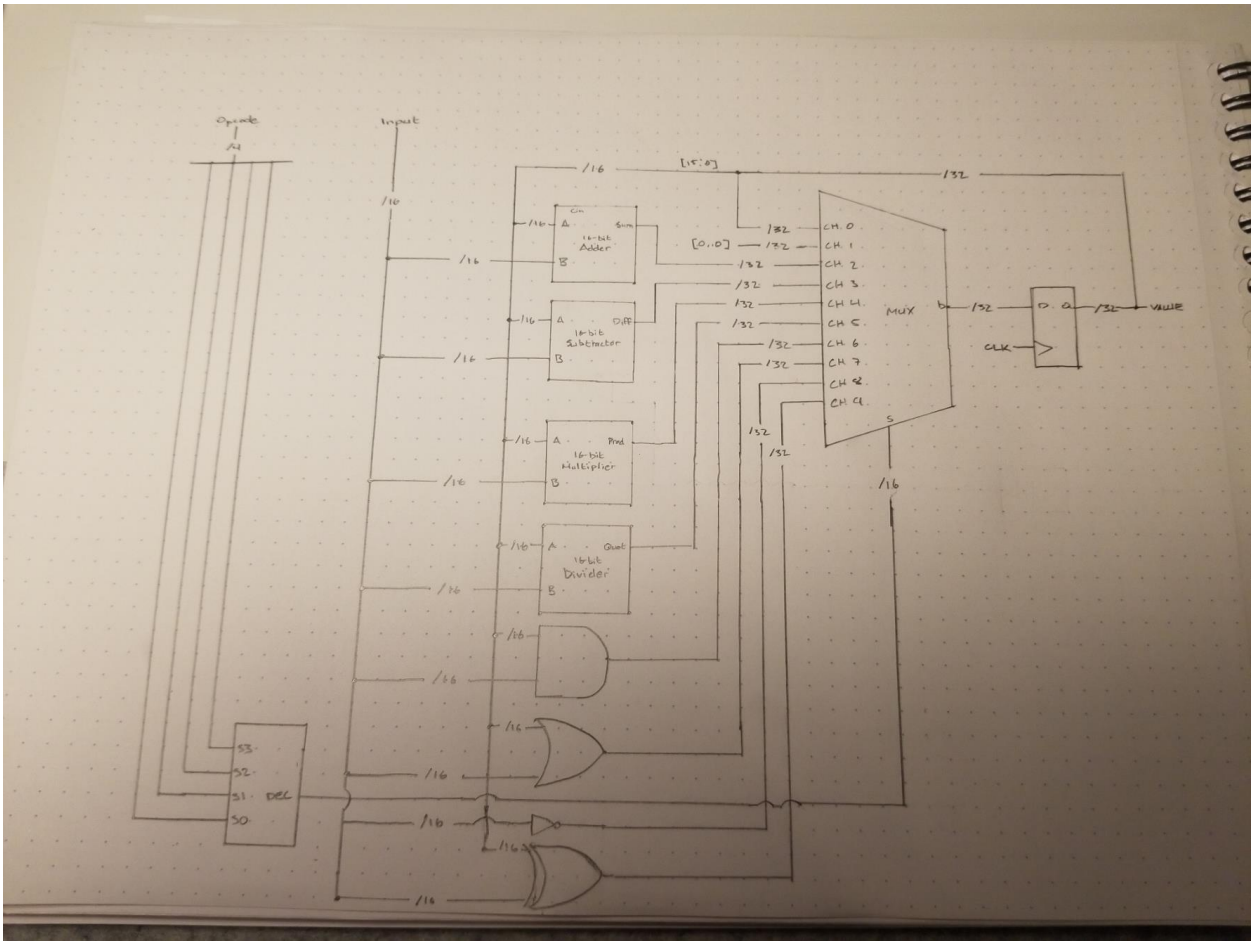
Wires

- 16-bit input
- 32-bit output (goes into accumulator register)
- 4-bit Opcode

Gates and Combination Logic Components

- 16x32 bit MUX
- 32-bit Accumulator (made up of 32 1 bit D Flip-Flops)
- 4-bit Decoder
- 16-bit Adder
- 16-bit Subtractor
- 16-bit Multiplier
- 16-bit Divisor
- 16-bit AND
- 16-bit OR
- 16-bit NOT
- 16-bit XOR

Circuit Diagram



OpCode Table

Command	Description	Op-Code	Multiplexer Channel
No-Op	Refreshes the Accumulator with Feedback	0000	Channel 0
Done	Returns to ready state after finished operation	0000	Channel 0
Reset	Sets accumulator to all 0s	0001	Channel 1
Add	Adds the input from the lower 16 bits of the accumulator	0010	Channel 2
Subtract	Subtracts the input from the lower 16 bits of the accumulator	0011	Channel 3
Multiply	Multiplies the input from the lower 16 bits of the accumulator	0100	Channel 4
Divide	Divides the input from the lower 16 bits of the accumulator	0101	Channel 5
AND	ANDs the input with the lower 16 bits of the accumulator	0110	Channel 6
OR	ORs the input with the lower 16 bits of the accumulator	0111	Channel 7
NOT	NOTs the input received	1000	Channel 8
XOR	XORs the input with the lower 16 bits of the accumulator	1001	Channel 9

State Machine