LETTER

doi:10.1038/nature11817

Magnetic-field-controlled reconfigurable semiconductor logic

Sungjung Joo[1,2], Taeyueb Kim[1,2], Sang Hoon Shin[3], Ju Young Lim[3], Jinki Hong[2], Jin Dong Song[3], Joonyeon Chang[1], Hyun-Woo Lee[4], Kungwon Rhie[2], Suk Hee Han[1], Kyung-Ho Shin[1] & Mark Johnson[5]

Logic devices based on magnetism show promise for increasing computational efficiency while decreasing consumed power. They offer zero quiescent power and yet combine novel functions such as programmable logic operation and non-volatile built-in memory[1–5]. However, practical efforts to adapt a magnetic device to logic suffer from a low signal-to-noise ratio and other performance attributes that are not adequate for logic gates. Rather than exploiting magnetoresistive effects that result from spin-dependent transport of carriers, we have approached the development of a magnetic logic device in a different way: we use the phenomenon of large magnetoresistance found in non-magnetic semiconductors in high electric fields[6,7]. Here we report a device showing a strong diode characteristic that is highly sensitive to both the sign and the magnitude of an external magnetic field, offering a reversible change between two different characteristic states by the application of a magnetic field. This feature results from magnetic control of carrier generation[8] and recombination in an InSb p–n bilayer channel[9]. Simple circuits combining such elementary devices are fabricated and tested, and Boolean logic functions including AND, OR, NAND and NOR are performed. They are programmed dynamically by external electric or magnetic signals, demonstrating magnetic-field-controlled semiconductor reconfigurable logic at room temperature. This magnetic technology permits a new kind of spintronic device, characterized as a current switch rather than a voltage switch, and provides a simple and compact platform for non-volatile reconfigurable logic devices.

High-electric-field magnetoresistance typically studied in Si (refs 6, 7, 10–12) has also been observed as a large magnetoconductance in an HgCdTe diode[8]. This large magnetoresistance effect derives from Lorentz forces acting on energetic carriers. Here we introduce a modified avalanche diode structure that adopts a structural asymmetry in the form of a p–n bilayer channel, thereby leading to an asymmetry in the dependence of recombination on the polarity of a magnetic field, B. The result is a current–voltage characteristic strongly dependent on magnetic field. As a second modification, we enhance the avalanche characteristics by use of a semiconductor with a small bandgap, resulting in very high magnetoconductance. Specifically, we chose InSb, which has a bandgap of 0.17 eV and an electronic effective mass that is 0.013 times the free electron mass.

We fabricated devices as follows. Sample NP had a p–n junction composed of a 0.2-μm-thick n-type InSb layer at the top, and a 6-μm-thick p-type InSb layer at the bottom of the channel (Fig. 1a). The channel width was 10 μm, and the length was 120 μm. The p-type layer in sample NP was characterized after removing the n-type by wet etching; we obtained values of carrier density and mobility (at 300 K) of $2.4 \times 10^{18}\,\mathrm{cm}^{-3}$ and $2.3 \times 10^{2}\,\mathrm{cm}^{2}\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$, respectively. To investigate the n-type layer, an auxiliary device, sample N, was fabricated with growth conditions identical to the n-type in sample NP, and its

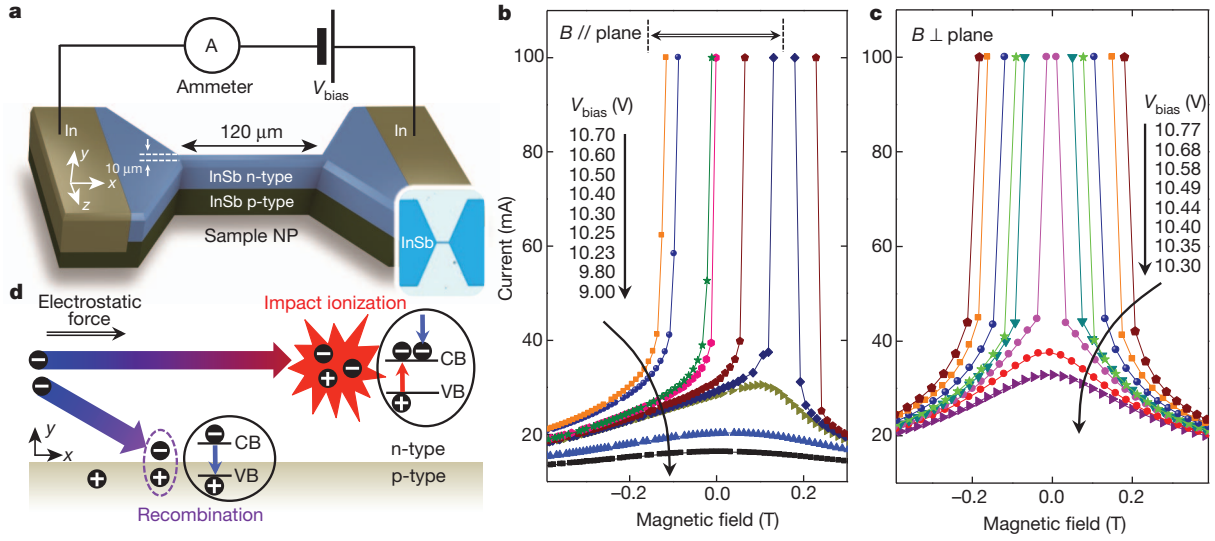


Figure 1 | Magnetoconductance tunable by external voltage. **a**, Schematic diagram and micrograph (bottom right inset) of an InSb device, sample NP. **b**, A family of plots of current versus magnetic field for sample NP (orientation B // plane, see main text). For a given bias voltage, there is a transition to a high-current state at a characteristic onset value of magnetic field. In the field region designated by a horizontal arrow (↔), the I–B characteristic resembles that of an electrical diode. **c**, A family of I–B plots for orientation B ⊥ plane (see main text). **d**, Schematic illustration of carrier transport processes in the channel. CB and VB represent the conduction band edge and valence band edge, respectively.

[1]Spin Convergence Research Center, KIST, Seoul 130-650, South Korea. [2]Department of Display and Semiconductor Physics, Korea University, Sejong 339-700, South Korea. [3]Nano Photonics Research Center, KIST, Seoul 130-650, South Korea. [4]Department of Physics, Pohang University of Science and Technology, Pohang 790-784, South Korea. [5]Naval Research Laboratory, Washington DC 20375, USA.

carrier density and mobility (at 300 K) were $2 \times 10^{16}\,cm^{-3}$ and $7.8 \times 10^{4}\,cm^{2}\,V^{-1}\,s^{-1}$, respectively. The thickness of the n-type layer in sample NP was less than the electron mean free path (~0.4 μm) of sample N. All measurements in this study were performed at room temperature using d.c. voltage sources. The current was intentionally limited to 100 mA to protect the device from damage. Two magnetic field configurations were used: B perpendicular to the x–z plane (that is, along the y axis in Fig. 1a) and B parallel to the x–z plane (along the z axis in Fig. 1a).

The unique $I(V, B)$ characteristic of our NP device is shown in Fig. 1b. We plot a family of traces showing channel current I as a function of magnetic field B ('B // plane') for a variety of bias voltages, V_{bias}. Considering data in the field region $-0.15\,T < B < +0.15\,T$ (designated by a horizontal arrow, ↔), each current trace monotonically increases with increasing field and there is an abrupt change in magnitude at a field value that represents the onset of the high-current state. This behaviour is similar to the characteristic of a p–n junction diode if the bias voltage is replaced by the magnetic field. Our device therefore can be considered to be a magnetic-field version of an electrical diode. Although conventional p–n junction diodes have a fixed onset voltage called the knee voltage, the onset field of our devices varies according to V_{bias}.

We define the magnetoconductance ratio (MC) of our devices as the ratio of the maximum to the minimum value of $I(B)/V_{bias}$ (that is, $MC \equiv I_{max}/I_{min}$) for a given bias voltage. The maximum current is limited at 100 mA, which artificially limits the magnetoconductance ratio. For magnetic fields ranging between −0.2 and 0.2 T, MC is a numeric factor greater than five. Because the device shows such an abrupt change in current, a high-current state (ON, digital '1') can be defined as an output current of 100 mA. A low-current state (OFF, digital '0') is similarly defined as an output current of 40 mA or less.

The structural asymmetry caused by the p–n bilayer channel distinguishes magnetoresistance in our structure from that in other devices. Conductivity is sensitive to a carrier generation process induced by impact ionization[13] and transport is influenced by field-dependent recombination rates (Fig. 1d)[14,15]. A large field along the negative z axis deflects energetic carriers in the n-type layer towards the p–n interface by a Lorentz force. Enhanced recombination depletes the carrier population and diminishes the current. By contrast with Fig. 1b, the data for $B \perp$ plane in Fig. 1c are symmetric with respect to the sign of magnetic field because the Lorentz force deflection is in the plane and does not affect recombination. Carrier generation at high bias was verified by Hall measurements, and magnetic-field-dependent recombination was confirmed using a photoconductivity measurement (Supplementary Information section 2).

New functionalities for information processing are enabled by the unique properties of our device; we fabricated several circuits and demonstrated magnetic-field-controlled reconfigurable Boolean logic gates at room temperature. We begin with a simple reconfigurable AND/OR gate, and then extend this gate to perform most of the Boolean logic functions. We further show that our device can be programmed by external binary parameters. These demonstrations rely on the magnetic conductance characteristics displayed in Fig. 1b, where the onset of the high-current state is a function of bias voltage.

An AND/OR gate was prepared to elucidate the principle of logic operation with our devices. We manufactured two devices (NP1 and NP2) with nearly identical structure and electrical properties, which are, for the purpose of this explanation, the same as those of sample NP. Each device was mounted on a separate sample holder, and an external magnetic field was applied to both sample holders. By rotating each sample holder, the orientation of the magnetic field applied to the devices could be controlled individually (Supplementary Fig. 1). Figure 2a depicts the circuit and field configurations. The field (B // plane) has an orientation either positive or negative along the z axis. The corresponding current–voltage curves for NP1 are displayed in Fig. 2b, and show an abrupt increase of current at the threshold voltage, V_{th}. The key feature of this circuit is that current I is the same for NP1 and NP2 in series, and the current has the high-state value $I = 100$ mA

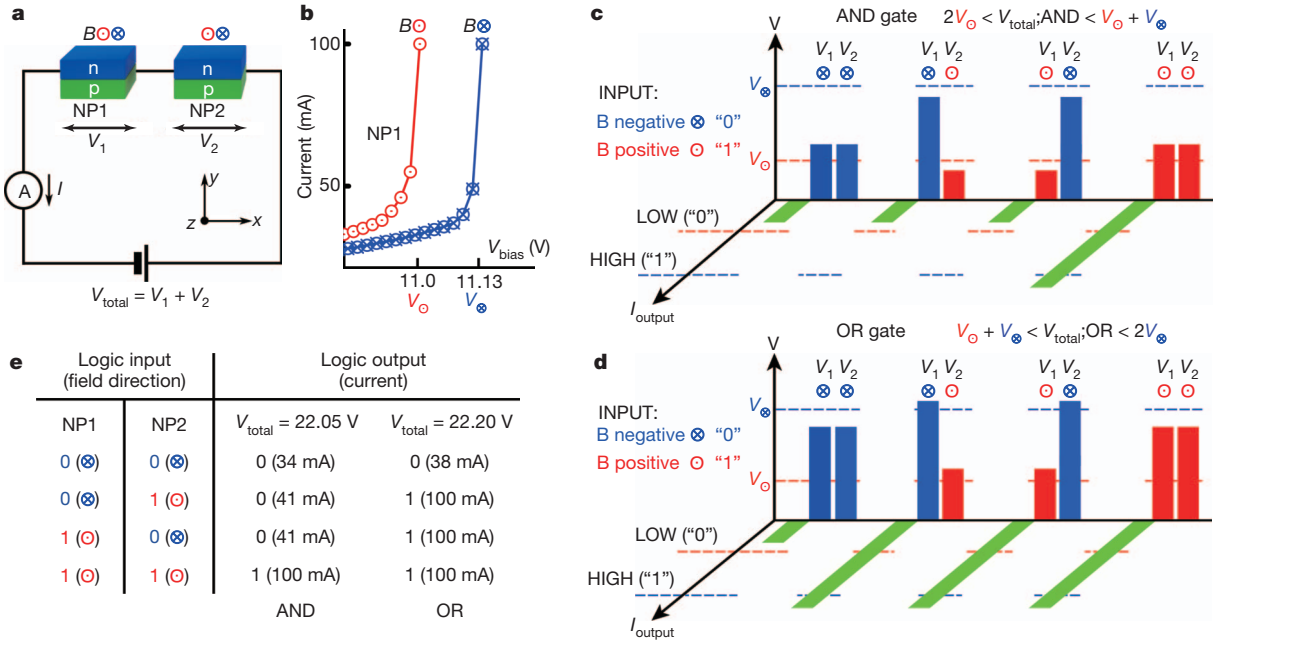


Figure 2 | Programmable logic operation demonstrated by an AND/OR gate. Positive (⊙) or negative (⊗) magnetic fields of −0.1 T and 0.1 T are applied to devices with orientation B // plane. **a**, The circuit used for demonstration of reprogrammable Boolean logic. V_1 and V_2 are the voltage drops across samples NP1 and NP2, respectively. Binary logic inputs are positive (negative) magnetic field, corresponding to binary 1 (0). Logic output is high (low) current, corresponding to binary 1 (0). The Boolean operation to be performed is programmed by setting the bias voltage V_{total} to 22.05 V for the AND operation or 22.20 V for the OR operation. **b**, Current–voltage characteristics of NP1. The threshold voltage of NP1 and NP2 at the negative field, $V_⊗$, is 11.13 V, and that at the positive field, $V_⊙$, is 11.0 V. **c**, Schematic explanation of AND gate operation, described in the main text. **d**, Schematic explanation of OR gate operation, described in the main text. **e**, Truth table summary of the operations described in **c** and **d**. Experimentally measured output values are included (all values were reproducible).

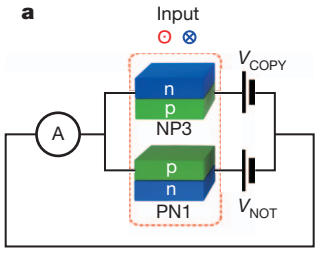
only if the voltage drops across devices NP1 and NP2 (referred to as V_1 and V_2) exceed the threshold voltages, that is, $V_1 > V_{th,1}$ and $V_2 > V_{th,2}$. If not, either $V_1 < V_{th,1}$ or $V_2 < V_{th,2}$, and the current has the low-state value. To describe binary logic operations, we define the inputs as the polarity of field B at NP1 and NP2, B positive (negative) corresponding to binary 1 (0) and represented in Fig. 2 by symbol $\odot$ ($\otimes$). The logical output is a high (low) current with value $I = 100$ mA ($I < 40$ mA) corresponding to binary 1 (0). The simple circuit of Fig. 2a is a reconfigurable gate, with either the AND or the OR logic function determined by the applied voltage, V_{total}.

The operation of programmable Boolean logic is illustrated in Fig. 2c and d. The V axis represents the voltage across each device, the I_{output} axis represents the output current, and bar plots for four different input configurations are staggered along the horizontal axis. Symbols $V_\odot$ and $V_\otimes$ represent the values of V_{th} for positive and negative field, respectively. In Fig. 2c, V_{total} is given a value of 22.05 V, in the range $2V_\odot < V_{total} < V_\odot + V_\otimes$. The vertical bars represent the voltage drops across each of the two devices, red (blue) corresponding to a device in the presence of positive (negative) field. The sum of the heights of the bars is constant for each of the four configurations. In the first configuration, NP1 and NP2 are in negative field, the inputs are binary 0 and 0, voltages V_1 and V_2 are both less than the threshold voltages $V_{th,1}$ and $V_{th,2}$ ($V_\otimes$ on the V axis), and the output current is necessarily low, OUTPUT = 0. In the second and third cases, one device is in a positive field and the other a negative field; the inputs are 0 and 1, $V_1 < V_{th,1}$ and $V_2 < V_{th,2}$, and OUTPUT = 0. In the final case, both NP1 and NP2 are in positive field, the inputs are binary 1 and 1, $V_1 > V_{th,1}$ and $V_2 > V_{th,2}$, and OUTPUT = 1. The truth table is summarized in Fig. 2e and represents the operation of an AND gate. In Fig. 2d, V_{total} is given a higher value of 22.20 V, in the range $V_\odot + V_\otimes < V_{total} < 2V_\otimes$. For inputs 0 and 0, we have $V_1 < V_{th,1}$ and $V_2 < V_{th,2}$ and OUTPUT = 0. For other configurations, we have $V_1 > V_{th,1}$ and $V_2 > V_{th,2}$ and OUTPUT = 1. The truth table (Fig. 2e) represents the operation of an OR gate. The summary provided by Fig. 2e includes values of output current that were experimentally measured in our circuit at room temperature. These results demonstrate that an external parameter, the total voltage bias, can be used to program dynamically the functional operation of the circuit as either an AND gate or an OR gate.

Such reprogrammability can be extended to other Boolean logic functions. Magnetic field is a pseudovector and its sign changes when taking a mirror image of a physical system[16]. Hence, a system is invariant under the substitution of its mirror image and reversal of the field direction. We introduce PN devices as mirror images of NP devices. NP devices have an n-type layer above a p-type layer, whereas PN devices have a reverse stack, an n-type beneath a p-type layer. Mirror reflection with respect to the p–n interface ensures the mirror image relation between these two types, and a PN device can be replaced by an NP with reversed magnetic field direction. Equivalently stated, PNs in Fig. 3 can be considered as NPs with logical negation at the inputs, because the Boolean negation for 1 (positive field) corresponds to 0 (negative field).

We now describe a wide variety of reconfigurable Boolean operations that are demonstrated in Fig. 3. PN and NP devices were distinguished from each other while mounting them on the sample holder (see Methods). Two NP devices, NP3 and NP4, and two PN devices, PN1 and PN2, have $V_\odot$ of 10.35, 10.11, 12.4 and 12.8 V, respectively, and $V_\otimes$ of 10.47, 10.23, 12.0 and 12.65 V, respectively. NP3 and PN1 were mounted on one sample holder, and NP4 and PN2 were mounted on the other.

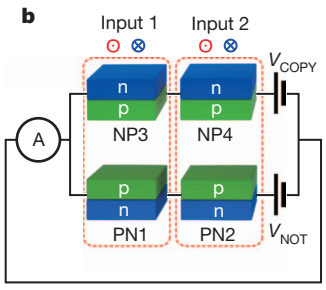
When V_{NOT} is zero, no current flows in the PN devices and the output is determined entirely by the NP devices and V_{COPY} (see Fig. 3a for V_{NOT} and V_{COPY}). The output of the circuit in Fig. 3a is low (high) current for the input $\otimes$ ($\odot$), when $V_{\odot,NP3} < V_{COPY}$ (= 10.42 V) $< V_{\otimes,NP3}$. This represents the logical COPY function. The circuit shown in Fig. 3b can be simplified as a series connection of NP3 and NP4 with a bias of V_{COPY}, representing the same circuit as that in Fig. 2a and performing the same reprogrammable AND/OR functions. Similarly, when V_{COPY} is zero, the NP devices carry no current, and the PN devices and bias V_{NOT} determine the output. Recalling the mirror symmetry relation that a PN can be treated as an NP if the logical inputs $\odot$ and $\otimes$ are interchanged, the circuit of Fig. 3a performs the NOT function and the circuit of Fig. 3b performs NOR/NAND functions.



Logical input (field direction)	Logical output (current)	
	V_{COPY} = 10.42 V, V_{NOT} = 0 V	V_{COPY} = 0 V, V_{NOT} = 12.10 V
0 (⊗)	0 (17.5 mA)	1 (100 mA)
1 (⊙)	1 (100 mA)	0 (35 mA)
	COPY	NOT

INPUT:
B negative ⊗ "0"
B positive ⊙ "1"

OUTPUT:
Current LOW "0"
Current HIGH "1"



Logical input (field direction)		Logical output (current)			
Input 1	Input 2	V_{COPY} =20.50 V, V_{NOT} =0 V	V_{COPY} =20.64 V, V_{NOT} =0 V	V_{COPY} =0 V, V_{NOT} =24.7 V	V_{COPY} =0 V, V_{NOT} =25.1 V
0 (⊗)	0 (⊗)	0 (22.5 mA)	0 (25.5 mA)	1 (100 mA)	1 (100 mA)
0 (⊗)	1 (⊙)	0 (24.3 mA)	1 (100 mA)	0 (38.2 mA)	1 (100 mA)
1 (⊙)	0 (⊗)	0 (26.6 mA)	1 (100 mA)	0 (36.0 mA)	1 (100 mA)
1 (⊙)	1 (⊙)	1 (100 mA)	1 (100 mA)	0 (30.1 mA)	0 (36.1 mA)
		AND	OR	NOR	NAND

Figure 3 | Demonstration of various Boolean operations. Left, a pair of NP and PN devices, shown boxed by red dotted lines, receives a common input signal (magnetic field): one pair is NP3 and PN1 and the second pair is NP4 and PN2. NP and PN devices are driven by bias voltage V_{COPY} and V_{NOT}, respectively. Right, the total current is a summation of the currents driven by these two voltage sources, and the logic output is determined by this total current. Experimentally measured output currents are listed in parentheses for various bias voltages and input values. The outputs of the circuit shown in **a** represent the Boolean logic function COPY or NOT, and those of circuit shown in **b** represent AND, OR, NOR or NAND functions. Thus, several elementary functions are possible with a single circuit system: two functions for the circuit shown in **a** and four functions for the circuit shown in **b**. Each function can be programmed by pre-setting the bias voltage values.

Experimental results for the two circuits are listed in the truth tables in Fig. 3, demonstrating that our reconfigurable logic gates provide the basic Boolean operations, with each logic function programmed by pre-setting the bias voltages. Complex operations can be accomplished by building on these elementary functions. We further experimentally demonstrate logic gates for which the function is programmed using a binary parameter, positive or negative field directions $\odot$ and $\otimes$, rather than bias voltage (Supplementary Fig. 2). Binary programming avoids errors that might arise from narrow margins of control voltage.

We have demonstrated unique performance characteristics of p-n bilayer avalanche diodes by fabricating devices with dimensions of the order of 10 μm and using external magnetic fields. However, digital electronics applications require integrated devices fabricated with sub-micrometre feature size. Issues for the miniaturization of our device can be divided into two parts, the diode current channel and the source of local magnetic field. The minimum size of the channel is determined by the 'dead space', the distance that a carrier travels before acquiring enough energy from the electric field to participate in impact ionization. For an electric field of the order of 10^5 V cm^{-1}, which is less than values used in commercial avalanche diodes, the dead space of about 20 nm for InSb represents a scaling limit for our device. Avalanche diodes with Si (ref. 17) and AlAsSb (ref. 18) channels having 100-nm dimensions have already been demonstrated. Because the Lorentz force is determined by carrier mobility in diffusive systems and high mobility can be maintained at small sizes, the magnetic field sensitivity of our devices should be scalable.

The second issue is the source of magnetic field. An appropriate integrated source of field can be provided by fabricating a patterned ferromagnetic element next to a passivated device channel. The fringe field associated with the ferromagnetic element has a magnitude that depends on the mean distance to the channel, but is roughly 0.2 T for a distance of 200 nm (ref. 19). Of greater importance, the magnetic field polarity can be controlled by switching the magnetization orientation of the ferromagnet between one of two bistable directions along a uniaxial anisotropy axis. The magnetization state of the ferromagnet is efficiently 'written' by spin transfer torque (STT) switching[20]. This technique scales with current density, and therefore STT writing scales with device area. A typical write current density is approximately 1×10^6 A cm^{-1} (refs 2, 20). For ferromagnetic elements with dimensions of the order of 100 nm, appropriate write current pulses have amplitude 0.2 mA and duration 2 ns.

Following these considerations, our InSb avalanche diode, if reduced to dimensions of channel length, width and thickness of roughly 100 nm, is expected to have a threshold voltage V_{th} of about 9 mV and an output of 40 μA in the low-current state. Provided that output is limited to five times the low-current value, the high-current output is 0.2 mA. Unlike voltage-controlled semiconductor devices, magnetization switching is driven by current. Our device is a current switch, and the 0.2-mA output is sufficiently large to provide STT write current input to a subsequent device. Our device is therefore unique in the field of spintronics because it is intrinsically adapted to device fan-out, a requirement for digital logic applications.

Our device, if scaled to submicrometre feature size with a patterned ferromagnetic element, promises further advantages. It is important to note that magnetization orientation is maintained as a non-volatile state because of the bistability of magnetic hysteresis. Our approach could be called non-volatile reconfigurable logic. By adding a magnetic memory device to an elementary logic unit such as an AND or OR gate, any circuit or sub-circuit would remember its most recent configuration and the latest logical result. Circuits, blocks of circuits, or entire chips could be powered off when not in use, followed by 'instant-on' performance when powered up for an operation. Compared to complementary metal oxide semiconductor (CMOS) devices which need power in quiescent mode, both the duty cycle and the average power could be reduced substantially. The energy per operation would be a characteristic parameter, rather than operating power. For a 2-ns pulse duration, we estimate the largest dissipation in the channel (high-current state) would be 3.6 fJ and an STT write process would dissipate 40 aJ, if the size of the channel and ferromagnetic element were of the order of 100 nm. As a final note, four of our magnetic diodes are adequate to perform the four Boolean functions in our reconfigurable gate (see Fig. 3). This promises that a future version of our device would be more compact than a comparable logic unit in a CMOS gate array, and could lead to higher packing density and faster operating speed. Of greater importance, our architecture for logic operation offers dynamic reconfigurability, as demonstrated in this study. This reconfiguration could be performed in a single clock cycle in the future device.

METHODS SUMMARY

An indium antimonide (InSb) wafer was grown on a GaAs substrate using molecular beam epitaxy[21]. A wafer grown without intentional doping showed n-type conduction with a carrier density of nearly intrinsic level. p-Type layers were obtained by beryllium doping during the growth process. The device shape was defined by conventional photolithographic techniques and formed by low-energy ion milling and subsequent wet-chemical etching. Ohmic electrodes were made by electron-beam evaporation of indium. A d.c. voltage source and an ammeter were connected through the electrodes.

To avoid Joule heating, a copper block was installed on the sample holder (Supplementary Fig. 1). Devices were mounted on this copper block with Apiezon H grease, which is a thermal conductor (but an electrical insulator) and provides thermal contact to the copper block. Electric currents were measured in steps of bias voltage sweep or magnetic field sweep. For each measurement step, a current value was collected after applying d.c. voltage for a sufficient time ($\sim$3 s) to guarantee an electrical steady state. During the time interval ($>$10 s) between successive measurement steps, the bias voltage was reduced to 0 V to minimize Joule heating in the devices.

Both NP and PN devices consist of an n-type layer grown on a p-type layer, and their fabrication processes were the same. NP devices were mounted on sample holders with the n-type layer on the top and the p-type layer on the bottom. However, PN devices were mounted by turning the n-type layer down to the sample holders, resulting in the p-type layer on the top and the n-type layer on the bottom. An electrical insulator (Apiezon H grease) was used to prevent leakage current between the devices and the surface of sample holders.

Received 31 July; accepted 20 November 2012.
Published online 30 January 2013.

1. Moodera, J. S. & Leclair, P. Spin electronics: a quantum leap. *Nature Mater.* **2,** 707–708 (2003).
2. Ney, A., Pampuch, C., Koch, R. & Ploog, K. H. Programmable computing with a single magnetoresistive element. *Nature* **425,** 485–487 (2003).
3. Dery, H., Dalal, P., Cywinski, L. & Sham, L. J. Spin-based logic in semiconductors for reconfigurable large-scale circuits. *Nature* **447,** 573–576 (2007).
4. Xu, P. *et al.* An all-metallic logic gate based on current-driven domain wall motion. *Nature Nanotechnol.* **3,** 97–100 (2008).
5. Behin-Aein, B., Datta, B. D., Salahuddin, S. & Datta, S. Proposal for an all-spin logic device with built-in memory. *Nature Nanotechnol.* **5,** 266–270 (2010).
6. Delmo, M. *et al.* Large positive magnetoresistive effect in silicon induced by the space-charge effect. *Nature* **457,** 1112–1115 (2009).
7. Wan, C. *et al.* Geometrical enhancement of low-field magnetoresistance in silicon. *Nature* **477,** 304–307 (2011).
8. Lee, J. *et al.* An electrical switching device controlled by a magnetic field-dependent impact ionization process. *Appl. Phys. Lett.* **97,** 253505 (2010).
9. Hong, J. *et al.* Magnetic field dependent impact ionization in InSb. Preprint at http://arxiv.org/abs/1206.1094v1 (2012).
10. Schoonus, J. J. H. M., Bloom, F. L., Wagemans, W., Swagten, H. J. M. & Koopmans, B. Extremely large magnetoresistance in boron-doped silicon. *Phys. Rev. Lett.* **100,** 127202 (2008).
11. Delmo, M. P., Kasai, S., Kobayashi, K. & Ono, T. Current-controlled magnetoresistance in silicon in non-Ohmic transport regimes. *Appl. Phys. Lett.* **95,** 132106 (2009).
12. Ciccarelli, C., Park, B. G., Ogawa, S., Ferguson, A. J. & Wunderlich, J. Gate controlled magnetoresistance in a silicon metal-oxide-semiconductor field-effect-transistor. *Appl. Phys. Lett.* **97,** 082106 (2010).
13. Sze, S. M. *Semiconductor Devices, Physics and Technology* 2nd edn, 78, 118 (Wiley and Sons, 2002).
14. Chovet, A. Study of recombination processes from the magnetoconcentration effect. *Phys. Status Solidi A* **28,** 633–645 (1975).
15. Cristoloveanu, S. & Lee, J. H. Magnetoconcentration and related galvanomagnetic effects in non-intrinsic semiconductors. *J. Phys. C* **13,** 5983–5997 (1980).
16. Fulling, S. A., Sinyakov, M. N. & Tischchenko, S. V. *Linearity and the Mathematics of Several Variables* 343 (World Scientific, 2000).

17. Massey, D. J. *et al.* Impact ionization in submicron silicon devices. *J. Appl. Phys.* **95,** 5931–5933 (2004).
18. Xie, J. J. *et al.* Excess noise characteristics of thin AlAsSb APDs. *IEEE Trans. Electron. Dev.* **59,** 1475–1479 (2012).
19. Hong, J. *et al.* Local Hall effect in hybrid ferromagnetic/semiconductor devices. *Appl. Phys. Lett.* **90,** 023510 (2007).
20. Hosomi, M. *et al.* A novel nonvolatile memory with spin torque transfer magnetization switching: spin-RAM. In *Proc. Electron Devices Meeting, 2005* 459–462 (IEDM Technical Digest, IEEE International, 2005).
21. Lim, J. Y., Song, J. D., Ahn, J.-P., Rho, H. & Yang, H. S. Effect of thin intermediate-layer of InAs quantum dots on the physical properties of InSb films grown on (001) GaAs. *Thin Solid Films* **520,** 6589–6594 (2012).

Supplementary Information is available in the online version of the paper.

Acknowledgements This work was supported by the KIST vision 21 programme, NRF grants funded by MEST (2010-0000506, 2011-0012386 and 2012-0005631), the industrial strategic technology development programme funded by MKE (KI002182), the Dream project, MEST (2012K001280), GRL and the Office of Naval Research.

Author Contributions J.H. and J.D.S. planned the project and supervised the research. S.J. and T.K. fabricated the devices and collected the data. J.D.S, S.H.S. and J.Y.L. grew the materials. J.C., H.-W.L., K.R., S.H.H. and K.-H.S. analysed and discussed the data. J.C., J.H. and M.J. wrote the manuscript, which was edited and approved by all co-authors.

Author Information Reprints and permissions information is available at www.nature.com/reprints. The authors declare no competing financial interests. Readers are welcome to comment on the online version of the paper. Correspondence and requests for materials should be addressed to J.H. (jkhongjkhong@korea.ac.kr) or J.D.S. (jdsong@kist.re.kr).