Physical Probabilistic Computing: Implementation of Logic Gates Using Biased Spinning Tops

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Abstract

We present a novel approach to physical computing using mechanically biased spinning tops as probabilistic computing elements. This work introduces a framework for implementing basic logic gates through physical probability manipulation, bridging concepts from mechanical computing and probabilistic processing. We demonstrate the feasibility of NOT, AND, and OR gates using this system and discuss implications for physical neural networks and probabilistic computing architectures.

1 Introduction

The intersection of physical computing and probabilistic processing presents unique opportunities for novel computational architectures. While quantum computing has dominated recent discussions of probabilistic computation, simpler mechanical systems may offer practical advantages for certain applications. This paper introduces a system of biased spinning tops that can implement basic logic gates through controlled probability manipulation.

2 Methods

2.1 Physical Implementation

Each computing element consists of a spinning top with adjustable internal weight distribution, allowing for controlled bias in its binary outcome states. The tops are arranged in addressable grids with automated spin and reset mechanisms, and state detection through conductive surfaces.

2.2 State Detection Mechanism

The binary state detection of each top is achieved through differential conductivity between the two faces of the top. When the top falls, it makes contact with a capacitive sensing grid embedded in the computing surface. One face of the top is designed with higher conductivity (e.g., through metallic coating or conductive polymer), while the other face maintains lower conductivity. This creates a detectable difference in capacitive coupling when the top settles, allowing reliable state readout without mechanical contacts. This approach provides several advantages:

- Non-contact sensing reduces mechanical wear
- Grid addressing enables parallel readout of multiple tops
- Capacitive sensing is robust to environmental variations
- The same mechanism could potentially enable position tracking during spin

The detection threshold between states can be calibrated through the grid's sensing parameters, providing flexibility in accommodating manufacturing variations in the tops' conductive properties.

2.3 Logic Gate Implementation

Basic logic gates are implemented through specific arrangements of these probabilistic elements:

- NOT gate: Single inverted-bias top
- AND gate: Three-top arrangement with threshold combination
- OR gate: Three-top arrangement with cumulative probability

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