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Name	**SID #**

EEM16/CSM51A (Fall 2017)

Logic Design of Digital Systems

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Problem set 4 | **Assigned Monday Nov. 27, 2017**
Extra credit | **due 4pm Wednesday Dec. 6, 2017**

Instructions

This homework is to be done individually. You may consult with others to share thoughts and ideas, but all of your submitted work must be yours alone. Be sure to indicate with whom you've collaborated and in what manner.

You may use any tools or refer to published papers, books, or course notes. You're allowed to make use of online tools such as Logisim, WolframAlpha, etc., provided you properly cite them in the space below.

You must submit this cover sheet plus all pages of your solutions based on the procedure below. Please write clearly and neatly — if we cannot easily decipher what you have written, you will get zero credit.

Submission procedure

You need to submit your solution online at Gradescope:

https://gradescope.com/

Please see the following guide from Gradescope for submitting homework. You will need to upload a PDF and mark where each question is answered.

http://gradescope-static-assets.s3-us-west-2.amazonaws.com/help/submitting_hw_guide.pdf

Collaborators

Identify with whom you've collaborated and in what manner, if any.

Amit Mondal
Cade Mallet
Jair Hinojosa
- Discussion of ideas

Online resources

Identify which online tools you've used, if any.

None

Kyle Romero
12/2/2017

Problem Set #4

1.1 a)

$$t_{CLK} \geq \max(t_{PD,FA}, t_{PD,AND}) + t_{PD,d\text{-}reg} + t_{setup}$$

$$t_{CLK} \geq 3ns + 3ns + 6ns$$

$$\boxed{t_{CLK} \geq 12ns}$$

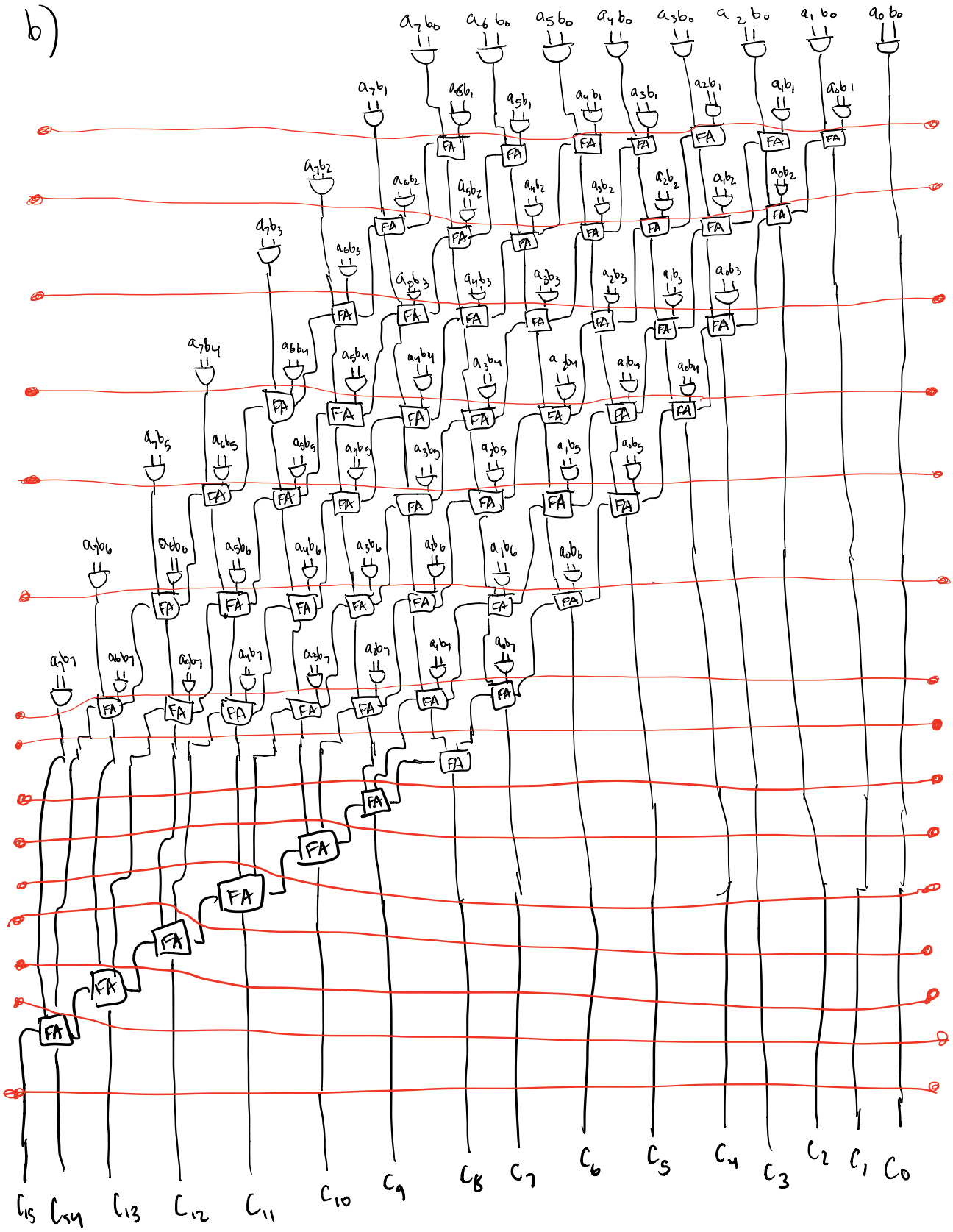
$$\text{Latency} = 16(t_{PD,FA}) + 8(t_{PD,AND})$$

$$= 16(3ns) + 8(2ns)$$

$$= 48ns + 16ns$$

$$\boxed{= 64ns}$$

$$\boxed{\text{Throughput} = \frac{1}{\text{Latency}} = \frac{1}{64}}$$


b)
FA
C_{15} C_{14} C_{13} C_{12} C_{11} C_{10} C_9 C_8 C_7 C_6 C_5 C_4 C_3 C_2 C_1 C_0

Notes:
- Assume all red dots join together like following 
- Assume all ANDs are computed in 1st pipelined stage
- Assume that all lines exiting AND gates are then extended upward and then pass through pipelined stage

From the above diagram we have k = 15 pipelined stages

c) Latency = (t_{CLK})(# of pipelined stages)

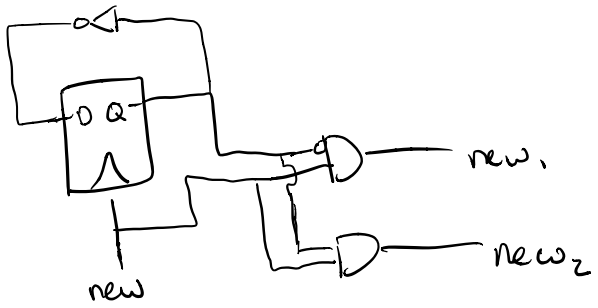
$= (12ns)(15)$

$= 180\ ns$

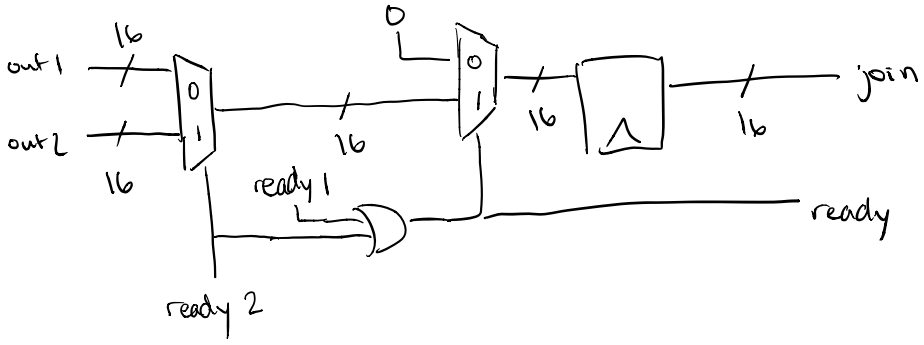
$$\text{Throughput} = \frac{1\ op}{t_{CLK}} = \frac{1\ op}{12ns}$$

1.2

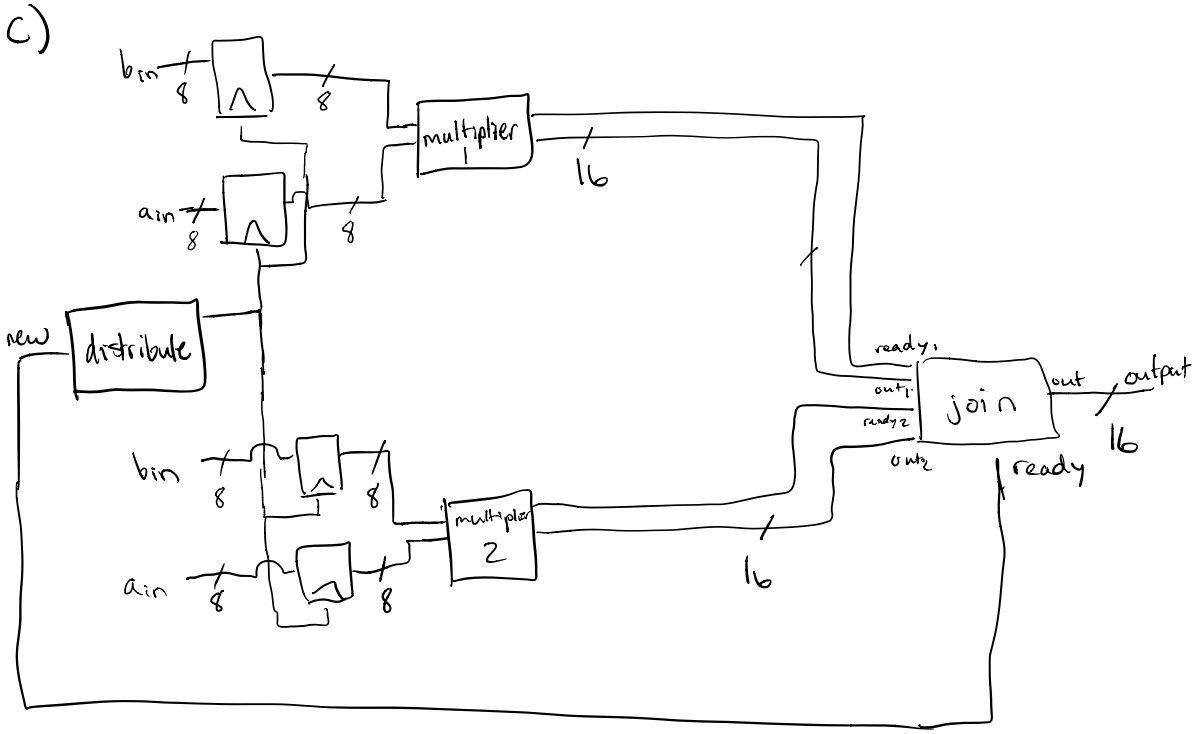
a)


D Q
new1
new2
new

b)


out1
16
out2
16
0
1
16
0
1
16
16
join
ready1
ready
ready2

c)


bin
8
8
multiplier 1
16
ain
8
8
new
distribute
ready1
out1
ready2
out2
join
out
output
16
ready
bin
8
8
multiplier 2
16
ain
8
8

d) The area of this circuit is significantly less than that of the pipelined multiplier

The parallel multiplier uses roughly twice the # of transistors of the original combinational multiplier (because there are two of them)

The pipelined multiplier adds a lot of transistors for each pipelined stage across each of the inputs