## AIPU system registers

### AIPU architectural system register summary

This section identifies the architectural system registers implemented in the AIPU core.

Table x-x AIPU Control Registers Group 1

|  |  |  |  |
| --- | --- | --- | --- |
| Address | Name | Reset value | Description |
| 0x000 | Base Address 0 For TEC 0 | 0xf0000000 | Base Address Register 0 For TEC 0 |
| 0x001 | Base Address 1 For TEC 0 | 0xf0080000 | Base Address Register 1 For TEC 0 |
| 0x002 | Base Address 2 For TEC 0 | 0xf0000000 | Base Address Register 2 For TEC 0 |
| 0x003 | Base Address 3 For TEC 0 | 0xf0000000 | Base Address Register 3 For TEC 0 |
| 0x020 | Base Address 0 For TEC 1 | 0xf0100000 | Base Address Register 0 For TEC 1 |
| 0x021 | Base Address 1 For TEC 1 | 0xf0180000 | Base Address Register 1 For TEC 1 |
| 0x022 | Base Address 2 For TEC 1 | 0xf0100000 | Base Address Register 2 For TEC 1 |
| 0x023 | Base Address 3 For TEC 1 | 0xf0100000 | Base Address Register 3 For TEC 1 |
| 0x040 | Base Address 0 For TEC 2 | 0xf0200000 | Base Address Register 0 For TEC 2 |
| 0x041 | Base Address 1 For TEC 2 | 0xf0280000 | Base Address Register 1 For TEC 2 |
| 0x042 | Base Address 2 For TEC 2 | 0xf0200000 | Base Address Register 2 For TEC 2 |
| 0x043 | Base Address 3 For TEC 2 | 0xf0200000 | Base Address Register 3 For TEC 2 |
| 0x060 | Base Address 0 For TEC 3 | 0xf0300000 | Base Address Register 0 For TEC 3 |
| 0x061 | Base Address 1 For TEC 3 | 0xf0380000 | Base Address Register 1 For TEC 3 |
| 0x062 | Base Address 2 For TEC 3 | 0xf0300000 | Base Address Register 2 For TEC 3 |
| 0x063 | Base Address 3 For TEC 3 | 0xf0300000 | Base Address Register 3 For TEC 3 |

## Control Registers Group

### Base Address Register 0 For TEC [N]

The following figure shows the Base Address Register 0 For TEC [N] bit assignments

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 |  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0 |
| ls0\_base0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Figure x-x Base Address Register 0 For TEC [N] bit assignments

The following table shows the Base Address Register 0 For TEC [N] bit assignments

Table x-x Base Address Register 0 For TEC [N] bit assignments

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Name | Default value | Access | Description |
| 31:0 | LSRAM Address Base 0 | 0xF0000000 + N \* 0x00100000 | RO | Fixed address pointer to point to the start of LSRAM 0. |

### Base Address Register 1 For TEC [N]

The following figure shows the Base Address Register 1 For TEC [N] bit assignments

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 |  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0 |
| ls1\_base1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Figure x-x Base Address Register 1 For TEC [N] bit assignments

The following table shows the Base Address Register 1 For TEC [N] bit assignments

Table x-x Base Address Register 1 For TEC [N] bit assignments

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Name | Default value | Access | Description |
| 31:0 | LSRAM Address Base 1 | 0xF0080000 + N \* 0x00100000 | RO | Fixed address pointer to point to the start of LSRAM 1. |

### Base Address Register 2 For TEC [N]

The following figure shows the Base Address Register 2 For TEC [N] bit assignments

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 |  | | | | | | | | | | 20 | 19 | 18 |  | | 15 | 14 |  | | | | | | | | | | | | | 0 |
| ls0\_base2\_h | | | | | | | | | | | | address\_bit | rsd\_0 | | | | ls0\_base2\_l | | | | | | | | | | | | | | |

Figure x-x Base Address Register 2 For TEC [N] bit assignments

The following table shows the Base Address Register 2 For TEC [N] bit assignments

Table x-x Base Address Register 2 For TEC [N] bit assignments

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Name | Default value | Access | Description |
| 31:20 | LSRAM0 Address Base 2 High Address | 0xF00 + N \* 0x001 | RO | Fixed address for each TEC. |
| 19 | Address bit | 0x0 | RW | Address bit to point to either LSRAM 0/1. |
| 18:15 | Reserved | 0x0 | RO | - |
| 14:0 | LSRAM0 Address Base 2 Low Address | 0x0 | RW | Base address. |

### Base Address Register 3 For TEC [N]

The following figure shows the Base Address Register 3 For TEC [N] bit assignments

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 |  | | | | | | | | | | 20 | 19 | 18 |  | | 15 | 14 |  | | | | | | | | | | | | | 0 |
| ls1\_base3\_h | | | | | | | | | | | | address\_bit | rsd\_0 | | | | ls1\_base3\_l | | | | | | | | | | | | | | |

Figure x-x Base Address Register 3 For TEC [N] bit assignments

The following table shows the Base Address Register 3 For TEC [N] bit assignments

Table x-x Base Address Register 3 For TEC [N] bit assignments

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bits | Name | Default value | Access | Description |
| 31:20 | LSRAM1 Address Base 3 High Address | 0xF00 + N \* 0x001 | RO | Fixed address for each TEC. |
| 19 | Address bit | 0x0 | RW | Address bit to point to either LSRAM 0/1. |
| 18:15 | Reserved | 0x0 | RO | - |
| 14:0 | LSRAM0 Address Base 3 Low Address | 0x0 | RW | Base address. |