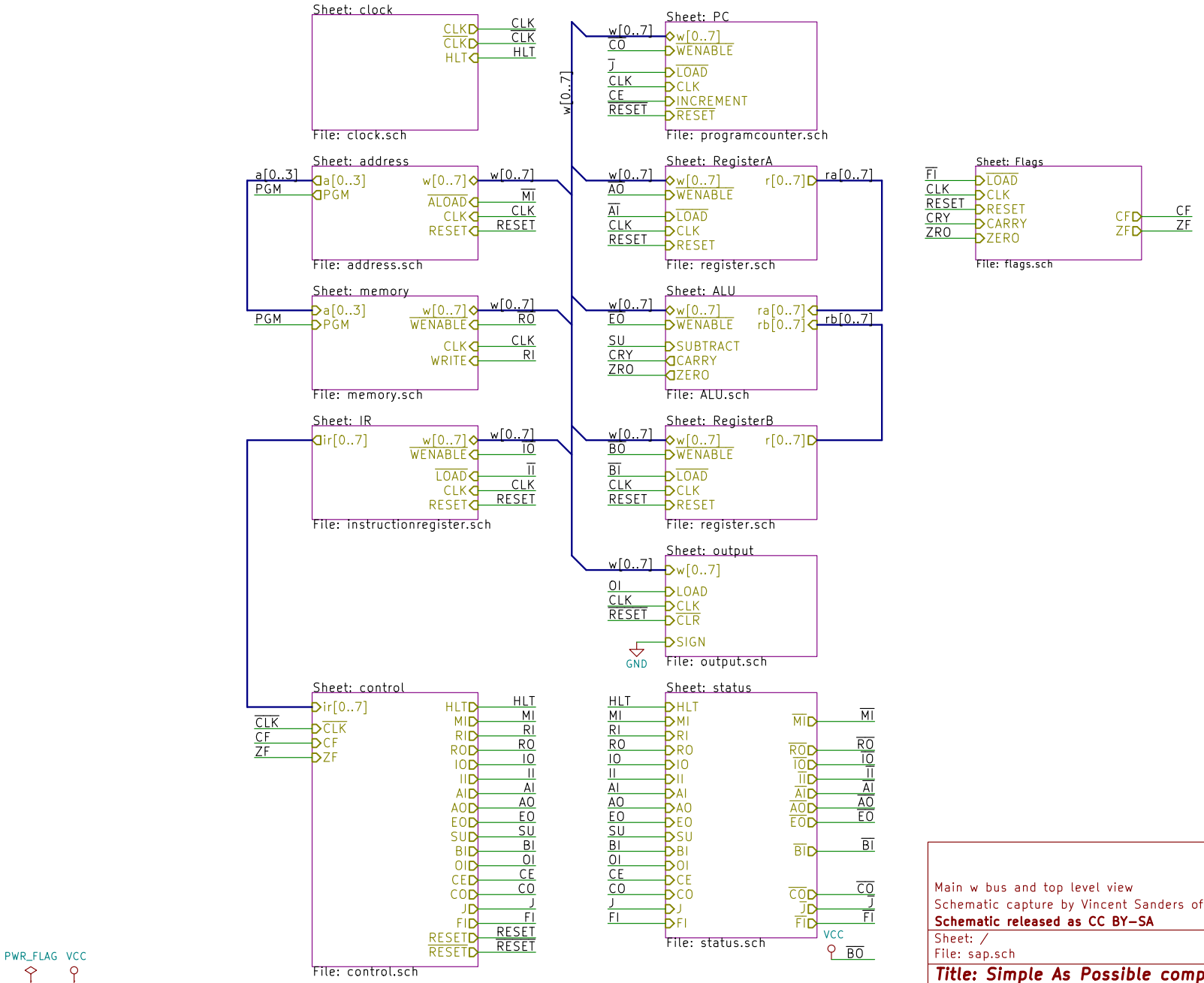
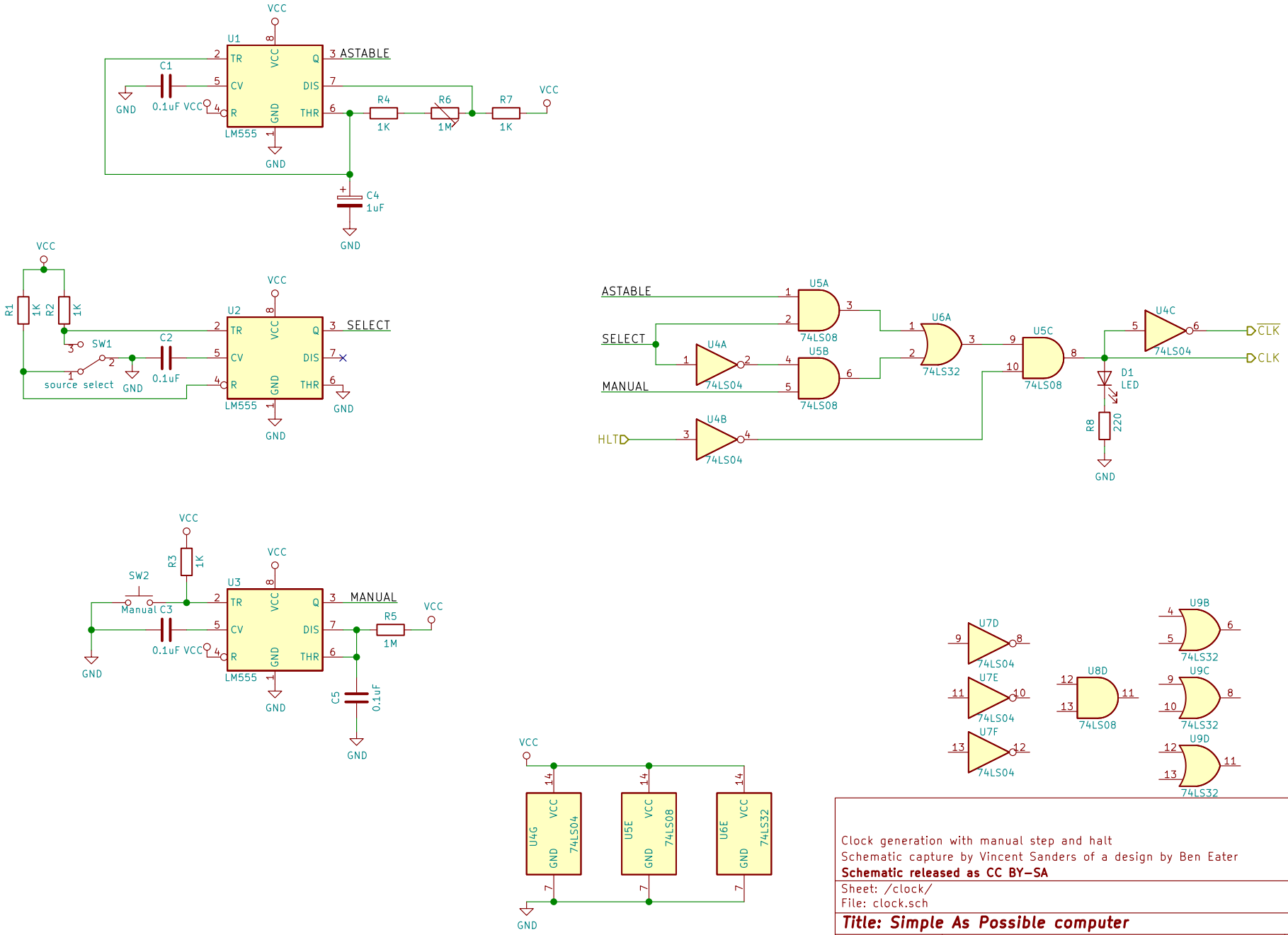

Sheet: clock
File: clock.sch
Sheet: PC
File: programcounter.sch
Sheet: address
File: address.sch
Sheet: RegisterA
File: register.sch
Sheet: Flags
File: flags.sch
Sheet: memory
File: memory.sch
Sheet: ALU
File: ALU.sch
Sheet: IR
File: instructionregister.sch
Sheet: RegisterB
File: register.sch
Sheet: output
File: output.sch
Sheet: control
File: control.sch
Sheet: status
File: status.sch
PWR_FLAG VCC
GND PWR_FLAG
Main w bus and top level view
Schematic capture by Vincent Sanders of a design by Ben Eater
Schematic released as CC BY-SA
Sheet: /
File: sap.sch
Title: Simple As Possible computer
Size: A4
Date: 2017-05-10
Rev: 1
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1
Id: 1/13

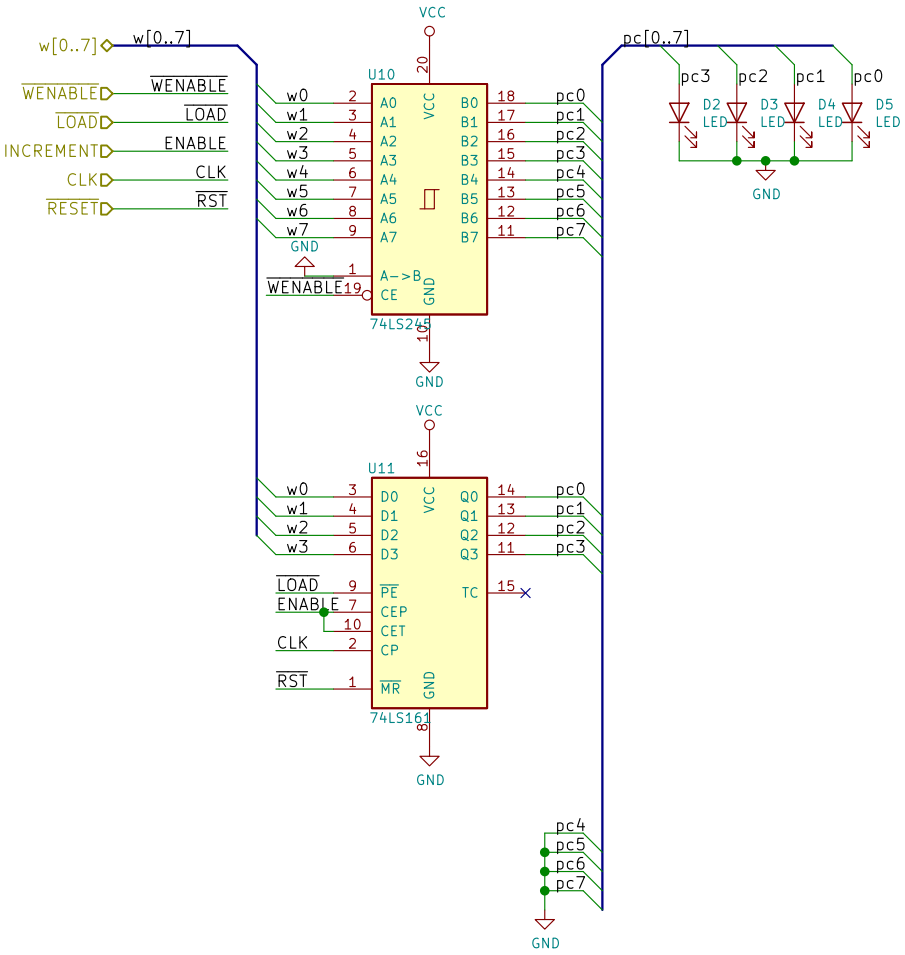


Clock generation with manual step and halt
Schematic capture by Vincent Sanders of a design by Ben Eater
Schematic released as CC BY-SA

Sheet: /clock/
File: clock.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 2/13

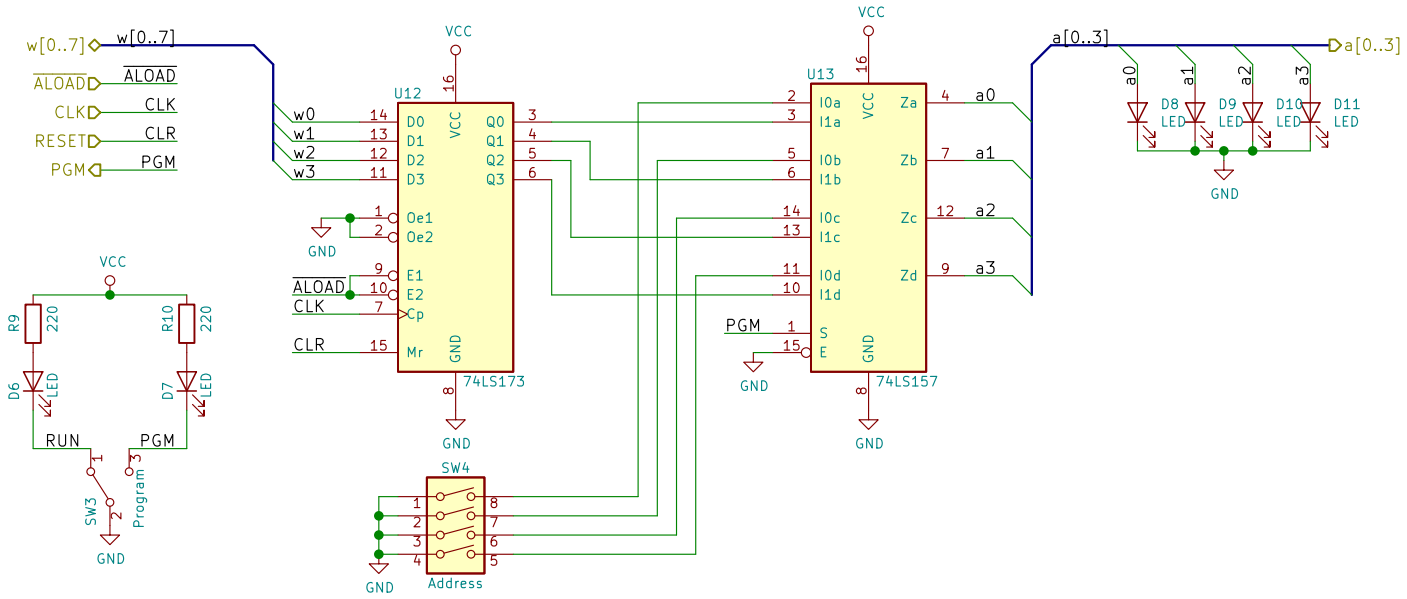


Program counter
Schematic capture by Vincent Sanders of a design by Ben Eater
Schematic released as CC BY-SA

Sheet: /PC/
File: programcounter.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 3/13

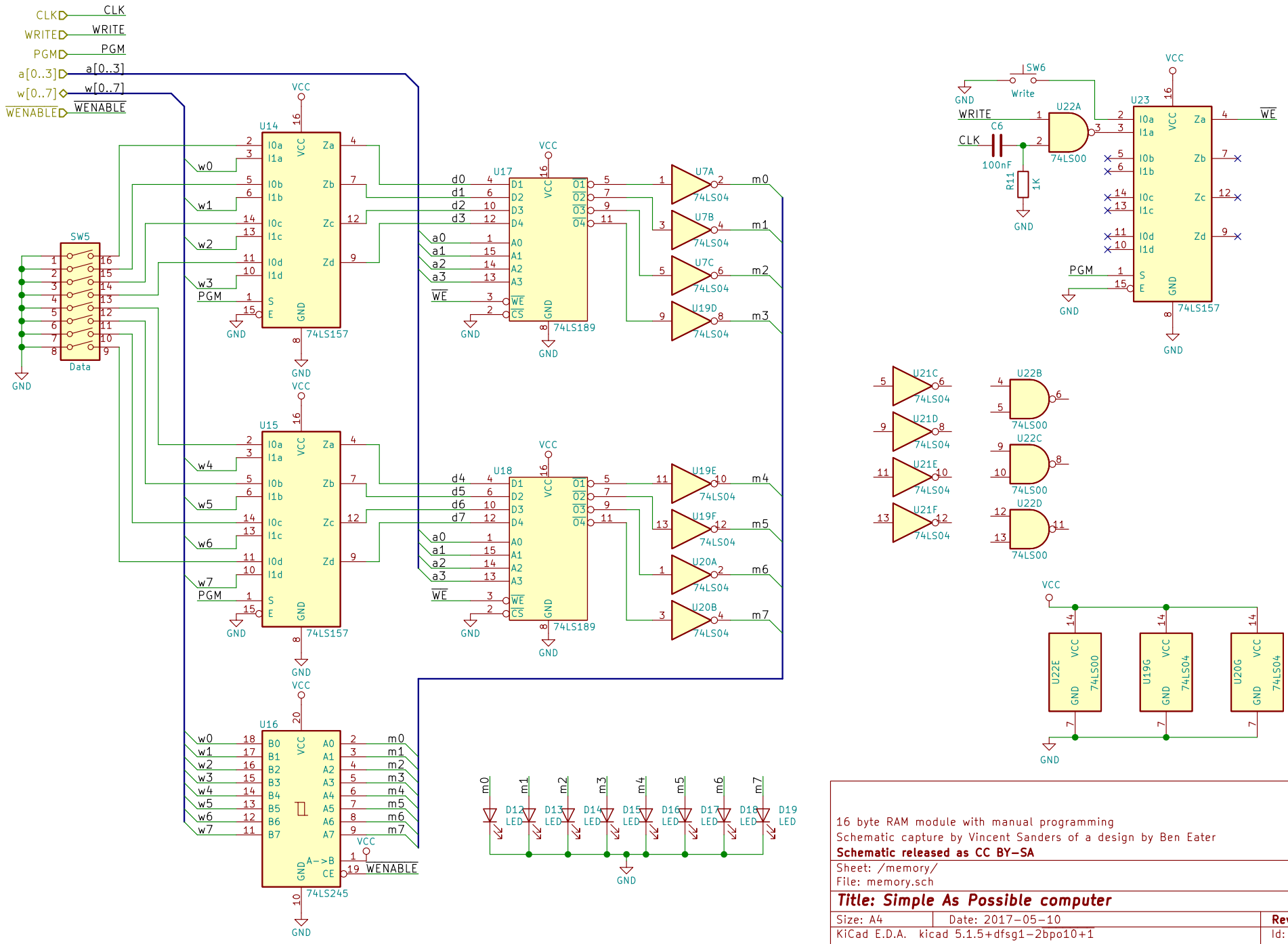


Address latch with manual programming
Schematic capture by Vincent Sanders of a design by Ben Eater
Schematic released as CC BY-SA

Sheet: /address/
File: address.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 4/13

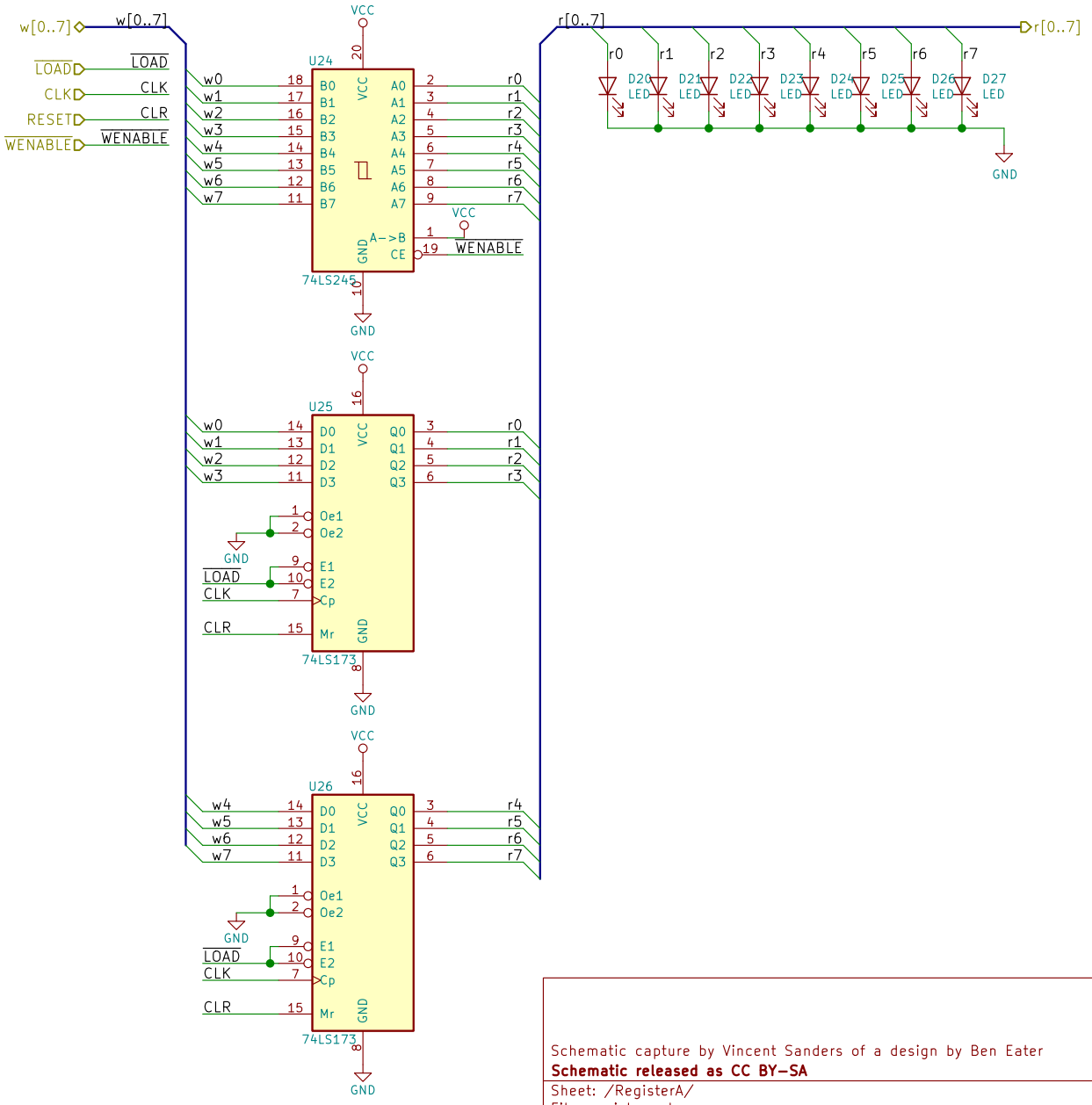


16 byte RAM module with manual programming
Schematic capture by Vincent Sanders of a design by Ben Eater
Schematic released as CC BY-SA

Sheet: /memory/
File: memory.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 5/13



Schematic capture by Vincent Sanders of a design by Ben Eater

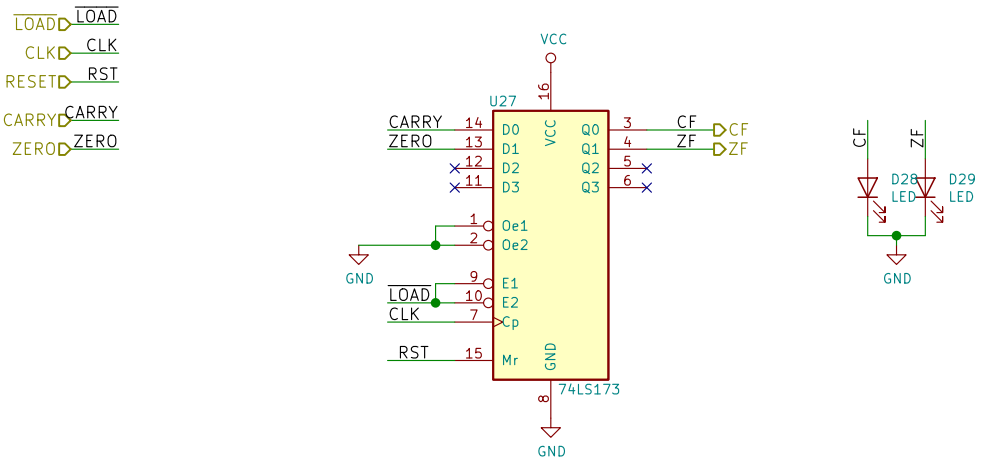
Schematic released as CC BY-SA

Sheet: /RegisterA/

File: register.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 6/13



Flags register

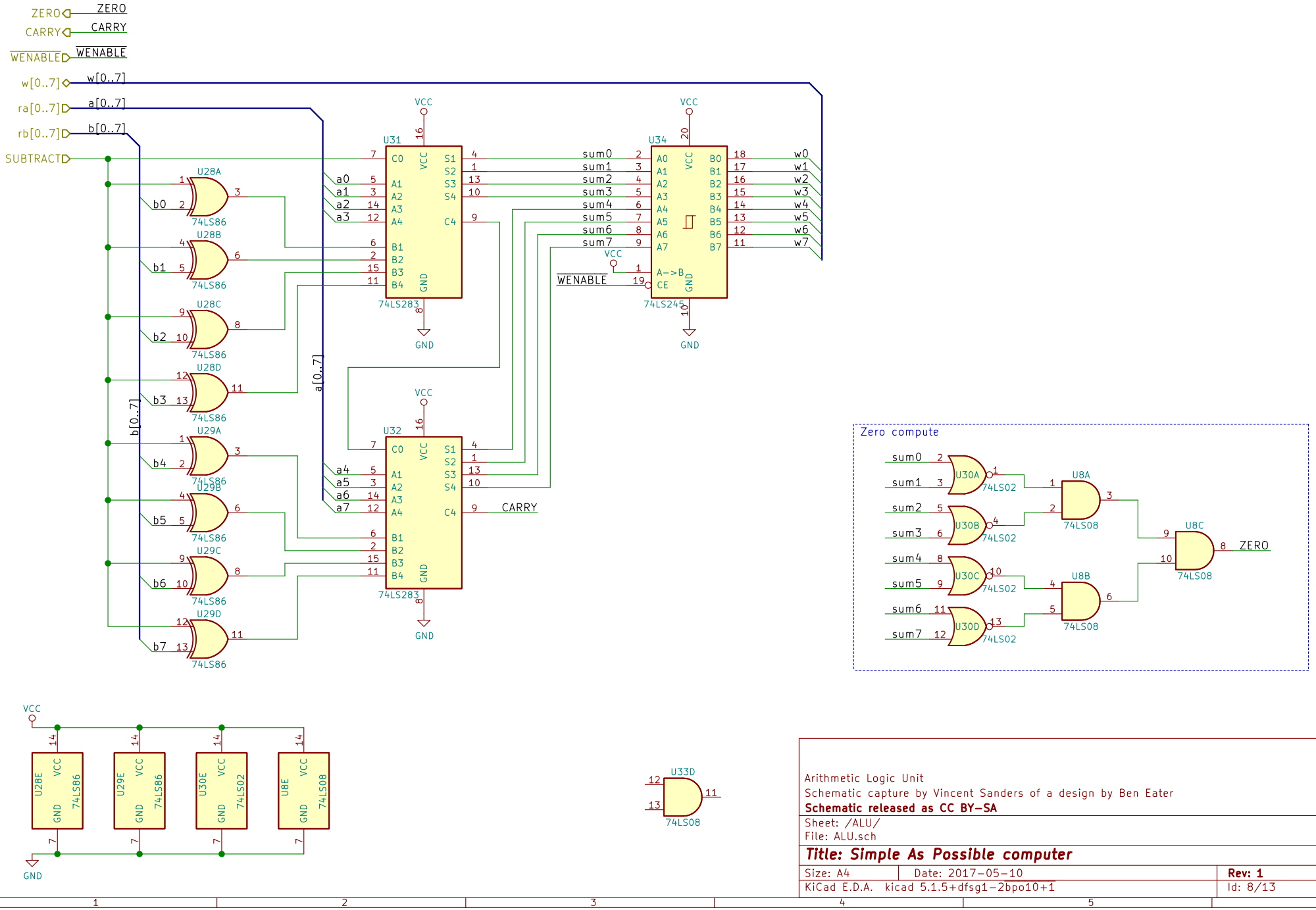
Schematic capture by Vincent Sanders of a design by Ben Eater

Sheet: /Flags/

File: flags.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 7/13

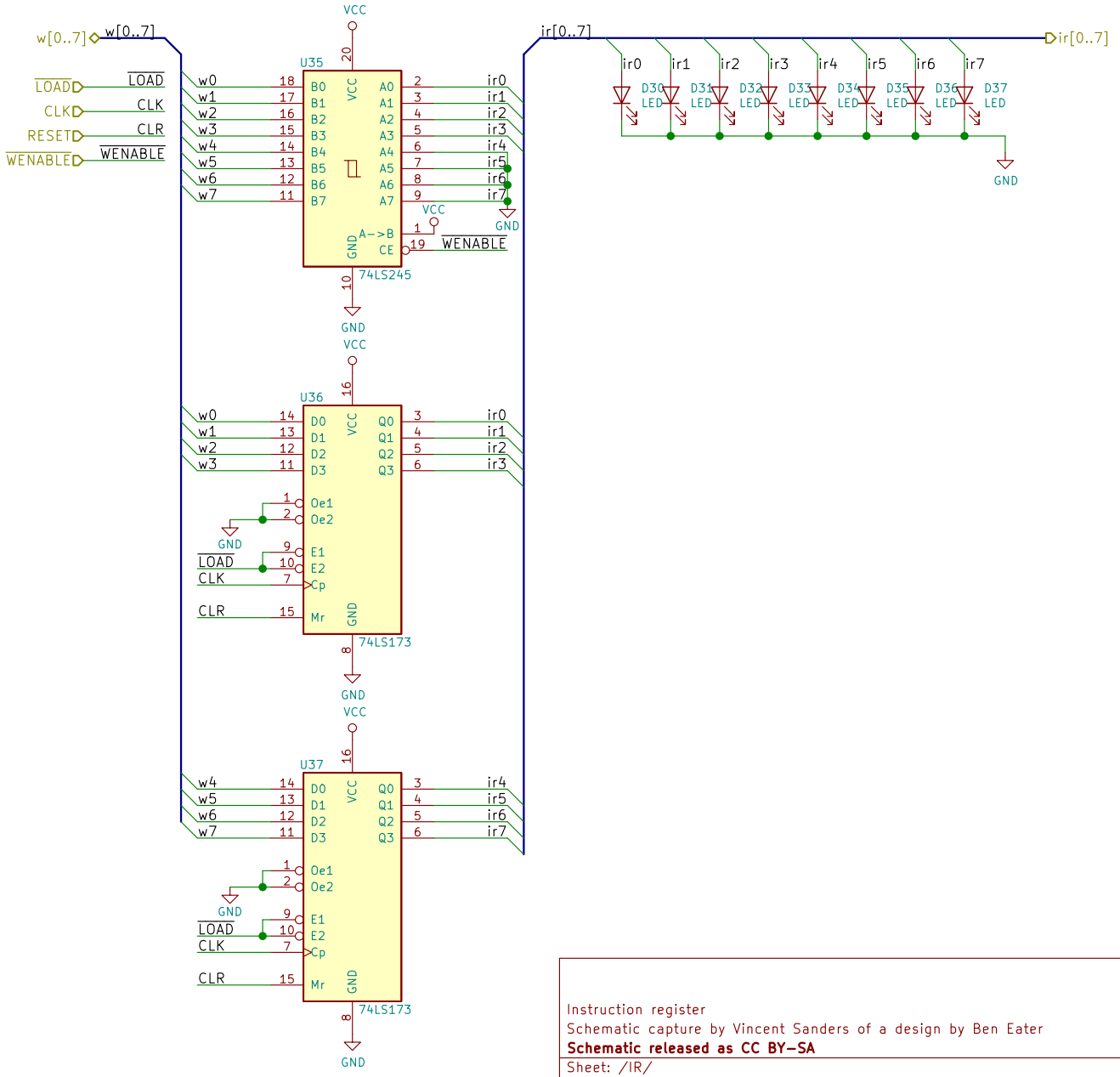


Arithmetic Logic Unit
Schematic capture by Vincent Sanders of a design by Ben Eater
Schematic released as CC BY-SA

Sheet: /ALU/
File: ALU.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 8/13

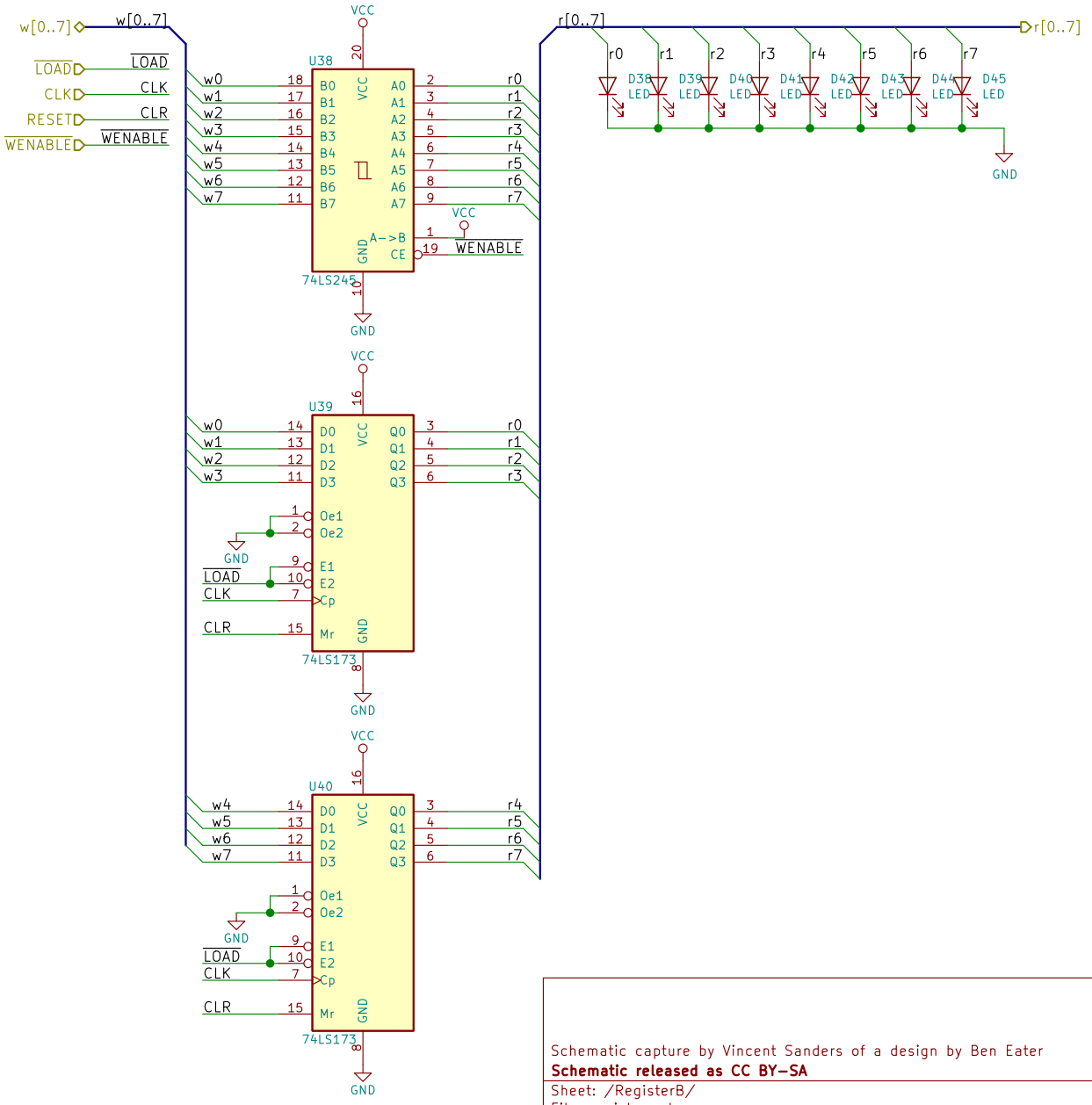


Instruction register
Schematic capture by Vincent Sanders of a design by Ben Eater
Schematic released as CC BY-SA

Sheet: /IR/
File: instructionregister.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 9/13



Schematic capture by Vincent Sanders of a design by Ben Eater

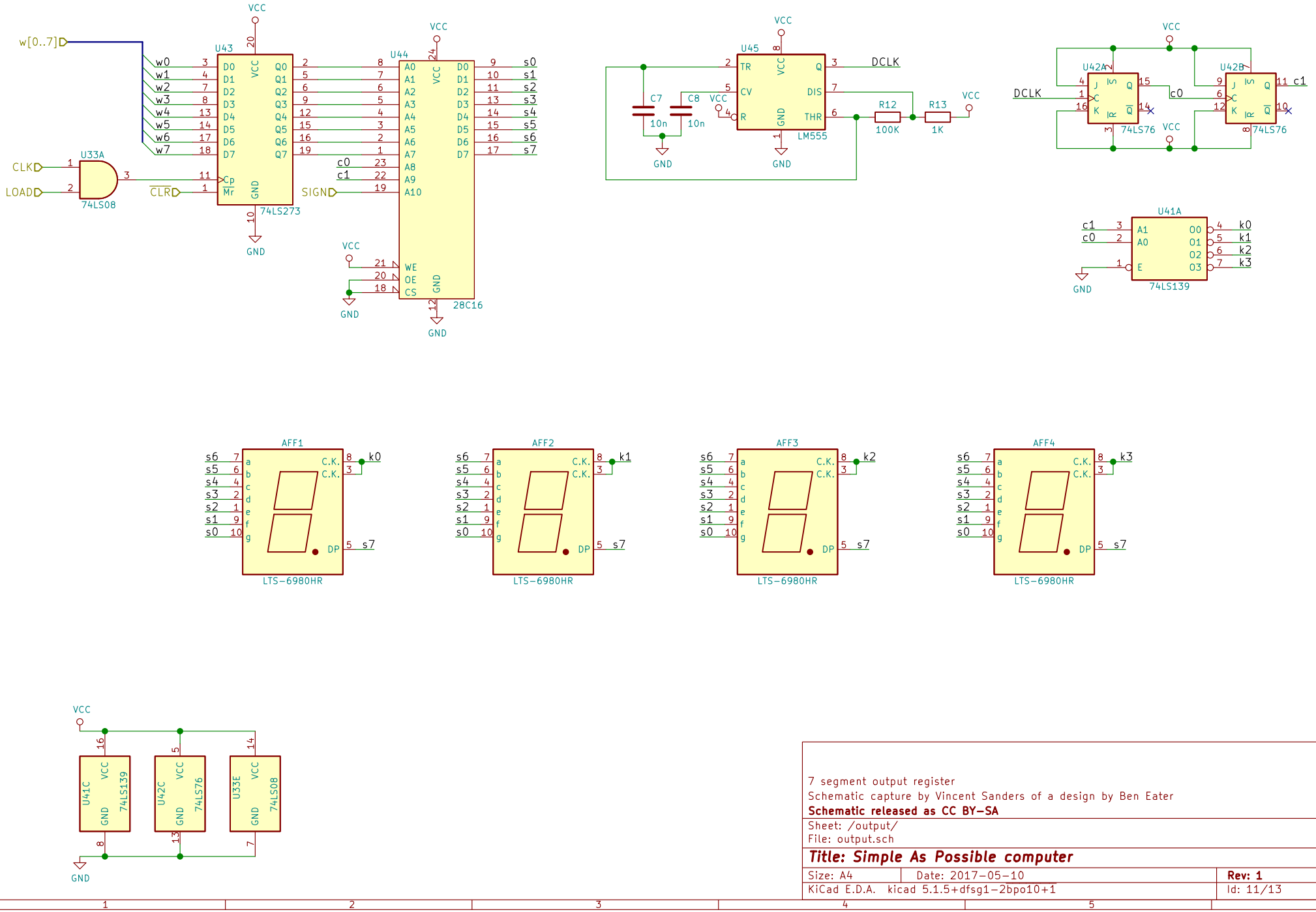
Schematic released as CC BY-SA

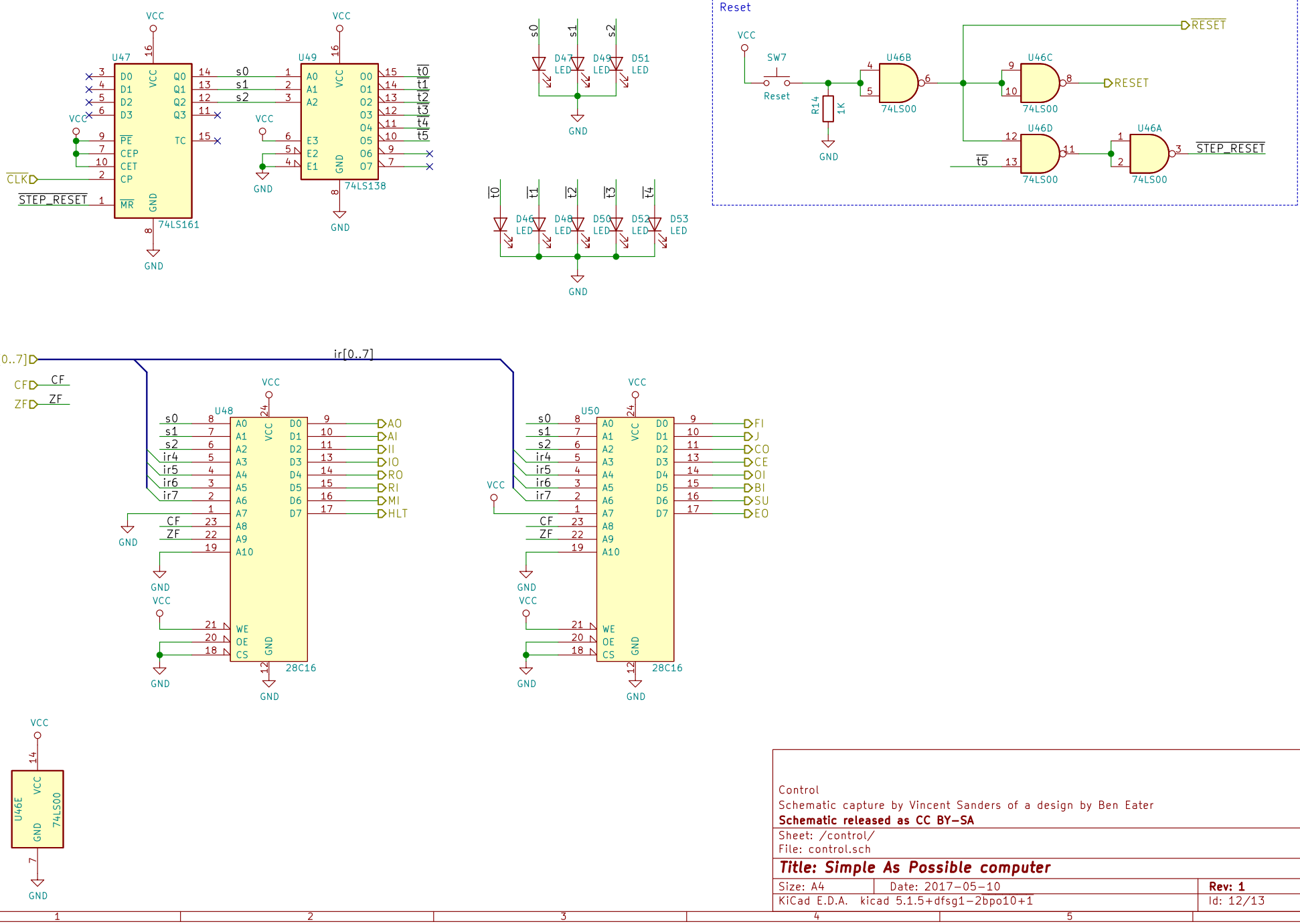
Sheet: /RegisterB/

File: register.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 10/13

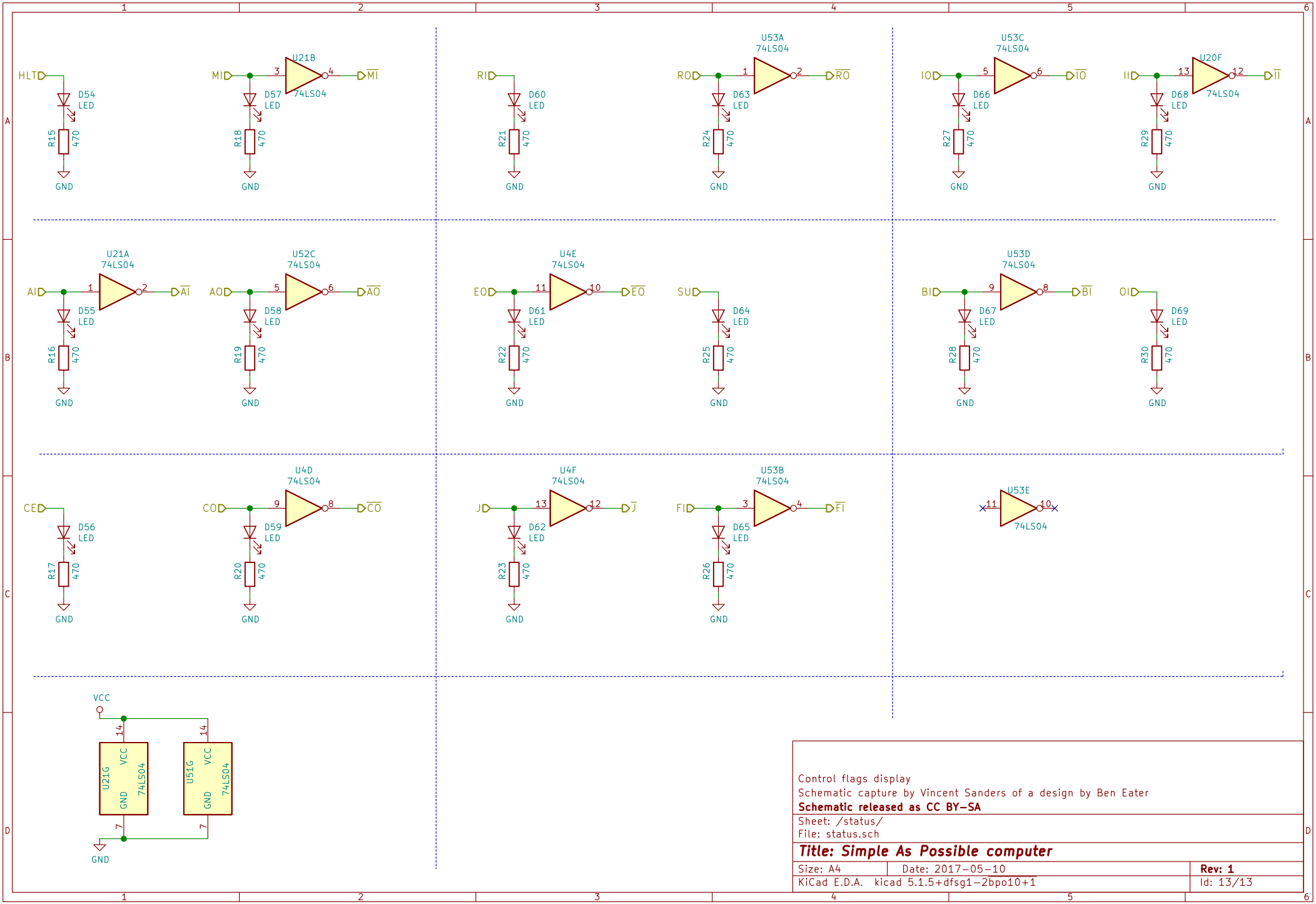

w[0..7]
U43
74LS273
U44
28C16
U33A
74LS08
CLK
LOAD
CLR
SIGN
c0
c1
VCC
GND
U45
LM555
C7
C8
10n
R12
100K
R13
1K
DCLK
U42A
U42B
74LS76
c0
c1
U41A
74LS139
k0
k1
k2
k3
AFF1
AFF2
AFF3
AFF4
LTS-6980HR
s0
s1
s2
s3
s4
s5
s6
s7
U41C
U42C
U33E
7 segment output register
Schematic capture by Vincent Sanders of a design by Ben Eater
Schematic released as CC BY-SA
Sheet: /output/
File: output.sch
Title: Simple As Possible computer
Size: A4
Date: 2017-05-10
Rev: 1
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1
Id: 11/13



Control
Schematic capture by Vincent Sanders of a design by Ben Eater
Schematic released as CC BY-SA
Sheet: /control/
File: control.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 12/13


HLT
D54
LED
R15
470
GND
MI
U21B
74LS04
D57
LED
R18
470
GND
RI
D60
LED
R21
470
GND
RO
U53A
74LS04
D63
LED
R24
470
GND
IO
U53C
74LS04
D66
LED
R27
470
GND
II
U20F
74LS04
D68
LED
R29
470
GND
AI
U21A
74LS04
D55
LED
R16
470
GND
AO
U52C
74LS04
D58
LED
R19
470
GND
EO
U4E
74LS04
D61
LED
R22
470
GND
SU
D64
LED
R25
470
GND
BI
U53D
74LS04
D67
LED
R28
470
GND
OI
D69
LED
R30
470
GND
CI
D56
LED
R17
470
GND
CO
U4D
74LS04
D59
LED
R20
470
GND
J
U4F
74LS04
D62
LED
R23
470
GND
FI
U53B
74LS04
D65
LED
R26
470
GND
U53E
74LS04
VCC
U21G
U51G
74LS04
GND
Control flags display
Schematic capture by Vincent Sanders of a design by Ben Eater
Schematic released as CC BY-SA
Sheet: /status/
File: status.sch
Title: Simple As Possible computer
Size: A4
Date: 2017-05-10
Rev: 1
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1
Id: 13/13