

Main w bus and top level view
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /
File: sap-be.sch

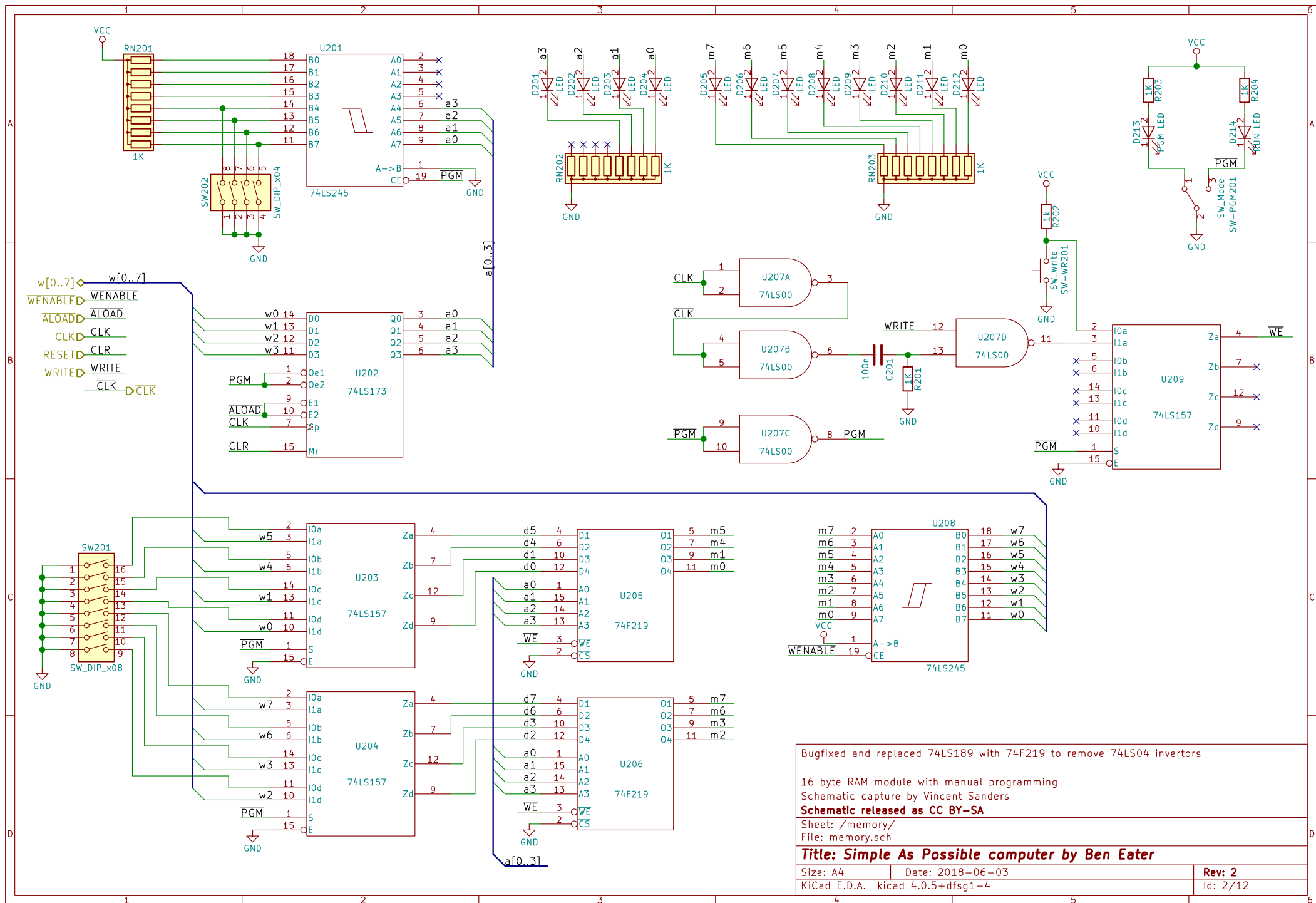
Title: Simple As Possible computer by Ben Eater

Size: A4 Date: 2018-06-03

KiCad E.D.A. kicad 4.0.5+dfsg1-4

Rev: 2

Id: 1/12



Bugfixed and replaced 74LS189 with 74F219 to remove 74LS04 invertors

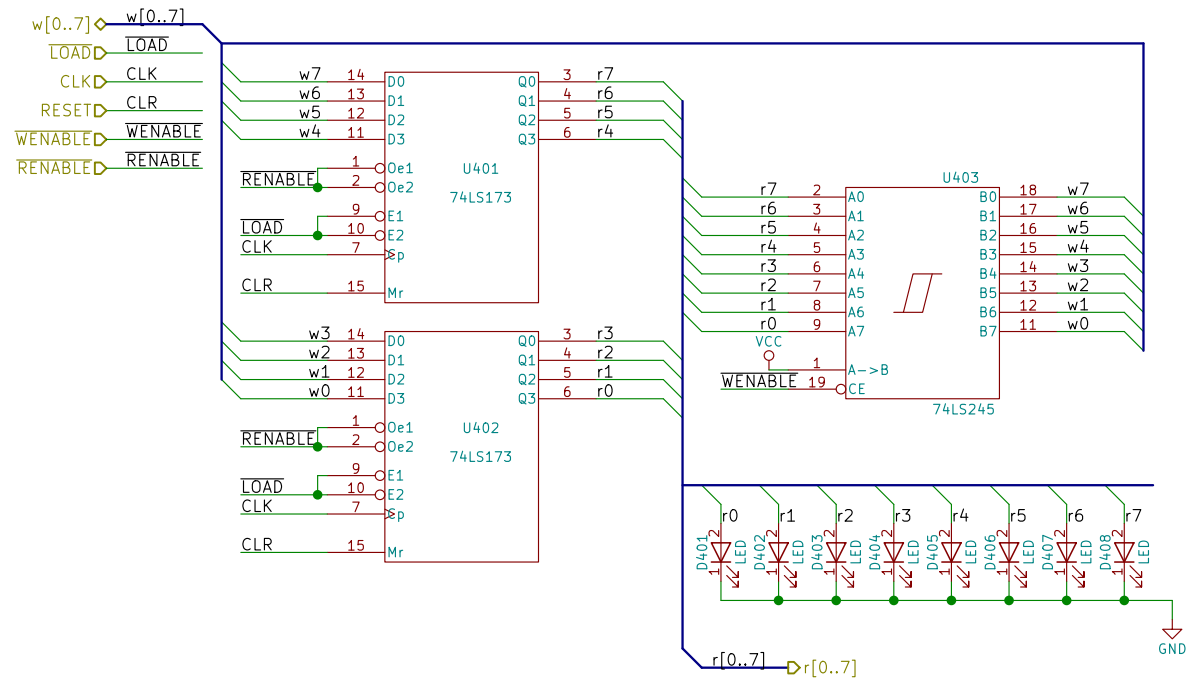
16 byte RAM module with manual programming
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /memory/
File: memory.sch

Title: Simple As Possible computer by Ben Eater

Size: A4	Date: 2018-06-03	Rev: 2
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Id: 3/12



Schematic capture by Vincent Sanders

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Sheet: /RegisterB/

File: register.sch

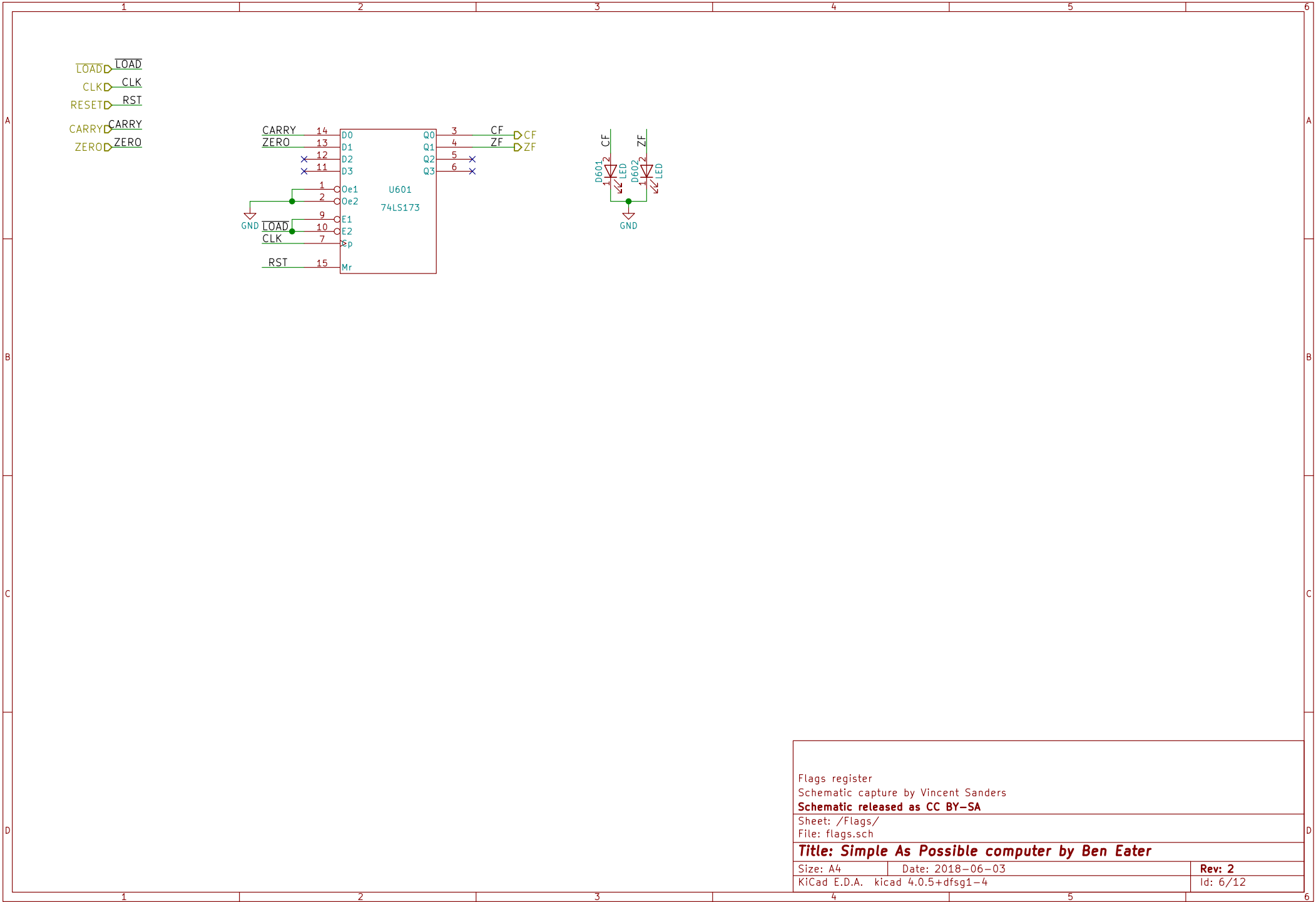
Title: Simple As Possible computer by Ben Eater

Size: A4 Date: 2018-06-03

KiCad E.D.A. kicad 4.0.5+dfsg1-4

Rev: 2

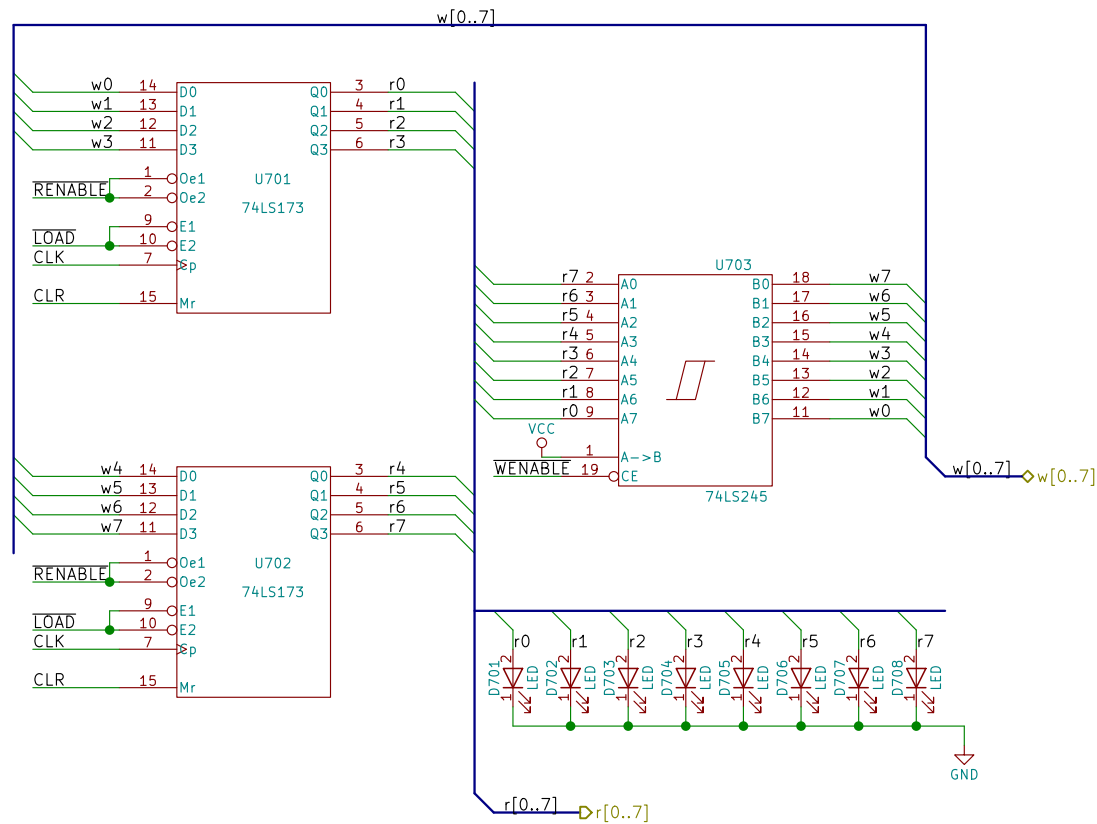
Id: 4/12



Flags register
Schematic capture by Vincent Sanders
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Sheet: /Flags/
File: flags.sch

Title: Simple As Possible computer by Ben Eater		
Size: A4	Date: 2018-06-03	Rev: 2
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LOAD \triangleright LOAD
 CLK \triangleright CLK
 RESET \triangleright CLR
 WENABLE \triangleright WENABLE
 RENABLE \triangleright RENABLE



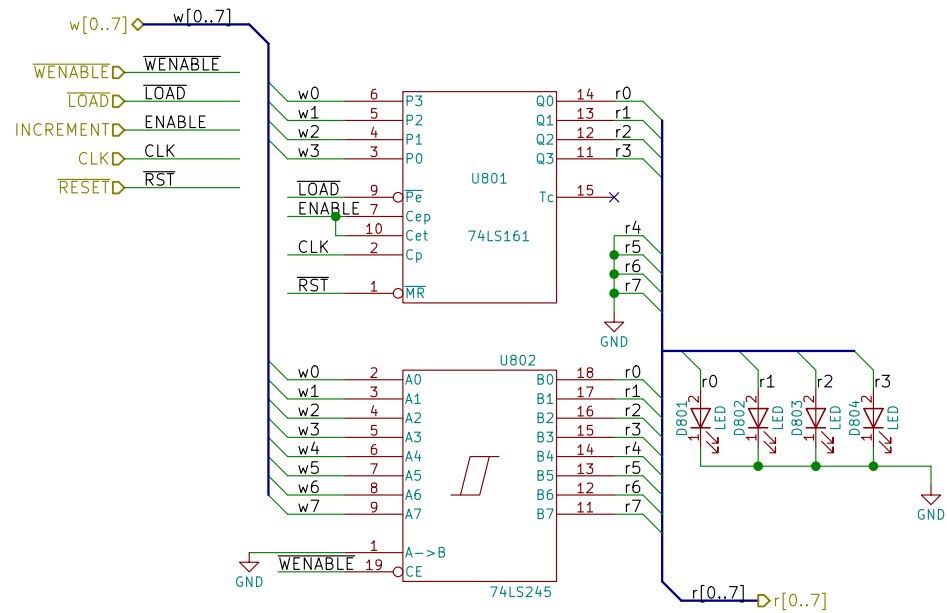
Instruction register
 Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /IR/
 File: instructionregister.sch

Title: Simple As Possible computer by Ben Eater

Size: A4
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Date: 2018-06-03
 Rev: 2
 Id: 7/12



Program counter
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /PC/
File: programcounter.sch

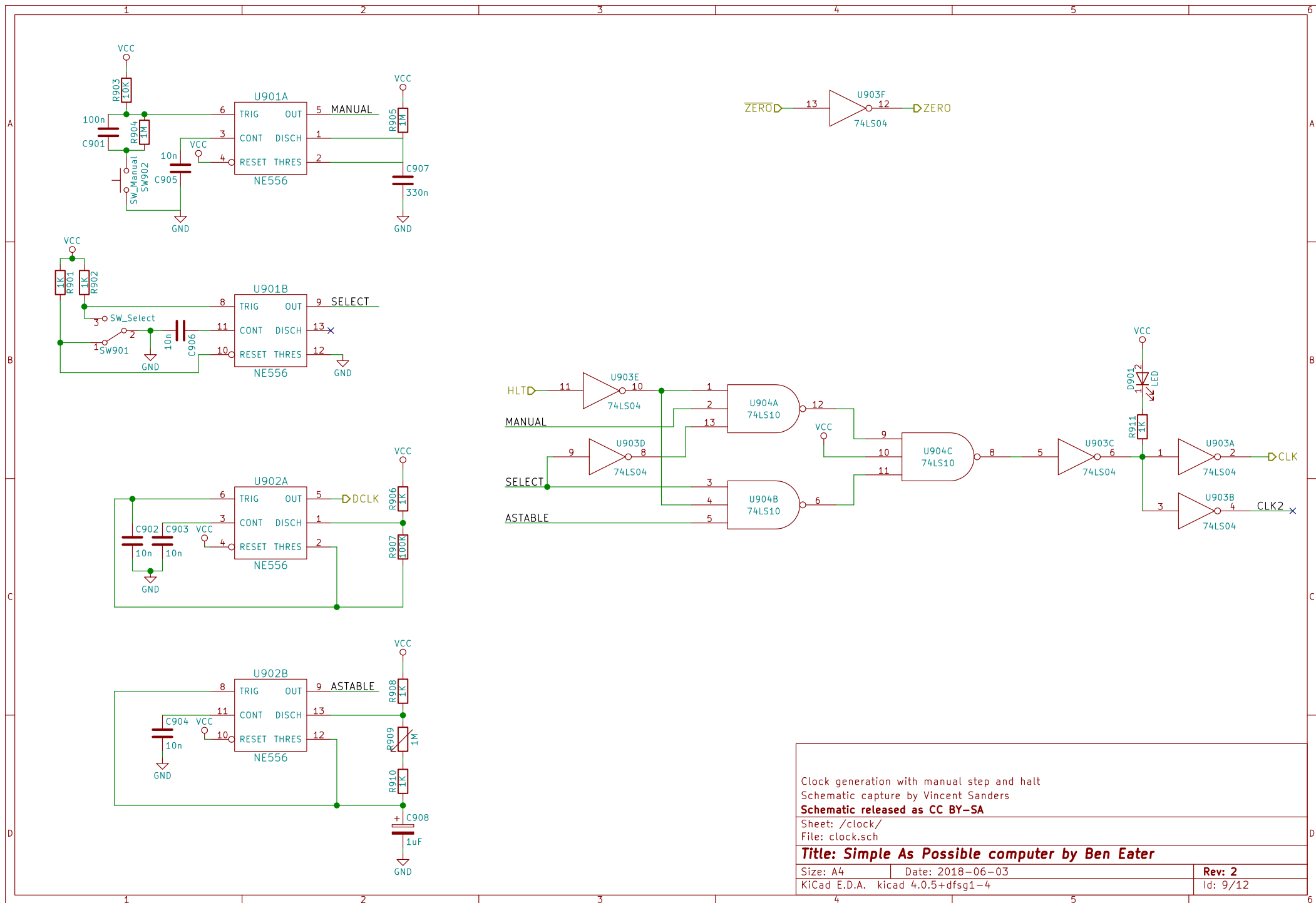
Title: Simple As Possible computer by Ben Eater

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Rev: 2

Id: 8/12



Clock generation with manual step and halt
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /clock/
File: clock.sch

Title: Simple As Possible computer by Ben Eater

Size: A4 Date: 2018-06-03

KiCad E.D.A. kicad 4.0.5+dfsg1-4

Rev: 2

Id: 9/12

