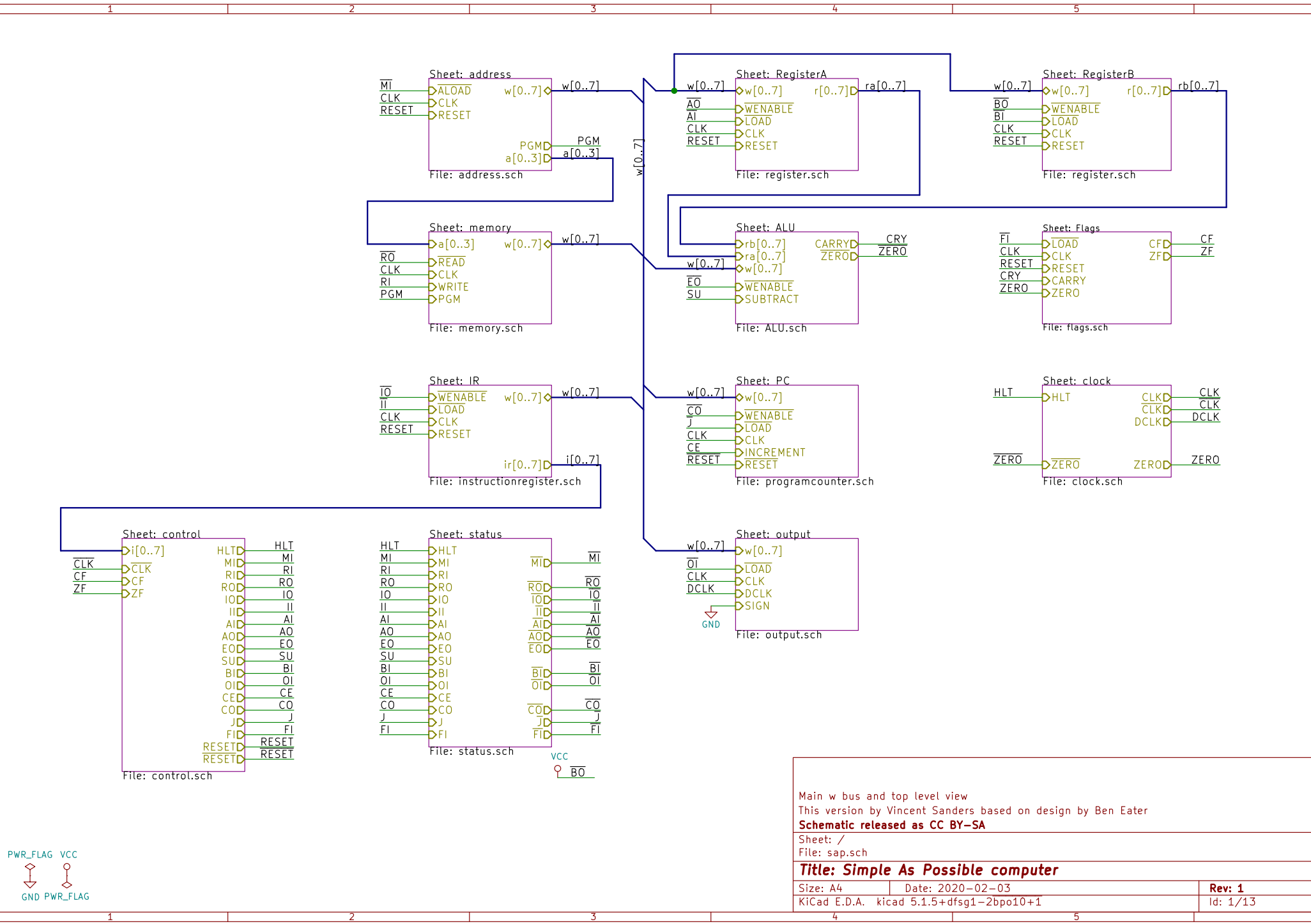
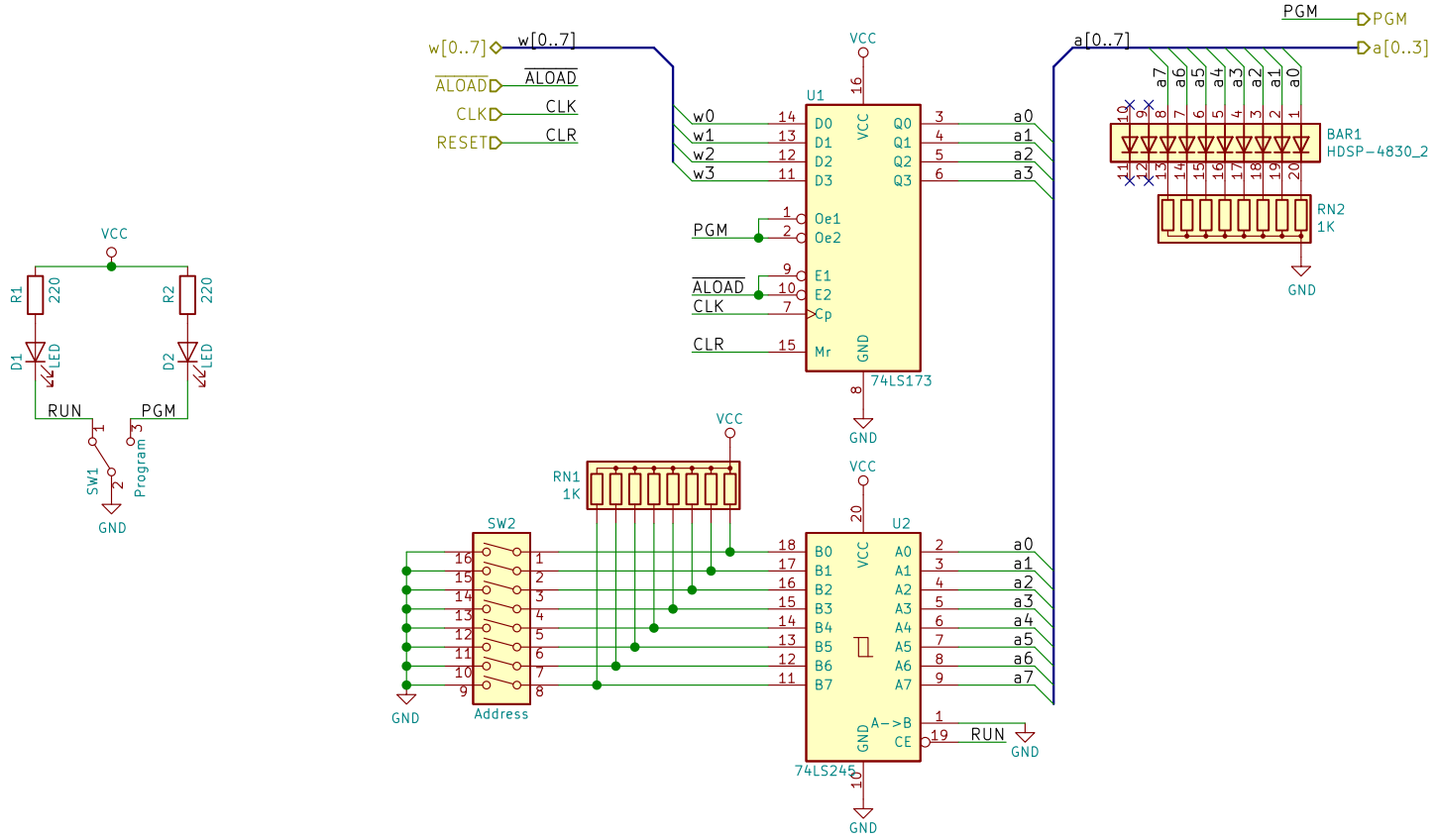

Sheet: address
MI
CLK
RESET
ALOAD
CLK
RESET
w[0..7]
PGM
a[0..3]
File: address.sch
Sheet: RegisterA
w[0..7]
AO
AI
CLK
RESET
w[0..7]
r[0..7]
WENABLE
LOAD
CLK
RESET
ra[0..7]
File: register.sch
Sheet: RegisterB
w[0..7]
BO
BI
CLK
RESET
w[0..7]
r[0..7]
WENABLE
LOAD
CLK
RESET
rb[0..7]
File: register.sch
Sheet: memory
a[0..3]
RO
CLK
RI
PGM
w[0..7]
READ
CLK
WRITE
PGM
File: memory.sch
Sheet: ALU
rb[0..7]
ra[0..7]
w[0..7]
EO
SU
CARRY
ZERO
WENABLE
SUBTRACT
CRY
ZERO
File: ALU.sch
Sheet: Flags
FI
CLK
RESET
CRY
ZERO
LOAD
CLK
RESET
CARRY
ZERO
CF
ZF
CF
ZF
File: flags.sch
Sheet: IR
IO
II
CLK
RESET
w[0..7]
WENABLE
LOAD
CLK
RESET
ir[0..7]
i[0..7]
File: instructionregister.sch
Sheet: PC
w[0..7]
CO
J
CLK
CE
RESET
w[0..7]
WENABLE
LOAD
CLK
INCREMENT
RESET
File: programcounter.sch
Sheet: clock
HLT
ZERO
HLT
ZERO
CLK
CLK
DCLK
CLK
CLK
DCLK
ZERO
ZERO
File: clock.sch
Sheet: control
i[0..7]
CLK
CF
ZF
CLK
CF
ZF
HLT
MI
RI
RO
IO
II
AI
AO
EO
SU
BI
OI
CE
CO
J
FI
RESET
RESET
HLT
MI
RI
RO
IO
II
AI
AO
EO
SU
BI
OI
CE
CO
J
FI
RESET
RESET
File: control.sch
Sheet: status
HLT
MI
RI
RO
IO
II
AI
AO
EO
SU
BI
OI
CE
CO
J
FI
HLT
MI
RI
RO
IO
II
AI
AO
EO
SU
BI
OI
CE
CO
J
FI
MI
RO
IO
II
AI
AO
EO
BI
OI
CO
J
FI
MI
RO
IO
II
AI
AO
EO
BI
OI
CO
J
FI
File: status.sch
VCC
BO
Sheet: output
w[0..7]
OI
CLK
DCLK
GND
w[0..7]
LOAD
CLK
DCLK
SIGN
File: output.sch
w[0..7]
PWR_FLAG
VCC
GND
PWR_FLAG
Main w bus and top level view
This version by Vincent Sanders based on design by Ben Eater
Schematic released as CC BY-SA
Sheet: /
File: sap.sch
Title: Simple As Possible computer
Size: A4
Date: 2020-02-03
Rev: 1
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1
Id: 1/13

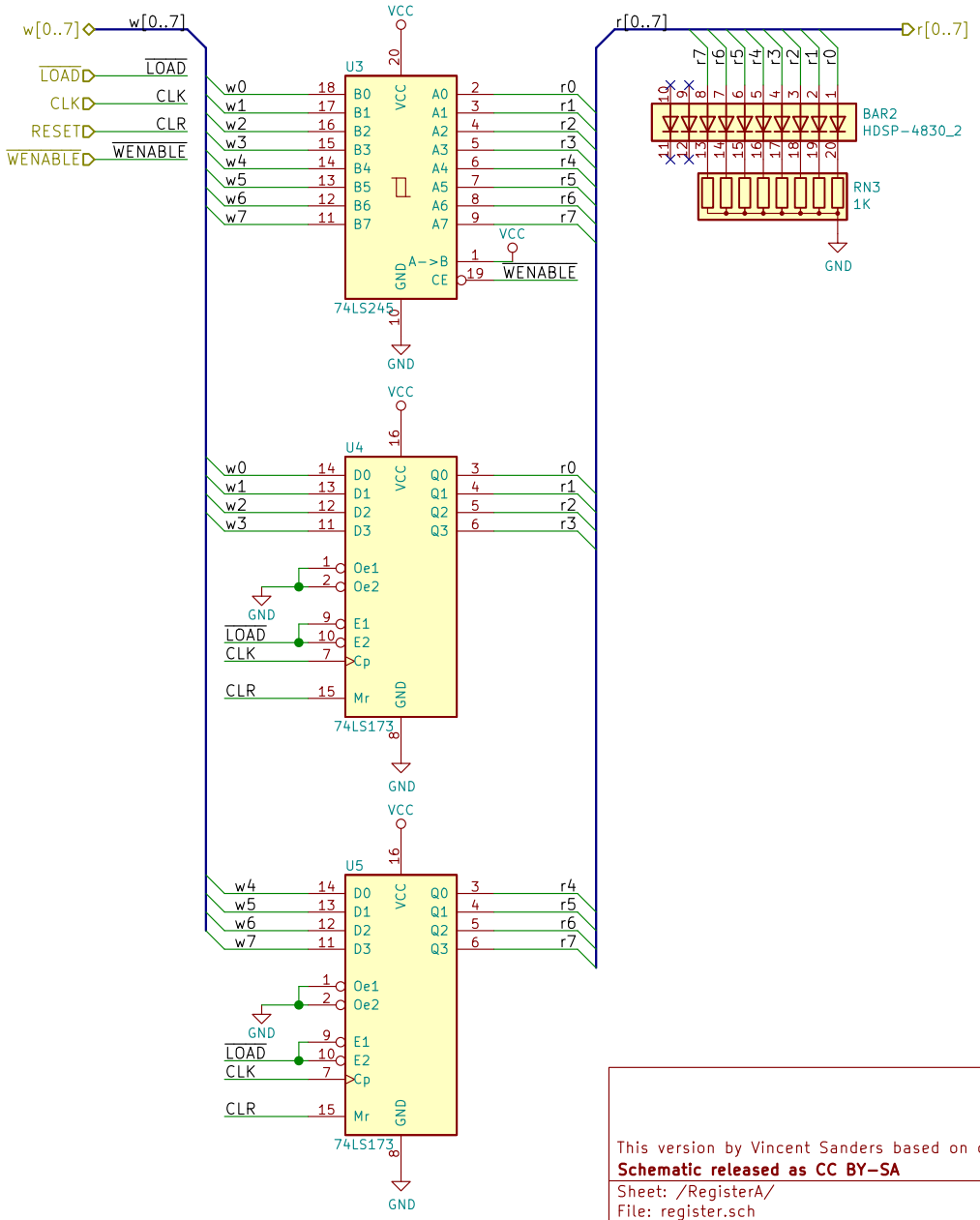


Address latch with manual programming
This version by Vincent Sanders based on design by Ben Eater
Schematic released as CC BY-SA

Sheet: /address/
File: address.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 2/13



This version by Vincent Sanders based on design by Ben Eater

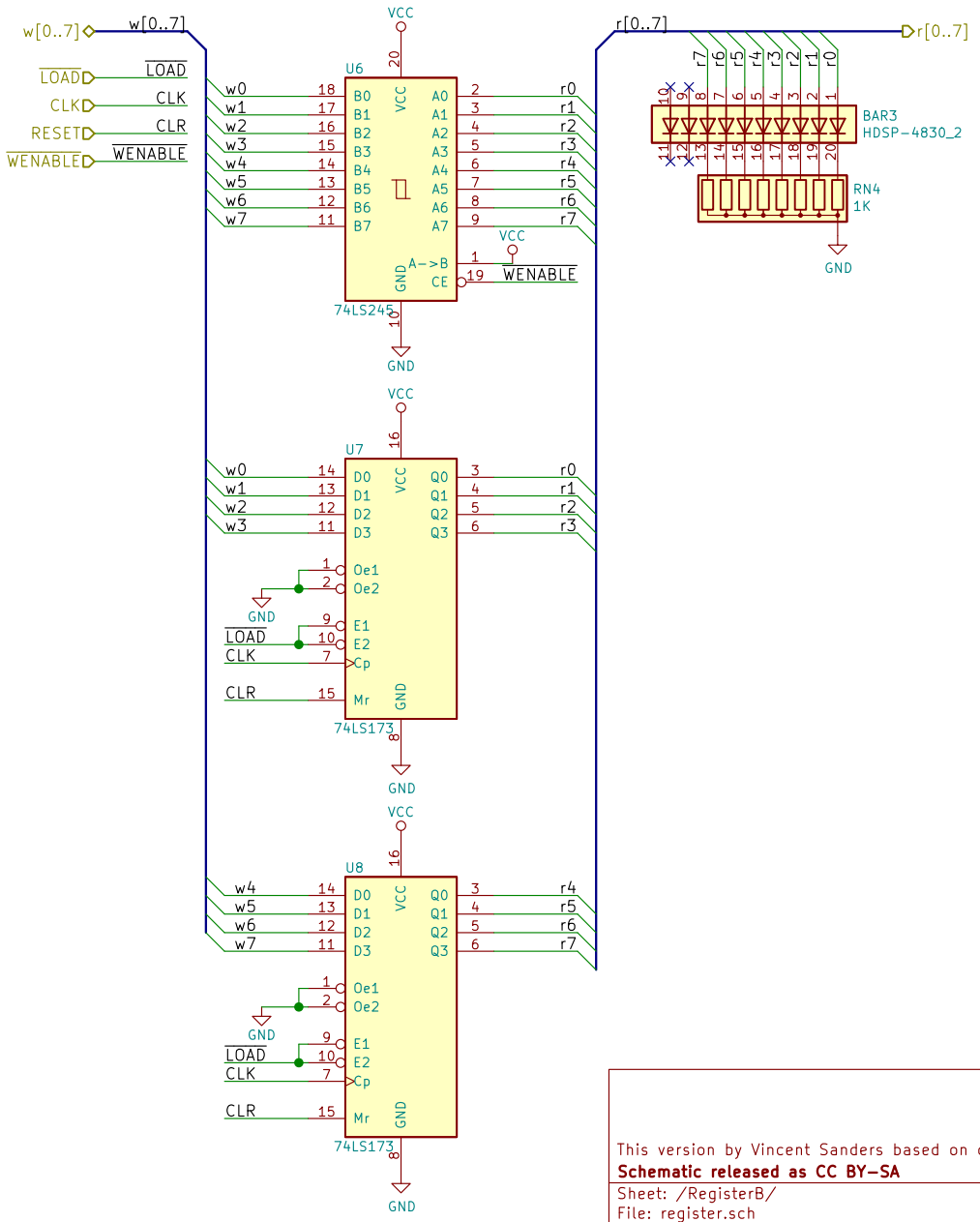
Schematic released as CC BY-SA

Sheet: /RegisterA/

File: register.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 3/13



This version by Vincent Sanders based on design by Ben Eater

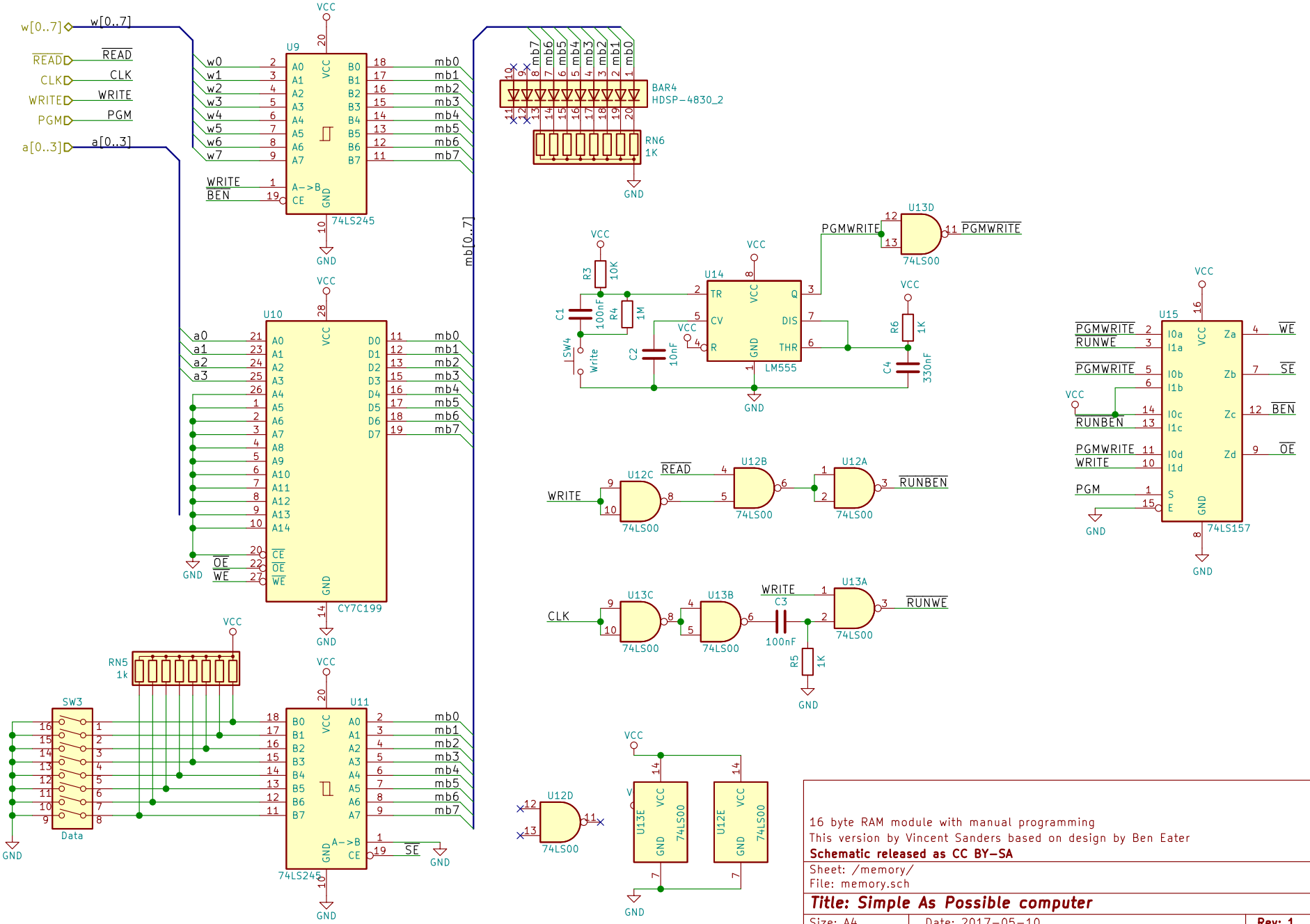
Schematic released as CC BY-SA

Sheet: /RegisterB/

File: register.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 4/13

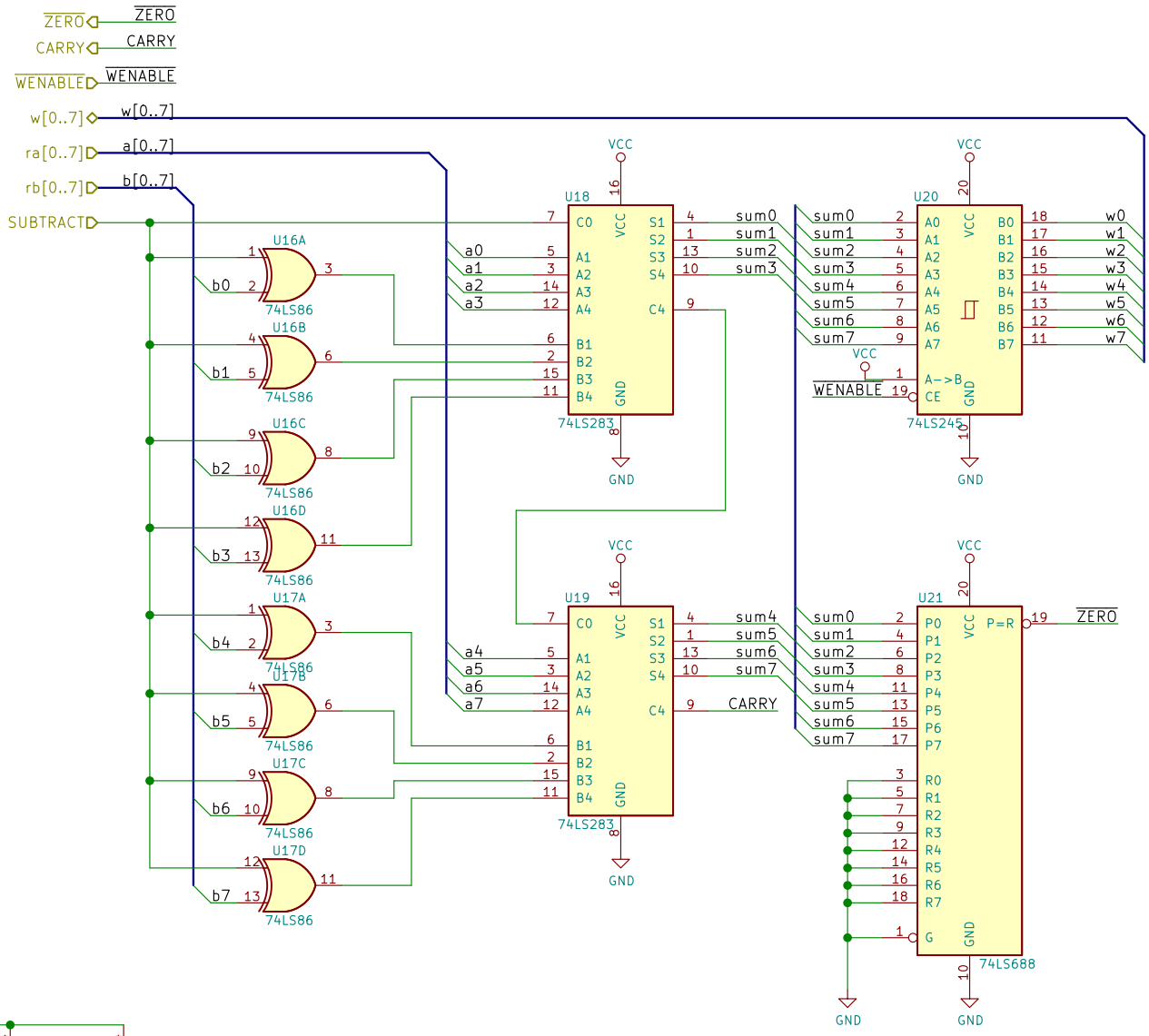


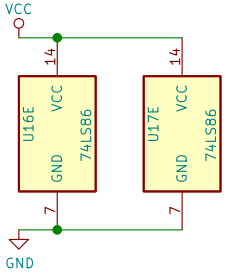
16 byte RAM module with manual programming
This version by Vincent Sanders based on design by Ben Eater
Schematic released as CC BY-SA

Sheet: /memory/
File: memory.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 5/13





Arithmetic Logic Unit

This version by Vincent Sanders based on design by Ben Eater

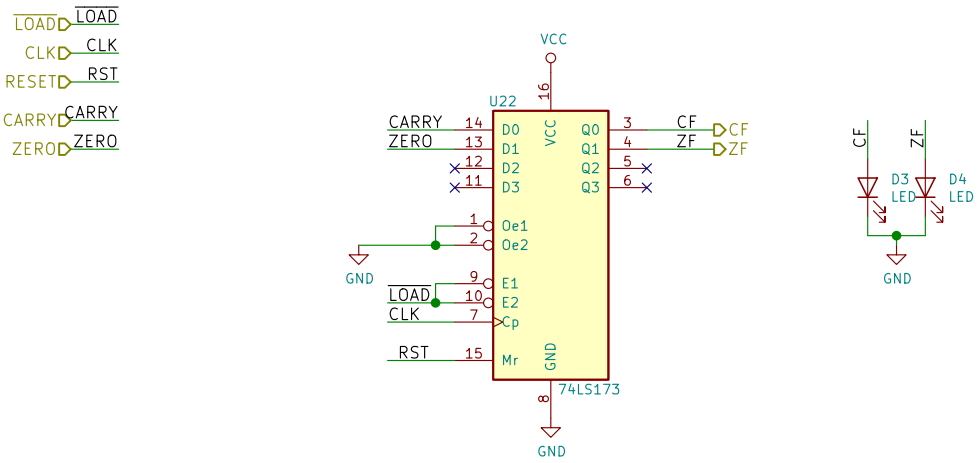
Schematic released as CC BY-SA

Sheet: /ALU/

File: ALU.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 6/13



Flags register

This version by Vincent Sanders based on design by Ben Eater

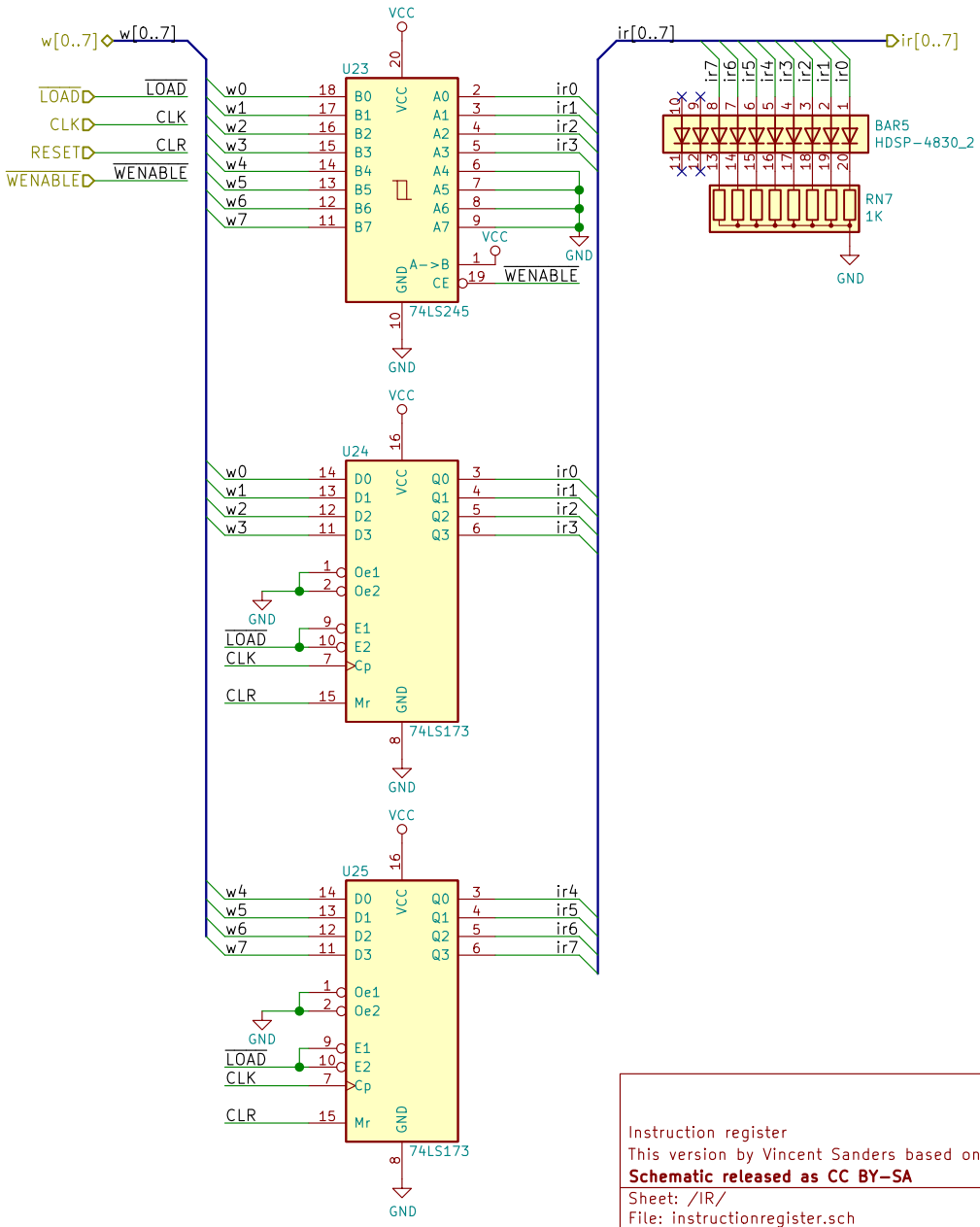
Schematic released as CC BY-SA

Sheet: /Flags/

File: flags.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 7/13

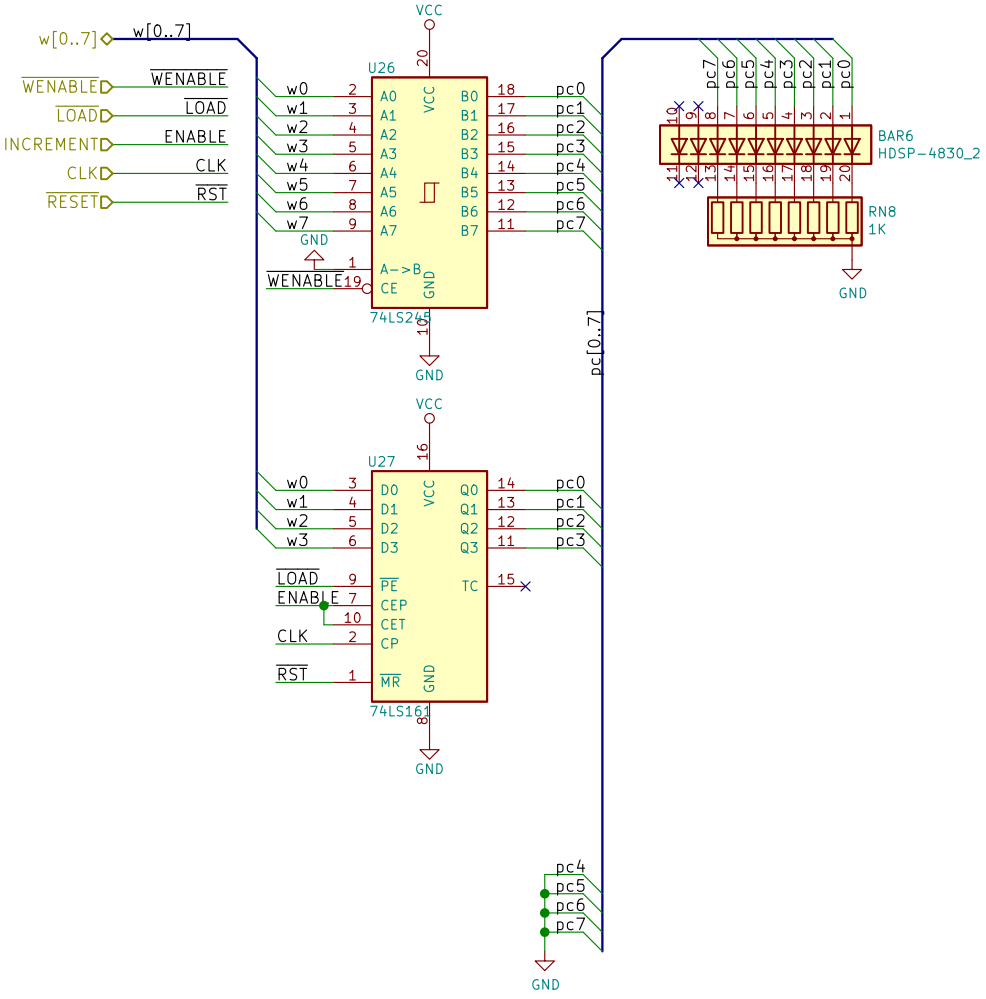


Instruction register
This version by Vincent Sanders based on design by Ben Eater
Schematic released as CC BY-SA

Sheet: /IR/
File: instructionregister.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 8/13

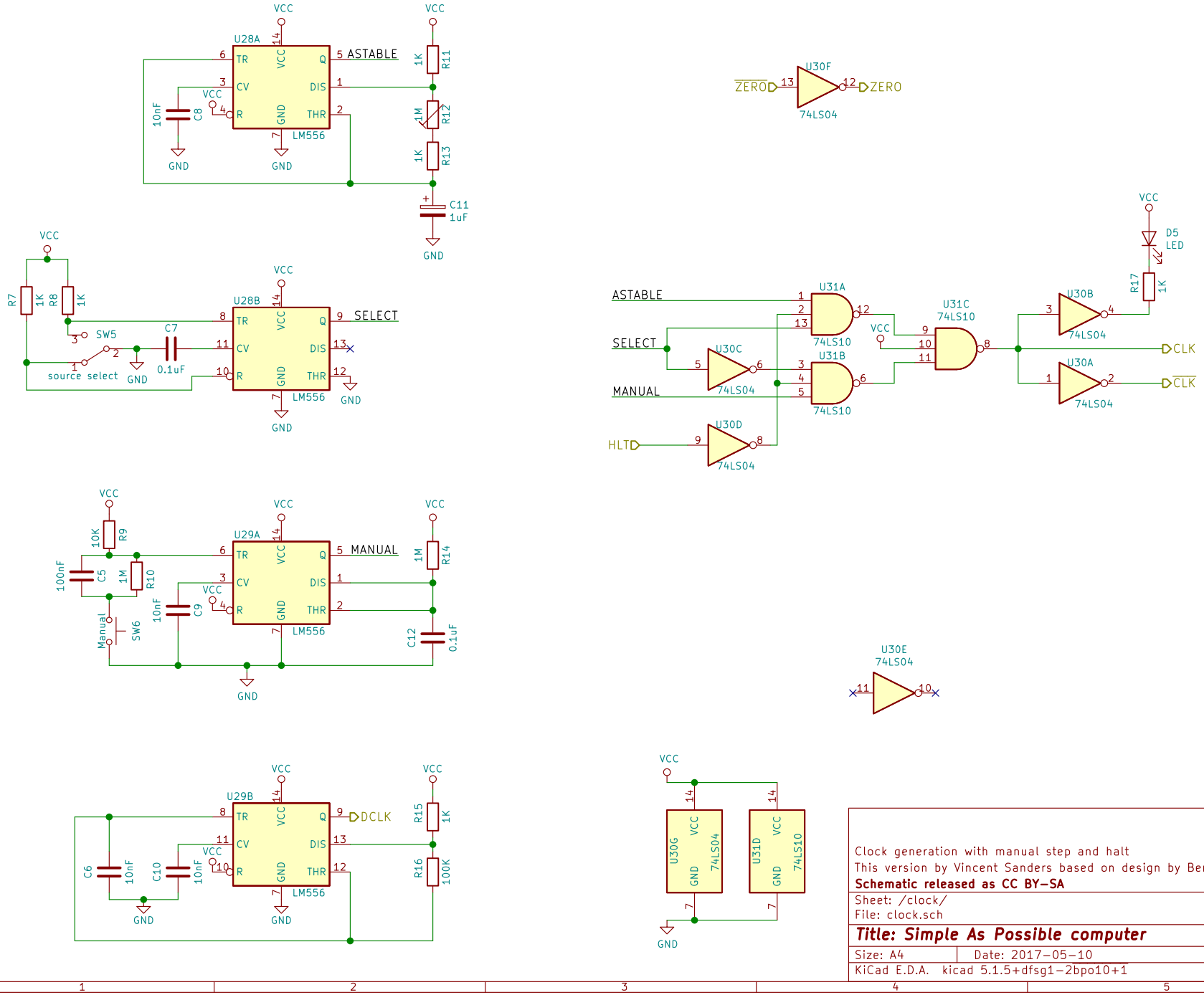


Program counter
This version by Vincent Sanders based on design by Ben Eater
Schematic released as CC BY-SA

Sheet: /PC/
File: programcounter.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 9/13

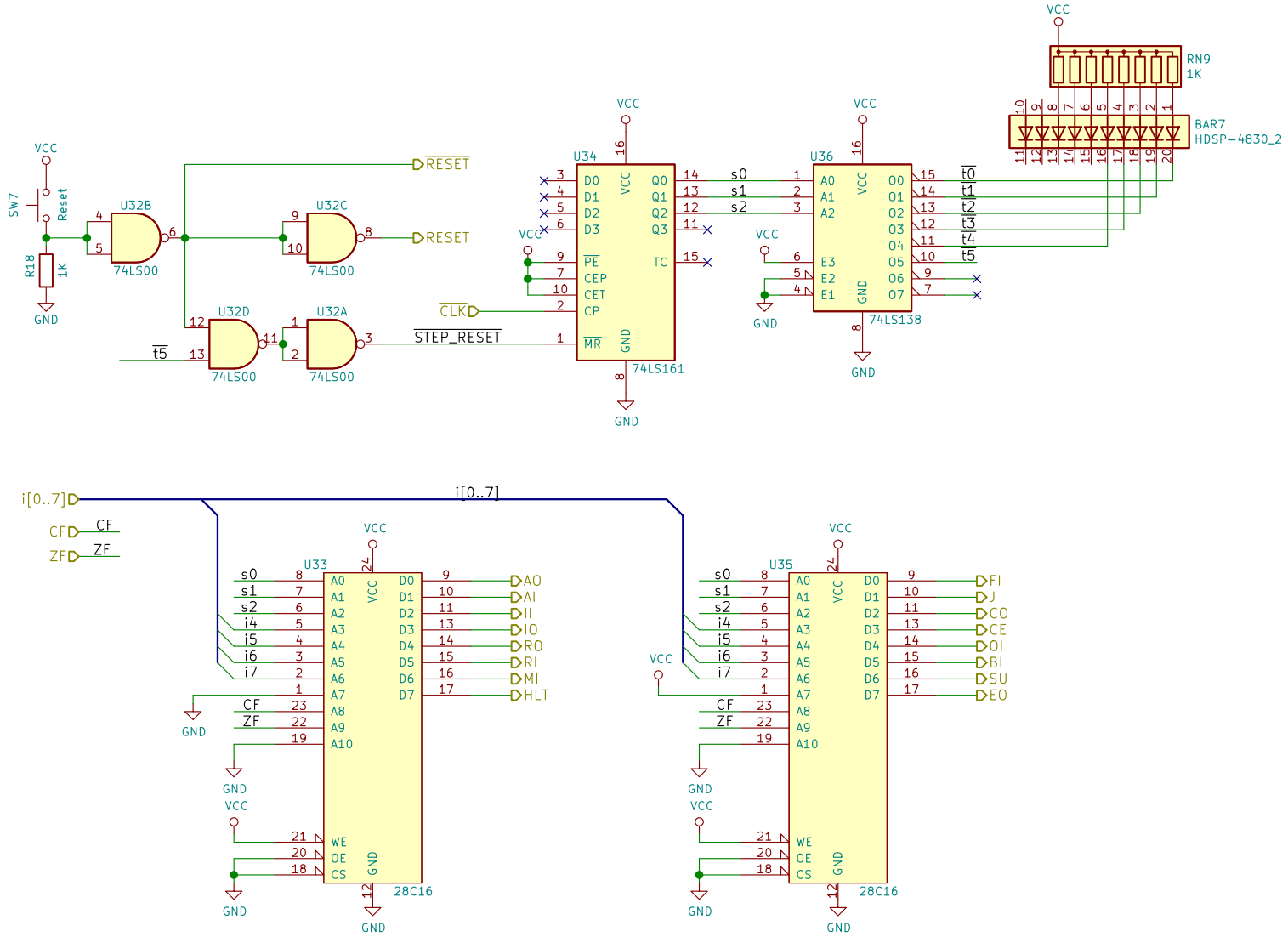


Clock generation with manual step and halt
This version by Vincent Sanders based on design by Ben Eater
Schematic released as CC BY-SA

Sheet: /clock/
File: clock.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 10/13

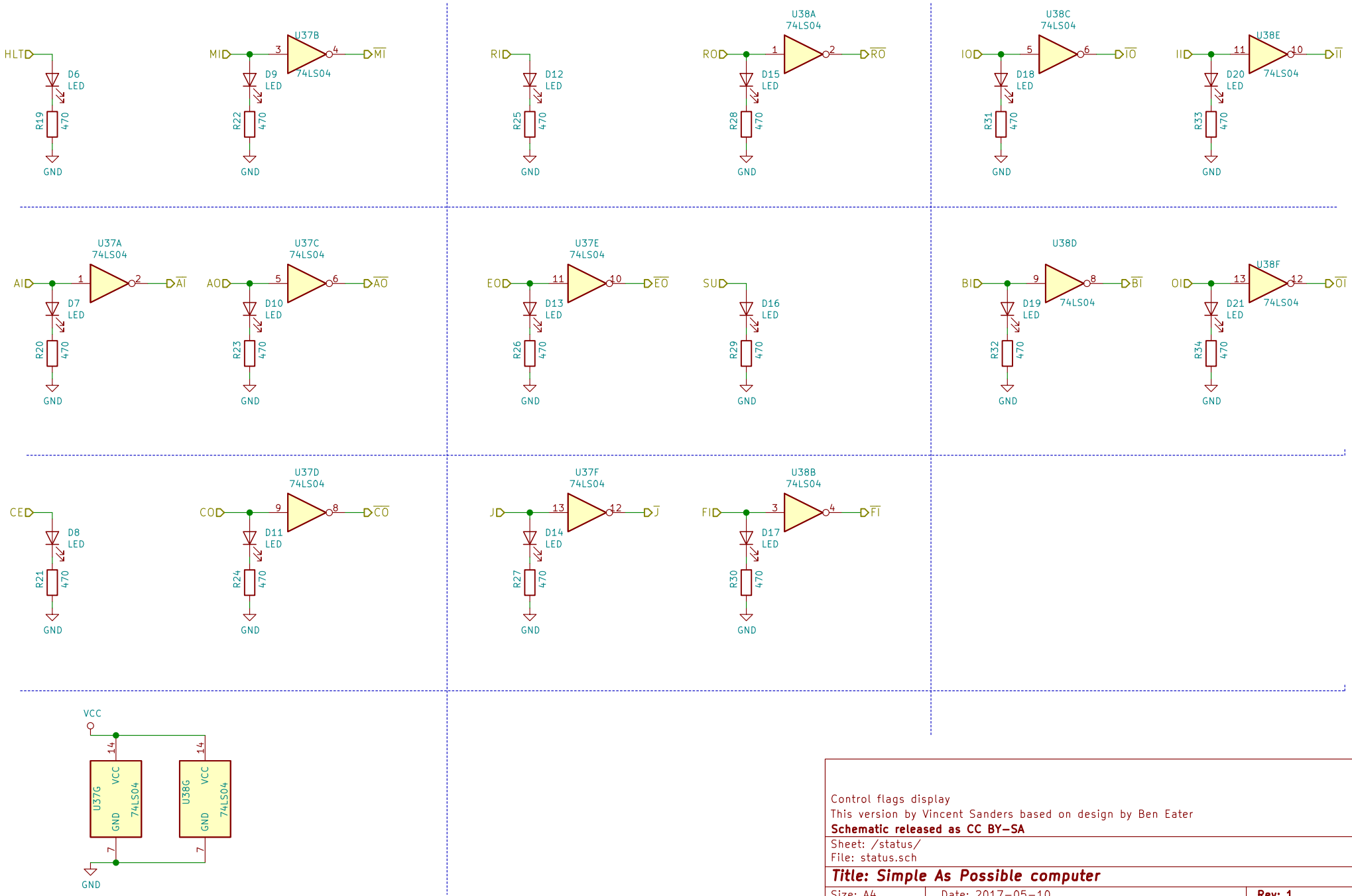


Control
This version by Vincent Sanders based on design by Ben Eater
Schematic released as CC BY-SA

Sheet: /control/
File: control.sch

Title: Simple As Possible (SAP) computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 11/13



Control flags display

This version by Vincent Sanders based on design by Ben Eater

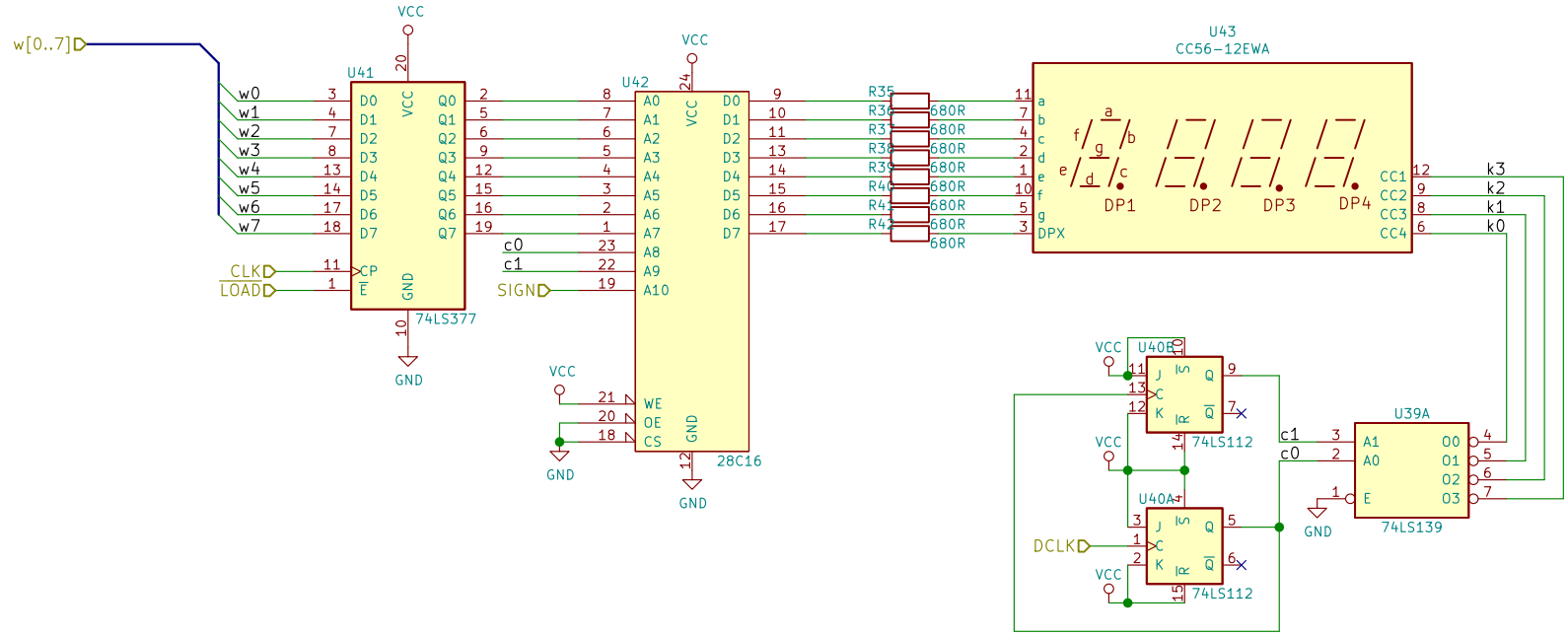
Schematic released as CC BY-SA

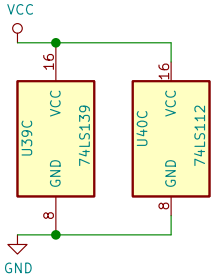
Sheet: /status/

File: status.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 12/13





7 segment output register
This version by Vincent Sanders based on design by Ben Eater
Schematic released as CC BY-SA

Sheet: /output/
File: output.sch

Title: Simple As Possible computer

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 13/13