Introduction to Digital Logic Design Lab
EECS 31L

Lab 2

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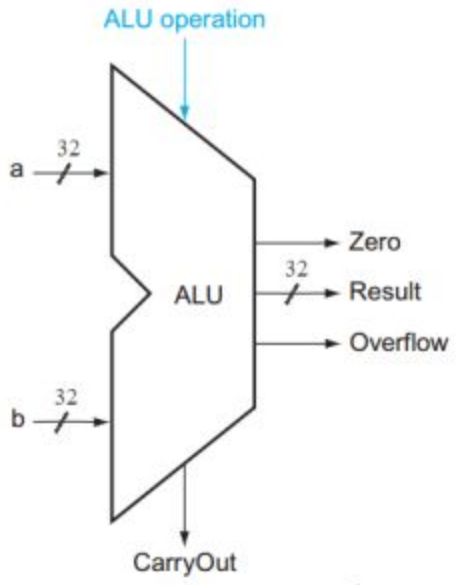
1 - Objective

The objective of this lab was to design a 32-Bit Arithmetic Logic Unit (ALU). The ALU consists of 3 inputs; 2 32-Bit inputs A and B and a 4-bit select input (ALU_Sel) designated to different ALU operations. Also consisting of 4 outputs; The main output, a Zero output, Overflow, and CarryOut.

Below is the diagram as described before.

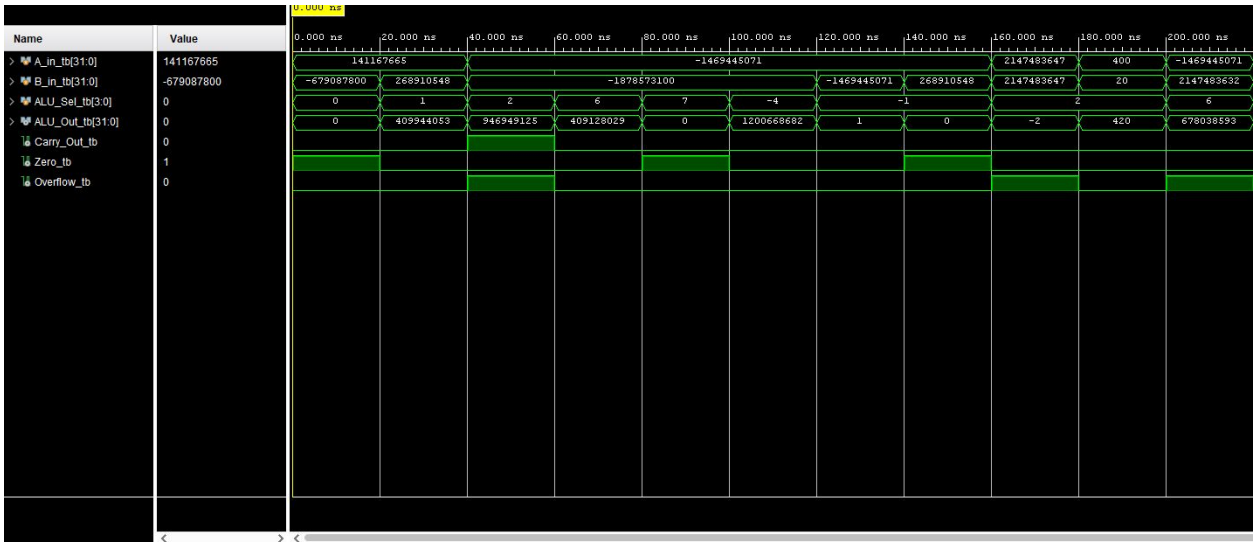


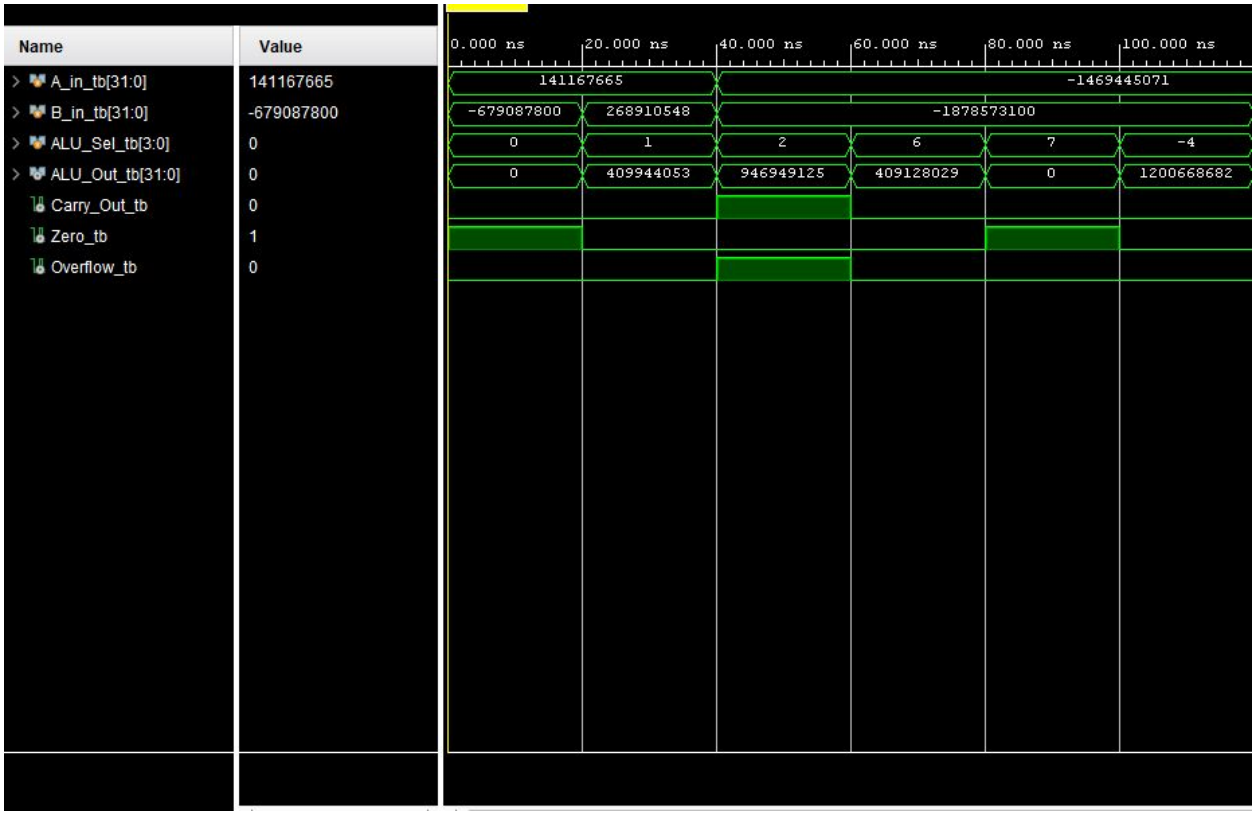
2 - Procedure

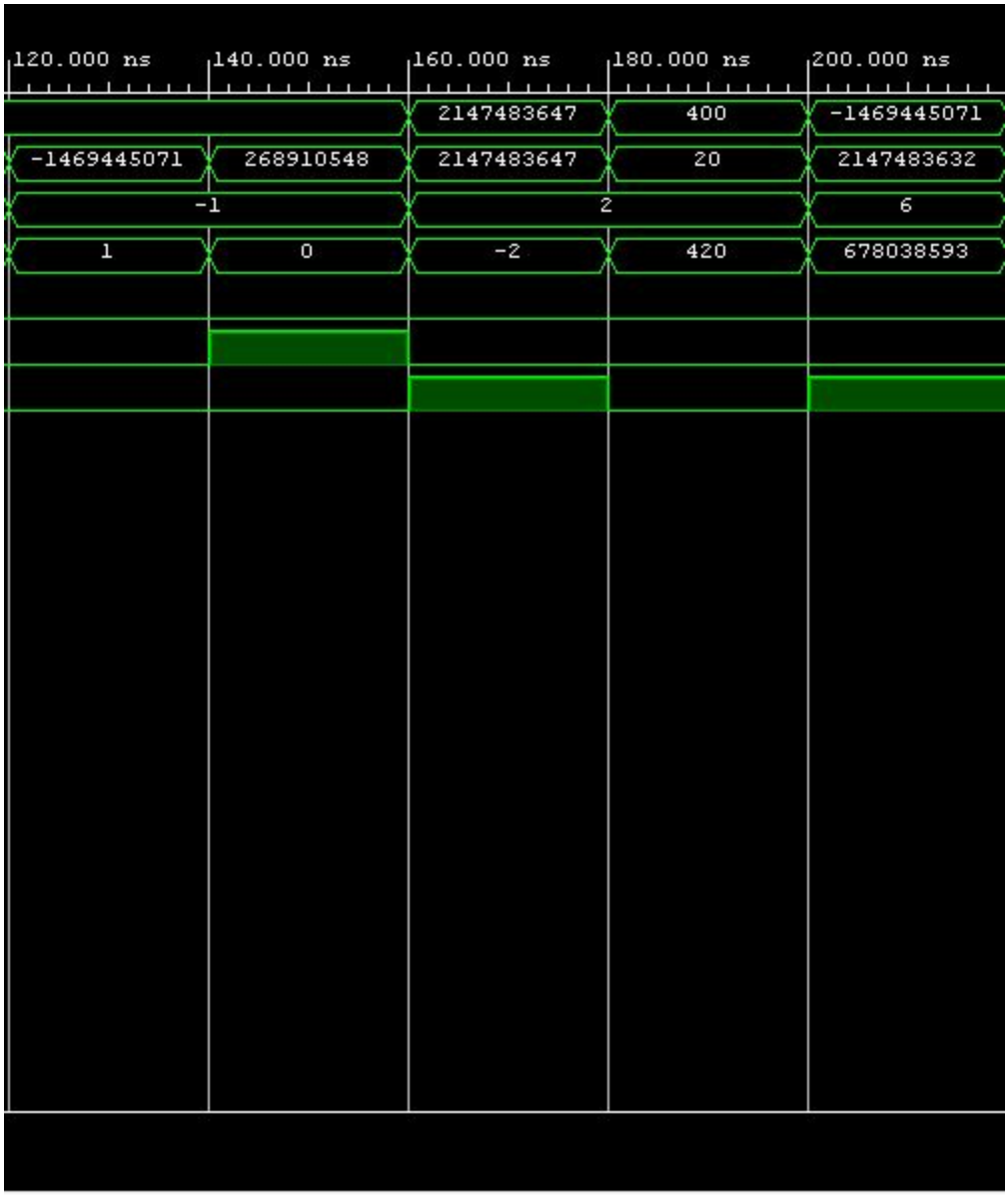
The ALU has 7 different operations; Bitwise AND, Bitwise OR, Addition, Subtraction, Set Less Than, Bitwise NOR, and Equal Comparison. The simplest and most consolidated approach was to use sequential statements. The statements reside inside an always block that would be sensitive to the select input. Inside the always block would have a case block that would have behaviour corresponding to the operation. Depending on the operation, the result would be based on either an arithmetic operation or relational operation.

3 - Simulation Results

All results came as expected, no other operation should have had a CarryOut besides the Add operation. The Zero output reflects all results (ALU_Out) that are zero. The first eight test cases are the ones provided by the lab manual. I verified the add and sub operations by running the inputs through a hexadecimal calculator. A hexadecimal calculator was also used to verify the results for Zero and Overflow. All other operations logically made sense. Additional test cases were added just to verify that the Overflow for Add and Sub operations were working correctly. These test cases were labelled inside the test bench file as //Test420 and //TestSubOverflow and //TestAddOverflow.


Name
Value
A_in_tb[31:0]
141167665
B_in_tb[31:0]
-679087800
ALU_Sel_tb[3:0]
0
ALU_Out_tb[31:0]
0
Carry_Out_tb
0
Zero_tb
1
Overflow_tb
0
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
120.000 ns
140.000 ns
160.000 ns
180.000 ns
200.000 ns
141167665
-1469445071
2147483647
400
-1469445071
-679087800
268910548
-1878573100
-1469445071
268910548
2147483647
20
2147483632
0
1
2
6
7
-4
-1
2
6
0
409944053
946949125
409128029
0
1200668682
1
0
-2
420
678038593


Name
Value
A_in_tb[31:0]
141167665
B_in_tb[31:0]
-679087800
ALU_Sel_tb[3:0]
0
ALU_Out_tb[31:0]
0
Carry_Out_tb
0
Zero_tb
1
Overflow_tb
0
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
141167665
-1469445071
-679087800
268910548
-1878573100
0
1
2
6
7
-4
0
409944053
946949125
409128029
0
1200668682


120.000 ns
140.000 ns
160.000 ns
180.000 ns
200.000 ns
2147483647
400
-1469445071
-1469445071
268910548
2147483647
20
2147483632
-1
2
6
1
0
-2
420
678038593