Introduction to Digital Logic Design Lab
EECS 31L

Lab 1

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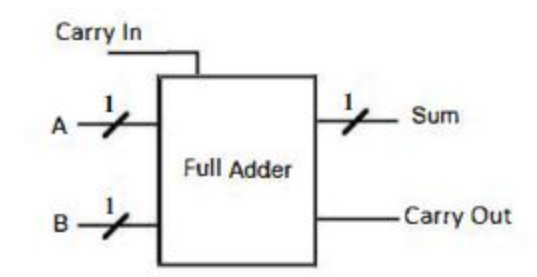
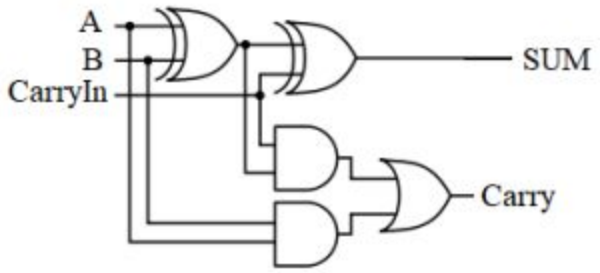
1 - Objective

In this lab, we are meant to design basic logic blocks within Verilog. We had designed 5 basic blocks: Half Adder, 1-bit Full Adder, 4-bit Full Adder, 2 to 1 Multiplexer, and 4 to 1 Multiplexer. The Half Adder had already been provided from the lab instructions, so that block diagram will be omitted from this lab report.
Detailed descriptions of each block will be found below.

1.1 - 1-bit Full Adder

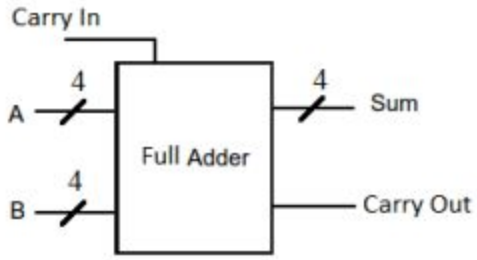
Below is the diagram for the 1-bit Full Adder. Adds 2 inputs and produces the sum and carry out.





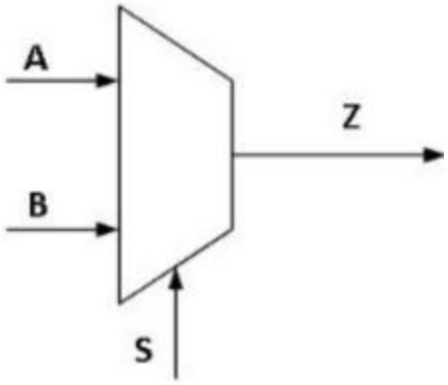
1.2 - 4-bit Full Adder

Block diagram for 4-bit Full Adder. Adds 2 4-bit inputs and produces the sum and carry out.



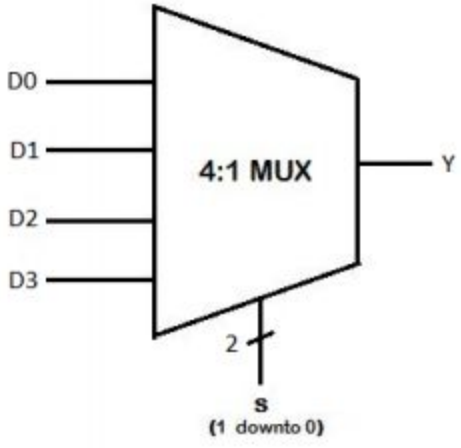
1.3 - 2 to 1 Multiplexer

Block diagram for 2:1 Multiplexer. Produces output based on 2 different inputs that the select input will choose from.



1.4 - 4 to 1 Multiplexer

Block diagram for 4:1 Multiplexer. Produces output based on 4 different inputs that the select input will choose from.



2 - Procedure

For both Adder blocks, their respective truth tables were utilized to derive the boolean equation used to describe the behaviour of the block.

As for the multiplexers, the output was produced by assigning inputs to logical operators.

2.1 - 1-bit Full Adder and 4-bit Full Adder

Both designs were derived from the same truth table since they have the same exact behaviour. The 4-bit Full Adder is just made up of 4 connected 1-bit Full Adders.

Full Adder –Truth Table				
Input			Output	
A	B	Carry in	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

2.3 - 2 to 1 Multiplexer

The Y output would be produced by choosing the input that passes through based on the value of the select input. The multiplexer works similar to an analog dial.

The equation for a 2 to 1 multiplexer is

Y = S ? A : B

2.4 - 4 to 1 Multiplexer

Similar to the 2 to 1 multiplexer where output is produced by choosing from 4 different inputs based on the select input.

The equation for a 4 to 1 multiplexer is

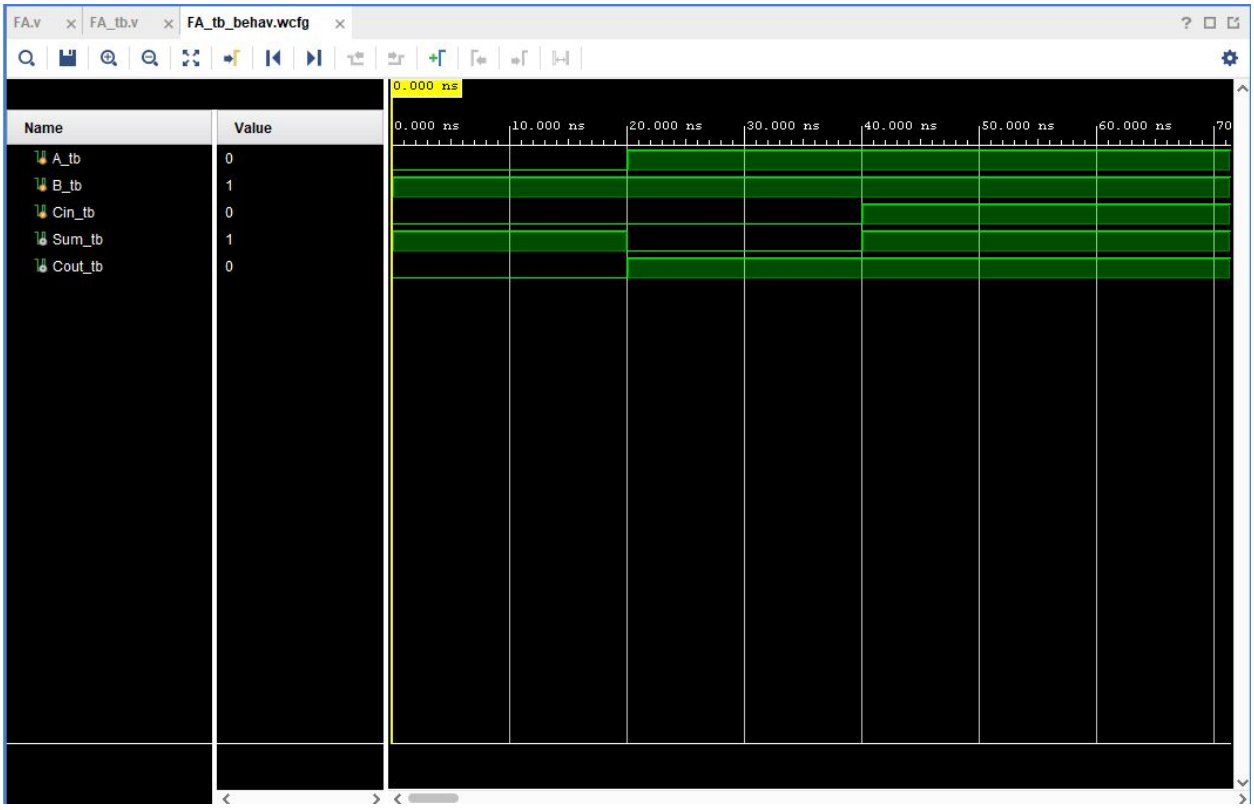
Y = (S == 2'b00) ? D1: (S == 2'b01) ? D2: (S == 2'b10) ? D3: D4

3 - Simulation Results

All results were as expected. Both the 1-bit Full Adder and 4-bit Full Adder produced the expected sum and carry out. After 20ns for each block, a new test case is run and will therefore produce a different output. Each block tests several cases and appears to work as expected. The multiplexers contains a test case for each possible select input.

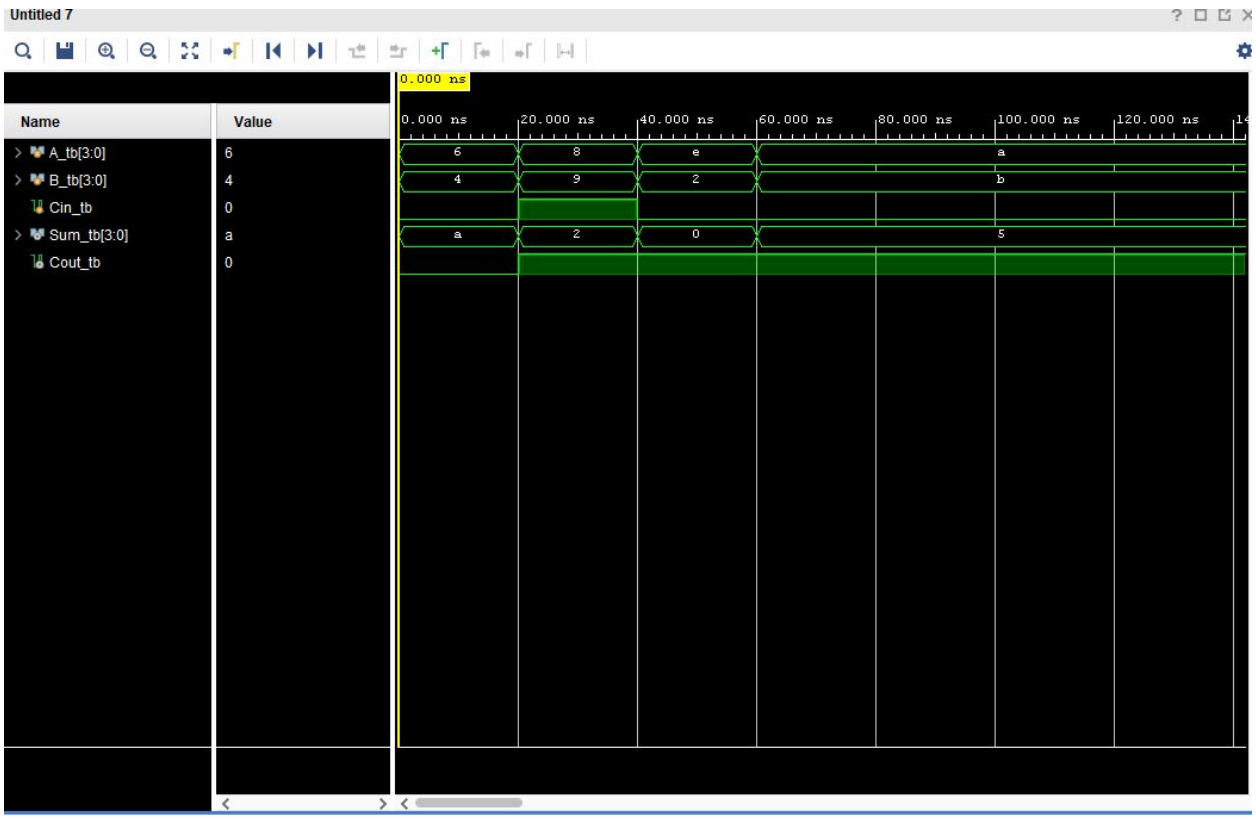
3.1 - 1-bit Full Adder

Signals A, B, Cin are input signals. Signals Sum and Cout are output signals.



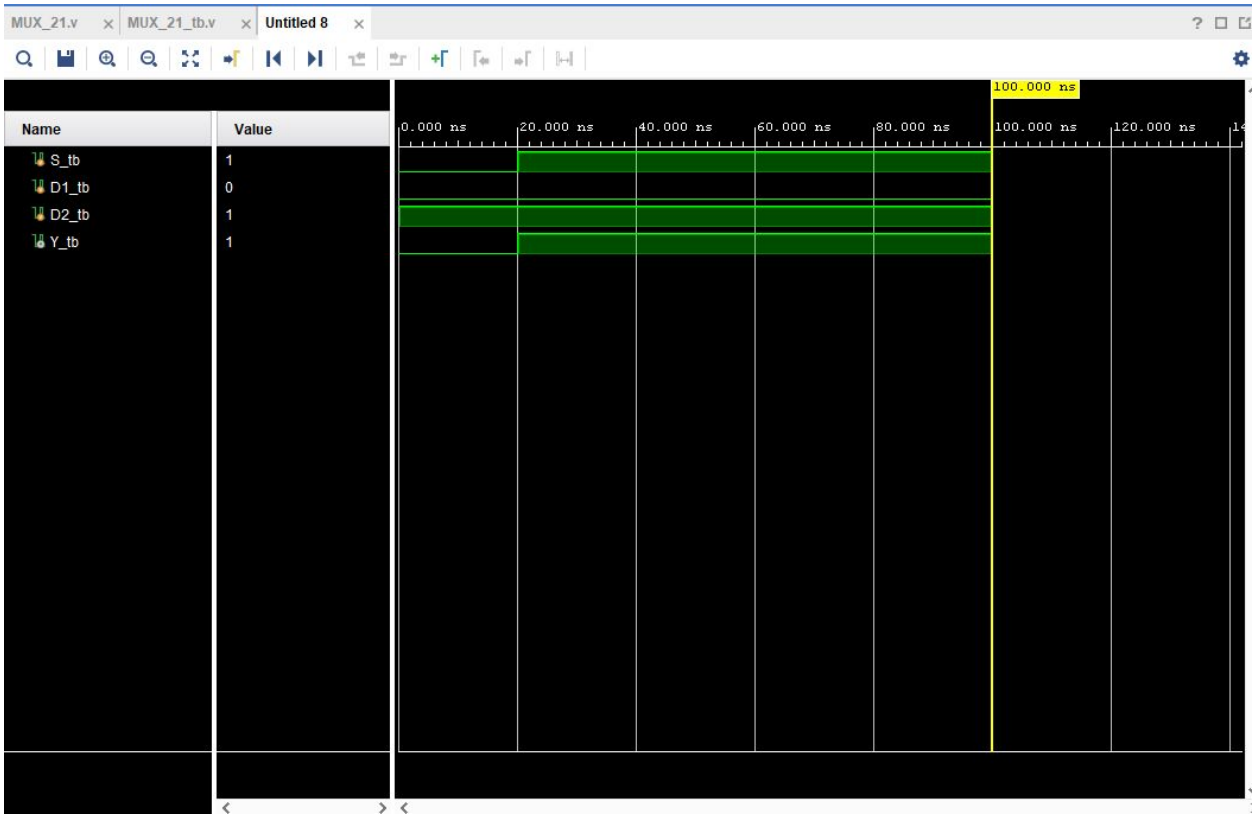
3.2 - 4-bit Full Adder

Signals A and B are 4-bit inputs. Signal Cin is a 1-bit input. Signals Sum and Cout are 4-bit output signals.



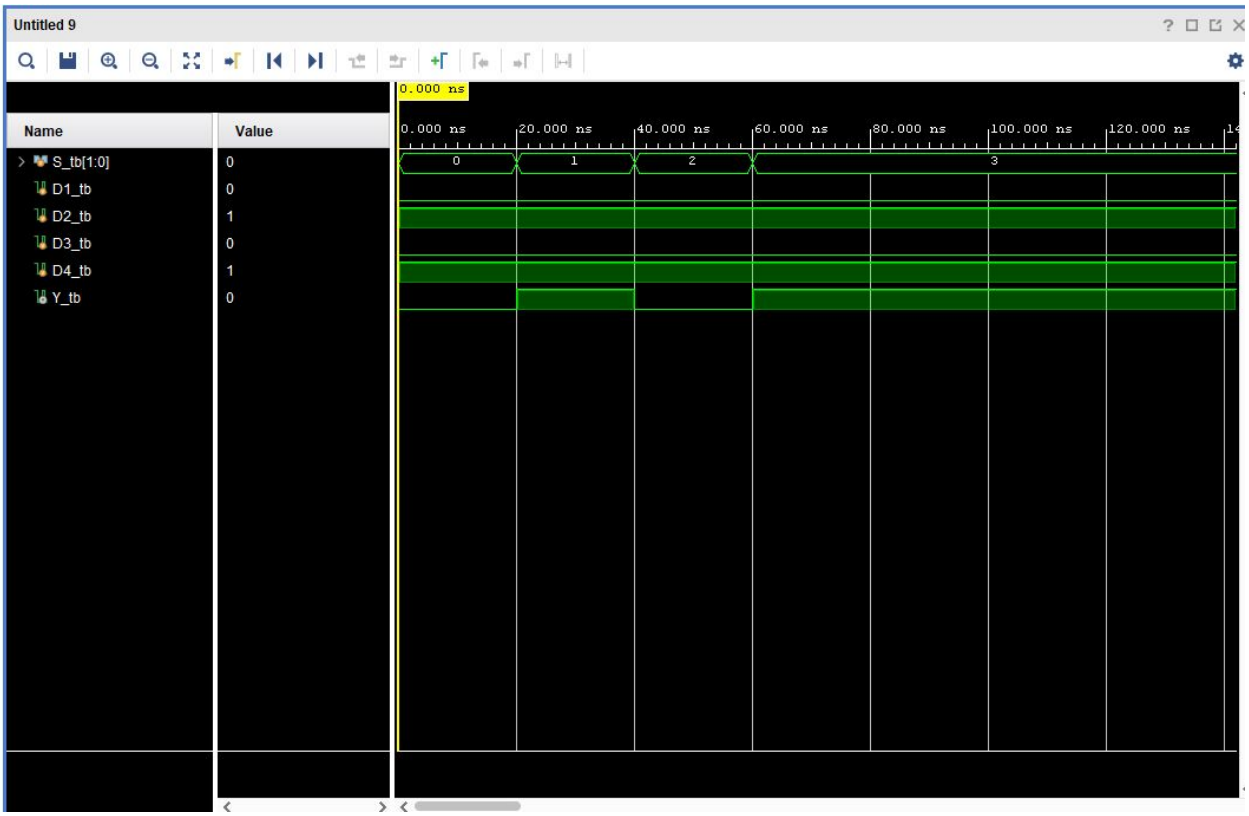
3.3 - 2 to 1 Multiplexer

Singal S is the select input. D1 and D2 are inputs. Signal Y is the output signal



3.4 - 4 to 1 Multiplexer

Signal S is the select signal. Signals D1-D4 are input signals. Signal Y is the output signal.


Untitled 9
Name
Value
S_tb[1:0]
D1_tb
D2_tb
D3_tb
D4_tb
Y_tb
0
0
1
0
1
0
0.000 ns
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
120.000 ns
0
1
2
3