SHRIKANT BHISE

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Seeking for a challenging role wherein my technical Skills and Knowledge can be improved along with organizational objectives.

TECHNICAL SKILLS

IP Characterization **|** Static Timing Analysis **|** Standard cell Characterization | Digital Electronics **|** TCL Scripting **|** Verilog | Debugging **|**

◆ EDA Tools

Primetime | Tempus **|** Liberate **|** Calibre **|** Xcelium **|** Crossfire **|** Virtuoso | Spectre

WORK EXPERIENCE

Lead Product Engineer | **Cadence Design System (Korea Branch)** Sep,2021 – Present

- Enabling tempus STA flow for Samsung IP's.
- Deployment of DSTA (Distributed STA) for Samsung IP's
- Performs validation (glitch and delay) on testcases to evaluate impact of methodology update using Tempus and Spectre.
- Library Characterization on 3/5 nm Samsung IP's (timing, power, constraints, leakage, and noise).
- Monte-Carlo simulations for LVF modeling of Standard cells.
- Understanding of Characterization methodology of timing, power, leakage.
- Supporting customer for their queries related to STF.
- Worked on deployment of scripts for Samsung liberty files.
- Understanding of NLDM, CCS liberty files and concept of Crosstalk Noise.

Senior Design Engineer | **ST Microelectronics** Jun,2019 – Aug,2021

- Design Engineer - ST Microelectronics (May 2019 – Apr 2021)
- Proficient in Arc identification methodology and digital characterization of complex AMS IP's like USB2OTG, SGM-PHY using internal tool (wrapper on Primetime).
- Knowledge of OCV and POCV analysis.
- Skilled in successful deployment of LVF modelling in ST liberty files and POCV analysis using Primetime.
- Experienced in basic Static Timing Analysis (STA) flow execution using Primetime.
- Worked on complex digital characterization including multiple generated clocks.
- Detail Understanding of inhouse tool for Noise and Timing characterization, based on Prime-Time and presented their algorithms in team successfully.
- Modification in existing methodology of in-house tool for identification and characterization of timing arcs.
- Generation and delivery of different CAD views to customer.
- Familiar with basic Prime-Time commands used for characterization methodology.

Intern | **ST Microelectronics** May,2018 – May,2019

- Proficient in Deployment of internal clock characterization tool and its new version.
- Performed changes in methodology of extraction of Min Pulse Width (MPW) arcs and LVF modelling.

PRESENTATIONS AND APPEARANCES

A step towards Accurate Timing Analysis

TechWeek 2019 – ST conference

- Enabling aging .lib support for AMS IP's. (y and 2y)
- Designing methodology in internal tool of digital characterization to support accurate values in STF files.
- Suggested an efficient methodology (using min and max_library) for calculation of constraint values for IP's using aging (y and 2y) STF files.

PROJECTS

Provided solution for large constraint and MPW values in liberty.

- Analysis of existing methodology for finding values of constraint and MPW values.
- Observation of waveforms related to nodes in spectre causing problem, and evaluation. Based on this workaround is provided to the customer.

Validation of tool with different customer cases.

- After addition of different new feature thorough validation of tool with different validation of cases.
- New features are depending upon technology changes.

Projects on tool enhancement.

- Different projects related to tool enhancement based on change in cell structure, large data files, ccb selection are analyzed and provided solution to customer.

Methodology for managing accurate digital Characterization of AMS blocks.

- Designing methodology in internal tool of digital characterization to support accurate values in STF files.
- Suggested an efficient methodology for calculation of constraint values for IP's using aging STF files using min and max library concept within in-house tool (which is based on Primetime).

Methodology for managing negative MPW in digital Characterization.

- Performed Analysis for negative MPW being calculated when there is large difference in rise and fall path delay.
- Proposed a solution based on analysis.

Academic Qualifications:

EXAM	BOARD/UNIVERSITY	PERCENTAGE/CGPA
MTech	MIT, Manipal	8.5
B.E.	University of Pune	67.76%
H.S.C	Maharashtra Board	84.5%
S.S.C	Maharashtra Board	90.69%

ACHIVEMENTS

- Runner-Up in Intercollege Paper Presentation Competition.
- Book Award Central Government Scholarship holder in School.
- MTS Prize winner in School.
- Poster and Paper Presentation in ST Microelectronics on new developed idea for in house tool.

PERSONAL DOSSIER

Father name – Sarangdhar Bhise

Date of Birth – 12th Jan 1992

Current Location – Gyeonggi-do, South Korea - 16710

Language Known – English, Hindi, and Marathi

I hereby declare that the above information provided by me is true and have all the relevant documents to authenticate thesame.

SHRIKANT BHISE