P2597-C02

Jetson TX1/TX2 Developer Kit Carrier Board
Supports Jetson TX1/TX2/TX2i

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P2597 I2C Port Assignments

Slave Device	BUS:Device address
INA3221 (Power measurement)	I2C Gen 2 : 7'h42
INA3221 (Power measurement)	I2C Gen 2 : 7'h43
TCA9539 (GPIO Expander)	I2C Gen 2 : 7'h74
TCA9539 (GPIO Expander)	I2C Gen 2 : 7'h77
BOARDID EEPROM	I2C Gen 3 : 7'57h

P2180 I2C Port Assignments

Slave Device	BUS:Device address
TMP451 (Thermal)	I2C Gen 1 : 7'h4C
ADS1015 (ACA detection)	I2C Gen 2 : 7'h4A
INA226 (Power measurement)	I2C Gen 2 : 7'h46
INA3221 (Power measurement)	I2C Gen 2 : 7'h40

ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
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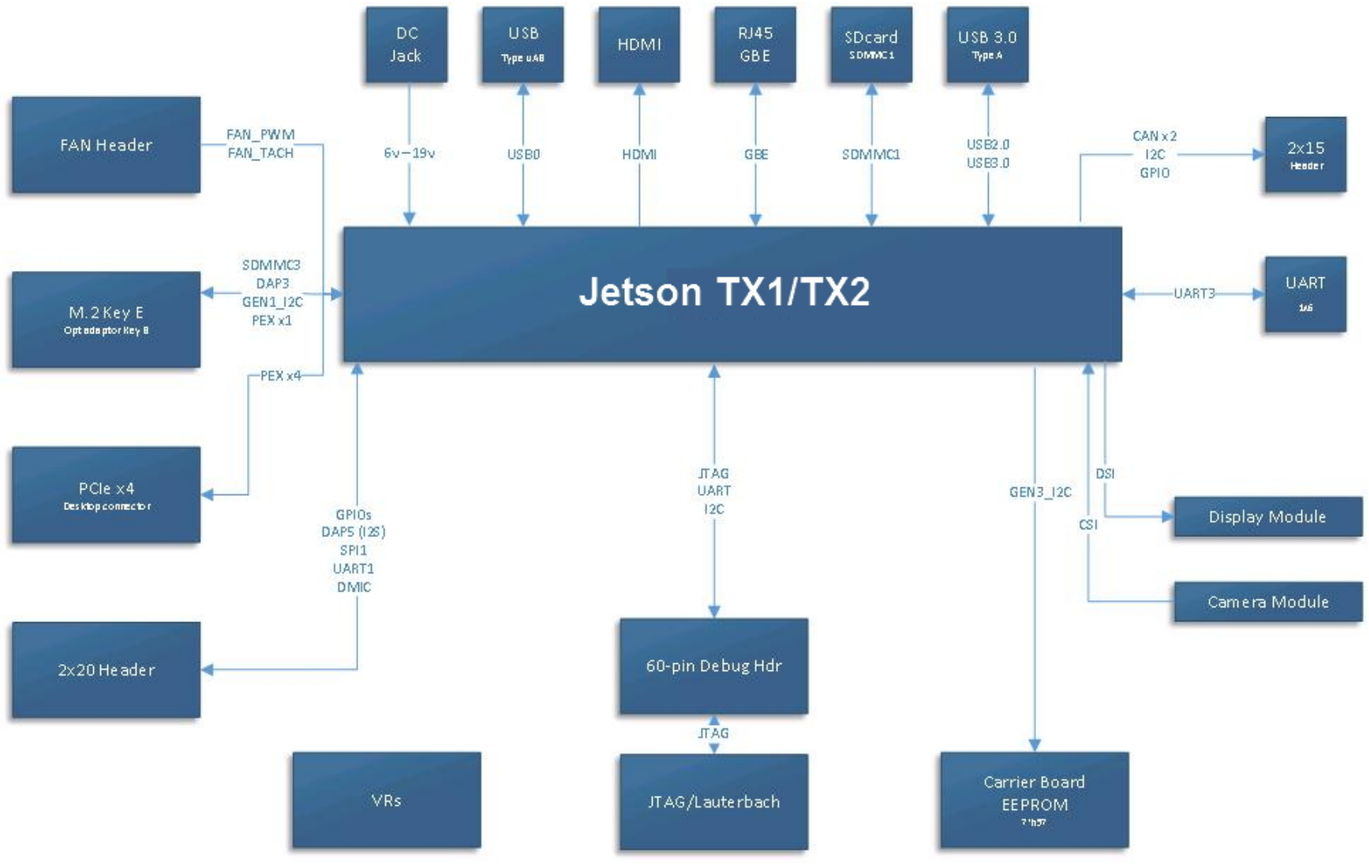

ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	Block Diagram

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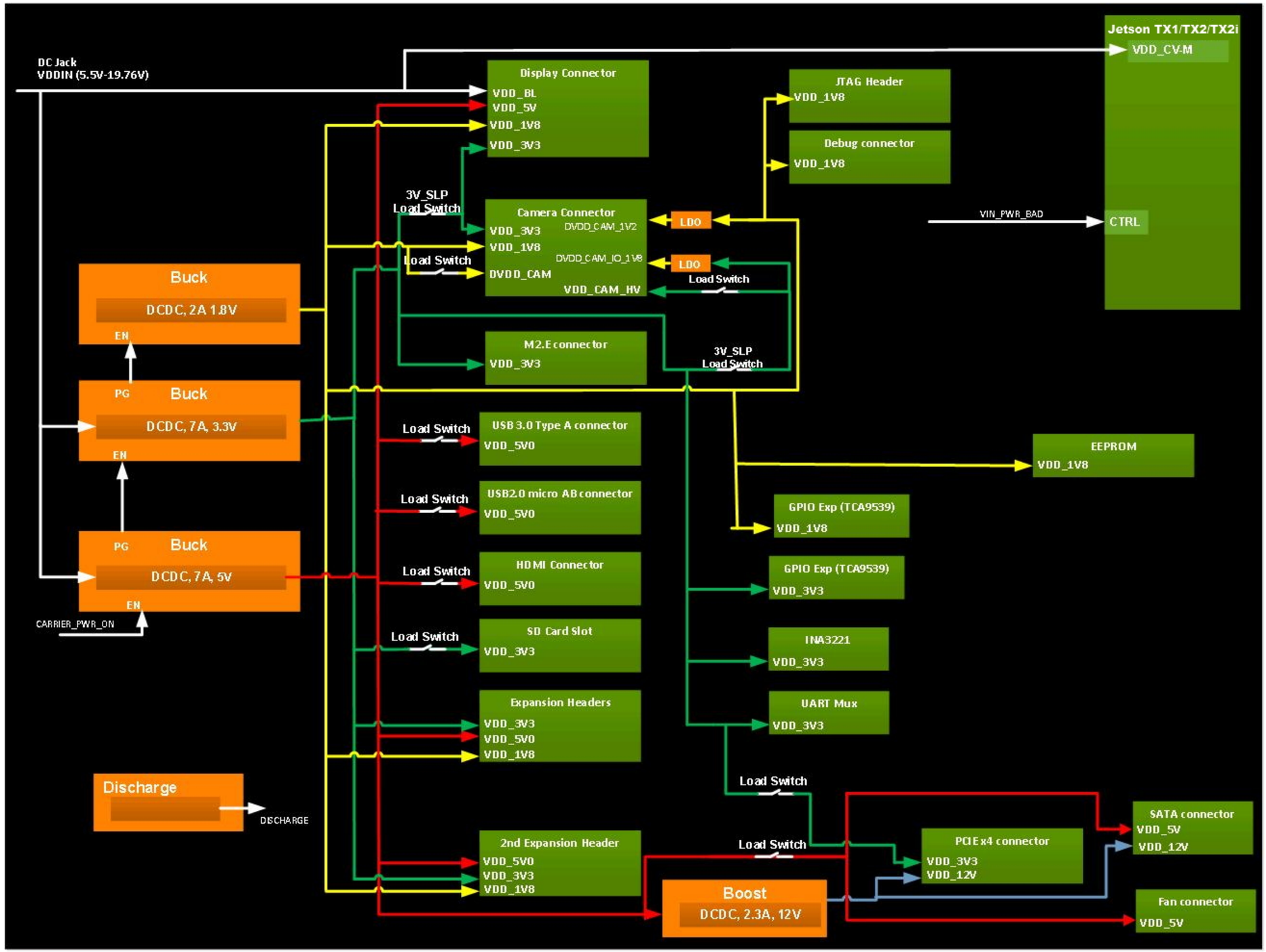
Power Tree



ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	Power Tree

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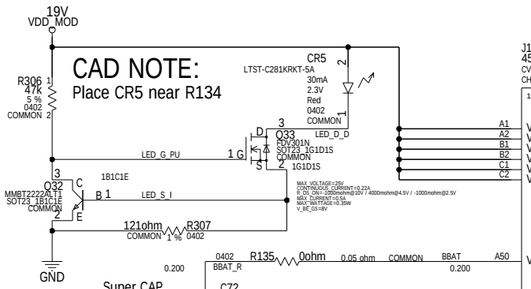
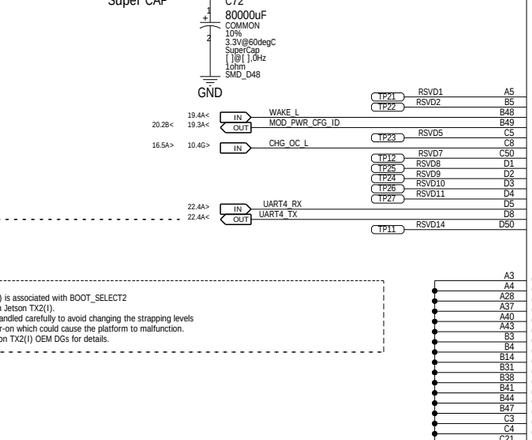
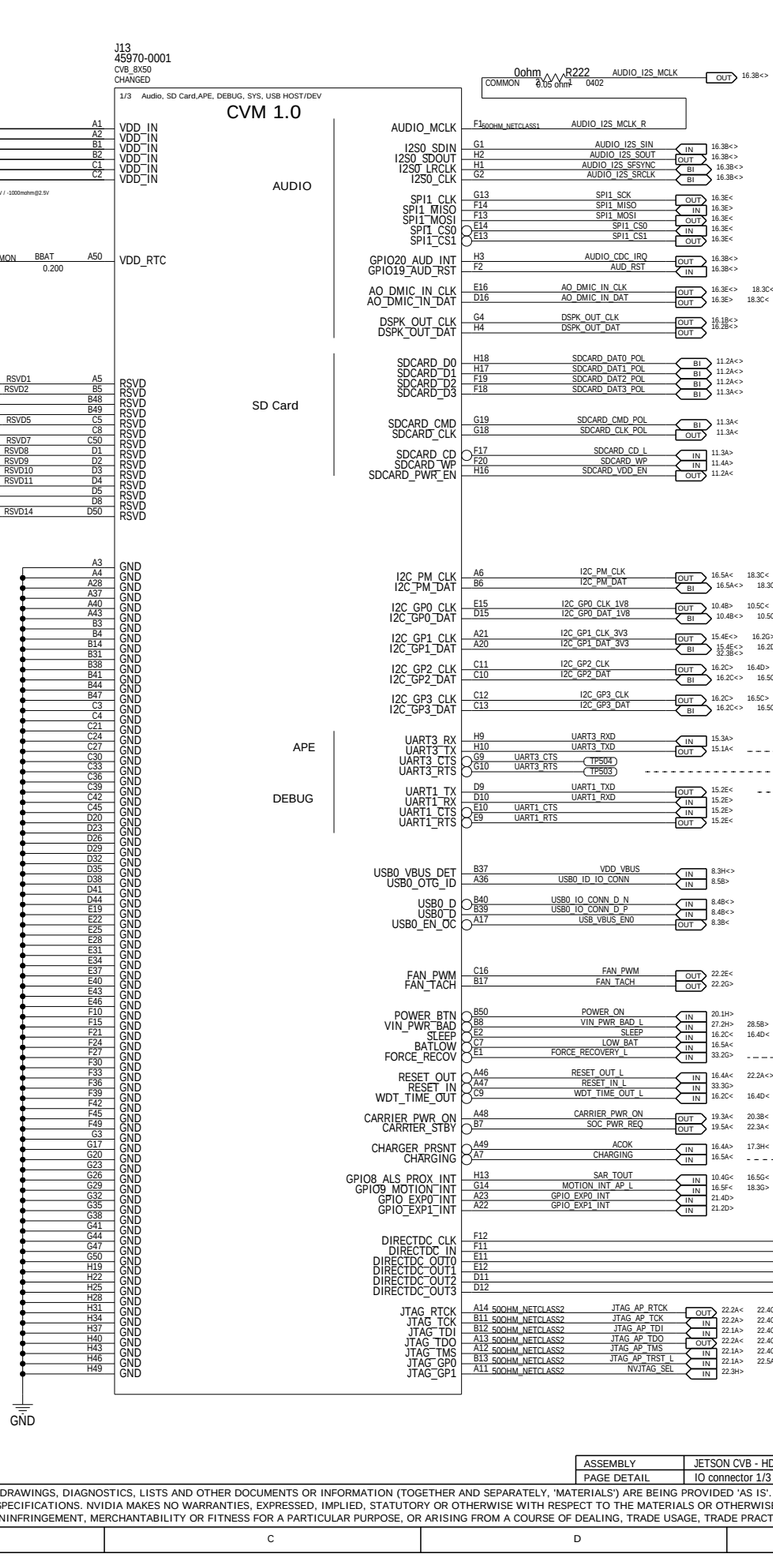
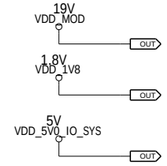
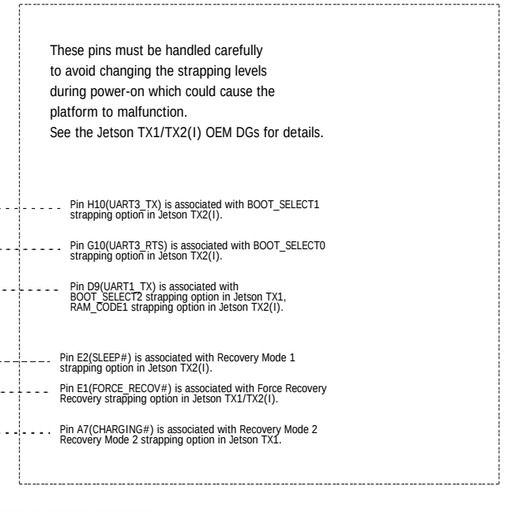


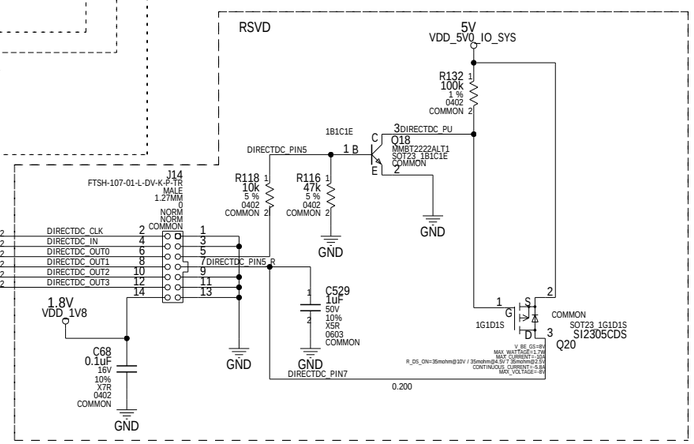








Pin D8(UART4_TX) is associated with BOOT_SELECT2 strapping option in Jetson TX2(I).
It must be handled carefully to avoid changing the strapping levels during power-on which could cause the platform to malfunction.
See the Jetson TX2(I) OEM DGs for details.



ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
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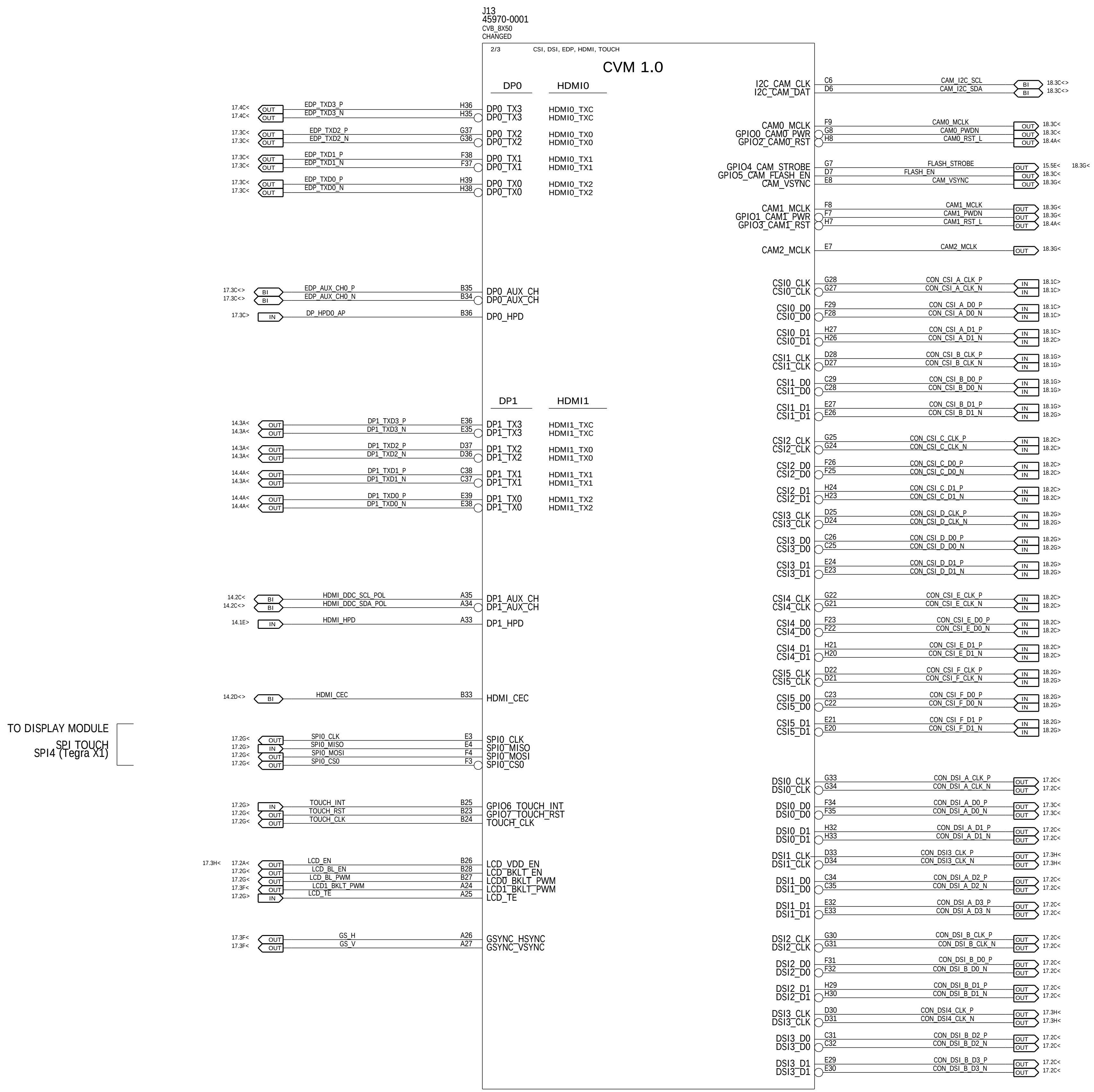
J13
45970-0001
CVB_8X50
CHANGED
2/3
CSI, DSI, EDP, HDMI, TOUCH
CVM 1.0
DP0
HDMI0
17.4C< OUT EDP_TXD3_P H36 DP0_TX3 HDMI0_TXC
17.4C< OUT EDP_TXD3_N H35 DP0_TX3 HDMI0_TXC
17.3C< OUT EDP_TXD2_P G37 DP0_TX2 HDMI0_TX0
17.3C< OUT EDP_TXD2_N G36 DP0_TX2 HDMI0_TX0
17.3C< OUT EDP_TXD1_P F38 DP0_TX1 HDMI0_TX1
17.3C< OUT EDP_TXD1_N F37 DP0_TX1 HDMI0_TX1
17.3C< OUT EDP_TXD0_P H39 DP0_TX0 HDMI0_TX2
17.3C< OUT EDP_TXD0_N H38 DP0_TX0 HDMI0_TX2
17.3C<> BI EDP_AUX_CH0_P B35 DP0_AUX_CH
17.3C<> BI EDP_AUX_CH0_N B34 DP0_AUX_CH
17.3C> IN DP_HPD0_AP B36 DP0_HPD
DP1
HDMI1
14.3A< OUT DP1_TXD3_P E36 DP1_TX3 HDMI1_TXC
14.3A< OUT DP1_TXD3_N E35 DP1_TX3 HDMI1_TXC
14.3A< OUT DP1_TXD2_P D37 DP1_TX2 HDMI1_TX0
14.3A< OUT DP1_TXD2_N D36 DP1_TX2 HDMI1_TX0
14.4A< OUT DP1_TXD1_P C38 DP1_TX1 HDMI1_TX1
14.3A< OUT DP1_TXD1_N C37 DP1_TX1 HDMI1_TX1
14.4A< OUT DP1_TXD0_P E39 DP1_TX0 HDMI1_TX2
14.4A< OUT DP1_TXD0_N E38 DP1_TX0 HDMI1_TX2
14.2C< BI HDMI_DDC_SCL_POL A35 DP1_AUX_CH
14.2C<> BI HDMI_DDC_SDA_POL A34 DP1_AUX_CH
14.1E> IN HDMI_HPD A33 DP1_HPD
14.2D<> BI HDMI_CEC B33 HDMI_CEC
TO DISPLAY MODULE
SPI TOUCH
SPI4 (Tegra X1)
17.2G< OUT SPI0_CLK E3 SPI0_CLK
17.2G> IN SPI0_MISO E4 SPI0_MISO
17.2G< OUT SPI0_MOSI F4 SPI0_MOSI
17.2G< OUT SPI0_CS0 F3 SPI0_CS0
17.2G> IN TOUCH_INT B25 GPIO6_TOUCH_INT
17.2G< OUT TOUCH_RST B23 GPIO7_TOUCH_RST
17.2G< OUT TOUCH_CLK B24 TOUCH_CLK
17.3H< 17.2A< OUT LCD_EN B26 LCD_VDD_EN
17.2G< OUT LCD_BL_EN B28 LCD_BKLT_EN
17.2G< OUT LCD_BL_PWM B27 LCD0_BKLT_PWM
17.3F< OUT LCD1_BKLT_PWM A24 LCD1_BKLT_PWM
17.2G> IN LCD_TE A25 LCD_TE
17.3F< OUT GS_H A26 GSYNC_HSYNC
17.3F< OUT GS_V A27 GSYNC_VSYNC
I2C_CAM_CLK C6 CAM_I2C_SCL BI 18.3C<>
I2C_CAM_DAT D6 CAM_I2C_SDA BI 18.3C<>
CAM0_MCLK F9 CAM0_MCLK OUT 18.3C<
GPIO0_CAM0_PWR G8 CAM0_PWDN OUT 18.3C<
GPIO2_CAM0_RST H8 CAM0_RST_L OUT 18.4A<
GPIO4_CAM_STROBE G7 FLASH_STROBE OUT 15.5E< 18.3G<
GPIO5_CAM_FLASH_EN D7 FLASH_EN OUT 18.3C<
CAM_VSYNC E8 CAM_VSYNC OUT 18.3G<
CAM1_MCLK F8 CAM1_MCLK OUT 18.3G<
GPIO1_CAM1_PWR F7 CAM1_PWDN OUT 18.3G<
GPIO3_CAM1_RST H7 CAM1_RST_L OUT 18.4A<
CAM2_MCLK E7 CAM2_MCLK OUT 18.3G<
CSI0_CLK G28 CON_CSI_A_CLK_P IN 18.1C>
CSI0_CLK G27 CON_CSI_A_CLK_N IN 18.1C>
CSI0_D0 F29 CON_CSI_A_D0_P IN 18.1C>
CSI0_D0 F28 CON_CSI_A_D0_N IN 18.1C>
CSI0_D1 H27 CON_CSI_A_D1_P IN 18.1C>
CSI0_D1 H26 CON_CSI_A_D1_N IN 18.2C>
CSI1_CLK D28 CON_CSI_B_CLK_P IN 18.1G>
CSI1_CLK D27 CON_CSI_B_CLK_N IN 18.1G>
CSI1_D0 C29 CON_CSI_B_D0_P IN 18.1G>
CSI1_D0 C28 CON_CSI_B_D0_N IN 18.1G>
CSI1_D1 E27 CON_CSI_B_D1_P IN 18.1G>
CSI1_D1 E26 CON_CSI_B_D1_N IN 18.2G>
CSI2_CLK G25 CON_CSI_C_CLK_P IN 18.2C>
CSI2_CLK G24 CON_CSI_C_CLK_N IN 18.2C>
CSI2_D0 F26 CON_CSI_C_D0_P IN 18.2C>
CSI2_D0 F25 CON_CSI_C_D0_N IN 18.2C>
CSI2_D1 H24 CON_CSI_C_D1_P IN 18.2C>
CSI2_D1 H23 CON_CSI_C_D1_N IN 18.2C>
CSI3_CLK D25 CON_CSI_D_CLK_P IN 18.2G>
CSI3_CLK D24 CON_CSI_D_CLK_N IN 18.2G>
CSI3_D0 C26 CON_CSI_D_D0_P IN 18.2G>
CSI3_D0 C25 CON_CSI_D_D0_N IN 18.2G>
CSI3_D1 E24 CON_CSI_D_D1_P IN 18.2G>
CSI3_D1 E23 CON_CSI_D_D1_N IN 18.2G>
CSI4_CLK G22 CON_CSI_E_CLK_P IN 18.2C>
CSI4_CLK G21 CON_CSI_E_CLK_N IN 18.2C>
CSI4_D0 F23 CON_CSI_E_D0_P IN 18.2C>
CSI4_D0 F22 CON_CSI_E_D0_N IN 18.2C>
CSI4_D1 H21 CON_CSI_E_D1_P IN 18.2C>
CSI4_D1 H20 CON_CSI_E_D1_N IN 18.2C>
CSI5_CLK D22 CON_CSI_F_CLK_P IN 18.2G>
CSI5_CLK D21 CON_CSI_F_CLK_N IN 18.2G>
CSI5_D0 C23 CON_CSI_F_D0_P IN 18.2G>
CSI5_D0 C22 CON_CSI_F_D0_N IN 18.2G>
CSI5_D1 E21 CON_CSI_F_D1_P IN 18.2G>
CSI5_D1 E20 CON_CSI_F_D1_N IN 18.2G>
DSI0_CLK G33 CON_DSI_A_CLK_P OUT 17.2C<
DSI0_CLK G34 CON_DSI_A_CLK_N OUT 17.2C<
DSI0_D0 F34 CON_DSI_A_D0_P OUT 17.3C<
DSI0_D0 F35 CON_DSI_A_D0_N OUT 17.3C<
DSI0_D1 H32 CON_DSI_A_D1_P OUT 17.2C<
DSI0_D1 H33 CON_DSI_A_D1_N OUT 17.2C<
DSI1_CLK D33 CON_DSI3_CLK_P OUT 17.3H<
DSI1_CLK D34 CON_DSI3_CLK_N OUT 17.3H<
DSI1_D0 C34 CON_DSI_A_D2_P OUT 17.2C<
DSI1_D0 C35 CON_DSI_A_D2_N OUT 17.2C<
DSI1_D1 E32 CON_DSI_A_D3_P OUT 17.2C<
DSI1_D1 E33 CON_DSI_A_D3_N OUT 17.2C<
DSI2_CLK G30 CON_DSI_B_CLK_P OUT 17.2C<
DSI2_CLK G31 CON_DSI_B_CLK_N OUT 17.2C<
DSI2_D0 F31 CON_DSI_B_D0_P OUT 17.2C<
DSI2_D0 F32 CON_DSI_B_D0_N OUT 17.2C<
DSI2_D1 H29 CON_DSI_B_D1_P OUT 17.2C<
DSI2_D1 H30 CON_DSI_B_D1_N OUT 17.2C<
DSI3_CLK D30 CON_DSI4_CLK_P OUT 17.3H<
DSI3_CLK D31 CON_DSI4_CLK_N OUT 17.3H<
DSI3_D0 C31 CON_DSI_B_D2_P OUT 17.2C<
DSI3_D0 C32 CON_DSI_B_D2_N OUT 17.2C<
DSI3_D1 E29 CON_DSI_B_D3_P OUT 17.2C<
DSI3_D1 E30 CON_DSI_B_D3_N OUT 17.2C<

ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	IO connector 2/3

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J13
45970-0001
CVB_8X50
CHANGED

3/3 GBE, WIFI, BT, MODEM, GPS, PCIE, SATA, USB

CVM 1.0

13.3A<	OUT	GBE_MDI0_P	E48	GBE_MDI0		
13.3A<	OUT	GBE_MDI0_N	E49	GBE_MDI0		
13.3A<	OUT	GBE_MDI1_P	F47	GBE_MDI1		
13.3A<	OUT	GBE_MDI1_N	F48	GBE_MDI1		
13.3A<	OUT	GBE_MDI2_P	G48	GBE_MDI2		
13.3A<	OUT	GBE_MDI2_N	G49	GBE_MDI2		
13.3A<	OUT	GBE_MDI3_P	H47	GBE_MDI3		
13.3A<	OUT	GBE_MDI3_N	H48	GBE_MDI3		
13.4E<	OUT	GBE_LED0_SPICSB	E47	GBE_LINK_ACT		
13.4E<	OUT	GBE_LED1_SPISCK	F50	GBE_LINK100		
	TP8	GBE_LED2	F46	GBE_LINK1000		
	TP7	GBE_CTREF	H50	GBE_CTREF		
10.3H<>	BI	SDIO_D0	B32	SDIO_D0		
10.3H<>	BI	SDIO_D1	A32	SDIO_D1		
10.3H<>	BI	SDIO_D2	A31	SDIO_D2		
10.3H<>	BI	SDIO_D3	A30	SDIO_D3		
10.3H<	BI	SDIO_CMD	B29	SDIO_CMD		
10.3H<	OUT	SDIO_CLK	B30	SDIO_CLK		
10.3H<	OUT	WIFI2_EN	A29	SDIO_RST		
10.3H<	IN	WIFI2_WAKE_AP_L	B20	GPIO10_WIFI_WAKE_AP		
10.4G<	OUT	AP_WAKE_MDM_1V8	A8	GPIO14_AP_WAKE_MDM		
10.3C>	IN	I2S2_SDIN	G6	I2S2_SDIN		
10.3C<	OUT	I2S2_SDOUT	H6	I2S2_SDOUT		
10.3C<	BI	I2S2_LRCLK	H5	I2S2_LRCLK		
10.3C<	BI	I2S2_CLK	G5	I2S2_CLK		
10.3C<	OUT	UART2_TXD	B16	UART2_TX		
10.3C>	IN	UART2_RXD	B15	UART2_RX		
10.2C<	OUT	UART2_RTS	A16	UART2_RTS		
10.2C>	IN	UART2_CTS	A15	UART2_CTS		
10.3A<	OUT	BT2_EN	B21	GPIO12_BT_EN		
10.3C>	IN	BT2_WAKE_AP_L	B22	GPIO13_BT_WAKE_AP		
16.3E<	OUT	AP_WAKE_BT	B19	GPIO11_AP_WAKE_BT		
16.5C<	IN	I2S1_SDIN	C14	I2S1_SDIN		
16.5C<	OUT	I2S1_SDOUT	D14	I2S1_SDOUT		
16.3C<	BI	I2S1_LRCLK	D13	I2S1_LRCLK		
16.3E<	BI	I2S1_CLK	C15	I2S1_CLK		
10.4G>	IN	MDM_COLDBOOT_1V8	B10	GPIO18_MDM_COLDBOOT		
18.3C>	IN	MDM2AP_READY_1V8	B9	GPIO17_MDM2AP_READY		
16.4D<	OUT	AP2MDM_READY	A9	GPIO15_AP2MDM_READY		
16.3B<>	IN	MDM_WAKE_AP_1V8	A10	GPIO16_MDM_WAKE_AP		
15.4A<	OUT	UART0_TXD	H12	UART0_TX		
15.4D>	IN	UART0_RXD	G12	UART0_RX		
15.3A<	OUT	UART0_RTS	G11	UART0_RTS		
15.3K>	IN	UART0_CTS	H11	UART0_CTS		
18.3G<>	BI	I2S3_CLK	E6	I2S3_CLK		
18.3G<>	BI	I2S3_LRCLK	F5	I2S3_LRCLK		
18.3G>	IN	I2S3_SDIN	E5	I2S3_SDIN		
18.3G<	OUT	I2S3_SDOUT	F6	I2S3_SDOUT		
17.3G<	OUT	SPI2_SCK	H14	SPI2_CLK		
17.3G>	IN	SPI2_MISO	H15	SPI2_MISO		
17.3G<	OUT	SPI2_MOSI	G15	SPI2_MOSI		
17.4F<	OUT	SPI2_CS0	G16	SPI2_CS0		
18.2G<	OUT	SPI2_CS1	F16	SPI2_CS1		
16.2C<	16.18< IN	GNSS_PPS	B18	GNSS_PPS		

WIFI

BT

MODEM

Pin B16(UART2_TX)) is associated with
RAM_CODE3 strapping option in Jetson TX2(I).
Pin A16(UART2_RTS#) is associated with
RAM_CODE2 strapping option in Jetson TX2(I).

These pins must be handled carefully to avoid
changing the strapping levels during power-on
which could cause the platform to malfunction.
See the Jetson TX1/TX2(I) OEM DGs for details.

Pin H12(UART0_TX) is associated with
RAM_CODE1 strapping option in Jetson TX1.
Pin G11(UART0_RTS#) is associated with
RAM_CODE0 strapping option in Jetson TX1/TX2(I).

PEX_WAKE	D48	PCIE_WAKE_L	IN	9.2F>	10.2H>	
PEX0_RST	C49	PCIE0_L0_RST	OUT	9.3F<		
PEX0_CLKREQ	C48	PCIE0_L0_CLKREQ	IN	9.2B>		
PEX0_REFCLK	A44	PEX_CLK0_P	OUT	9.3F<		
PEX0_REFCLK	A45	PEX_CLK0_N	OUT	9.3F<		
PEX0_RX	H44	PEX_RX4_P	IN	9.3F>		
PEX0_RX	H45	PEX_RX4_N	IN	9.3F>		
PEX0_TX	E44	PEX_TX4_P	OUT	9.5C<		
PEX0_TX	E45	PEX_TX4_N	OUT	9.5C<		
PEX1_RST	E50	PCIE_L1_RST	OUT	10.2A<		
PEX1_CLKREQ	C47	PCIE_L1_CLKREQ	IN	10.2H>		
PEX1_REFCLK	B45	PEX_CLK1_P	OUT	10.2H<		
PEX1_REFCLK	B46	PEX_CLK1_N	OUT	10.2H<		
PEX1_RX	H41	PEX_RX0_AP_P	IN	10.2H>		
PEX1_RX	H42	PEX_RX0_AP_N	IN	10.2H>		
PEX1_TX	E41	PEX_TX0_AP_P	OUT	10.2H<		
PEX1_TX	E42	PEX_TX0_AP_N	OUT	10.2H<		
PEX2_RST	D49	PEX2_RST_L		TP10		
PEX2_CLKREQ	C46	PEX2_CKREQ_L		TP16		
PEX2_REFCLK	A41	PEX2_REFCLK_P	90DIFF_NETCLASS1	TP18		
PEX2_REFCLK	A42	PEX2_REFCLK_N	90DIFF_NETCLASS1	TP17		
PEX2_RX	F40	PEX_RX2_P	IN	9.3F>		
PEX2_RX	F41	PEX_RX2_N	IN	9.3F>		
PEX2_TX	C40	PEX_TX2_P	OUT	9.4C<		
PEX2_TX	C41	PEX_TX2_N	OUT	9.4C<		
PEX_RFU_RX	G39	PEX_RX1_P	IN	9.3F>		
PEX_RFU_RX	G40	PEX_RX1_N	IN	9.3F>		
PEX_RFU_TX	D39	PEX_TX1_P	OUT	9.4C<		
PEX_RFU_TX	D40	PEX_TX1_N	OUT	9.4C<		
SATA_RX	G45	SATA_RX_P	IN	12.3C>		
SATA_RX	G46	SATA_RX_N	IN	12.2C>		
SATA_TX	D45	SATA_TX_P	OUT	12.2C<		
SATA_TX	D46	SATA_TX_N	OUT	12.2C<		
SATA_DEV_SLP	D47	SATA_DEV_SLP	OUT	12.3A<		
USB_SS0_RX	F43	USB3_RX1_P	IN	8.2B>		
USB_SS0_RX	F44	USB3_RX1_N	IN	8.2B>		
USB_SS0_TX	C43	USB3_TX1_P	OUT	8.2B<		
USB_SS0_TX	C44	USB3_TX1_N	OUT	8.2B<		
USB_SS1_RX	G42	PEX_RX3_P	IN	9.3F>		
USB_SS1_RX	G43	PEX_RX3_N	IN	9.3F>		
USB_SS1_TX	D42	PEX_TX3_P	OUT	9.5C<		
USB_SS1_TX	D43	PEX_TX3_N	OUT	9.5C<		
USB1_D	A38	USB1_D_P	BI	8.2B<>		
USB1_D	A39	USB1_D_N	BI	8.2B<>		
USB1_EN_OC	A18	USB_VBUS_EN1	OUT	8.1B<		
USB2_D	B42	USB2_D_P	BI	10.3H<>		
USB2_D	B43	USB2_D_N	BI	10.3H<>		
USB2_EN_OC	A19	USB_VBUS_EN2	TP14			
CAN_WAKE	C20	CAN_WAKE	IN	16.2B<	16.5D<	
CAN0_STBY	E17	CAN0_STBY	BI	16.2B<>	16.5D<>	
CAN0_RX	D18	CAN0_RX	IN	16.2B<	16.5D<	
CAN0_TX	D19	CAN0_TX	OUT	16.2B>	16.4C>	
CAN0_ERR	E18	CAN0_ERR	IN	16.2B<	16.5D<	
CAN1_STBY	C17	CAN1_STBY	BI	16.2B<>	16.5C<>	
CAN1_RX	D17	CAN1_RX	IN	16.2B<	16.4C<	
CAN1_TX	C18	CAN1_TX	OUT	16.2B>	16.4C>	
CAN1_ERR	C19	CAN1_ERR	IN	16.2B<	16.4C<	

It is recommended that
any unused USB 3.0, PCIe
or SATA RX lanes should
be connected to GND.

ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	IO connector 3/3

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ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	BLANK

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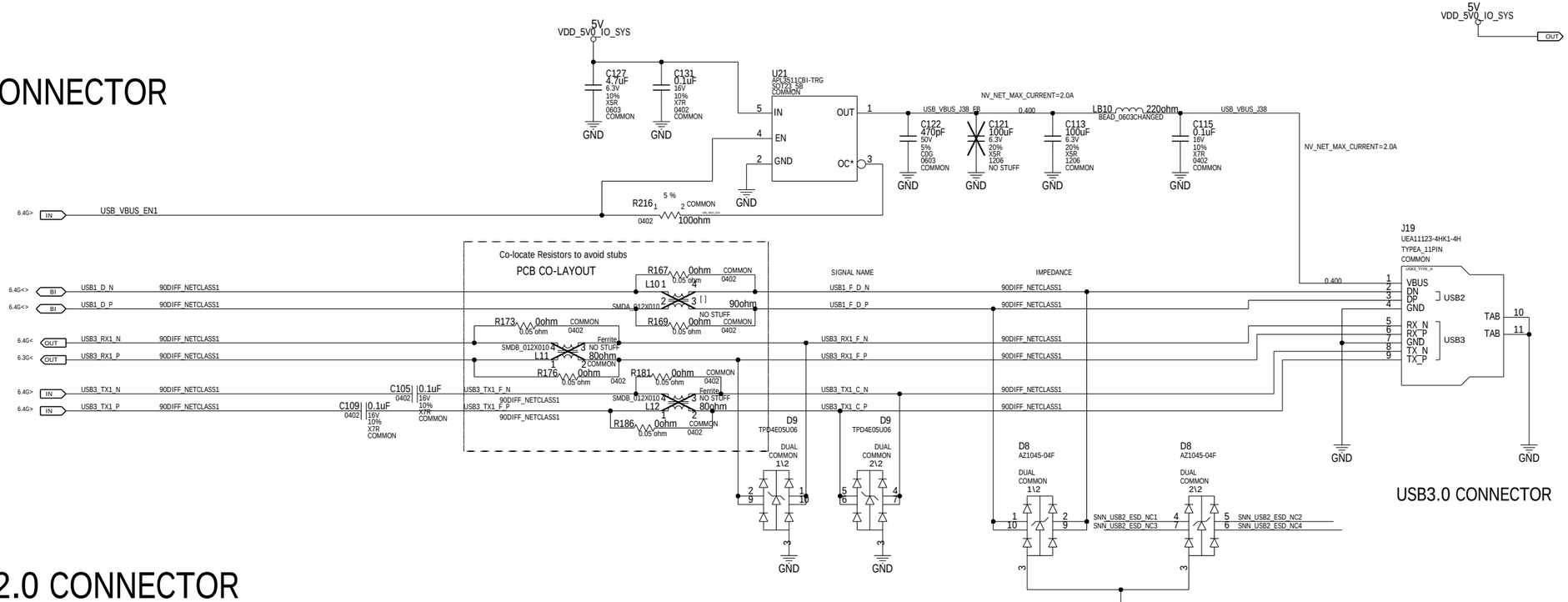
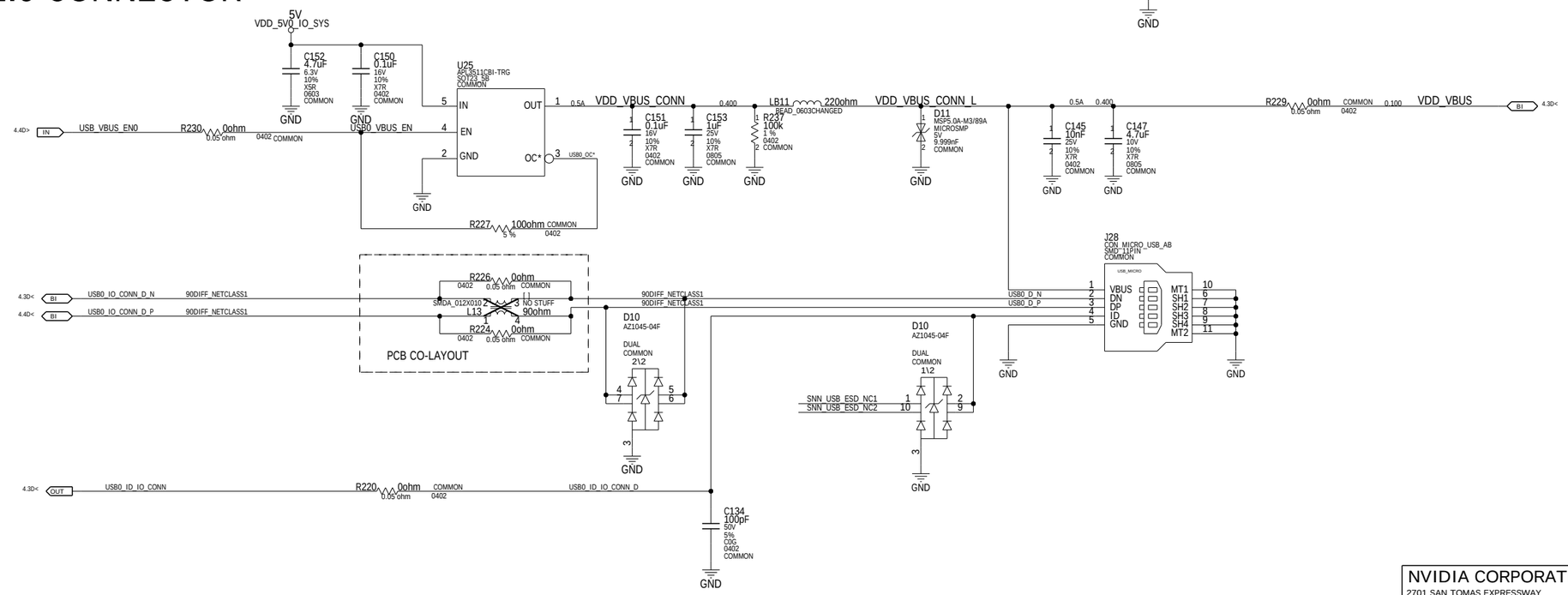
USB 3.0 TYPE A CONNECTOR



MICRO AB USB 2.0 CONNECTOR



ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	USB3.0 type A and USB2.0 micro

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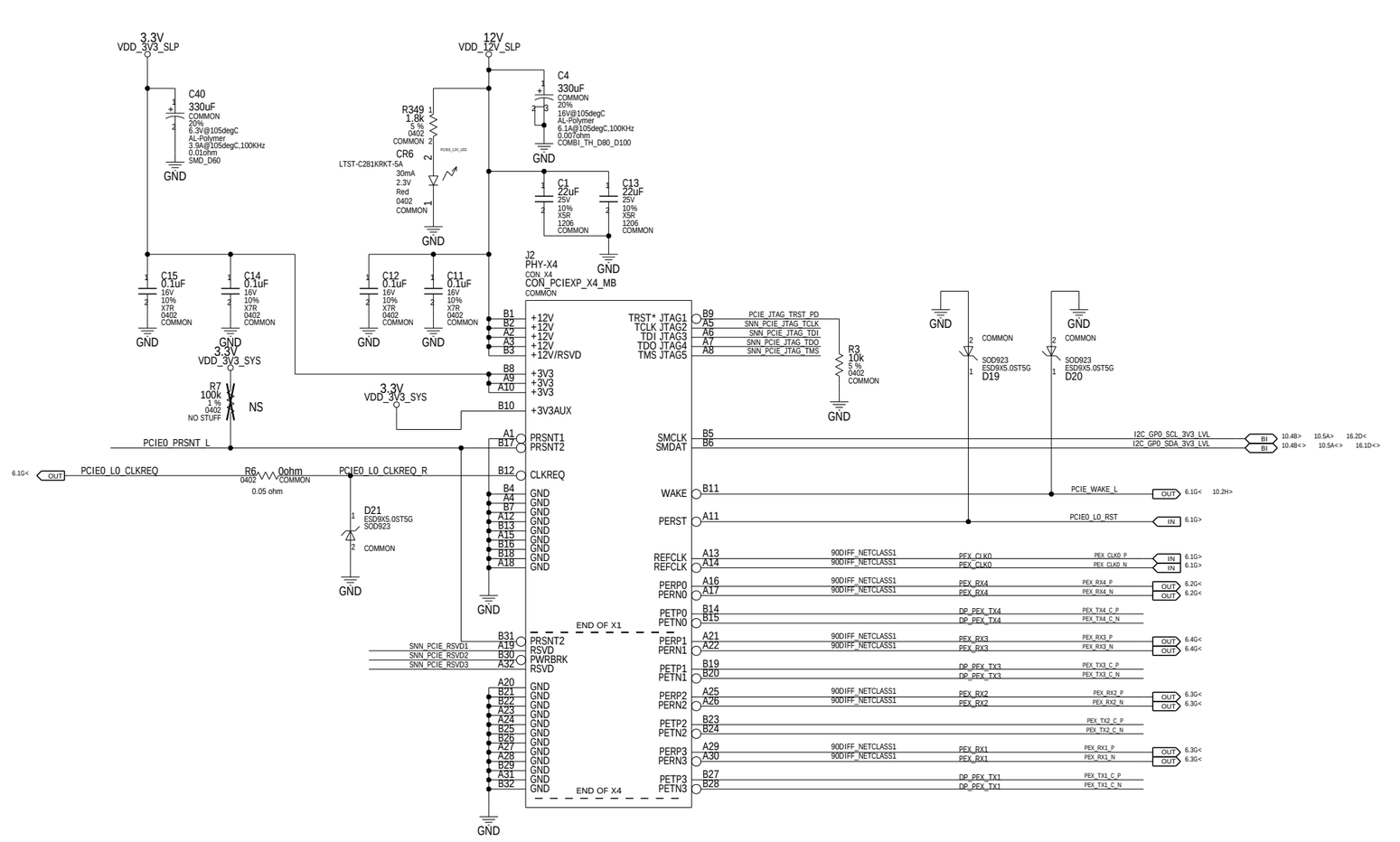

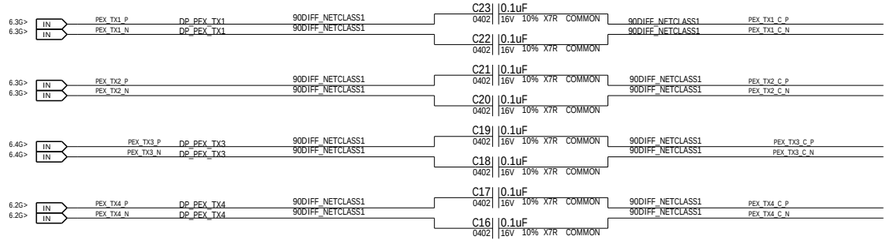

ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	PCIe x4 Connector

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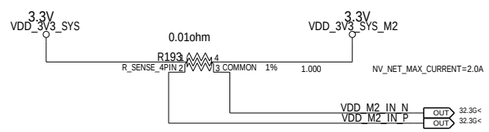
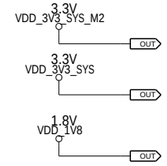
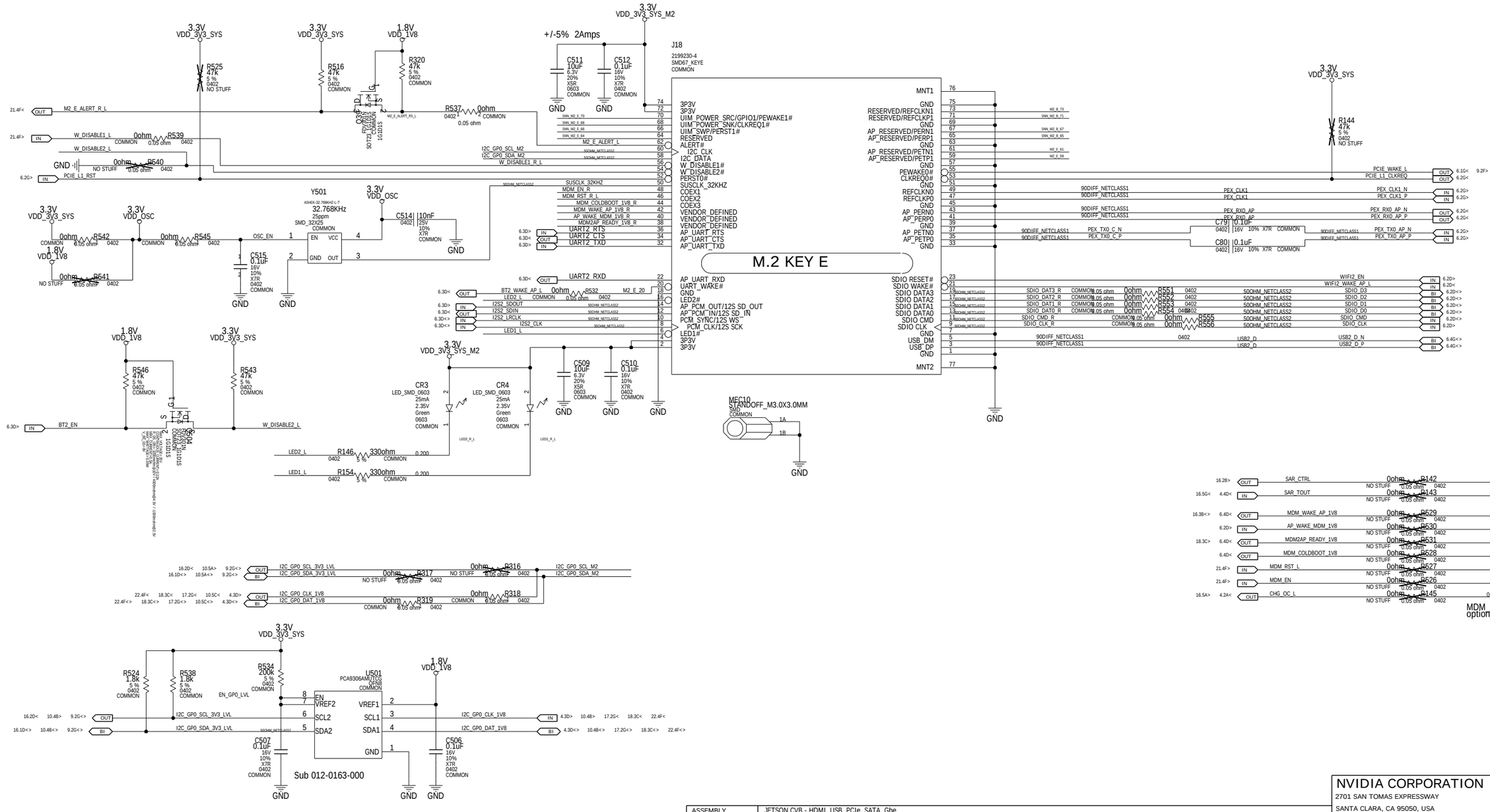
M.2 KEY E







ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	M.2 KEY E

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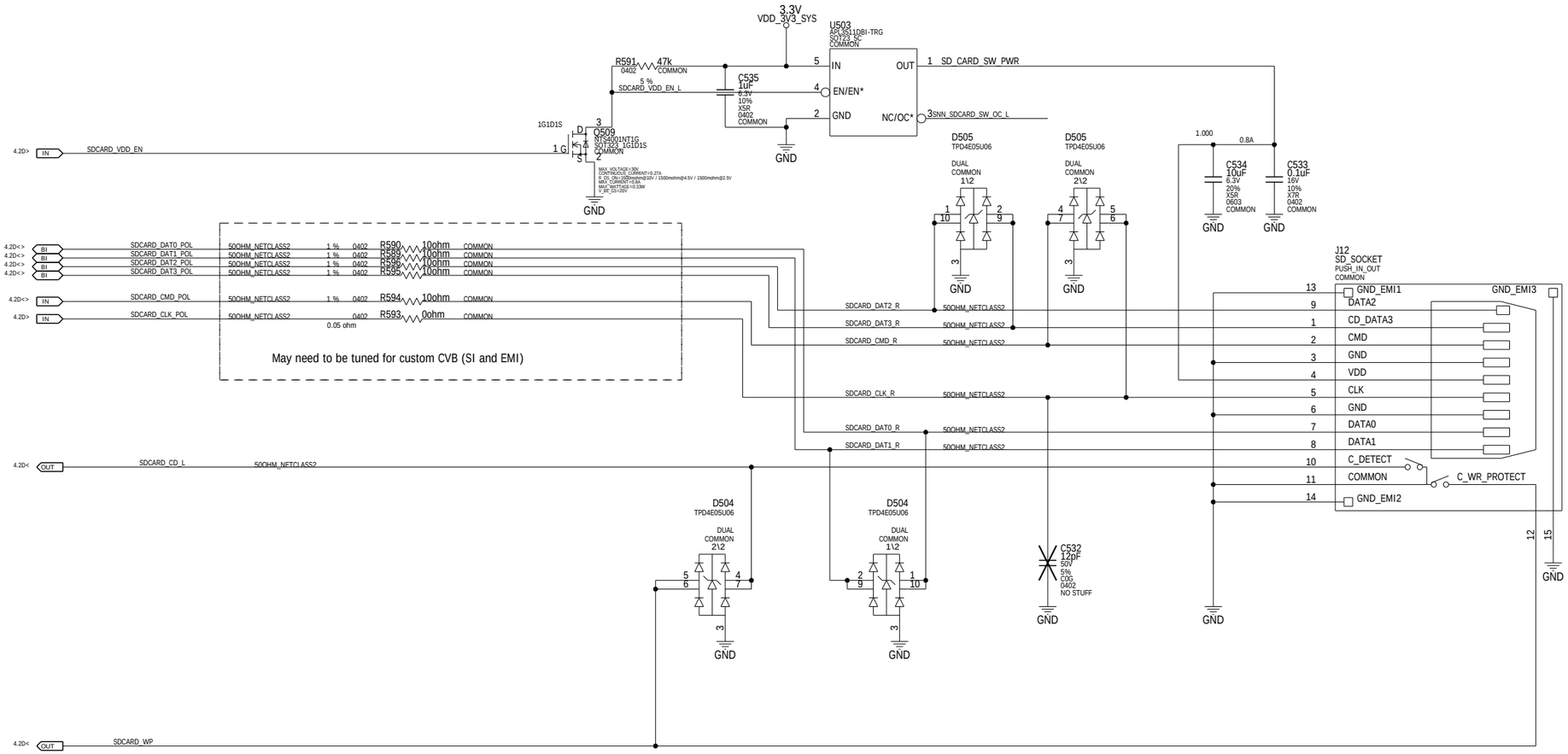
SD CARD SOCKET



ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	SDcard Slot

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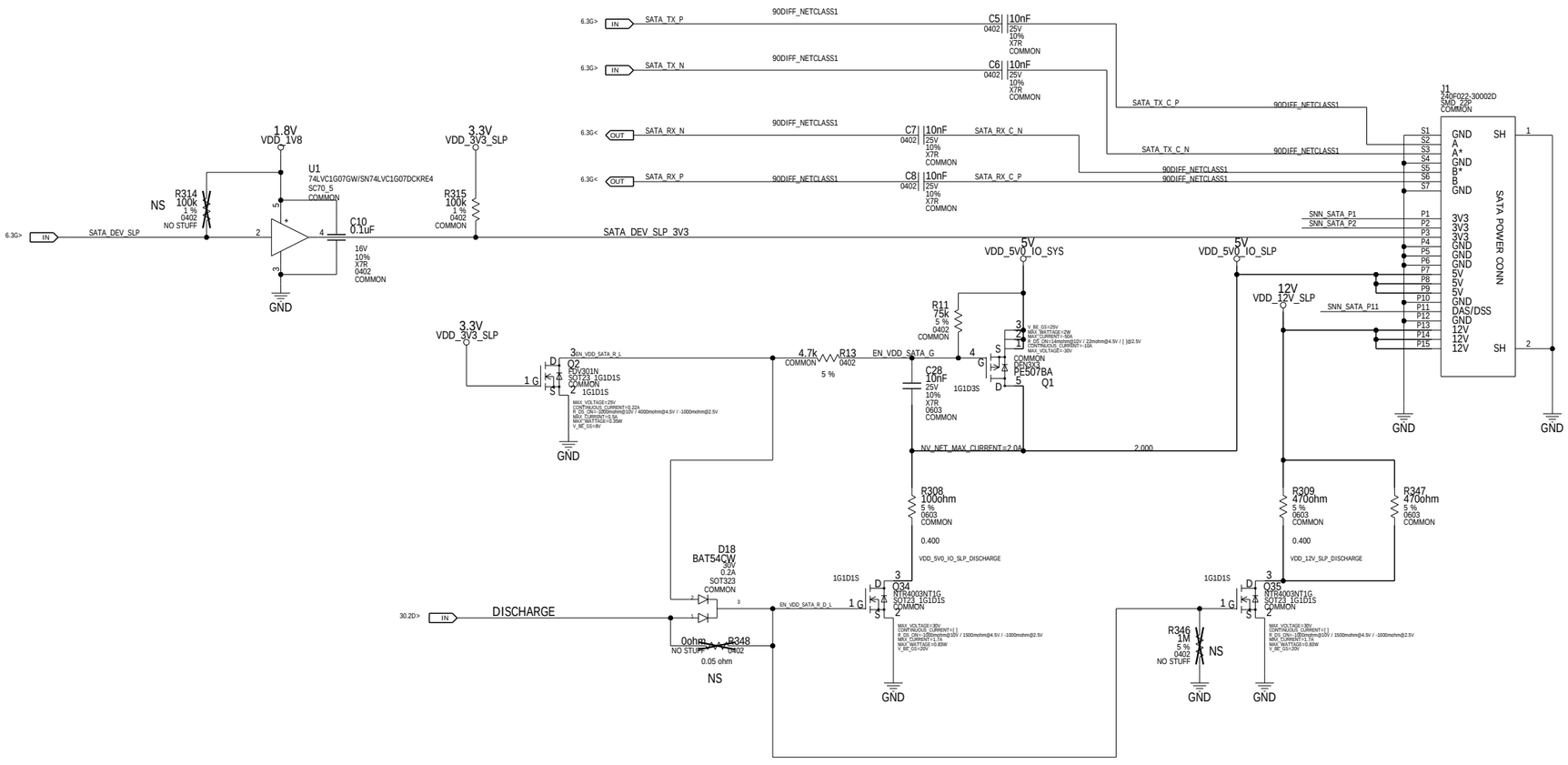
SATA Connector



ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	SATA

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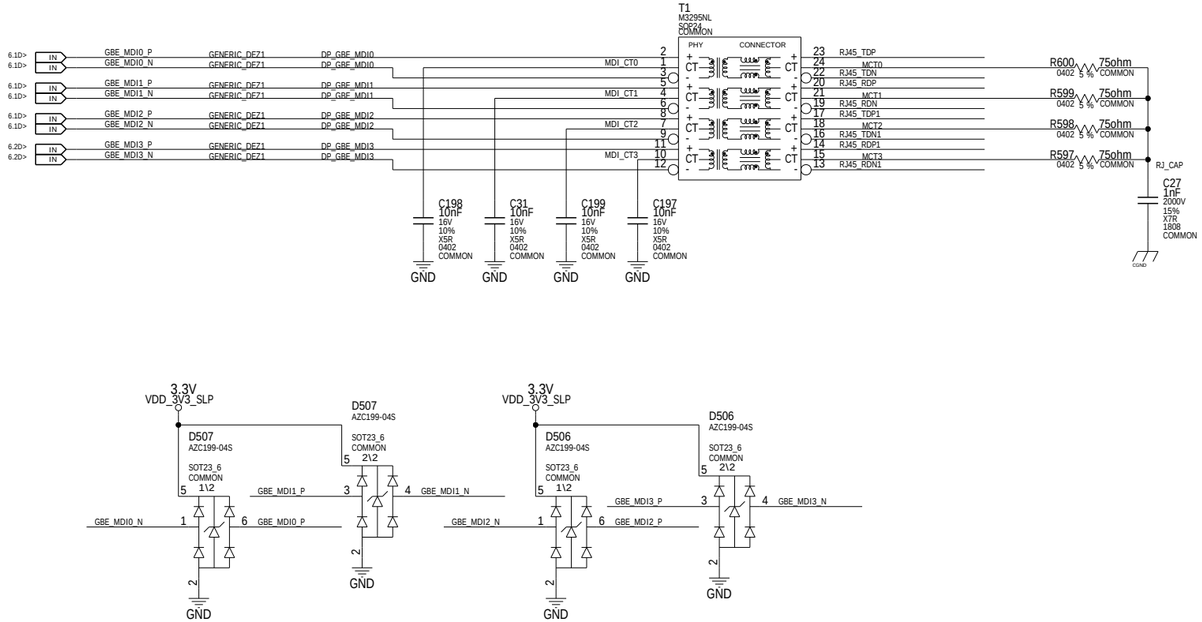
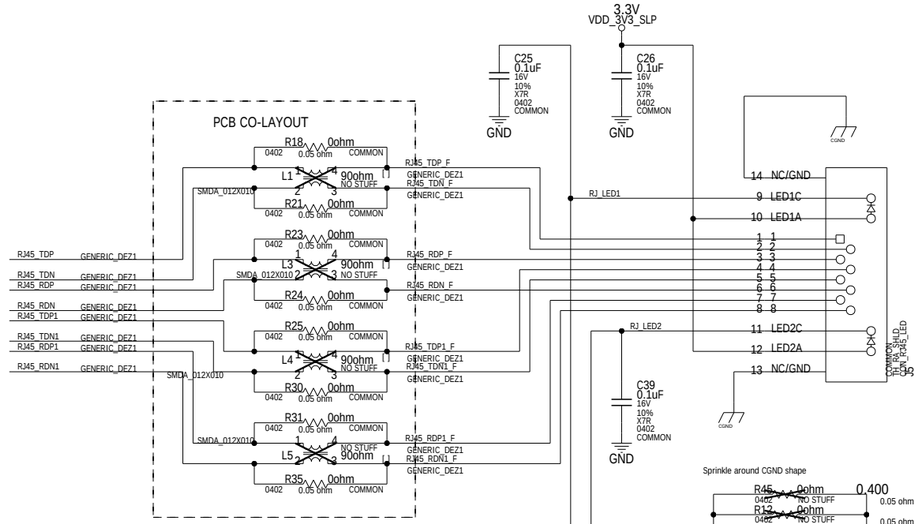
Gigiabit Ethernet





ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	Gigabit Ethernet

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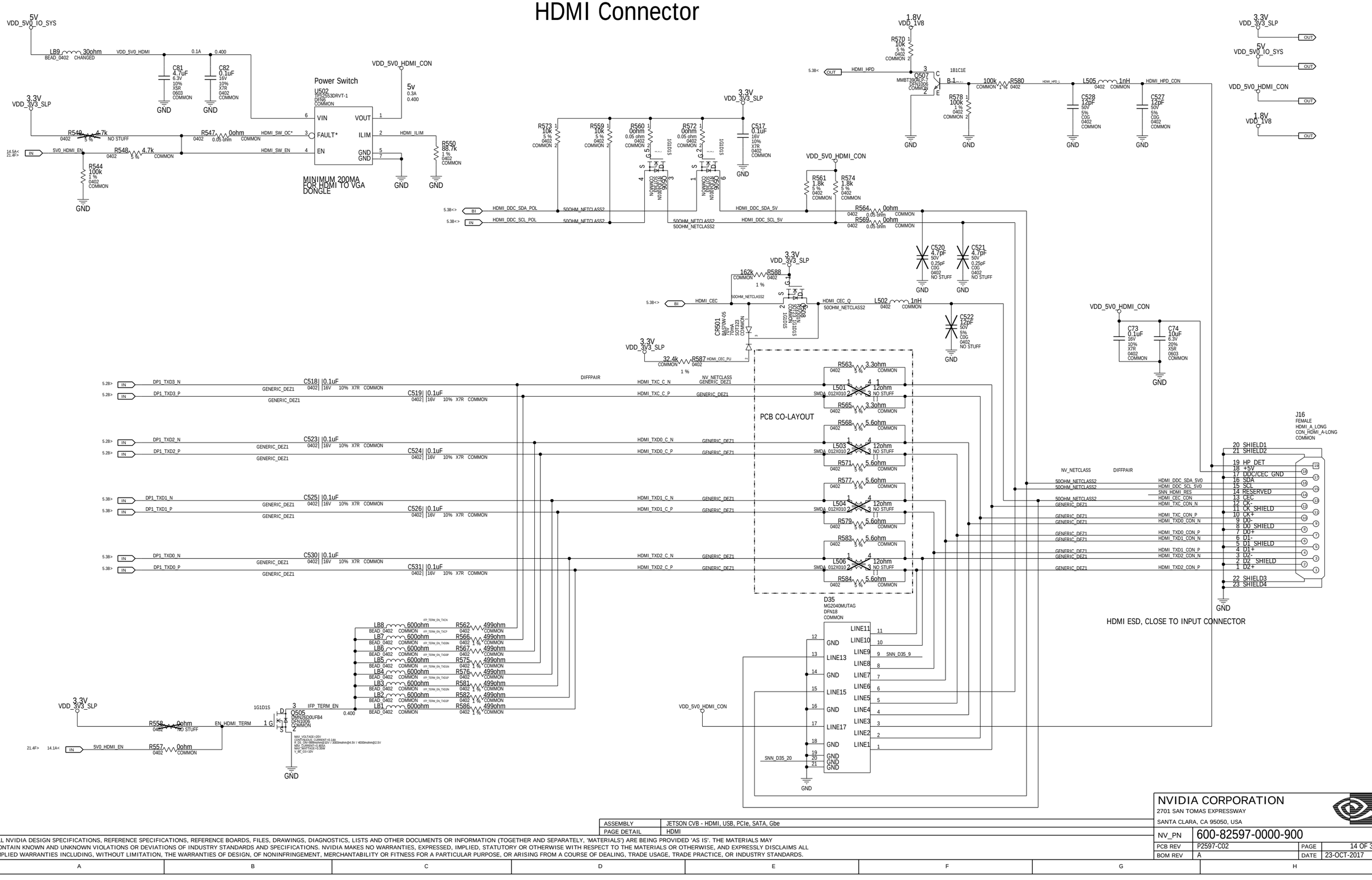
HDMI Connector



ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	HDMI

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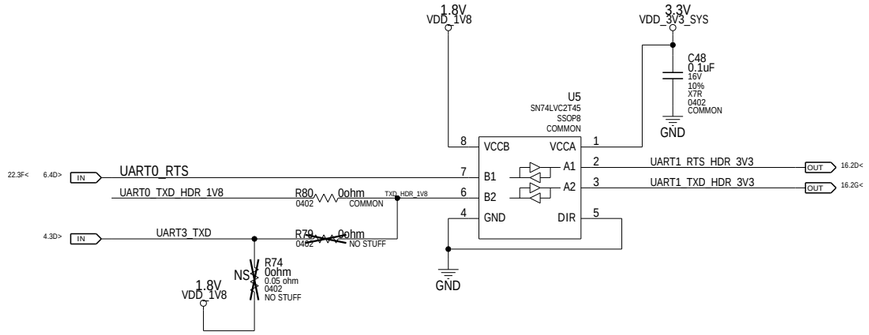
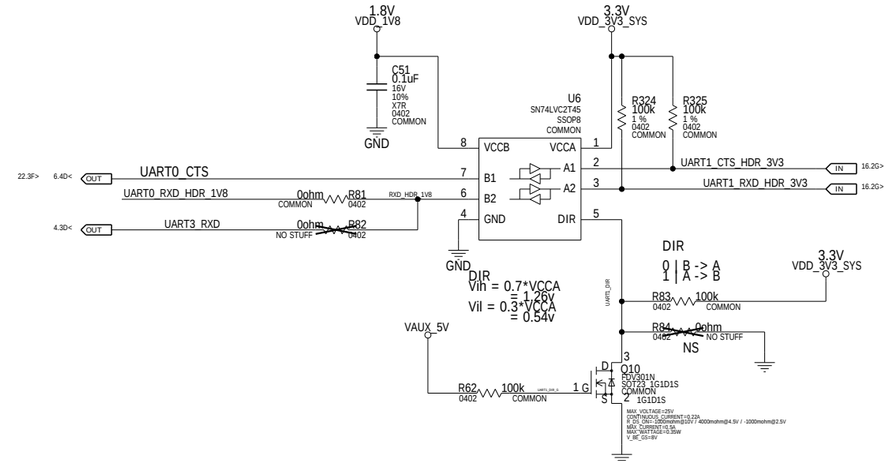
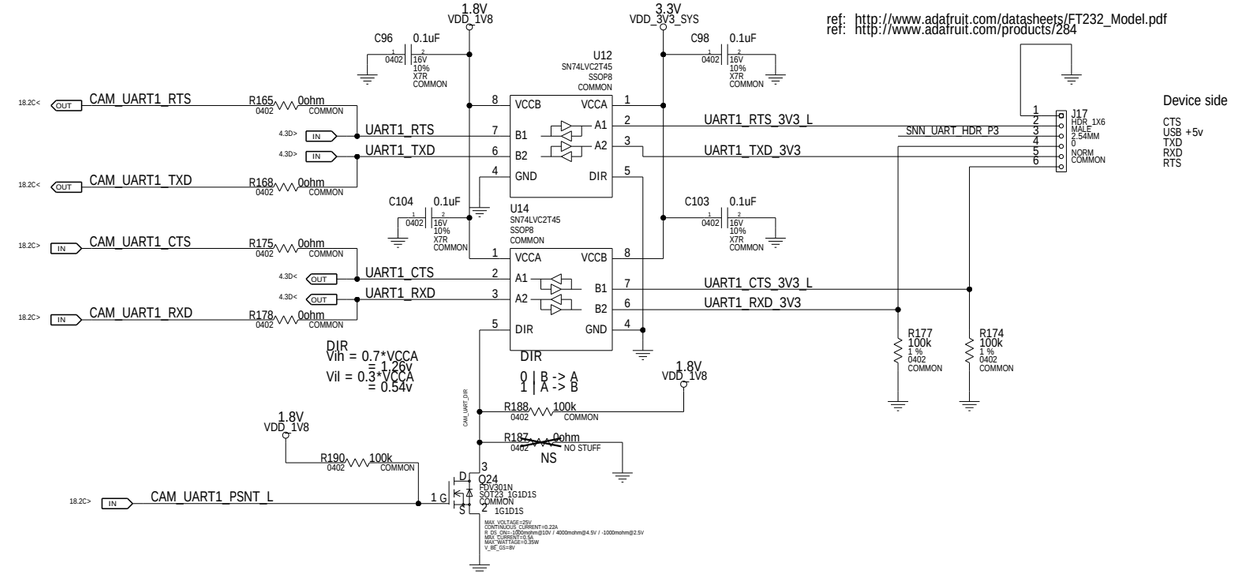
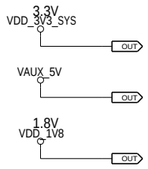
SERIAL PORT





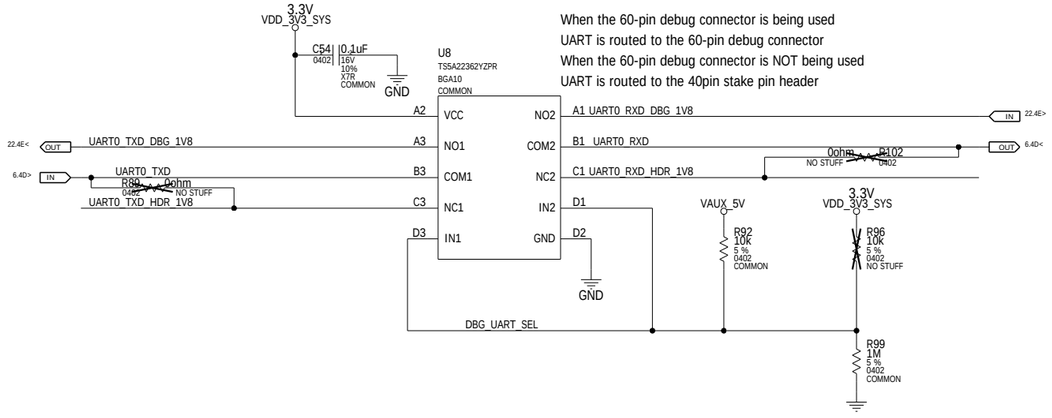


ref: http://www.adafruit.com/datasheets/FT232_Model.pdf
ref: http://www.adafruit.com/products/284

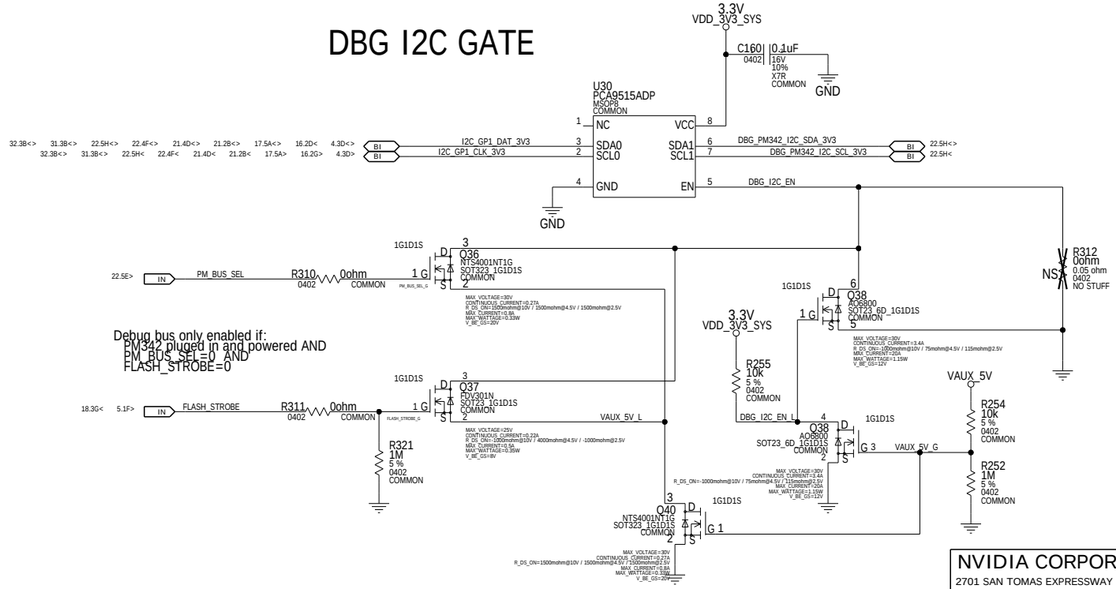


UART MUX

When the 60-pin debug connector is being used
UART is routed to the 60-pin debug connector
When the 60-pin debug connector is NOT being used
UART is routed to the 40pin stake pin header



DBG I2C GATE



ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	Serial port and JTAG

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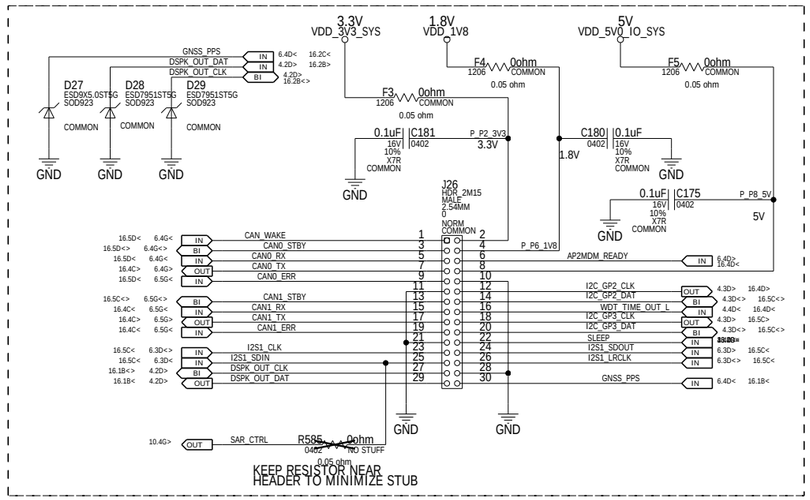
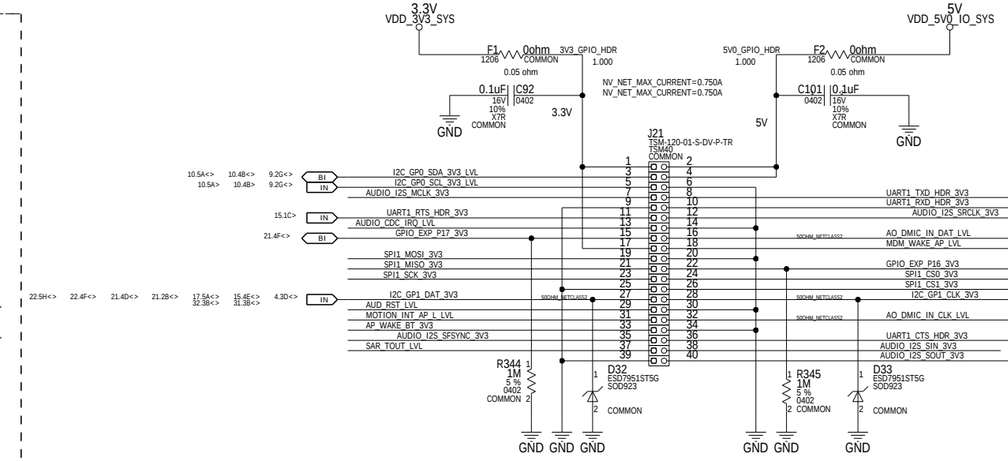
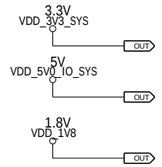
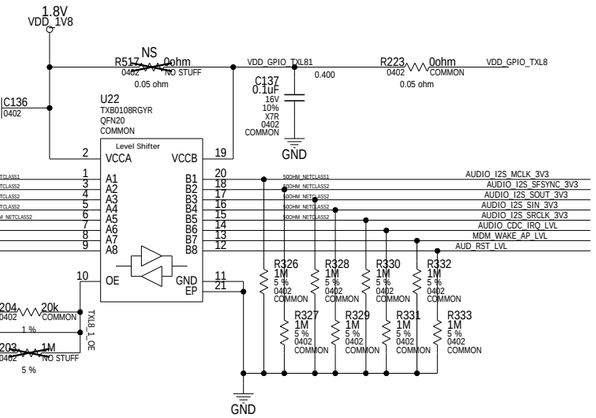
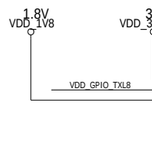
GPIO Expansion Headers

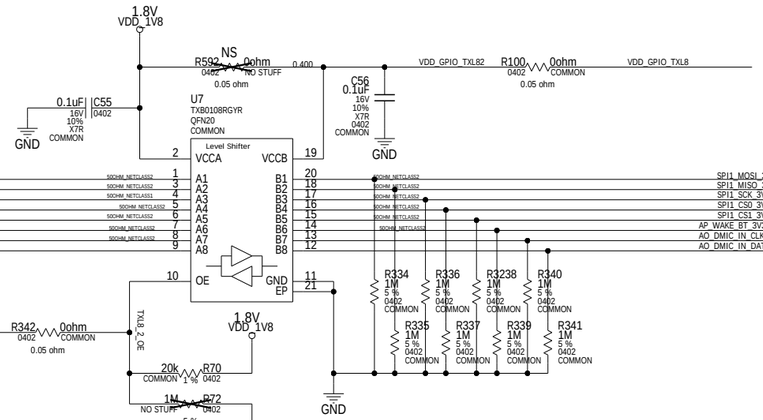




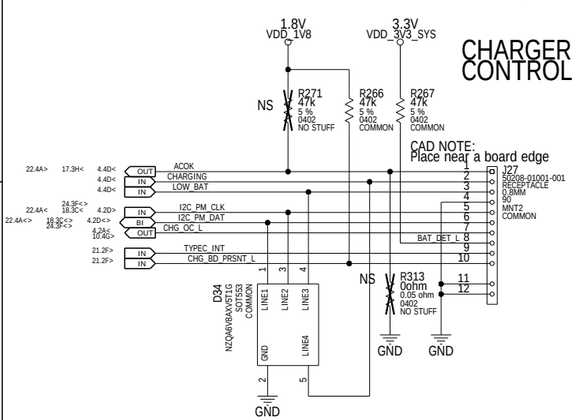


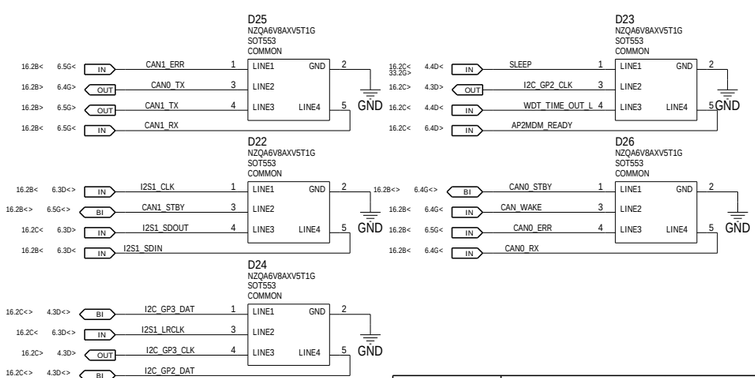


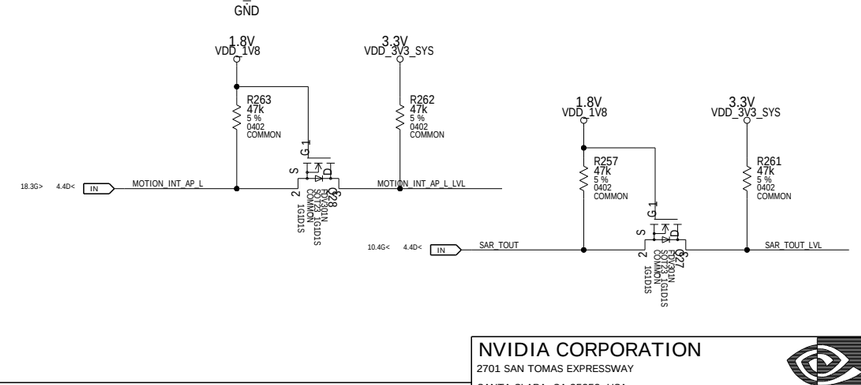




GPIO_PK0 I2S5B_FS
GPIO_PK2 I2S5B_SDOUT
GPIO_PK1 I2S5B_SDIN







ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	IO Expansion Connector

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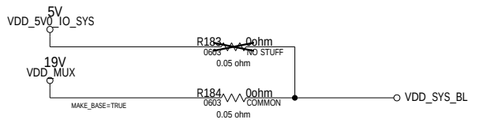
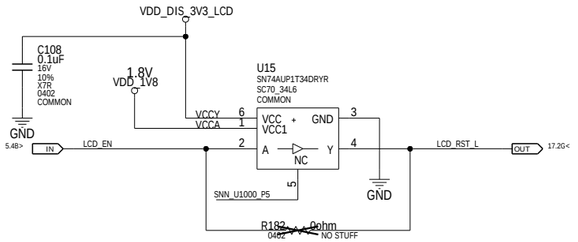
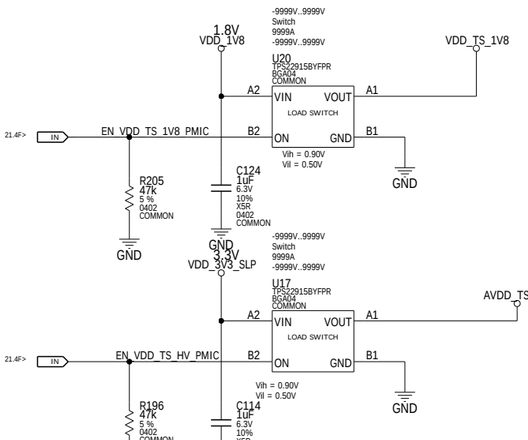
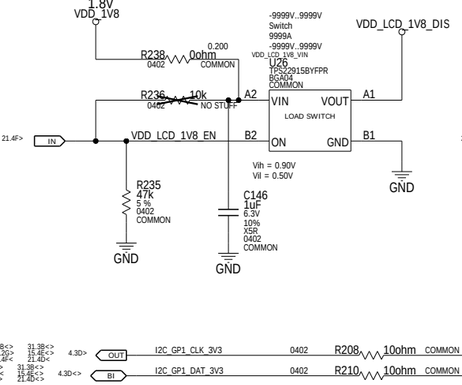
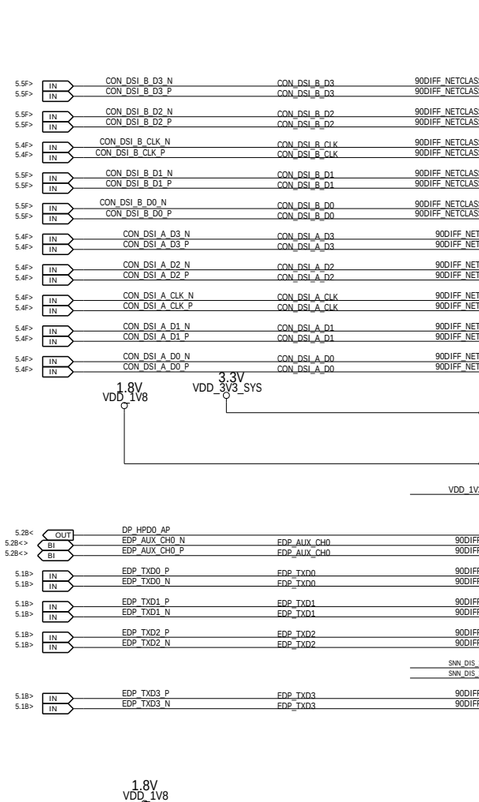
DISPLAY CONNECTOR

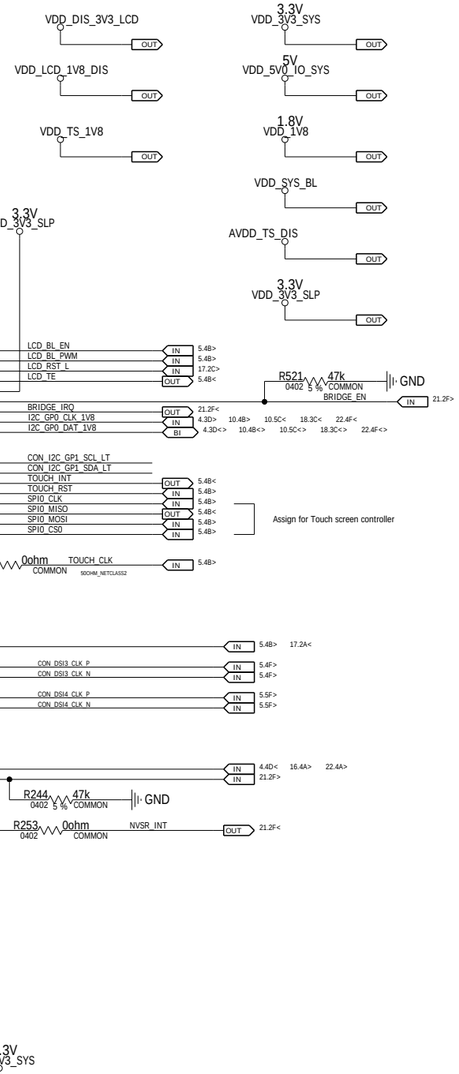


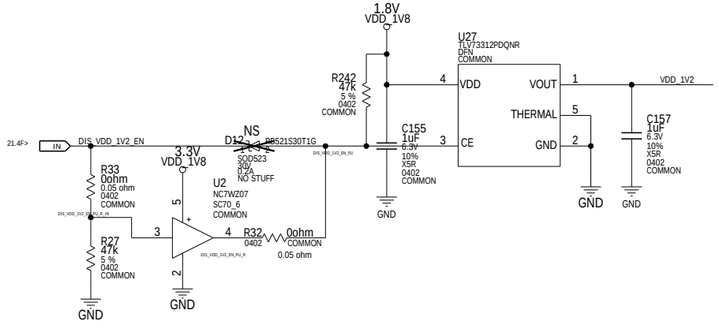


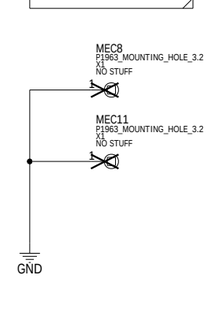


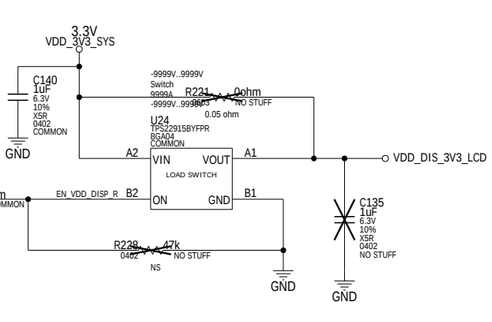












ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	DSI Connector

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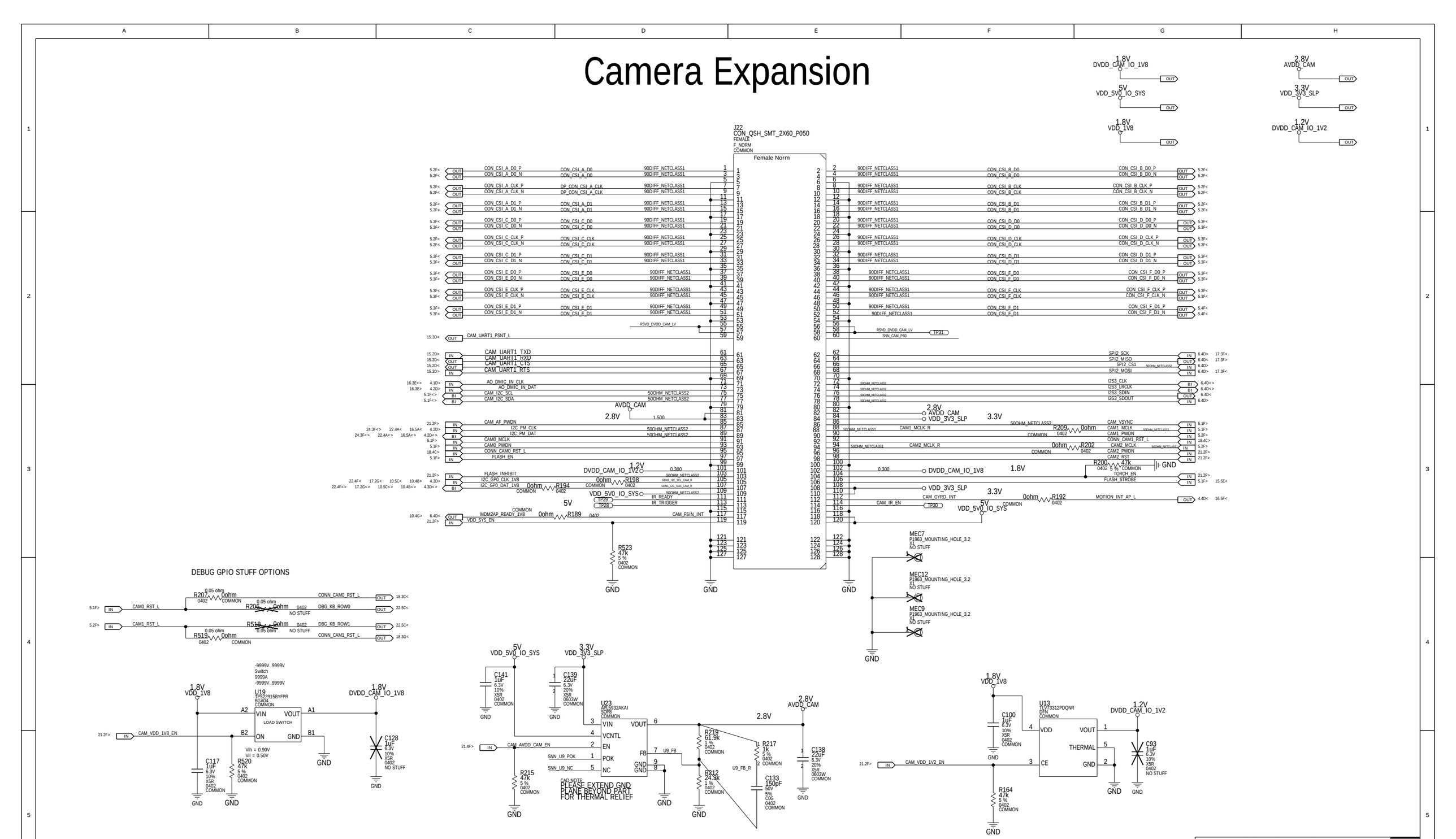
Camera Expansion



DEBUG GPIO STUFF OPTIONS

ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	CSI Connector

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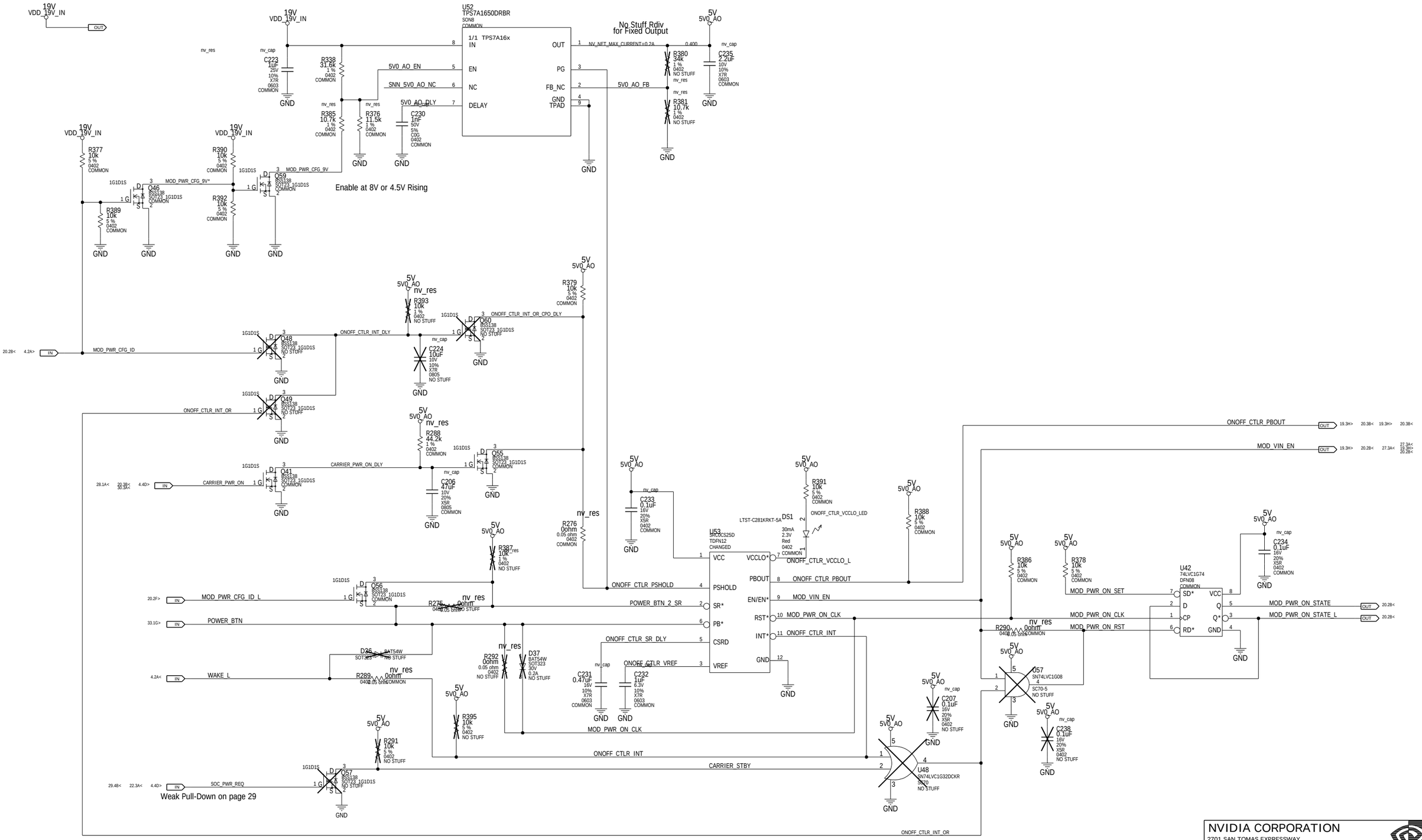

ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	ON OFF CONTROLLER

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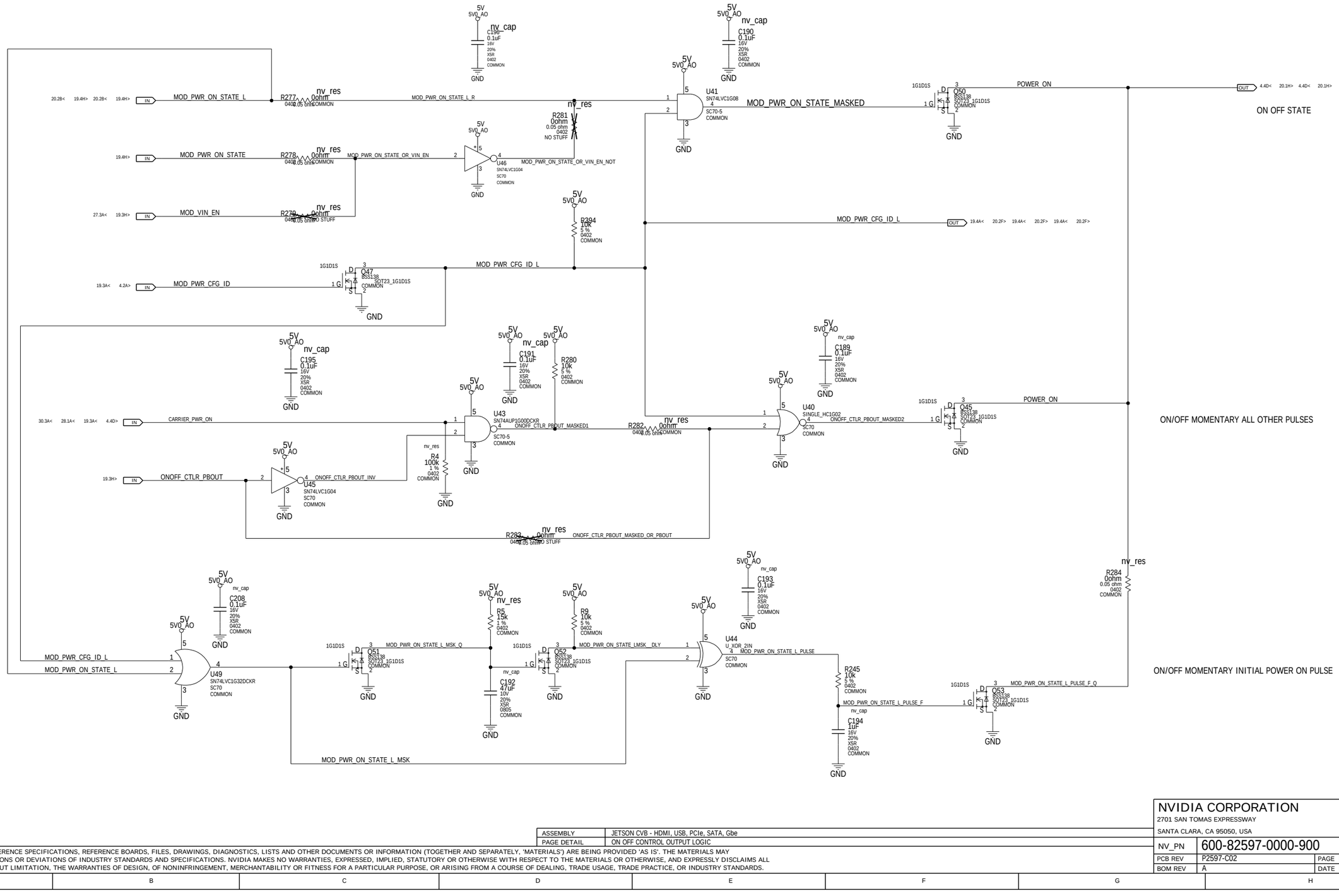

ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	ON OFF CONTROL OUTPUT LOGIC

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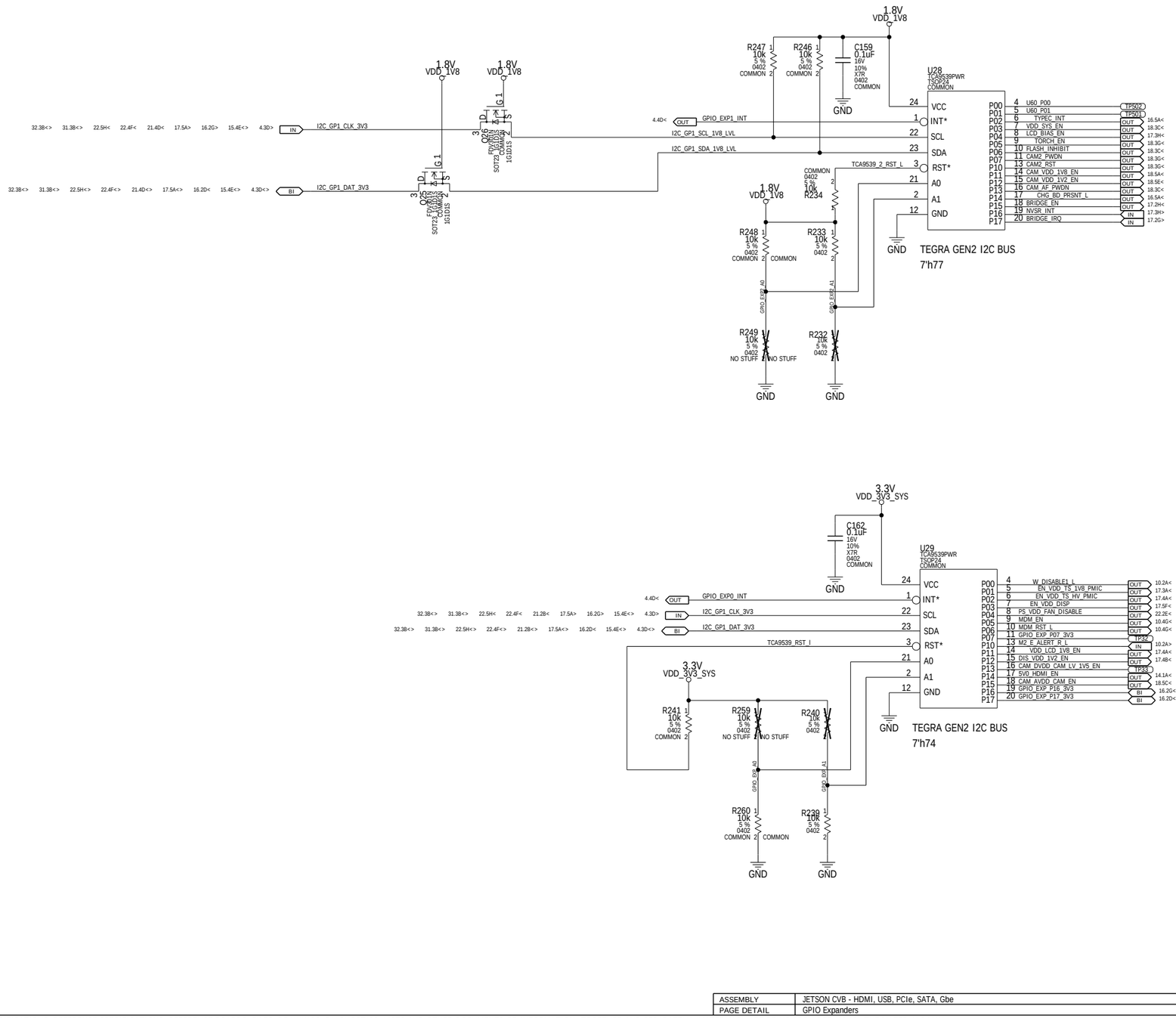
GPIO EXPANDERS



ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	GPIO Expanders

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JTAG HEADER

VAUX_5V, 1.8V VDD_1V8, 5V VDD_5V0_IO_SYS, 12V VDD_12V_SLP, 5V VDD_5V0_IO_SLP, 3.3V VDD_3V3_SYS (OUT)

Stuff R52 for boundary scan mode
OR ICT can drive JTAG_AP_TRST_L high

Empty R52 for debug mode

R52 0ohm 0402 0.05 ohm NO STUFF

R48, R19, R36, R39, R43 10k 5 % 0402 COMMON

J7 HDR_2X10 MALE 2.54MM 0 SHR_JTAG1 COMMON

1 VCC		VCC	2
3 TRST*		GND	4
5 TDI		GND	6
7 TMS		GND	8
9 TCK		GND	10
11 RTCK		GND	12
13 TDO		GND	14
15 RST		GND	16
17 PD		GND	18
19 PD		GND	20

JTAG_AP_TRST_L, JTAG_AP_TDI, JTAG_AP_TMS, JTAG_AP_TCK, JTAG_AP_RTCK, JTAG_AP_TDO, RESET_IN_R_L

JTAG_CN_TRST_R_L

JTAG_SRST_OD_L (JTAG_17, JTAG_19)

R20 0ohm 0402 COMMON 0.05 ohm

C43 0.1uF 16V 10% X7R 0402 COMMON

U2 NC7W207 SC70_6 COMMON

R17 0ohm 0.05 ohm 0402 NO STUFF

RESET_OUT_L → R28 0ohm 0402 COMMON 0.05 ohm → RESET_OUT_R_L

C30 0.1uF 16V 10% X7R 0402 COMMON

R26 0ohm 0.05 ohm 0402 NO STUFF

J8 HDR_1M2 MALE 2.54MM 0 NORM COMMON

Short for boundary scan test

R29, R22, R16, R15 47k / 10k 5 % 0402 COMMON

U3 NC7W207 SC70_6 COMMON

SOC_PWR_REQ → LED_VDD_CORE (OUT 33.5C<)

U3 NC7W207 SC70_6 COMMON

SNN_U3_P6 → C44 0.1uF 16V 10% X7R 0402 COMMON → U3_P1

R41 0ohm 0.05 ohm 0402 COMMON

SoC Fan Header 4pin

VDD_12V_SLP, VDD_5V0_IO_SLP, VDD_5V0_IO_SYS

R126 NS 0ohm 0603 NO STUFF 0.05 ohm

R130 0ohm 0603 COMMON 0.05 ohm

R134 0ohm 0603 NO STUFF 0.05 ohm

VDD_FAN 0.400

C64 10uF 25V 20% X5R 0603W CHANGED

C61 0.1uF 16V 10% X7R 0402 COMMON

R115 4.7k 5 % 0402 COMMON

R117 10k 5 % 0402 COMMON

R121 100k 1 % 0402 COMMON

FAN_PWM (IN 4.4D>, 50CHM_NETCLASS2) → R114 100k 1 % 0402 NO STUFF

Q17 AO6800 SOT23_6D_1G1D1S COMMON (1G1D1S)

MAX_VOLTAGE=30V CONTINUOUS_CURRENT=3.4A R_DS_ON=100mohm@10V / 75mohm@4.5V / 115mohm@2.5V MAX_DUTY=100% MAX WATTAGE=1.15W V_BE_GS=12V

R300 1000ohm 0402 5 % COMMON (4.4D> OUT)

FAN_PWM_Q_R → FAN_PWM_Q* → FAN_TACH

D30 ESD9X5.0ST5G SOD923 COMMON

D17 AOZ8231ADI-12 NORM 12V 14pF COMMON

C58 10pF 50V 5% C0G 0402 COMMON

C60 10pF 50V 5% C0G 0402 COMMON

J15 HDR_1X4 MALE 1.25MM 0 SD275-00471-003 COMMON

Vgs(th) = 0.8 to 1.5V

PS_VDD_FAN_DISABLE (IN 21.4F>) → R109 0ohm 0402 COMMON 0.05 ohm → PS_VDD_FAN_DISABLE_R

R112 100k 1 % 0402 COMMON

R113 NS 100k 1 % 0402 NO STUFF

Q17 AO6800 SOT23_6D_1G1D1S COMMON (1G1D1S)

MAX_VOLTAGE=30V CONTINUOUS_CURRENT=3.4A R_DS_ON=100mohm@10V / 75mohm@4.5V / 115mohm@2.5V MAX_DUTY=100% MAX WATTAGE=1.15W V_BE_GS=12V

DEBUG HEADER

Default UART0_CTS/RTS to debug pins

DBG_GPIO1 → R61 0ohm 0402 COMMON → UART0_CTS (OUT 6.4D< 15.2A>)

DBG_GPIO2 → R68 0ohm 0402 COMMON 0.05 ohm → UART0_RTS (IN 6.4D< 15.1A<)

NS 0.05 ohm → R67 0ohm 0402 NO STUFF → DBG_UART0_RTS

DBG_UART0_CTS → R66 0ohm 0402 NO STUFF NS 0.05 ohm

R148 10k 0402 COMMON → NVJTAG_SEL (OUT 4.5D<)

R149 10k 0402 COMMON

DBG_GPIO3 → R137 0ohm 0402 COMMON → DBG_GPIO

R159 0ohm 0402 NO STUFF 0.05 ohm

Q22 SSM3J01N SOT-323 2D1G1S COMMON (1G1D1S)

MAX_VOLTAGE=25V CONTINUOUS_CURRENT=0.22A R_DS_ON=3265mohm@10V / 4000mohm@4.5V / 10000mohm@2.5V MAX_CURRENT=0.5A MAX WATTAGE=0.35W V_BE_GS=8V

J10 QSH-030-01-L-D-A-K-TR F_NORM F_NORM COMMON

Rev 1.0

1		2	
3	D_FORCE_AC_NOT_OK_N	4	
5	JTAG_AP_TDI	6	UART0_TXD_DBG_1V8 (IN 15.4A>)
7	JTAG_AP_TMS	8	UART0_RXD_DBG_1V8 (OUT 15.4D<)
9	JTAG_AP_TCK	10	DBG_UART0_CTS
11	JTAG_AP_RTCK	12	DBG_UART0_RTS
13		14	
15	JTAG_AP_TDO	16	DBG_GEN1_I2C_SCL
17	RESET_IN_R_L	18	DBG_GEN1_I2C_SDA
19		20	I2C_GP1_SCL
21	VDD_1V8	22	I2C_GP1_SDA
23	500HM_NETCLASS2	24	50OHM_NETCLASS2
25	500HM_NETCLASS2	26	VDD_1V8
27	UART4_TX_DBG	28	LED_VDD_CORE
29	UART4_RX_DBG	30	SNN_LED_VDD_CPU
31	LED_VDD_CORE	32	DBG_GPIO1
33	CPU_PWR_REQ	34	DBG_GPIO2
35		36	
37	DBG_KB_ROW0	38	DBG_IRQ_N
39	DBG_KB_ROW1	40	SYS_RST_IN_DBG_C (50OHM_NETCLASS2, TP2) → R97 0ohm → RESET_IN_R_L (IN 22.2A> 22.4C<> 22.5E> 33.3G<)
41	DBG_KB_ROW2	42	FORCE_RECOVERY_R_L (OUT 33.3G<)
43	DBG_KB_COL0	44	RESET_IN_R_L (OUT 22.2A> 22.4C<> 22.5F< 33.3G<)
45	DBG_KB_COL1	46	POWER_BTN_R (OUT 33.1G<)
47	DBG_KB_COL2	48	PM_VCC
49	DBG_KB_COL3	50	PM_BUS_SEL (OUT 15.4E<)
51		52	
53	DBG_JTAG_TRST	54	DBG_PM_I2C_SCL_3V3 (50OHM_NETCLASS2)
55	D_FORCE_OFF_R_I	56	DBG_PM_I2C_SDA_3V3 (50OHM_NETCLASS2)
57	DBG_GPIO3	58	
59	SNN_D_MFG_MODE_N	60	VAUX_5V
61		62	NV_NET_MAX_CURRENT=0.1A MIN_LINE_WIDTH=0.400
63		64	

R270 0ohm 0402 COMMON (ACOK)

R268, R269 0ohm 0402 DBG_PWR_I2C (I2C_PM_DAT, I2C_PM_CLK; PWR_I2C_SDA_D, PWR_I2C_SCL_D)

R85 0ohm 0.05 ohm 0402 COMMON (UART4_TX, UART4_RX)

R323 4.7k 5 % 0402 COMMON

R87 0ohm 0.05 ohm 0402 (18.4C<)

R91 0ohm 0402 DBG_PWR_I2C (18.4C<)

TP3, TP3, TP4, TP5, TP6

R111 0ohm 0402 FORCE_OFF (JTAG_AP_TRST_L, D_FORCE_OFF_L)

R106 0ohm 0402 DBG_PWR_I2C

R69 0ohm 0402 DBG_PWR_I2C → R71 0ohm 0402 DBG_PWR_I2C → I2C_GP0_CLK_1V8 (IN 4.3D> 10.4B> 10.5C< 17.2G< 18.3C<)

R73 0ohm 0402 NO STUFF → R75 0ohm 0402 NO STUFF → I2C_GP1_CLK_3V3 (BI 4.3D> 10.4B< 10.5C<> 17.2G<> 18.3C<>)

I2C_GP1_SDA → I2C_GP1_DAT_3V3 (BI 4.3D> 15.4E<> 16.2D<> 17.5A<> 21.2B<> 21.4D<> 22.5H<> 31.3B<> 32.3B<>)

R305 0ohm 0402 COMMON → VDD_3V3_SYS 3.3V

Gate option for GP1 to debug
Stuff R107/R108 for direct
Stuff R103/R110 for gate

R107 0ohm 0402 NO STUFF → I2C_GP1_CLK_3V3 (IN 21.4D> 22.4F< 31.3B<> 32.3B<> 17.5A> 21.2B<; BI 21.4D<> 22.4F<> 31.3B<> 32.3B<>)

R108 0ohm 0402 NO STUFF → I2C_GP1_DAT_3V3 (IN 4.3D<> 15.4E<> 16.2D< 17.5A> 21.2B<; BI 4.3D<> 15.4E<> 16.2D<> 17.5A<> 21.2B<)

R103 0ohm 0402 COMMON → DBG_PM342_I2C_SCL_3V3 (IN 15.4G<>)

R110 0ohm 0402 COMMON → DBG_PM342_I2C_SDA_3V3 (IN 15.4G<>, BI 15.4G<>)

50OHM_NETCLASS2

ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	FAN AND DEBUG

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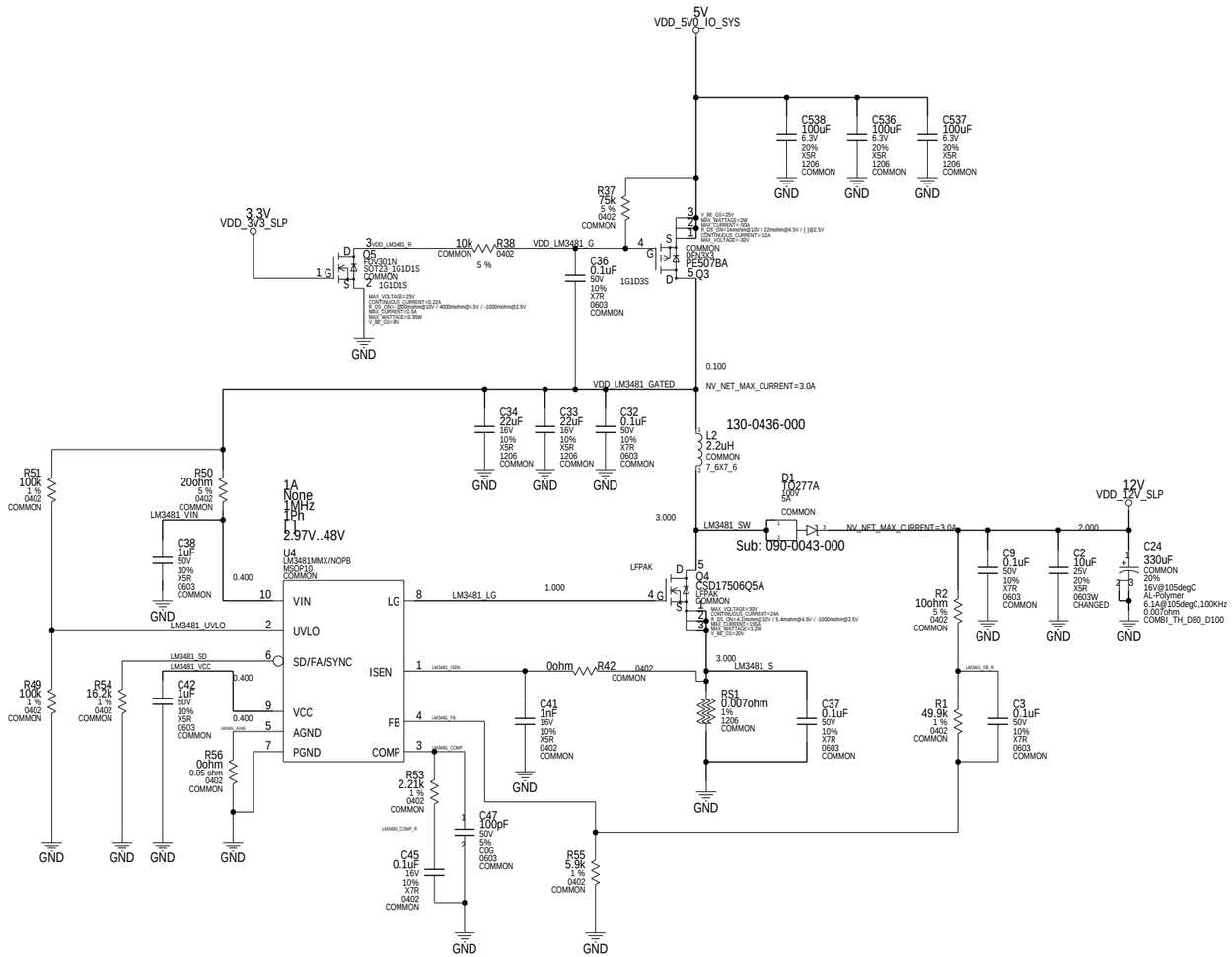

ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	12V BOOST

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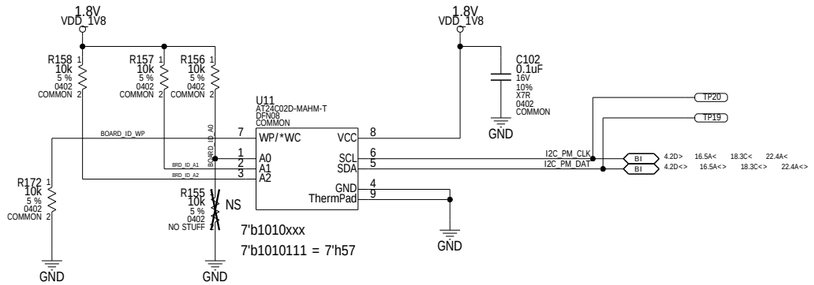
Carrier board config



ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	EEPROM

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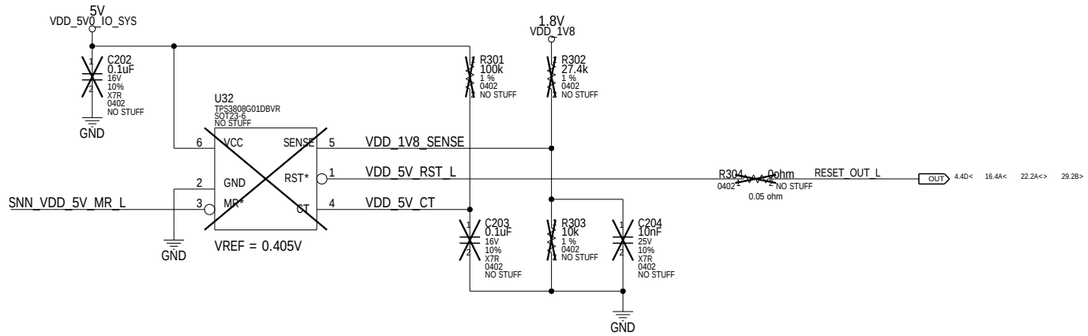

ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	Supervisor

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ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	BLANK

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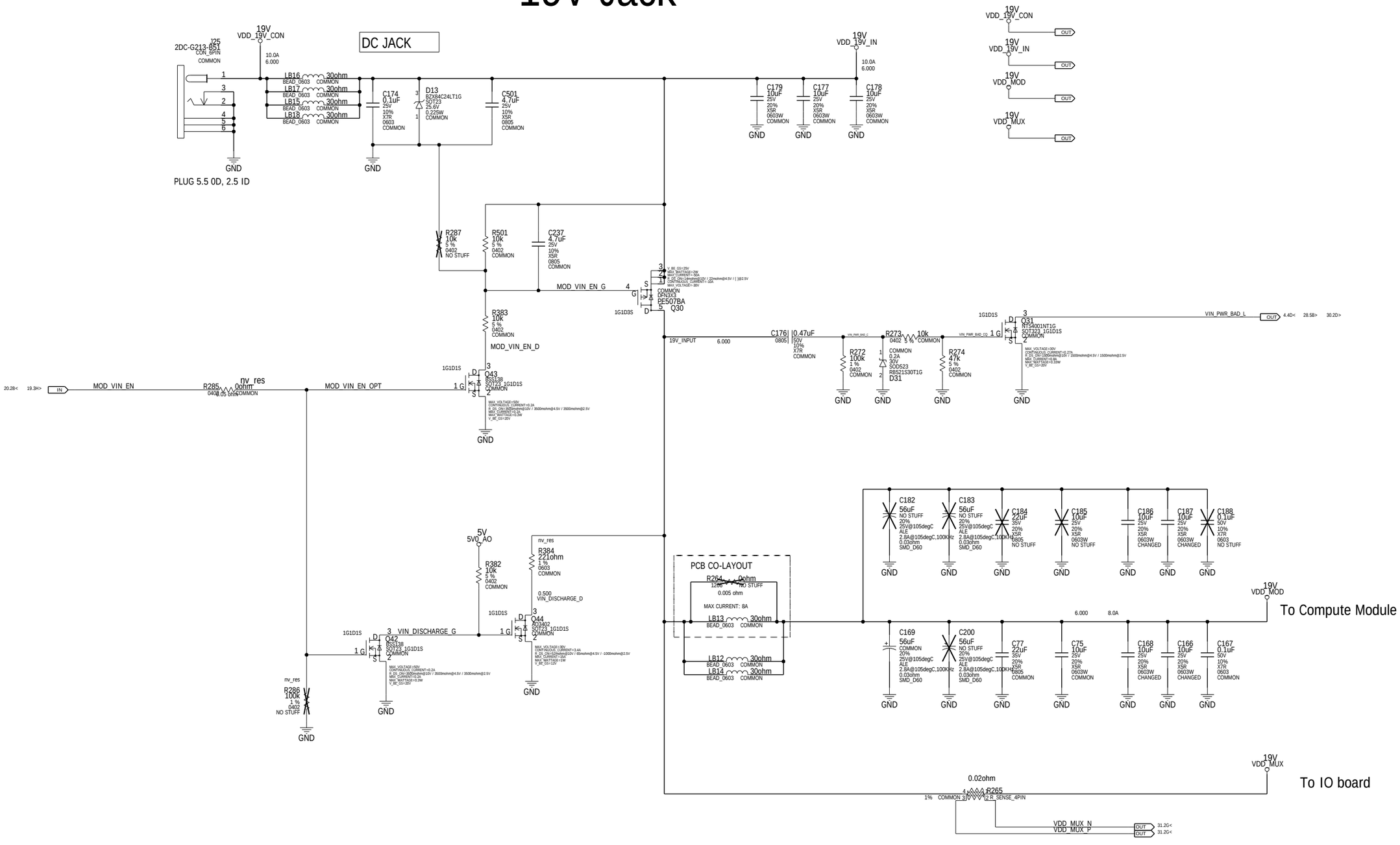
19V Jack



ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	DC Jack

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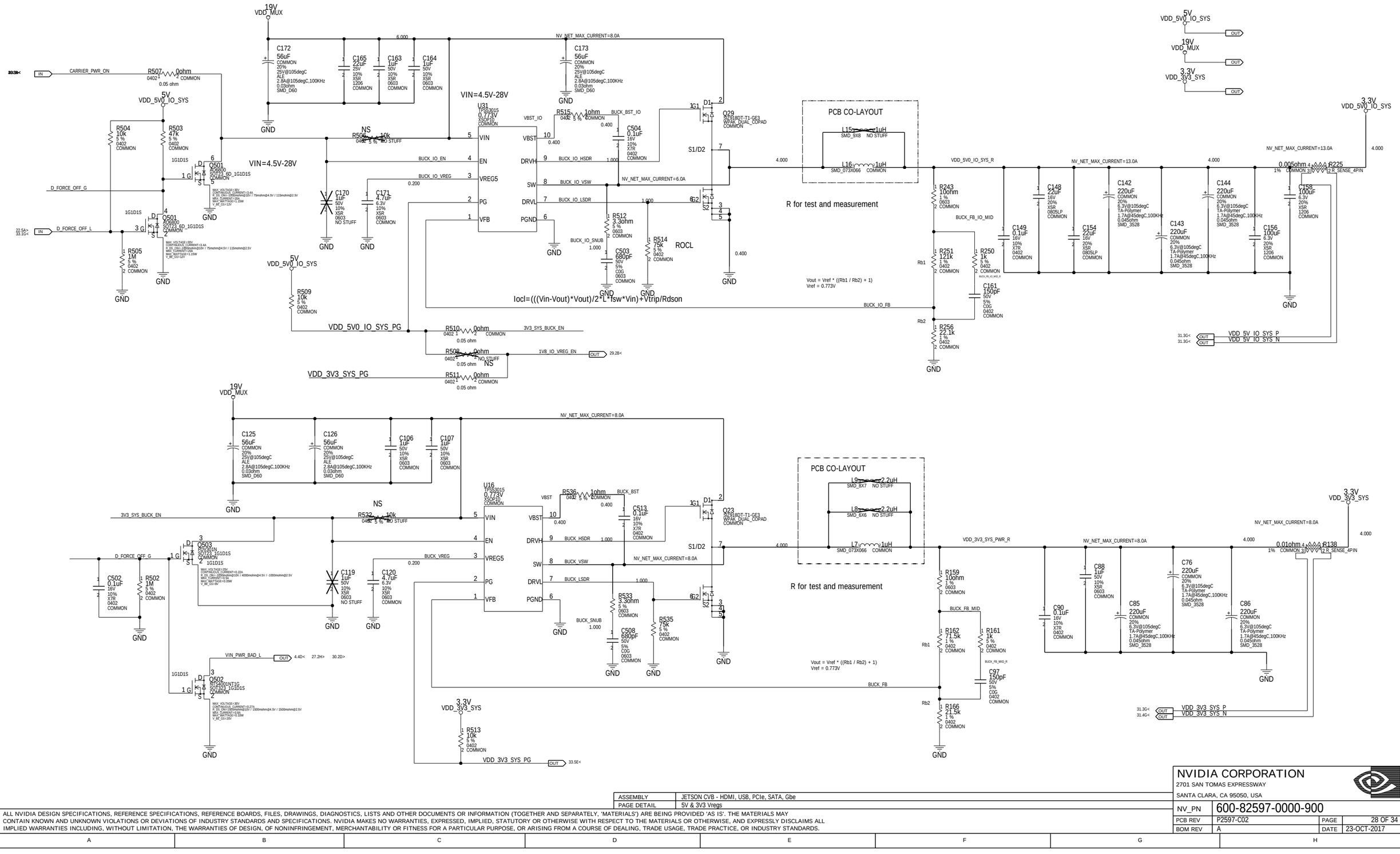
5V & 3V3 SYS POWER SUPPLIES



ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	5V & 3V3 Vregs

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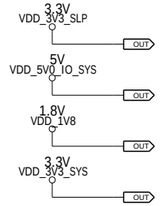
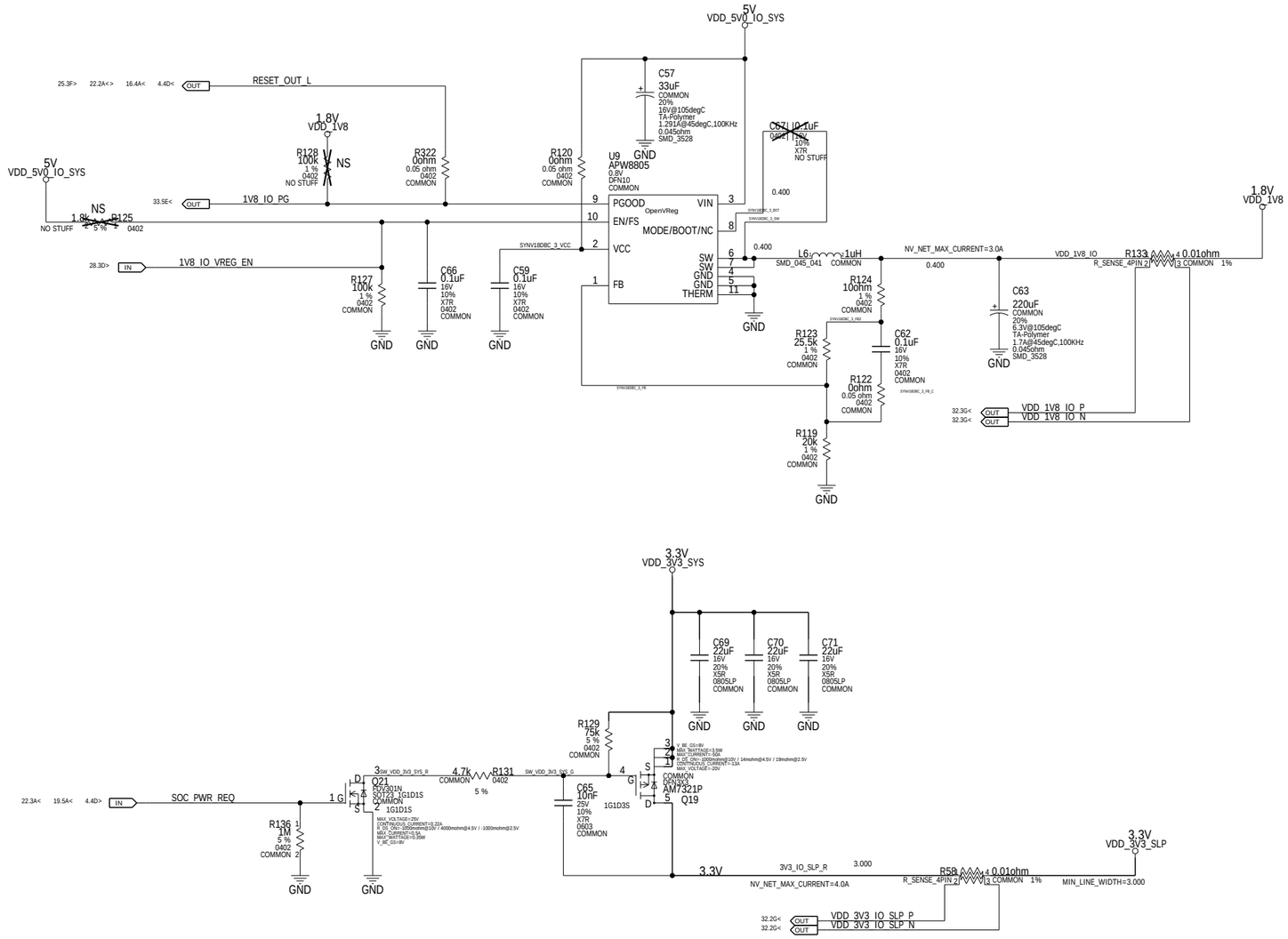
1V8 POWER SUPPLY AND 3V3_SYS





ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	3V3 SLP AND 1.8V Vregs

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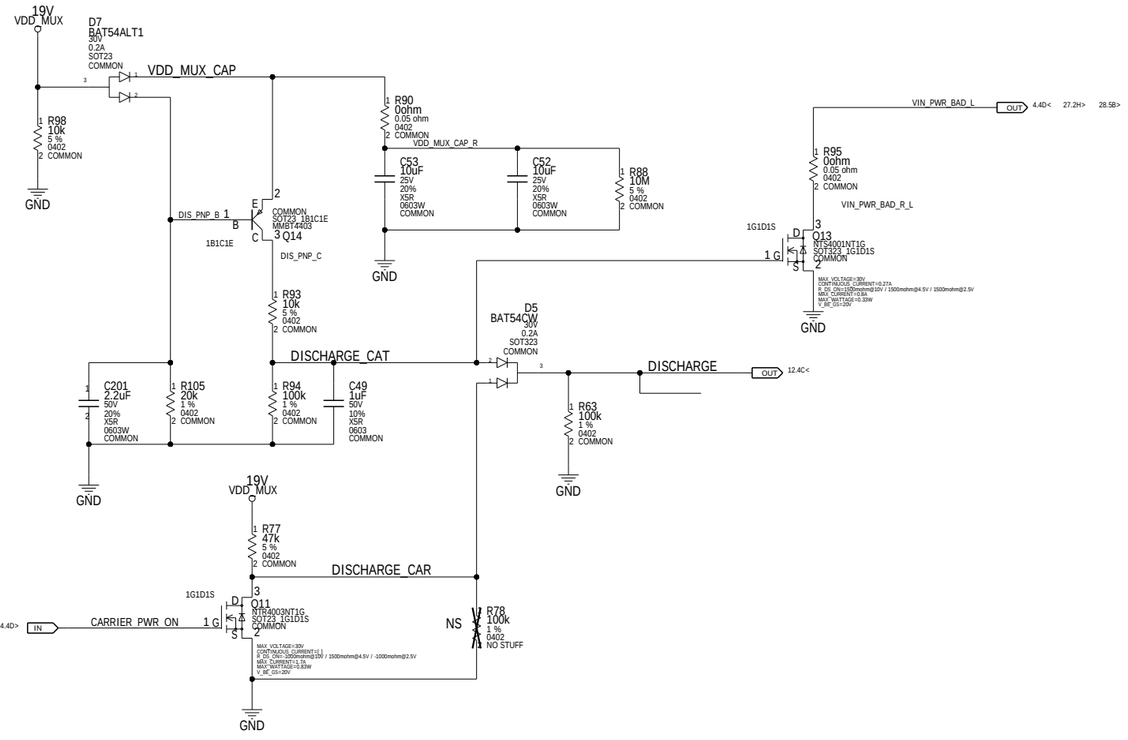
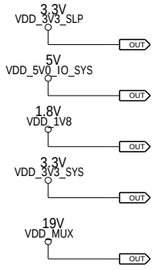
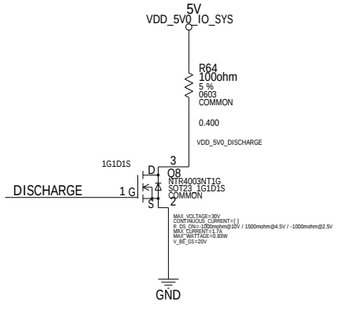
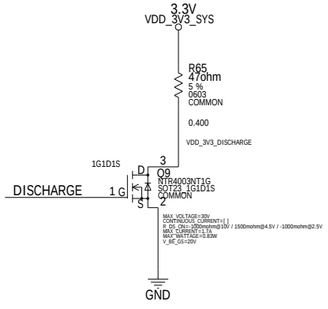
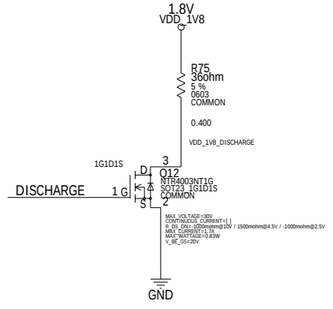
RAIL DISCHARGE

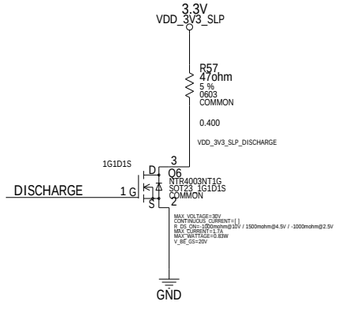












ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	Rail Discharge

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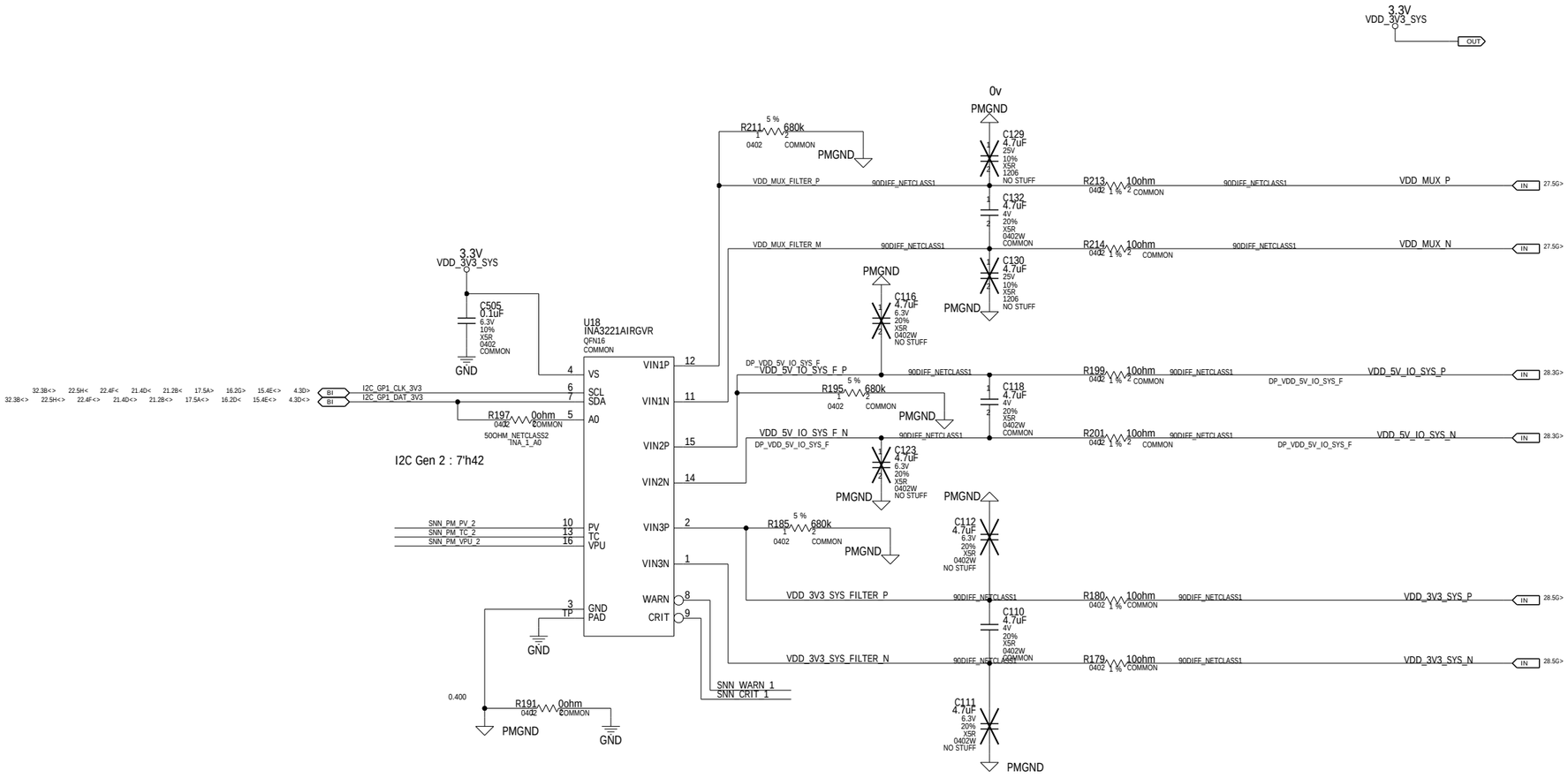
POWER MONITORS I



DC JACK to IO board

5V SYSTEM

3V3 SYSTEM

ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	Power Monitor I

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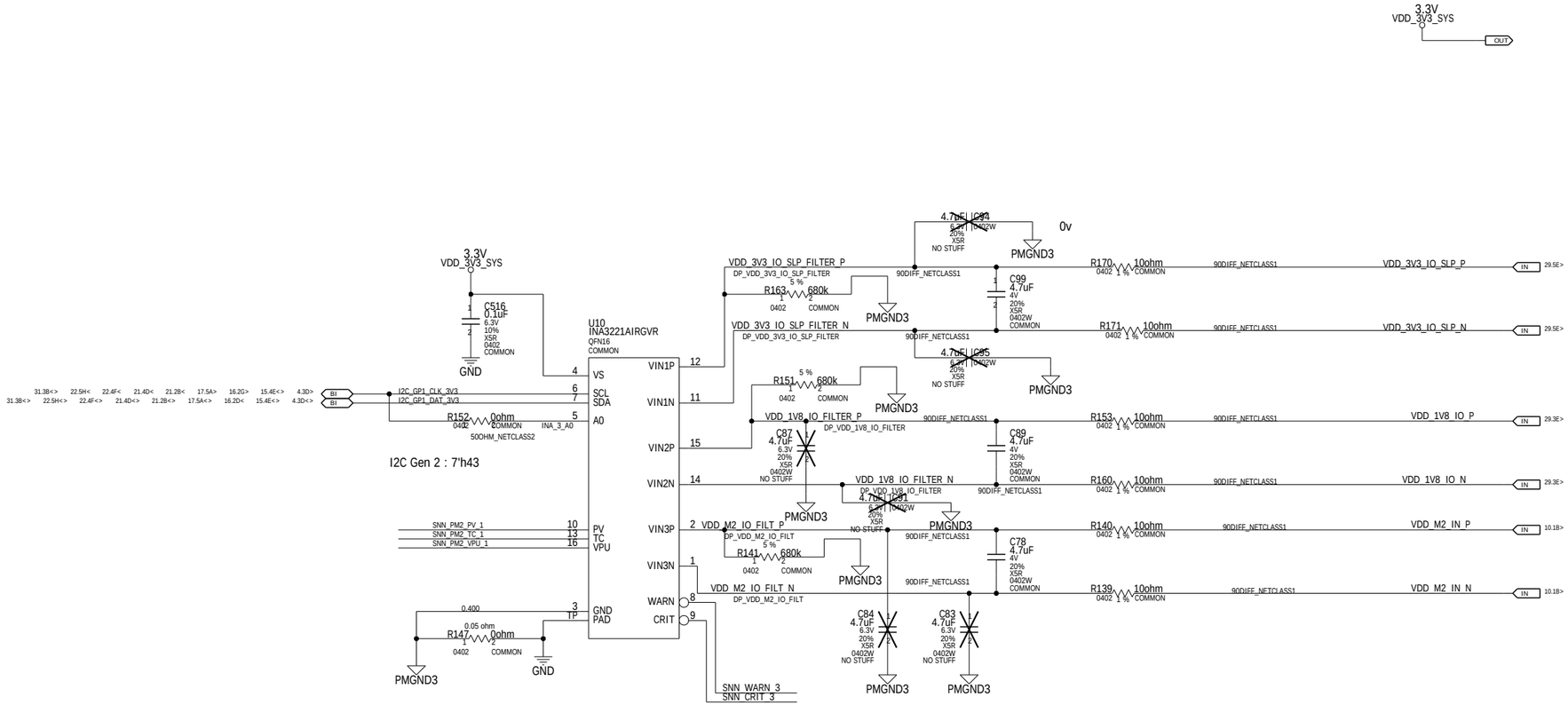
POWER MONITORS II



3V3 RUN RAIL

1.8V SYSTEM

M.2 3.3V

ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	Power Monitor II

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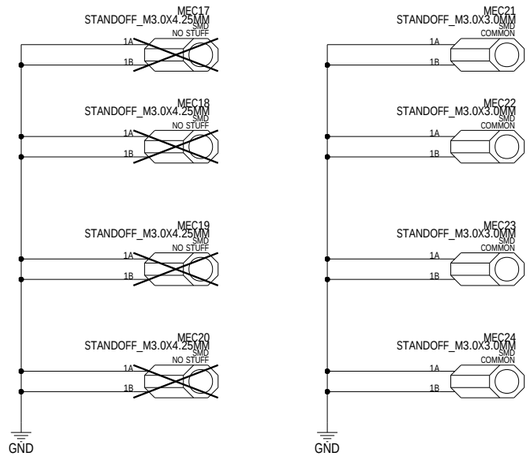
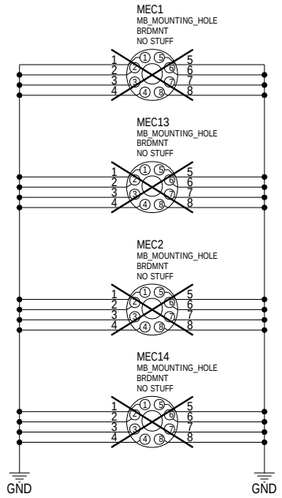
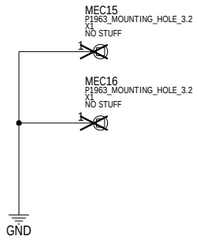
MODULE MOUNTING STANDOFFS
Top Side Botseltom Side

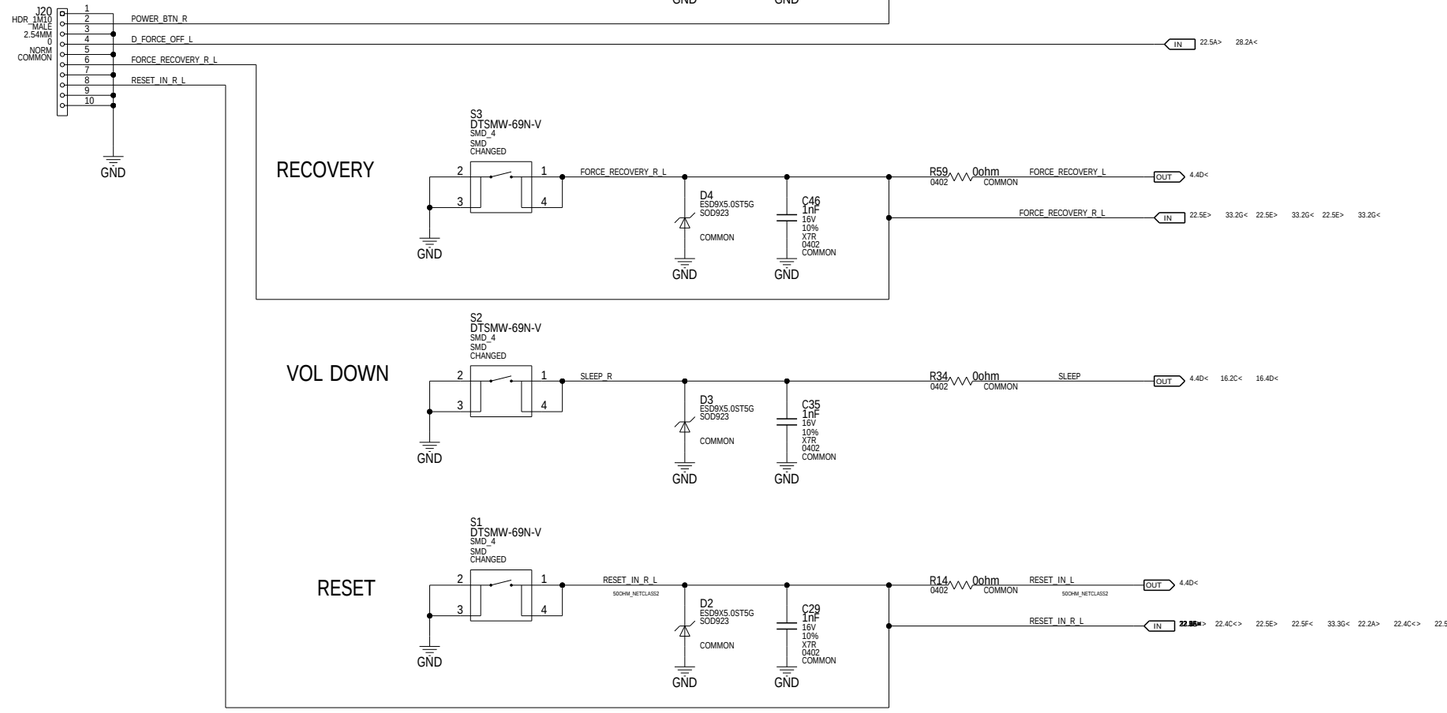


FOUR CORNER
miniITX MOUNTING HOLES

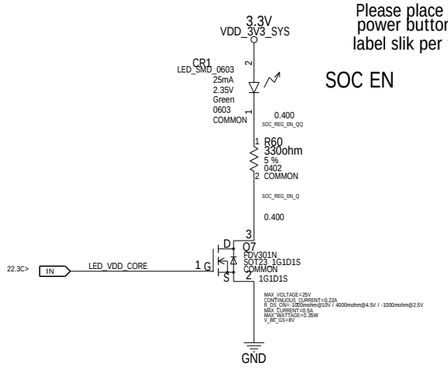


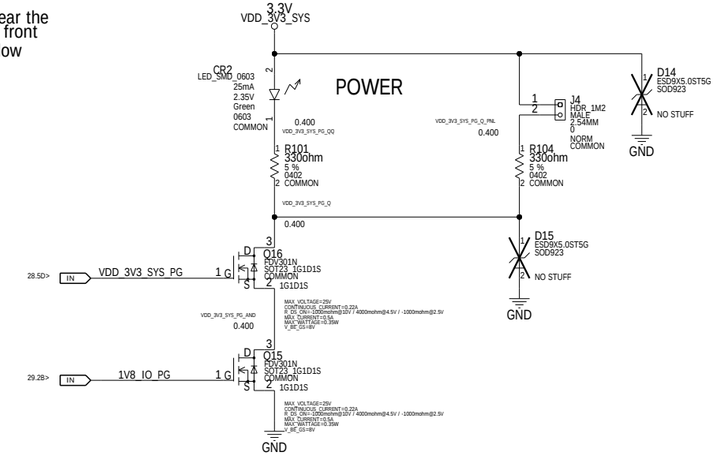
Antenna bracket mount





CAD NOTE:
Please place LEDs near the power button in the front label slik per text below





ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	Buttons and Mechanical

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Revision History

P2597-B03

Page 4: Added a red LED to indicate power is active on the CVM
Page 8: Replaced U21 due to EOL on previous part
Page 9: Changed an unused pull up to a TVS device on PCIe RST
PCIE_WAKE_L and PCIE_CLKREQ
Page 10: Change R524 and R538 to 1.8k (tune for gyro bypass)
Page 10: Changed M.2 I2C to 1.8v
Page 12: Added discharge for VDD_5V0_IO_SLP and VDD_12V_SLP
Added a red LED to 12v at PCIe connector
Changed DEV_SLP buffer to OD
Page 13: Changed R9 to 100pF cap C205 (EU emissions)
Page 14: Changed R548 to 4.7k ohm and R544 to 100k
Page 15: Changed DBG I2C MUX to I2C repeater with enable
Added pull ups on inputs to U6
Page 16: Added 1206 0ohm resistors on J26
Added pull downs on J21 side of U22 and U7
Added reset connection to U22 and U7
Added ESD protection
Page 22: Added pull-up on J10 pin 48 for direct INA support
Added 0ohm resistor on the fan PWM to allow always on
Added a pull down on UART4_TX
Added ESD protection to pins 4 and 6 of Q17
Page 24: Changed U11 EEPROM to AT24C02D-MAHM-T
Page 25: Added supervisor to hold Tegra in reset until 1.8v up
Page 27: Added additional bulk site on VDD_MOD
Page 28: Changed 5v and 3.3v VR FETs for better thermal perf
Page 30: Added C201 and changed C49 to 1uF to filter DC loss
Page 33: Added ESD option for power LED

P2597-B04

Corrected minor solderpaste issue
Page 12: Stuffed R315
Page 14: Changed R563 and R565 to 3.3ohm
Page 25: Unstuffed page

BOM rev B

Page 23: Changed C36 to 0.1uF
Page 30: Changed C201 to 2.2uF and R105 to 20k

P2597-C00

Page 13: Changed ENET CM Cap on transformer pirmary side from one shared to indiviual caps
Page 14: Changed HDMI ESD diode to a package with footprint compatible parts
Page 19: Added ON/OFF supervisor ckt to accomdate both AutoPMIC & MobilePMIC On/Off control
Page 20: Added ON/OFF Glue logic to accomdate both AutoPMIC & MobilePMIC On/Off control

P2597-C01

Page 12: Changed SATA to right angle connetor to remove interference with PCIe card
Page 19: Add seperate delay path for CARRIER_PWR_ON to allow power cycle on RESET
Add option for ON/OFF PB or INT to drive WAKE to allow short POWER_BTN press to wake module
Add logic qualifier to INT for DFF to WAKE not power down on PB press in SLEEP
Page 20: Add logic qualifier to gate initial momentary pulse in state mode to remove state PWR_ON glitch
Page 33: Changed 1x2 headers for buttons to 1x10 header, so customer won't poke finger on header while accessing buttons

ASSEMBLY	JETSON CVB - HDMI, USB, PCIe, SATA, Gbe
PAGE DETAIL	REVISION HISTORY

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