KYUNGWOOK CHANG

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RESEARCH INTERESTS

CAD Solutions for Physical Design Challenges:
In-depth studies (Ph.D.) on CAD solutions for low-power 3D ICs and power-delivery/thermal challenges

Artificial Intelligence:
Hardware acceleralation solutions for deep neural network

Design and Technology Co-Optimization:
Broad experience on hardware architecture, physical design, PDK in advanced technologies

Physical/Logic Design and Analysis:
Expertise in RTL design, synthesis, P&R, verification, and analysis on timing/power and power-supply/thermal-integrity

EDUCATION

Georgia Institute of Technology — **Atlanta, GA**
Ph.D. in Electrical and Computer Engineering, GPA: 4.0 / 4.0 — *2014–2019*
Thesis: "Design and Tool Solutions for Energy-efficient Reliable Monolithic 3D ICs"

Seoul National University — **Seoul, South Korea**
M.S. in Electrical Engineering and Computer Science, GPA: 4.12 / 4.30 — *2007–2010*
Thesis: "Memory-Centric Communication Architecture for Reconfigurable Computing"

Seoul National University — **Seoul, South Korea**
B.S. in Electrical Engineering, GPA: 3.74 / 4.30 — *2003–2007*

RESEARCH/WORK EXPERIENCE

Apple Inc. — **Austin, TX**
SEG-CAD & CSG — *2019–Present*

Graduate Research Assistant, Georgia Institute of Technology — **Atlanta, GA**
Georgia Tech Computer Aided Design Laboratory (Advisor: Dr. Sung Kyu Lim) — *2014–2019*
Physical design and tool solutions for low-power and reliable 3D ICs
- Physical design flow development for 3D ICs
- Analysis and physical design solutions for low-power 3D ICs in advanced technology nodes
- Design methodologies for deep neural network 3D ICs
- Analysis and optimization methodologies of power delivery network of 3D ICs
- Temperature-aware timing analysis and optimization for 3D ICs

R&D Intern, Arm Inc. — **Austin, TX**
Research Group — *2015–2016*
Analysis and physical design solutions for M3D (monolithic 3D) ICs on Arm cores
- Analysis on power benefits of M3D ICs on Arm cores
- Physical design solutions to improve power-supply integrity of M3D ICs
- Physical design flow development for M3D ICs

Associate Research Engineer, MtekVision Co., Ltd. — **Seongnam, South Korea**
SoC Design Lab., AP Team — *2010–2013*
Application processor (AP) logic design
- High-speed serial interface development between AP and modem
- Long MP3 playtime audio system development using Tensilica DSP
- Hardware and software solutions for voice recognition

Gradudate Research Assistant, Seoul National University — **Seoul, South Korea**
Design Automation Laboratory (Advisor: Dr. Kiyoung Choi) — *2007–2009*
Hardware and software architecture of coarse-grained reconfigurable architecture (CGRA)
- Software solutions for control-intensive kernels in CGRA
- Hardware/software solutions for floating-point operations in CGRA
- Architectural solutions for high-bandwidth memory system for CGRA
- Compiler development for CGRA

TEACHING EXPERIENCE

Teaching Assistant, Georgia Institute of Technology **Alanta, GA**
School of Electrical and Computer Engineering
– Physical Design Automation of VLSI Systems *Spring, 2018*
– Architecture, Concurrency, and Energy in Computation *Summer, 2016*

Teaching Assistant, Seoul National University **Seoul, South Korea**
Department of Electrical Engineering and Computer Science
– Introduction to Computer-Aided Design *Fall, 2008*
– Digital Logic Design and Lab *Fall, 2007*

PUBLICATIONS

Journals

[1] K. Chang, S. Das, S. Sinha, *et al.*, "System-Level Power Delivery Network Analysis and Optimization for Monolithic 3D ICs," *IEEE Trans. on Very Large Scale Integration Systems*, no. 4, pp. 888–898, 2019.

[2] K. Chang, D. Kadetotad, Y. Cao, *et al.*, "Power, Performance, and Area Benefit of Monolithic 3D ICs for On-Chip Deep Neural Networks Targeting Speech Recognition," *ACM Journal on Emerging Technologies in Computing Systems*, vol. 14, no. 4, 42:1–42:19, 2018.

[3] K. Chang, K. Acharya, S. Sinha, *et al.*, "Impact and Design Guideline of Monolithic 3-D IC at the 7-nm Technology Node," *IEEE Trans. on Very Large Scale Integration Systems*, vol. 25, no. 7, pp. 2118–2129, 2017.

[4] B. W. Ku, K. Chang, and S. K. Lim, "Compact-2D: A Physical Design Methodology to Build Two-Tier Gate-Level 3D ICs," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, (Under Review).

[5] K. Chang, S. Sinha, B. Cline, *et al.*, "Design-Aware Partitioning-Based 3D IC Design Flow with 2D Commercial Tools," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, (Under Review).

Conferences

[1] B. W. Ku, K. Chang, and S. K. Lim, "Compact-2D: A Physical Design Methodology to Build Commercial-Quality Face-to-Face-Bonded 3D ICs," in *Proc. Int. Symp. on Physical Design*, 2018.

[2] K. Chang, S. Pentapati, D. E. Shim, *et al.*, "Road to High-Performance 3D ICs: Performance Optimization Methodologies for Monolithic 3D ICs," in *Proc. Int. Symp. on Low Power Electronics and Design*, 2018.

[3] K. Chang, S. Das, S. Sinha, *et al.*, "Frequency and Time Domain Analysis of Power Delivery Network for Monolithic 3D ICs," in *Proc. Int. Symp. on Low Power Electronics and Design*, 2017.

[4] K. Chang, D. Kadetotad, Y. Cao, *et al.*, "Monolithic 3D IC Designs for Low-Power Deep Neural Networks Targeting Speech Recognition," in *Proc. Int. Symp. on Low Power Electronics and Design*, 2017.

[5] K. Chang, A. Koneru, K. Chakrabarty, *et al.*, "Design Automation and Testing of Monolithic 3D ICs: Opportunities, Challenges, and Solutions: (Invited Papaer)," in *Proc. Int. Conf. on Computer-Aided Design*, 2017.

[6] K. Chang, B. W. Ku, S. Sinha, *et al.*, "Full-Chip Monolithic 3D IC Design and Power Performance Analysis with ASAP7 Library: (Invited Paper)," in *Proc. Int. Conf. on Computer-Aided Design*, 2017.

[7] K. Acharya, K. Chang, B. W. Ku, *et al.*, "Monolithic 3D IC Design: Power, Performance, and Area Impact at 7nm," in *Proc. Int. Symp. on Quality Electronic Design*, 2016.

[8] K. Chang, S. Sinha, B. Cline, *et al.*, "Cascade2D: A Design-Aware Partitioning Approach to Monolithic 3D IC with 2D Commercial Tools," in *Proc. Int. Conf. on Computer-Aided Design*, 2016.

[9] K. Chang, S. Sinha, B. Cline, *et al.*, "Match-Making for Monolithic 3D IC: Finding the Right Technology Node," in *Proc. Design Automation Conf.*, 2016.

[10] K. Chang, K. Acharya, S. Sinha, *et al.*, "Power Benefit Study of Monolithic 3D IC at the 7nm Technology Node," in *Proc. Int. Symp. on Low Power Electronics and Design*, 2015.

[11] G. Lee, K. Chang, and K. Choi, "Automatic Mapping of Control-Intensive Kernels onto Coarse-Grained Reconfigurable Array Architecture with Speculative Execution," in *Proc. Int. Symp. on Parallel Distributed Processing, Workshops and Phd Forum*, 2010.

[12] K. Chang and K. Choi, "Memory-Centric Communication Architecture for Reconfigurable Computing," in *Reconfigurable Computing: Architectures, Tools and Applications*, 2010.

[13] M. Jo, G. Lee, K. Chang, *et al.*, "Coarse-Grained Reconfigurable Architecture for Multiple Application Domains: A Case Study," in *Proc. Int. Conf. on Hybrid Information Technology*, 2009.

[14] K. Chang and K. Choi, "Mapping Control Intensive Kernels onto Coarse-Grained Reconfigurable Array Architecture," in *Proc. Int. SoC Design Conf.*, 2008.

Patents

[1] S. P. Sinha, R. C. Aitken, B. T. Cline, *et al.*, "Using Inter-Tier Vias in Integrated Circuits," pat. US9929149B2, 2018.

[2] S. P. Sinha, K. Chang, B. T. Cline, *et al.*, "Method for Generating Three-Dimensional Integrated Circuit Design," pat. US20180060475A1, 2018.

[3] K. Y. Choi, K. Chang, and J. K. Paek, "Memory-Centered Communication Apparatus in a Coarse Grained Reconfigurable Array," pat. US8949550B2, 2015.

SKILLS

(Highly proficient skills are highlighted with underline)
EDA/CAD Tools: Cadence{Innovus/Encounter, Tempus, Voltus, Virtuoso, Genus/RTL Compiler, Liberate}, Synopsys{Design Compiler, PrimeTime, SiliconSmart}, Mentor Graphics Calibre, Ansys Redhawk

Design/Simulation Tools: Mentor Graphics ModelSim, Cadence{Incisive, Spectre}, Synopsys HSPICE, Arm SoC Designer, MATLAB, Ansys Fluent

Verification Tools: Cadence Conformal, Synopsys {Synplify, Formality, SpyGlass}, Xilinx ISE, Lauterbach TRACE32

Programming Languages: C/C++, Verilog, VHDL, Tcl/Tk, Perl, Java, SystemVerilog, SystemC, Python, Shell Script

SELECTED AWARDS AND HONORS

The President's Award for 21st Century's Most Leading Talented People *2003*
Grantor: The President of the Republic of Korea

Korea Olympiad in Informatics (Algorithm), Bronze Medal *2002, 1996*
Grantor: Ministry of Science, ICT and Future Planning

References

Dr. Sung Kyu Lim
Dan Fielder Endowed Chair Professor
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Georgia Institute of Technology
Atlanta, GA
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Dr. Saurabh Sinha
Staff Research Engineer
Arm Inc.
Austin, TX
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Dr. Kiyoung Choi
Full Professor
Department of ECE
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