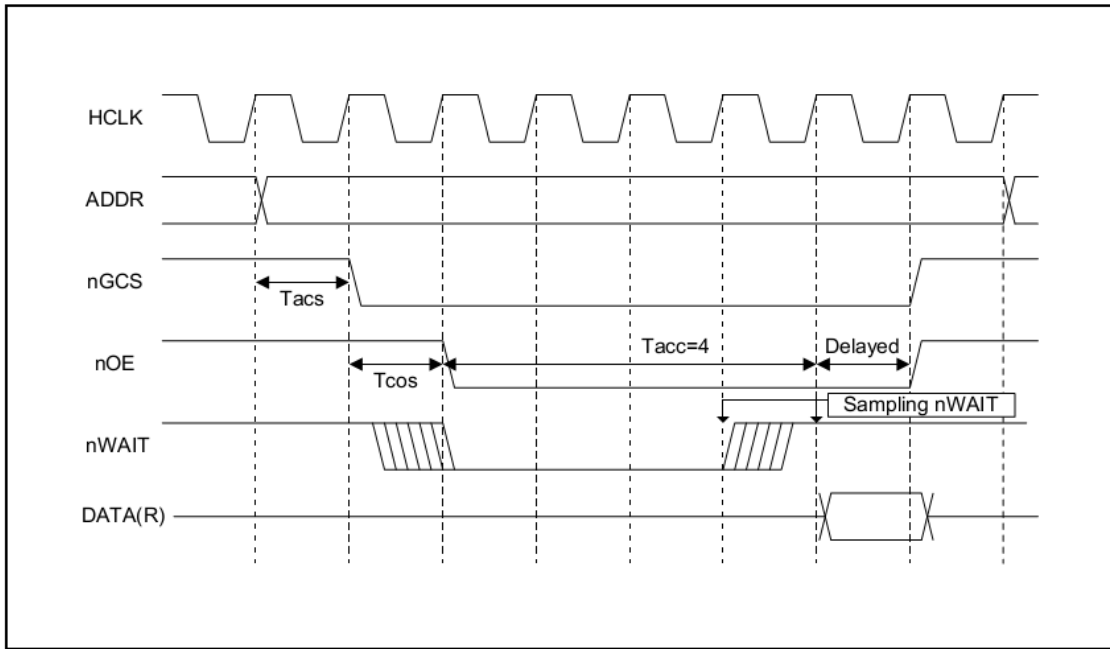
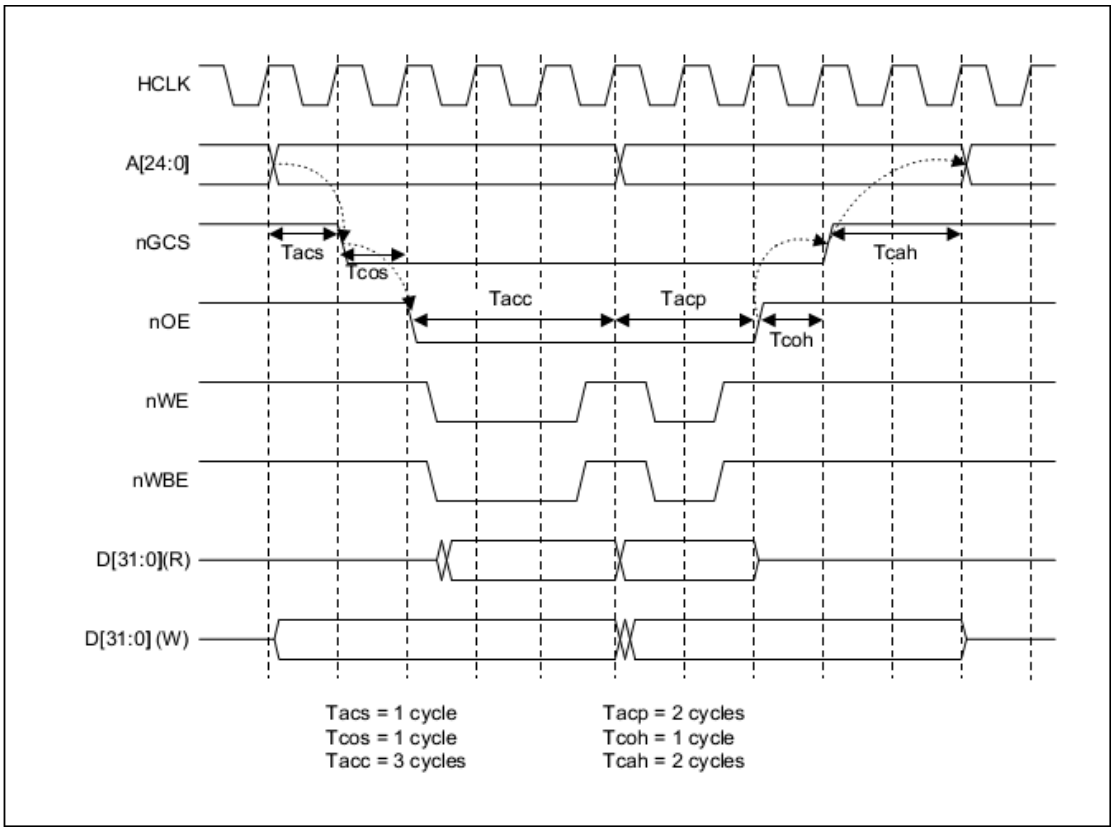
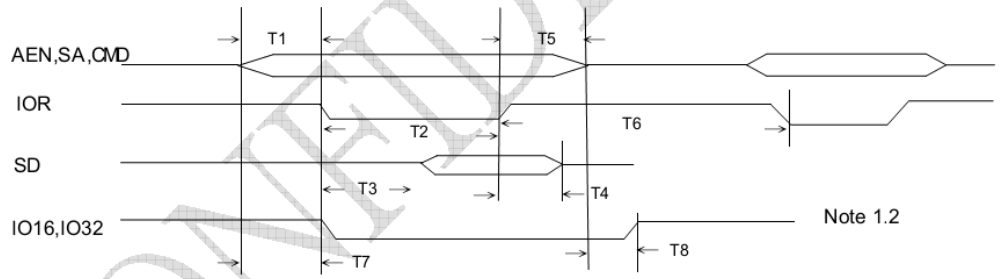

HCLK
ADDR
nGCS
Tacs
nOE
Tcos
Tacc=4
Delayed
Sampling nWAIT
nWAIT
DATA(R)


HCLK
A[24:0]
nGCS
Tacs
Tcos
Tacc
Tacp
Tcah
nOE
Tcoh
nWE
nWBE
D[31:0](R)
D[31:0] (W)
Tacs = 1 cycle
Tcos = 1 cycle
Tacc = 3 cycles
Tacp = 2 cycles
Tcoh = 1 cycle
Tcah = 2 cycles

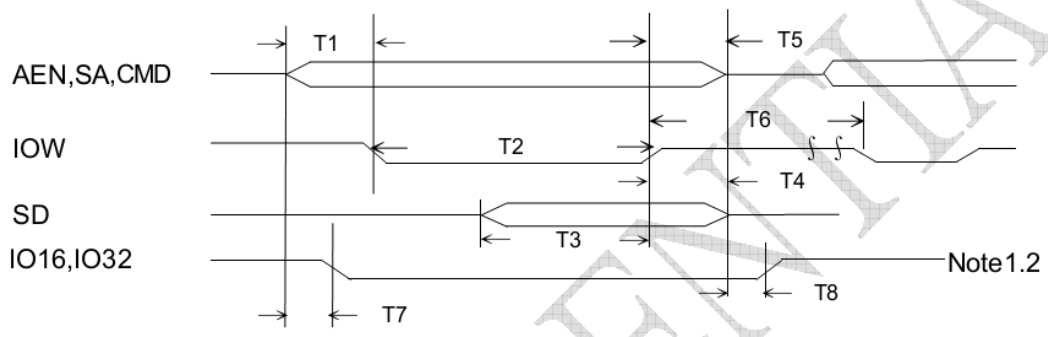
BANKCONn	Bit	Description	Initial State
Tacs	[14:13]	Address set-up time before nGCSn 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	00
Tcos	[12:11]	Chip selection set-up time before nOE 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	00
Tacc	[10:8]	Access cycle 000 = 1 clock 001 = 2 clocks 010 = 3 clocks 011 = 4 clocks 100 = 6 clocks 101 = 8 clocks 110 = 10 clocks 111 = 14 clocks Note: When nWAIT signal is used, Tacc ≥ 4 clocks.	111
Tcoh	[7:6]	Chip selection hold time after nOE 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	000
Tcah	[5:4]	Address hold time after nGCSn 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	00
Tacp	[3:2]	Page mode access cycle @ Page mode 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = 6 clocks	00
PMC	[1:0]	Page mode configuration 00 = normal (1 data) 01 = 4 data 10 = 8 data 11 = 16 data	00

10.4.3 Processor Register Read Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T_1	System address valid to IOR valid	5			ns
T_2	IOR width	22			ns
T_3	SD Setup time			10	ns
T_4	IOR invalid to SD invalid			4	ns
T_5	IOR invalid to system address invalid	5			ns
T_6	IOR invalid to next IOR valid （access DM9000）	80			ns
T_7	System address valid to IO16,IO32 valid			5	ns
T_8	System address invalid to IO16, IO32 invalid			5	ns

10.4.4 Processor Register Write Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
T_1	System Address Valid to IOW Valid	5			ns
T_2	IOW Width	22			ns
T_3	SD Setup Time	22			ns
T_4	SD Hold Time	5			ns
T_5	IOW Invalid to System Address Invalid	5			ns
T_6	IOW Invalid to Next IOW validaccess DM9000）	84			ns
T_7	System Address Valid to IO16, IO32 Valid			5	ns
T_8	System Address Invalid to IO16, IO32 Invalid			5	ns