SD Specifications
Part 1
UHS-II Simplified Addendum

Version 1.02

May 28, 2014

Addendum to:

SD Specifications
Part 1 Physical Layer Simplified Specification
Version 4.10 January 22, 2013, or later

Technical Committee
SD Card Association

Revision History

Date	Version	Changes compared to previous issue
November 8, 2013	1.01	The first release of UHS-II Simplified Addendum (Created by the UHS-II Addendum Version 1.01)
May 28, 2014	1.02	Fixed Section number from 3.2 to 3.5

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Conventions Used in This Document

Naming Conventions

- Some terms are capitalized to distinguish their definition from their common English meaning. Words not capitalized have their common English meaning.

Numbers and Number Bases

- Hexadecimal numbers are written with a lower case "h" suffix, e.g., FFFFh and 80h.
- Binary numbers are written with a lower case "b" suffix (e.g., 10b).
- Binary numbers larger than four digits are written with a space dividing each group of four digits, as in 1000 0101 0010b.
- All other numbers are decimal.

Key Words

- May: Indicates flexibility of choice with no implied recommendation or requirement.
- Shall: Indicates a mandatory requirement. Designers shall implement such mandatory requirements to ensure interchangeability and to claim conformance with the specification.
- Should: Indicates a strong recommendation but not a mandatory requirement. Designers should give strong consideration to such recommendations, but there is still a choice in implementation.

Application Notes

Some sections of this document provide guidance to the host implementers as follows:

Application Note:
This is an example of an application note.

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1. General

This Simpliied Addendum defines an additional category to the Part 1 Physical Layer Simplified Specification Version 4.10. The following sections describe additional and modified parts of the base specification for this new category.

Key background factors behind Ultra High Speed Type II (UHS-II) Specification are shown below:

- **High speed interface is required to handle large volumes of HD (High Definition) contents**
  In recent years, the number of SD-applications which handle large amount of data is increasing steadily with an increase in HD (High Definition) contents (HD, Super-HD, 3D-TV, etc.). At the same time, the data size of HD contents is also increasing year by year.
  UHS-II is necessary to meet the ultrahigh-speed requirement to handle HD contents and farther large-capacity contents in the future.

- **Interface should be widely available for many kinds of hosts**
  It is difficult to keep signal integrity at high-speed data transfer especially for mobile devices. Generally, board design of hosts becomes more difficult with high speed interface. UHS-II should be considered both high-speed and availability for many kinds of hosts.

- **Reusability of legacy resource (IPs, software, etc.) is important for host development**
  Hosts require the compatibility with legacy protocol for their efficient development.
  For example, in SD protocol, preserving the SD legacy infrastructures (CMD, RES, States, Status, Errors, etc.) provides efficient development with SD hosts, and this leads to a speedy expansion of UHS-II applications.

- **Interoperability and compatibility to Legacy SD I/F is important to avoid market confusion**
  Hosts and Devices require also the interoperability and compatibility with Legacy SD cards installed based to enable UHS-II specifications to be smoothly adopted by the market.

- **Low voltage, low power consumption and low EMI are needed for mobile devices**
  To apply new high-speed interface to many kinds of mobile devices, it is important to realize low power consumption and low EMI.
  Some low power and low EMI techniques need to be considered for UHS-II.

- **Multiple device connectivity for minimizing the number of ports and circuit size is required**
  Multi device connectivity is required to reduce the number of ports and circuit size for lower developing cost.

System features of UHS-II Specification based on the background are described in the next chapter.

2. System Features

From background factors mentioned in Chapter 1, the features of UHS-II are defined as follows:

(1) High speed interface up to 312MB/s
(2) Easy implementation for whole system
(3) Compatibility with Legacy SD interface
(4) Ensuring effective performance of data transfer
(5) Low voltage, low power consumption, low EMI
(6) Multiple device connectivity

The followings are additional explanations for system features.

- Interface speed
  (1) Full Duplex mode (abbreviated to "FD mode"): data rate from 39MB/sec to 156MB/sec in the specifications and up to double the throughput in the future.
  (2) Half Duplex with 2 Lanes mode (abbreviated to "2L-HD mode"): data rate from 78MB/sec to 312MB/sec in the specifications and up to double the throughput in the future.
  (3) Interface speed is continuously variable.
  (4) Infrastructure for additional Lanes is defined as follows, allowing future bit rate expansion. (Refer to Section 3.1 for the definition of downstream or upstream.)
    - Full Duplex with 2 Downstream and 1 Upstream Lanes mode (abbreviated to "2D1U-FD mode")
    - Full Duplex with 1 Downstream and 2 Upstream Lanes mode (abbreviated to "1D2U-FD mode")
    - Full Duplex with 2 Downstream and 2 Upstream Lanes mode (abbreviated to "2D2U-FD mode")
- Layering architecture
  (1) The system is divided into at least 4 layers, Mechanical, Physical, Link and Transaction.
  (2) Application specific layer can be introduced as a bridge between UHS-II common Transaction layer and the application.
- Legacy SD compatibility (for Card form factor)
  (1) Host and Device shall support Legacy SD I/F for ensuring fully backward compatibility.
  (2) Encapsulation of Legacy SD Format for Software Compatibility.
- Easy expansion for advanced features in the future
  (1) CMD Queuing: Another arbitrary command can be issued during some transaction.
  (2) Relaxed Ordering: Transaction order can be rearranged with reference to priority or processing speed.
  (3) Inter-device Communication: Some Device (called "CMD issuable Device") allows issuing commands and directly communicating to other Device.

3. UHS-II System Concept

In this chapter, the overall of UHS-II interface and system are described. UHS-II Card (or simply Card) denotes an SD memory card which supports UHS-II interface.

3.1 Interface Speed

UHS-II interface consists of at least two Lanes based on two differential signaling lines. Each Lane provides up to 156MB/sec.

Basically, direction of both Lanes is opposite each other, that is, one is from Host to Device (downstream) and the other is from Device to Host (upstream). This mode is defined as Full Duplex mode (abbreviated to "FD mode").

It is possible that both Lanes are set to transfer data in the same directions. In that case, overall interface speed is doubled up to 312MB/sec (twice as high as FD mode). This status is defined as Half Duplex with 2 Lanes mode (abbreviated to "2L-HD mode") and is optional in this specification. It is also possible to have more than two Lanes, 3 or 4 Lanes for increasing system speed. This behavior is optional in this specification.

Figure 3-1 illustrates interface speed comparison among bus modes in Legacy SD, UHS-I and UHS-II (for UHS-II interface of 2 Lanes is assumed).

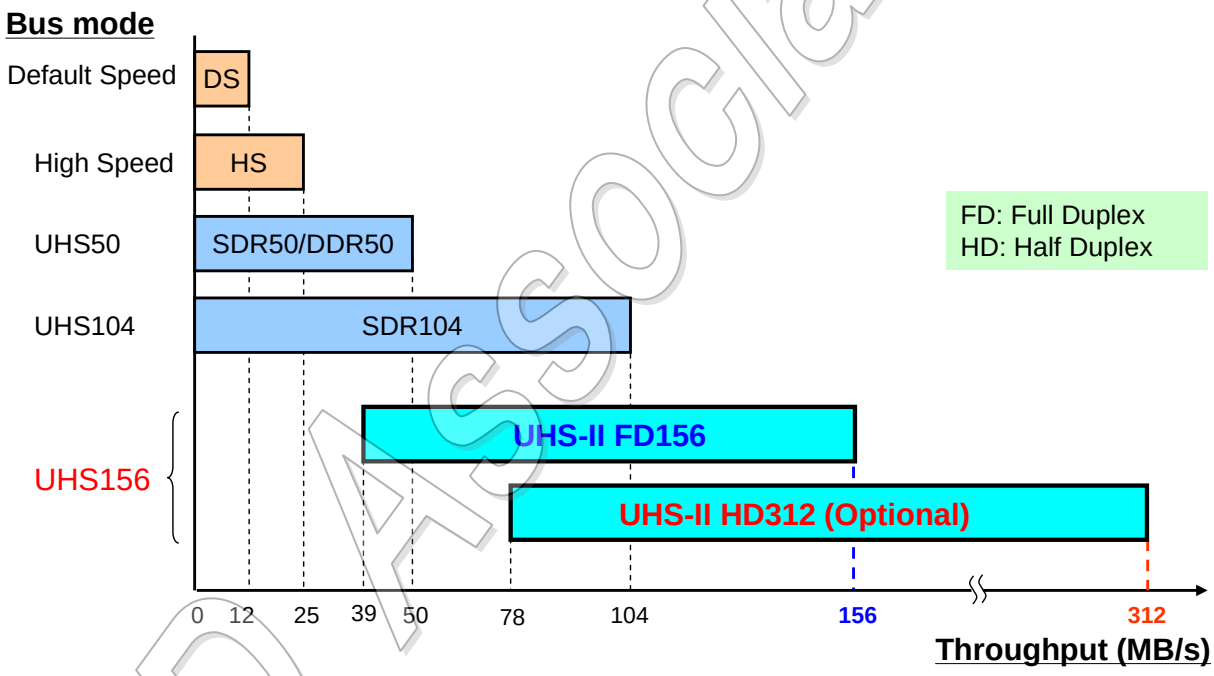


Figure 3-1 : Interface Speed Comparison

The interface speed shall be variable continuously.

3.2 Connection Topologies

3.2.1 Point to Point Connection

Minimum topology is consisting one Host and one Device is called "Point to Point" connection. Figure 3-2 shows the connection of a Host and a Device.

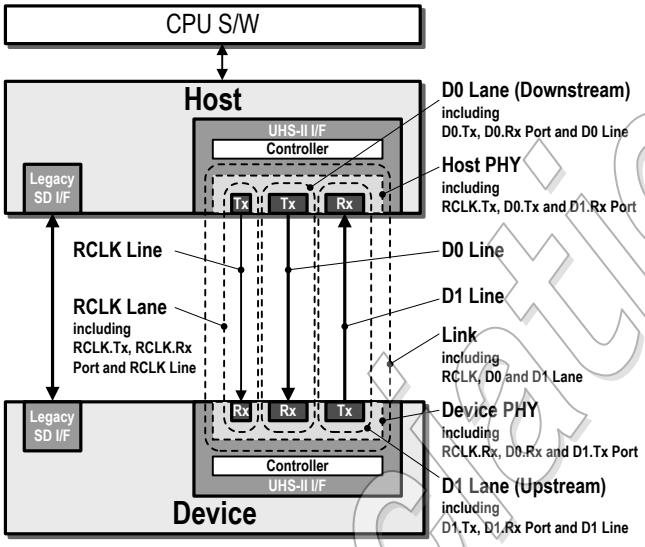


Figure 3-2 : Point to Point Topology (FD mode)

In UHS-II interface, both Host and Device have a PHY and a Controller which are responsible for performing Physical and Link / Transaction layer functions respectively. And UHS-II interface are connected by the following three Lanes.

- **RCLK:** transmits reference clock to Device from Host.
- **D0:** is a data Lane. It transmits commands, data, or other packets from Host to Device (downstream).
- **D1:** is another data Lane. It transmits responses, data, or other packets from Device to Host (upstream).

In general, each Lane consists of a Tx (Transmitter) Port and an Rx (Receiver) Port and a transmission Line between them. The notations used in this specification are used to specify each Tx or Rx Port clearly. For instance, Tx Port of RCLK Lane is described as RCLK.Tx and Rx Port of RCLK Lane is described as RCLK.Rx. The same rule is applied for other Lanes. And all Lanes are collectively called Link. Host PHY (PHY of Host) includes RCLK.Tx, D0.Tx and D1.Rx. Similarly, Device PHY (PHY of Device) includes RCLK.Rx, D0.Rx and D1.Tx.

All following descriptions relate to interface with two data Lanes. The optional case of 3 or 4 Lanes is described in Chapter 9.
Figure 3-3 shows the connection of Host and Device supporting 2L-HD mode.

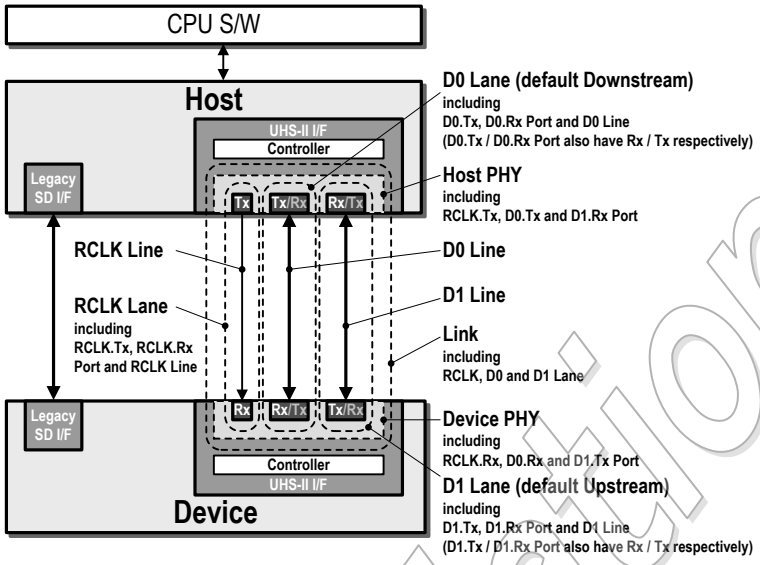


Figure 3-3 : Point to Point Topology (Supporting 2L-HD Mode)

The default direction of D0 Lane is downstream, and D1 is upstream. If Host decides to send data to Device in 2L-HD mode, D1 Lane changes downstream temporarily (Figure 3-4 (a)). Similarly if Host decides to get data from Device in 2L-HD mode, D0 changes upstream (Figure 3-4 (b)). As a result, all Ports for data Lanes are necessary to have both functions of Tx and Rx.

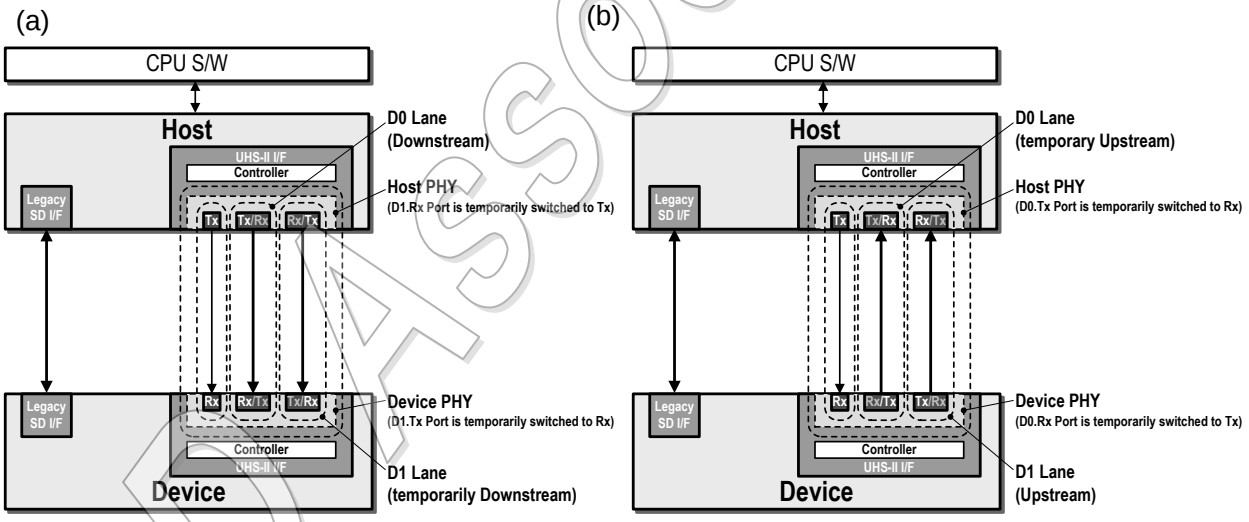


Figure 3-4 : Direction Changing in 2L-HD Mode

3.2.2 Multi-device Connection

In order that Host can control or communicate with multiple Devices, UHS-II provides Multi-device connection. There are two types of topologies to realize Multi-device connection, one is Ring connection and the other is Hub connection. Ring connection is introduced to realize a cost effective topology that minimizes the total number of PHY in the embedded system. And Hub connection is introduced to realize more flexible topology compared to Ring, in terms of capability of hot insertion and removal. Note that RCLK shall be distributed individually to removable Devices, and not only UHS-II interface but also Legacy SD interface shall be connected to removable Devices.

3.2.2.1 Ring Connection

Figure 3-5 illustrates an example of Ring connection. Connection rule of data Lanes is as follows. (Note that 2L-HD mode is not available in Ring connection in UHS-II Addendum Version 1.00.)

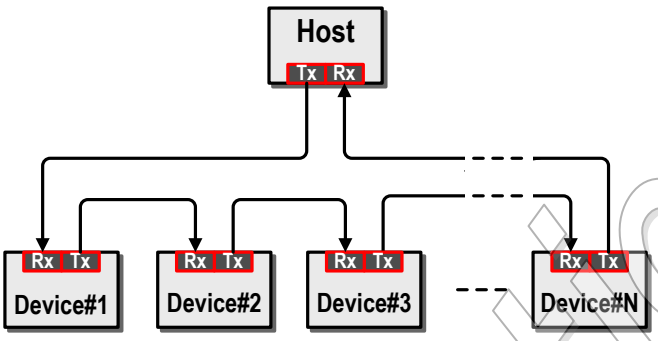


Figure 3-5 : Example of Ring Connection

(1) D0.Tx of Host is connected to D0.Rx of Device#1
(2) D1.Tx of Device#1 is connected to D0.Rx of Device#2, and this operation is repeated.
(3) D1.Tx of Device#N (final Device) is connected to D1.Rx of Host, and Ring connection completes.

Examples of RCLK distribution method are illustrated in Figure 3-6.

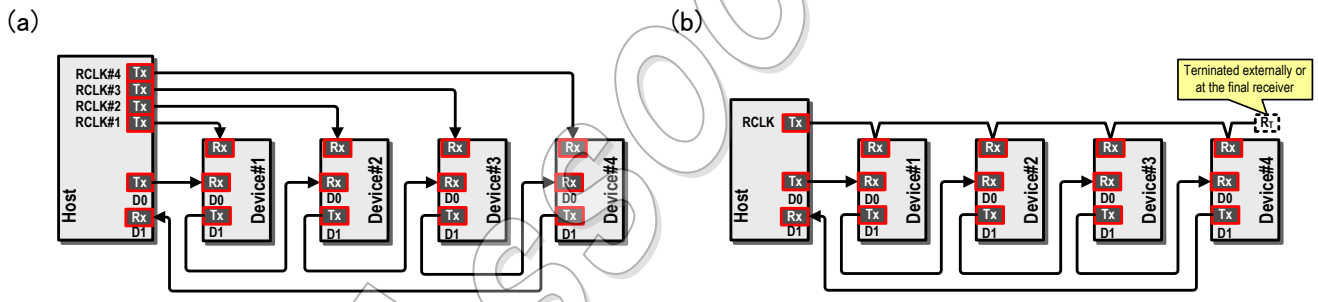


Figure 3-6 : Examples of RCLK distribution method for Ring

Figure 3-6 (a) shows a multiple point to point method which uses a separate RCLK driver (RCLK.Tx) for each Device. With this method, Host needs to have at least the same number of RCLK.Tx Ports as the number of connecting Devices. If Host has only one RCLK.Tx Port, multi-drop method can be applied to connect multiple Devices (Figure 3-6 (b)). With this method, RCLK bus is terminated externally or at the final receiver. In addition this method requires careful signal integrity design.
Note that Device has only one RCLK.Rx Port even in the case of Figure 3-6 (b).

3.2.2.2 Hub Connection

Figure 3-7 illustrates an example of Hub connection.
Hub shall have one Device PHY for Host connection and plural number of Host PHYs for Device connection. Hub also has functions such as transmitting signals to all connected Devices simultaneously, or selecting a packet destination according to its content.

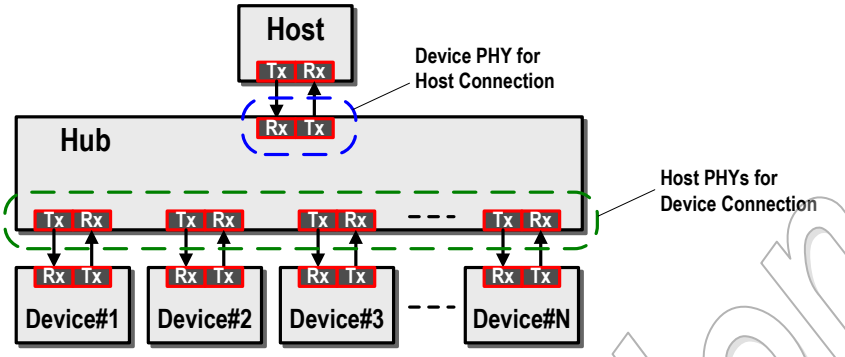


Figure 3-7 : Example of Hub Connection

Note that from Device point of view behavior does not depend on UHS-II topology. Hub specification is not described in this document.

3.3 Layering

Figure 3-8 shows the overview of UHS-II interface layer structure.

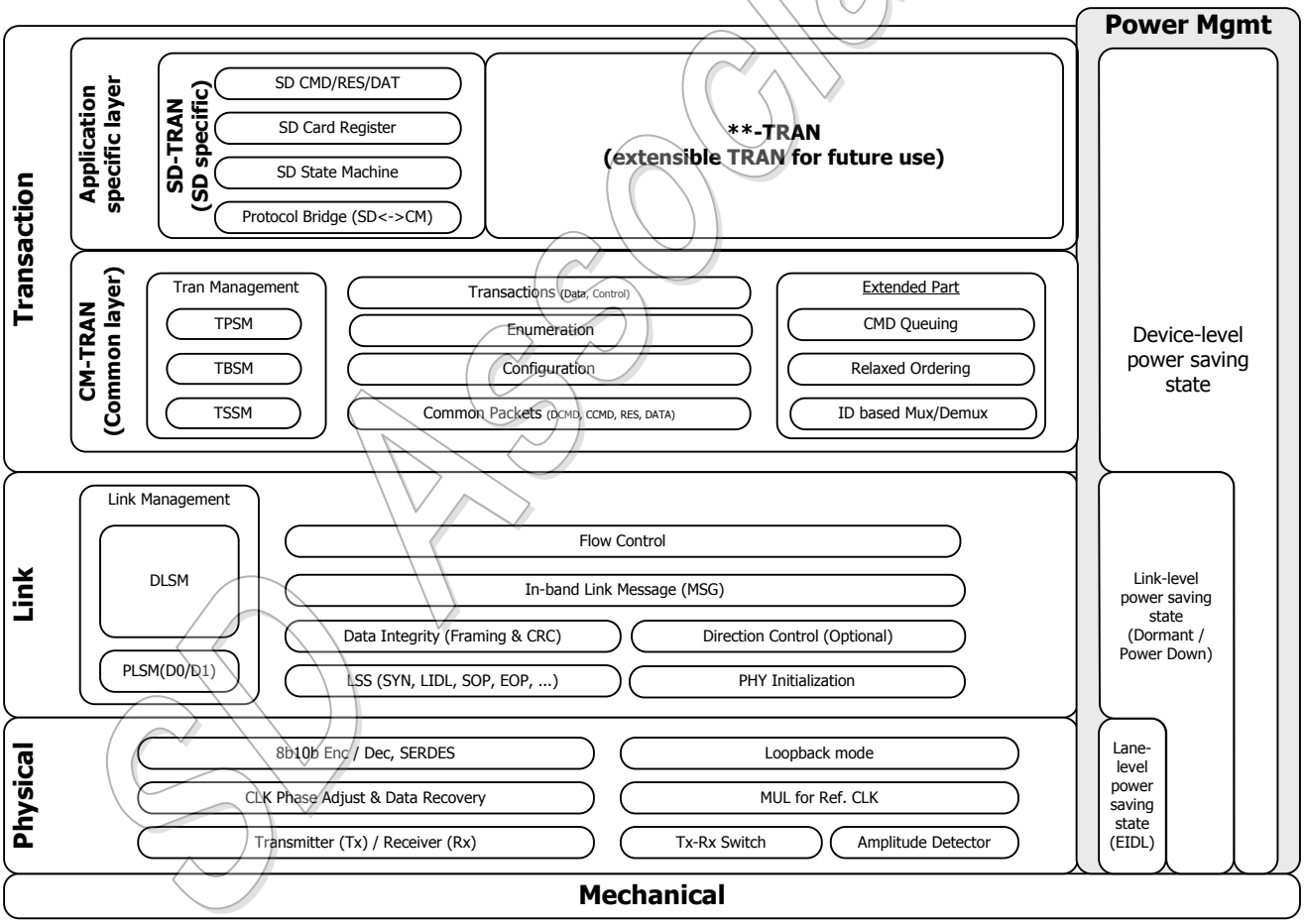


Figure 3-8 : Layering Overview

Basically, UHS-II interface consists of four layers described below.

- **Mechanical layer** defines mechanical specification such as card form factor, connector pins and so on.
- **Physical layer (denoted by PHY)** defines electrical specification such as signaling architecture, and handle bit or symbol encoding and decoding.
- **Link layer (denoted by LINK)** is responsible for Link management including PHY initialization, and data integrity (packet framing / de-framing and CRC generation / checking). It is also in charge of power management and flow control.
- **Transaction layer (denoted by TRAN)** is responsible for protocol-base management including packet generation and analysis, command-response handshake, and so on.

TRAN is split into sub layers, one is a common layer called CM-TRAN and the other is an application specific layer. CM-TRAN is responsible for Basic IO or Memory transaction and control. The application specific layer bridges CM-TRAN and upper application layer in order to keep compatibility. SD-TRAN is one of the application specific layers and bridges CM-TRAN and Legacy SD applications or drivers.
In this specification, SD-TRAN is also described. Other application specific layers can be defined in the future.

3.4 UHS-II Transaction

3.4.1 UHS-II Packet

The following five packet types are defined for UHS-II TRAN. UHS-II Packet other than MSG is also called Transaction Layer Packet (TLP).

- **Control command packet (denoted by CCMD)** is a command without Data packet transaction. There are two categories of CCMD, one is P2P CCMD and the other is broadcast CCMD. Refer to Section 6.2.2.3 for the details of them.
- **Data command packet (denoted by DCMD)** is a command accompanied with Data packet.
- **Response packet (denoted by RES)** is a response that Device returns to Host after receiving CCMD or DCMD.
- **Data packet (denoted by DATA)** is for transmitting data payload between Host and Device.
- **Message packet (denoted by MSG)** is for transmitting short information. Only MSG is generated or analyzed in LINK.

Basically, UHS-II packet consists the following three parts, Header, Argument, and Payload. The Header part is common for all types of packet.
TLP is basically packetized based on information provided by TRAN and depacketized in LINK. Refer to packet format described in Section 6.2.2 or Section 7.2.1 for the details of the information.

Let initiator denote a Node (Host or Device) that newly creates a packet and transmits it. The following table indicates the initiator for each packet type.

Packet Type	Initiator
CCMD/DCMD	Host (regardless of P2P CMD or broadcast CMD)
RES	Device
DATA	Node creating DATA packet (Host for write transaction, Device for read transaction)
MSG	Node creating MSG packet

Table 3-1 : Definition of Initiator

3.4.2 Data Transaction

Length Unit Mode is defined to specify the unit of total data transfer length (TLEN) transmitted by Data packet (DATA). Length Unit Mode has the following two modes, one is a Block Mode and the other is a Byte Mode. Note that these modes can be set as a parameter of DCMD.

- **Block Mode:** TLEN is specified by a unit of Block Length, which is a payload length for one block. Block Length is finally determined through Configuration (refer to Section 0 and 6.2.9) or settings in the application specific layers.
- **Byte Mode;** TLEN is specified by a unit of byte. TLEN shall be less than or equal to Block Length.

Also refer to Section 5.2.6 about a data framing rule of above two modes.
In addition, at most one data transaction can be executed in UHS-II Addendum Version 1.00.

3.4.3 CM-TRAN

As described in Figure 3-8, UHS-II transaction layer is split into common layer (CM-TRAN) and application specific layer (SD-TRAN in case of UHS-II Card).
CM-TRAN specifies the common protocol suitable for UHS-II PHY and LINK (UHS-II native protocol). CM-TRAN generates UHS-II packets and sends them in the transmitter side according to the UHS-II I/O Register, or analyzes received packets in the receiver side. UHS-II I/O register is accessed by the Application Driver (Host) or Backend (Device).

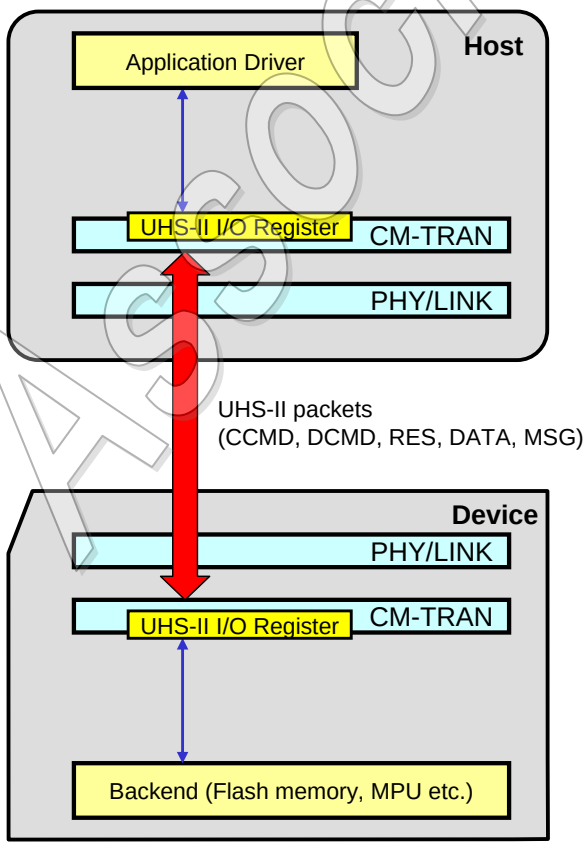


Figure 3-9 : Basic UHS-II Transaction

3.4.4 SD-TRAN

SD-TRAN bridges UHS-II interface (CM-TRAN) and Legacy SD IPs or software. SD-TRAN analyzes SD Host/Device Register and sets parameters to UHS-II I/O Register. In this case, CM-TRAN generates UHS-II packets which encapsulate Legacy SD command, response or data. Moreover, when CM-TRAN receives the encapsulated packets, CM-TRAN analyzes it and notifies to SD-TRAN.

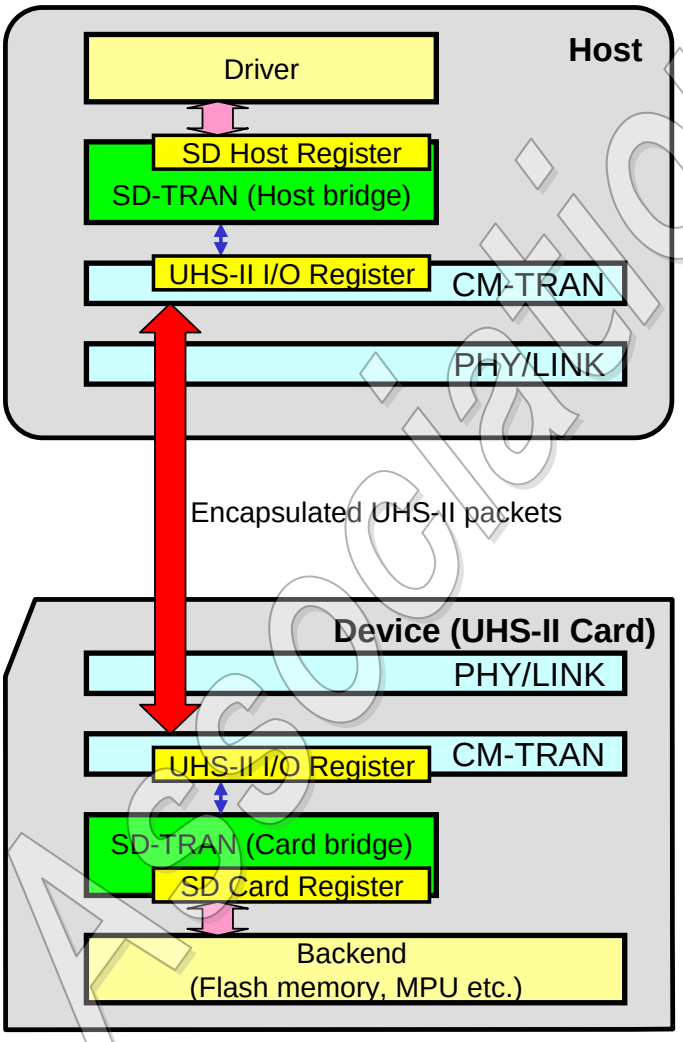


Figure 3-10 : UHS-II Transaction by SD-TRAN

3.4.5 Aborting Transaction

In UHS-II, TRANS_ABORT CCMD is introduced as following purposes.

- Terminating data transmission in UHS-II native protocol. (Note that the encapsulated CMD12 shall be used instead of TRANS_ABORT if SD-TRAN is implemented.)
- Aborting the outstanding transaction when timeout is detected.

3.5 UHS-II Initialization Outline

Host shall execute UHS-II Initialization flow as described in Section 3.5.1 (in case of without Boot Code Loading) or in Section 3.5.2 (in case of with Boot Code Loading). If Host violates those rules, Device operation is not guaranteed.

3.5.1 UHS-II Initialization Flow without Boot Code Loading

Figure 3-11 shows a UHS-II Initialization flow after I/F power cycle or issuing FULL_RESET command (refer to Table 6-20 for more details). Details of state transition are defined in Section 5.2.9.

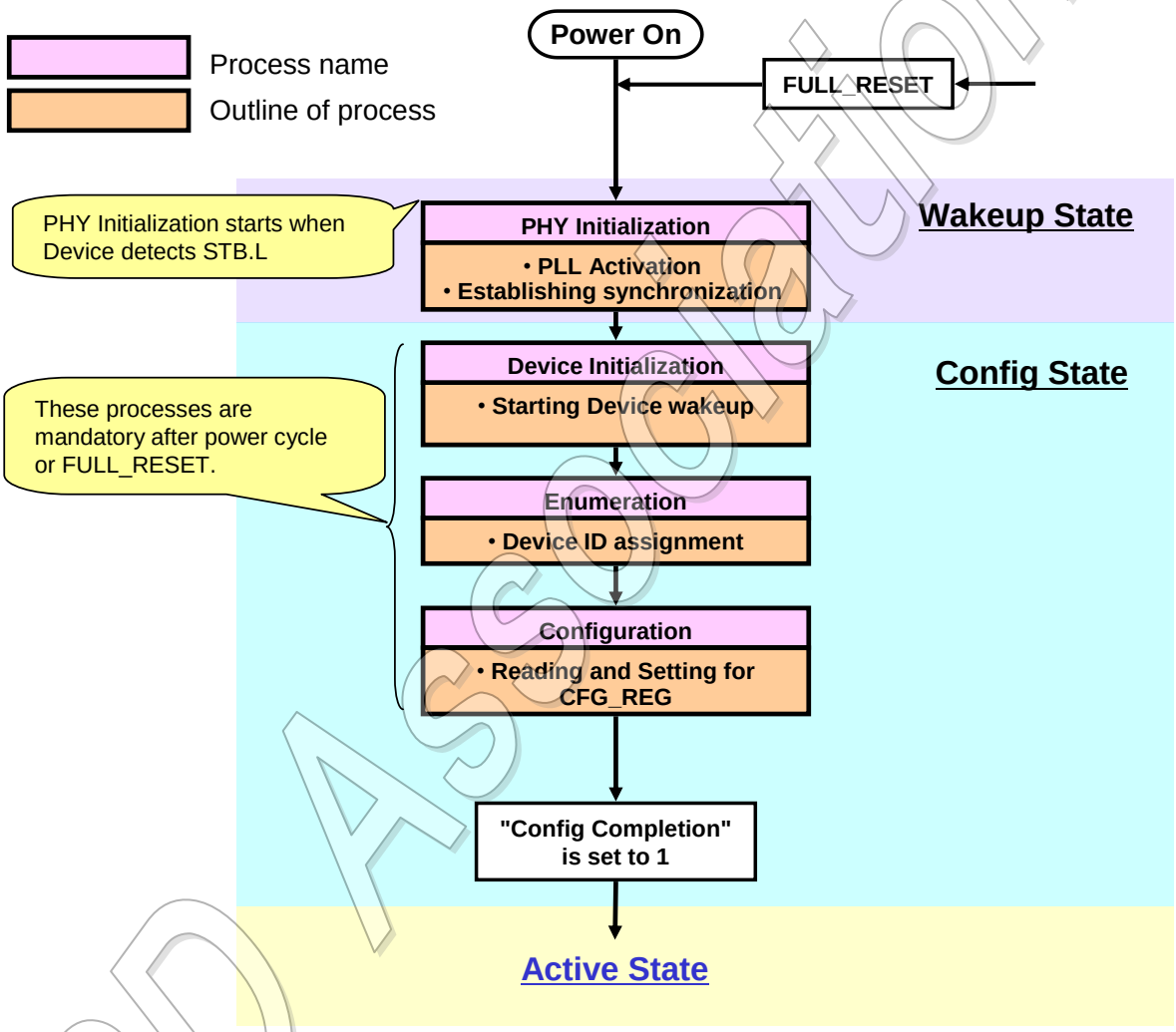


Figure 3-11 : UHS-II Initialization Flow

After I/F power cycle or FULL_RESET, PHY Initialization process is started by Host's providing RCLK and STB.L.
After finishing PHY Initialization, the state transits to Config State and the following three processes take place.

- **Device Initialization:** This process is executed by DEVICE_INIT CCMD and makes whole components in Device activated. Refer to Section 6.2.6 for more details.
- **Enumeration:** This process is executed by ENUMERATE CCMD and assigns Node IDs for each

Device uniquely. Refer to Section 0 for more details.

- **Configuration:** This process is for determination of parameters for transaction among Host and Devices. First Host reads capabilities or properties from Configuration Register (CFG_REG) of Devices, then determines the parameters for transaction, and finally writes the parameters to the register. Refer to Section 0 and 6.2.9 for more details.

If "Config Completion" flag defined in CFG_REG is set to 1 successfully during Configuration process, the state transits to Active State.
Before completing Device Initialization it shall not operate and not transmit RES or broadcast CCMD when Device receives CMD other than DEVICE_INIT CCMD.

3.5.2 UHS-II Initialization Flow with Boot Code Loading

It is possible for Host to load its Boot Code from one of connected Device, called Boot Device. Boot Device is optional in embedded system. It is required for Host to read the Boot Code as soon as possible.
Needless to say, Boot Device and Host are possible to transmit or receive Boot Code. In addition, considering the Ring connection, all other Devices also have functionality to bypass Boot Code and its related packets.
In this Section, the specification of loading Boot Code is described when the system includes Boot Device. This function is called "Boot Code Loading". Figure 3-12 shows UHS-II Initialization flow when Boot Code Loading is executed.

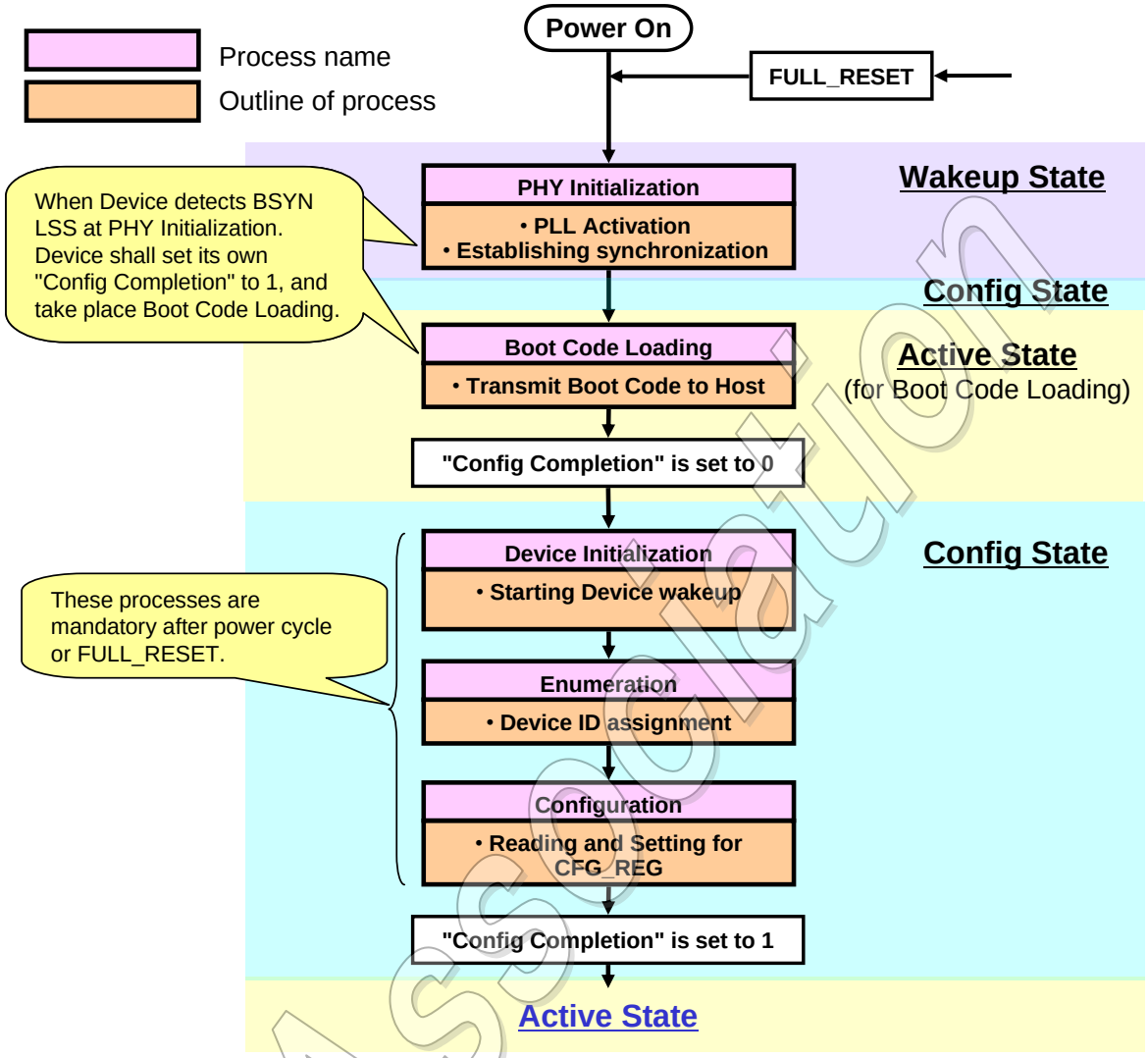


Figure 3-12 : UHS-II Initialization Flow When Boot Code Loading Is Executed

Different from Figure 3-11, Host transmits not SYN LSS but BSYN LSS in order to establish synchronization. At that time, all Devices shall set their own "Config Completion" to 1.
After finishing PHY Initialization, DLSM normally transits to Config state, but as "Config Completion" is equal to 1, DLSM immediately transits to Active state in order to execute Boot Code Loading.
After finishing Boot Code Loading, Host shall set "Config Completion" to 0 for all Devices before DEVICE_INIT CCMD. Device shall accept the Broadcast Write CCMD for setting "Config Completion" to 0 even before receiving DEVICE_INIT CCMD. Then DLSM transits to Config state. The rest of flow is same as Figure 3-11.

4. Physical Layer Specification

The details of UHS-II Physical layer such as signaling architecture electrical specification and handle bit or symbol encoding and decoding are described in this chapter.

The UHS-II standard is targeted for mobile, portable applications and home applications. It shall be compatible to legacy SD Cards. It provides enhanced data rate, while maintaining low power and low EMI. It is recommended for short cable length, typically below 20cm.

This UHS-II specification is defined for Card and also for Embedded Device. In this specification, "Device" means both Card and Embedded Device. If some specification items or descriptions are only for Card, "Card" is used. If some specification items or descriptions are only for Embedded Device, "Embedded Device" is used.

The key features of Physical Layer are defined as follows:

- Differential low voltage Signaling with DC coupling
- Flexibility of transmission rates
- Low Frequency Reference Clock (RCLK)
- Two types of duplex mode: FD mode (mandatory), 2L-HD mode (optional)
- Additional pins for High-Speed Differential transmission
- 8b/10b coding
- Enhanced power saving modes

4.1 Physical Layer Overview

Physical layer consists of the following functions:

- Differential Transmitter(Tx) and Receiver(Rx)
- CLK phase adjustment and Data recovery
- Serializer and De-serializer (SERDES)
- 8b/10b encoding and 10b/8b decoding
- Amplitude Detection
- Synthesizer for Reference CLK

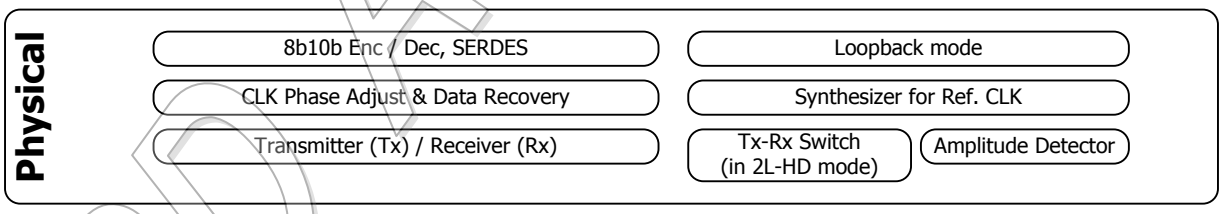


Figure 4-1: Physical Layer Overview

4.2 Physical Layer Interface Architecture

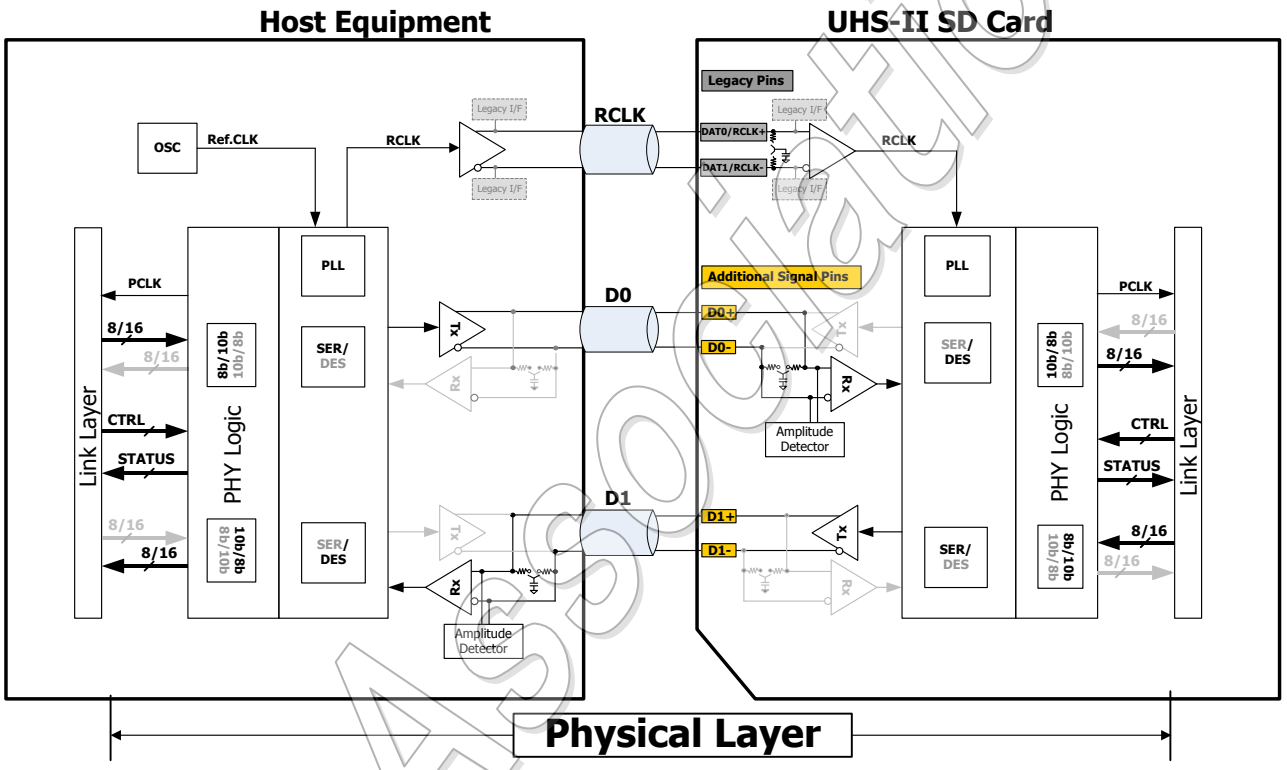
Figure 4-2 illustrates an example of the interface architecture of physical layer in case of point to point connection between Host and Card. The UHS-II interface utilizes transmission Lines (including socket and pins) and terminations which are meant to keep the impedance matching for high speed transmission. UHS-II interface introduces the additional pins for high speed data transmission.

UHS-II interface has continuous variable data rate from 39MB/sec to 156MB/sec as effective data rate. Device shall cover the whole range.

UHS-II has two data Lanes. As default, one Lane (D0) is used for downstream (from Host to Device), and another Lane (D1) is used for upstream (from Device to Host). Both data Lanes may be used for downstream Lanes or upstream Lanes at the same time by activating the 2L-HD mode (optional).
The transmitted data is encoded by 8b/10b encoder.

The Differential Clock (RCLK) may be tuned in the range of 26MHz to 52MHz. Regarding Card, RCLK is sent through the legacy SD transmission lines DAT0, DAT1 and corresponding Card pins.

Amplitude Detectors, which detect the Lane's electrical level, are equipped to Host side of D1 Lane (optional) and Device side of D0 Lane (mandatory). Amplitude Detectors make the I/O circuits, such as receiver, to wake up when transmission is resumed at the Lane after Dormant state.



Note 1: All function blocks and connection lines used in 2L-HD mode are colored by gray.
Note 2: I/O circuits of Legacy SD Interface, which are not used in UHS-II, are shown by dash-line and filled with light gray.
Note 3: RCLK termination of each device shall be switchable.

Figure 4-2: Physical Layer Interface Architecture

4.2.1 Lane Definition

Host and Device are connected by 3 differential Lanes with DC coupling:

- **High speed data Lanes (D0, D1):**
  D0 is used for downstream (from Host to Device), thus WRITE data and command are transferred from Host to Device on this Lane. However, when enabling the optional 2L-HD mode, it is possible to use D0 Lane as upstream (from Device to Host).
  D1 is used for upstream, thus READ data and response are transferred from Device to Host on this Lane. However, when enabling the optional 2L-HD mode, it is possible to use D1 Lane as downstream.
  D0 and D1 Lanes are used for differential transmission between Host and Device which are dedicated to UHS-II interface only, and are separate for signals of legacy SD interface. The D0

and D1 signals are encoded by 8b/10b code before transmission, and decoded by 10b/8b after receiving, as described in Section 4.5.

- **Reference clock Lane (RCLK):**
  RCLK is transmitted from Host to Device. Whenever Host output a RCLK to the UHS-II Device, the RCLK signal frequency and phase should be stable. The RCLK shall not be stopped and its frequency shall not be changed during UHS-II transmission, even within the same range. (Refer to Section 4.2.2 for the Range definition and Section 6.2.3 for frequency change procedure).
  The RCLK frequency is lower than lowest data rate. Therefore, the Device shall generate high frequency clock or multi-phase clocks internally for sampling the high-speed data. The RCLK frequency is in the range of 26MHz to 52MHz; Data rate is from 390Mbps to 1.56Gbps per Lane (Refer detail in Section 4.2.2).
  Regarding Card, RCLK is sent through DAT0 and DAT1 lines of legacy SD interface. Thus, RCLK does not require additional pins. Card RCLK receiver shall be tolerant to single ended voltage range of 0V to 3.6V DC.

For power save purposes, when no data is transferred each Lane may enter EIDL state individually, or all Lanes including RCLK Lane may enter EIDL state concurrently, which is called Dormant state. During those states and mode, an Amplitude Detector of each D0, D1 Lane is active, monitoring the Line voltage and flagging wakeup notice. After detecting the wakeup notice, the detector activates PHY circuits of own port.

4.2.2 Range Definition for Data Rate

In UHS-II, RCLK frequency is in the range 26MHz to 52MHz and Data rate is 390Mbps to 1.56Gbps per Lane accordingly. This range is divided to two ranges for the ease of PLL design as shown in Table 4-1.
Initialization of UHS-II interface after power down shall be done with the Range A.
Device PLL acquisition time shall be at most 2ms. But only the first PLL acquisition time after power up, PLL of Host and Device shall finish locking less than 100ms. This is Tactivate.

	RCLK Frequency	Data Rate/channel	Ratio (Data rate / RCLK Frequency)
Range A	26MHz to 52 MHz	390Mbps to 780Mbps	x 15
Range B		780Mbps to 1.56Gbps	x 30

Note: Even if supporting SSC, the minimum RCLK frequency shall not be lower than 26MHz.

Table 4-1: Range Definition for Data Rate

4.2.3 Power Supply Connections

Two power supply connections are needed for UHS-II interface, named VDD1 and VDD2, for powering the Device by the Host.
VDD1 is dedicated for powering the legacy SD interface, logic and the memory devices in the Device
VDD2 is used for powering UHS-II interface. It should power the PHY and upper layers logic.
GND node is common to all the devices and all the circuits. It is also used as reference for the UHS-II signaling levels, thus it is recommended that both Host and Device design for minimal DC variation and AC noise on this node.

Section 4.2.4 to Section 4.2.7 is a blank in the Simplified Addendum.

4.3 Electrical Specification

Section 4.3.1 to Section 4.3.2 is a blank in the Simplified Addendum.

4.3.3 Eye-mask Template

The eye-mask templates are the graphical representation of the limit for the voltage and jitter for the differential signals. The eye-mask templates of UHS-II are shown in Figure 4-6. The horizontal margin of eye-mask template is calculated as 1 UI - T_J.

For the transmitters of Host and Device, when transmitting differential signal, these signals including over/under-shoot shall remain in the white area of each Eye-mask template (Tx) in Figure 4-6 at any time except in EIDL state.
For the receivers of Host and Device, when receiving the differential signals that have the eye-opening shown in eye-templates (Rx) in Figure 4-6, receivers shall receive these signals correctly.

The eye mask templates specified in Figure 4-6 refers to measurements at standard measurement conditions and BER of 1E-12. The standard measurement conditions are described in UHS-II PHY Test Guideline document.

Note: The Host and Device are tested separately at "ideal" compliance environment, while in real system Host and Device are connected together, so there will be some mutual effects because of this connection. The margin between (2) to (3) Eye-masks and (4) Eye-mask to (5) Eye-mask are taken because of that. The following elements are covered by this margin:

A. Power delivery noise,
B. Internal Device Xtalk due to other internal activity

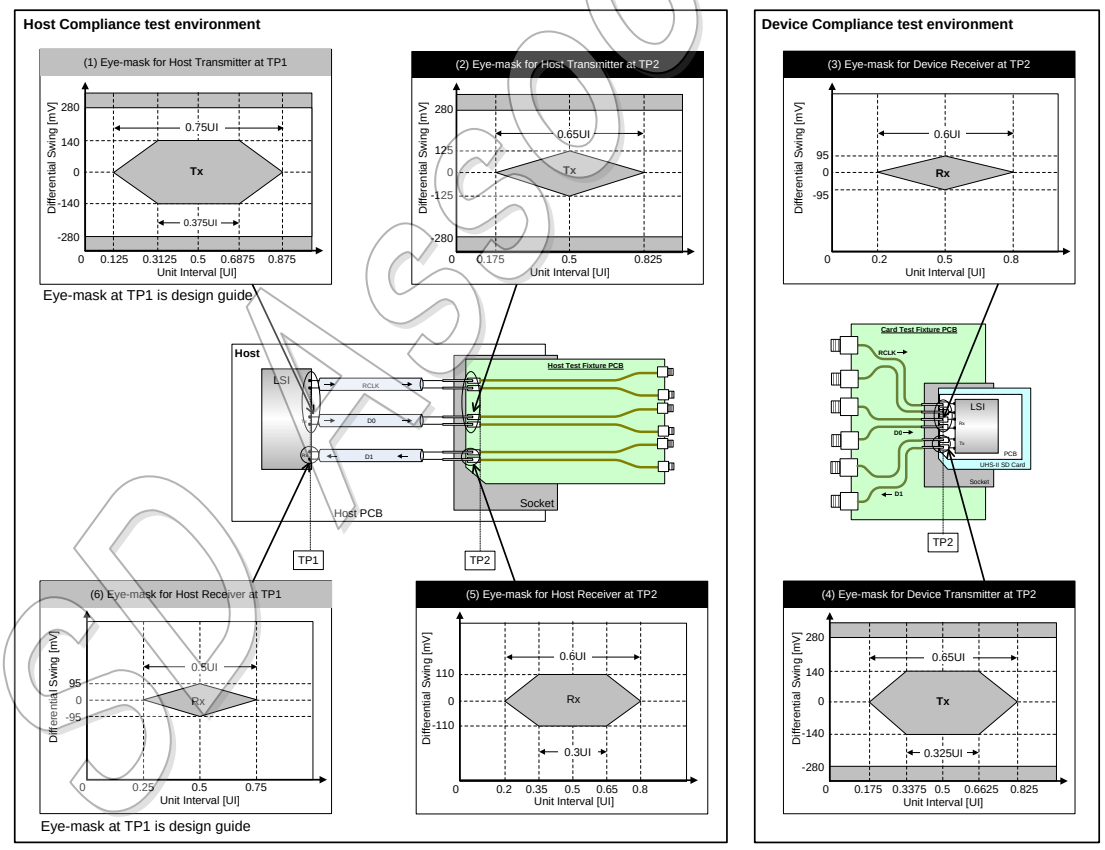


Figure 4-6: Eye-mask Templates

Notes of Figure 4-6 is a blank in the Simplified Addendum.

4.3.4 Jitter

The relation between eye-opening and total jitter is defined by Eye Opening = 1UI- T_J. The more jitter, the less eye-opening. Thus, for ensuring the interconnection between Host and Device, jitter specification shall be adhered for each differential Lane: RCLK, D0 and D1.

Total Jitter T_J consists of two jitter components: deterministic peak to peak jitter D_J and random root mean square jitter $R_{J\text{-}rms}$.
Total Jitter T_J is calculated by the following equation:

$$T_J = D_J + Q \cdot R_{J\_rms}$$

Where, Q factor is related to Bit error rate (BER). In UHS-II, BER performance of PHY shall be achieved by $10^{-12,}$ when Q is 14.1.
The D_J contains two elements D_J(ISI) which is the deterministic jitter caused by ISI and S_J which is a sinusoidal jitter component.
Test pattern, jitter element budgeting and jitter injection method is specified in UHS-II PHY Test Guideline document.

Section 4.3.4.1 to Section 4.3.4.2 is a blank in the Simplified Addendum.

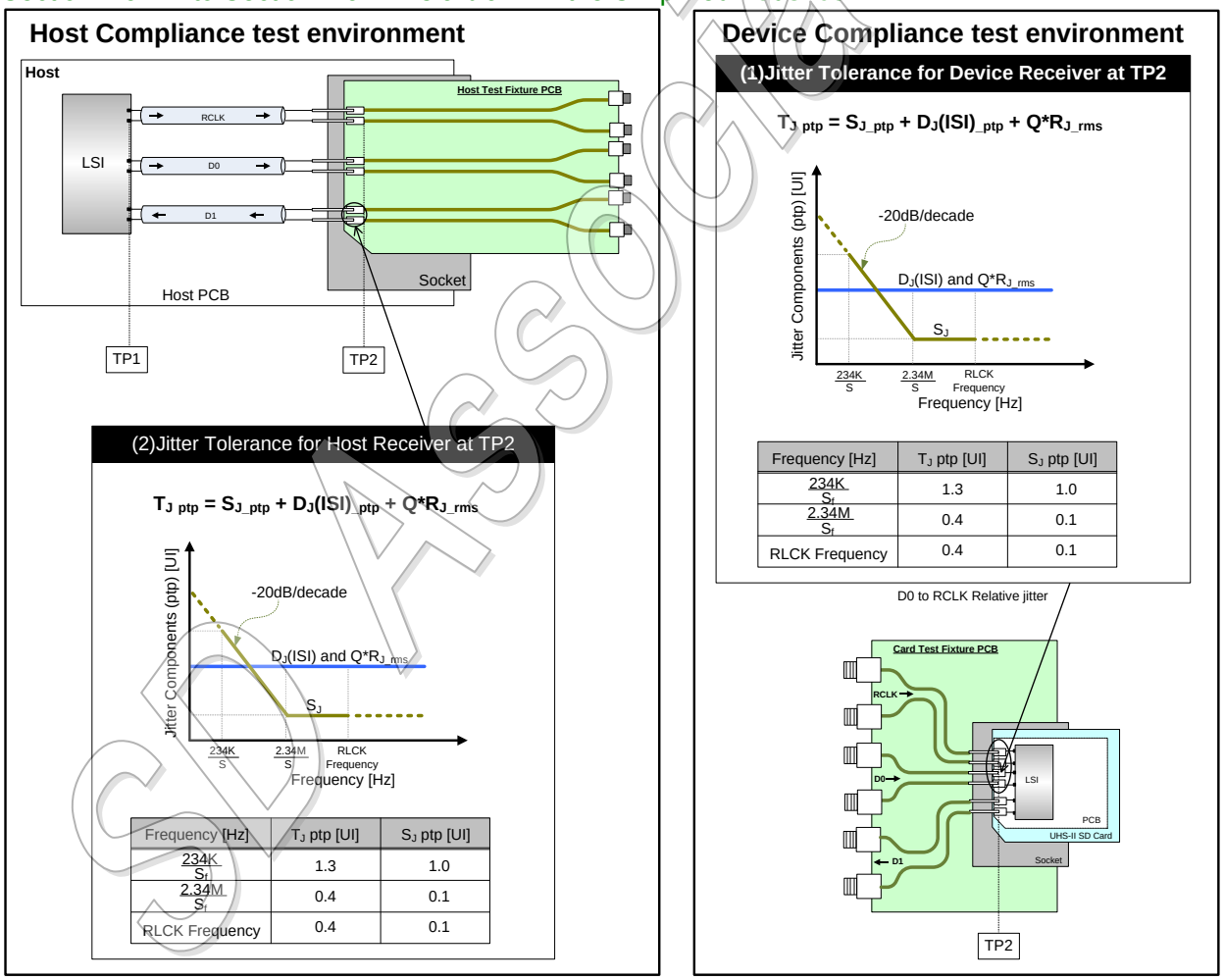


Figure 4-7: Jitter Tolerance Specification

Notes of Figure 4-7 is a blank in the Simplified Addendum.

4.3.5 Return Loss

The mismatch and unbalance of impedance between the components which form transmission Line causes the signal reflection. Signal reflection contributes to the degradation of signal integrity and EMI.

The return loss limits (differential return loss, common-mode return loss and common-to-differential return loss) are defined in UHS-II specification for keeping signal integrity and EMI mitigation.
Both transmitter and receiver shall comply with the return loss specification. When 2L-HD mode is supported, each port is bi-directional, thus return loss specification are applied for transmitter and receiver respectively.

The return loss is defined as the ratio of reflected power to incident power, and measured by using Test fixtures (Refer to Appendix C). The characteristic impedances of the Test Fixtures (mean differential impedance and common-mode impedance) are reference values for the return loss measurement. For Return Loss testing, De-embedding of the test fixture should be performed.
The detailed measurement method is described in UHS-II PHY Test Guideline document.

Following of Section 4.3.5 is a blank in the Simplified Addendum.

Section 4.3.6 to Section 4.3.7 is a blank in the Simplified Addendum.

Section 4.4 to Section 4.5 is a blank in the Simplified Addendum.

4.6 Loopback Mode

The PHY block in the Device and Host shall have loopback path that is needed for testability purposes, and the loopback path is also used for Devices in order to perform data bypassing in ring topology. It is expected that loopback path will have the same clocking scheme as Tx and Rx lanes in FD mode, for both forward and backward loopback.

The loopback causes the data that is received at the serial input of a Lane to transmit at the serial output of another Lane after recovery. The loopback is done from the output of the de-serializer in the receiver path, to the input of the serializer of the transmitter path, by dedicated 10 bit multiplexer in the transmitter block. This loopback enables testing the PHY with any symbols including patterns which are illegal for 10b/8b decoding.

In normal condition, the loopback path in the PHY of the Host is done from the D1 receiver to the D0 transmitter, as presented in Figure 4-15. This path is named "forward loopback". For testing the other direction, which test D0 as receiver and D1 as transmitter, which are used in 2L-HD mode, there is a need for backward loopback path, as shown in Figure 4-16.

In normal condition, the loopback path in the PHY of the Device is done from the D0 receiver to the D1 transmitter, as presented in Figure 4-17. This path is named "forward loopback". For testing the other direction, which test D1 as receiver and D0 as transmitter, which are used in 2L-HD mode, there is a need for backward loopback path, as shown in Figure 4-18.

The loopback modes are controlled by the LINK layer while in normal operation, while in Test mode loopback may also be controlled internally in the PHY. Each PHY vendor may specify additional loopback modes, but it is beyond the mandatory requirements of the standard.

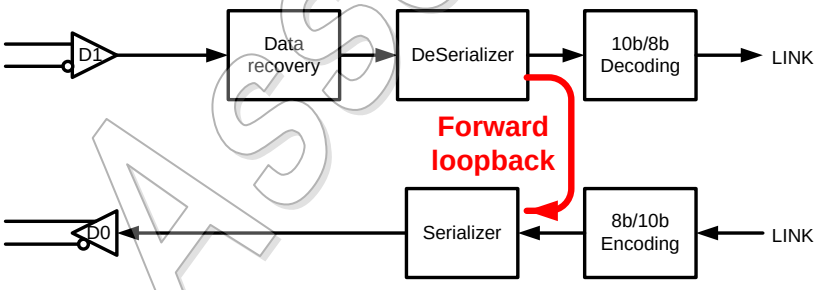


Figure 4-15: Location of Forward Loopback in PHY of the Host

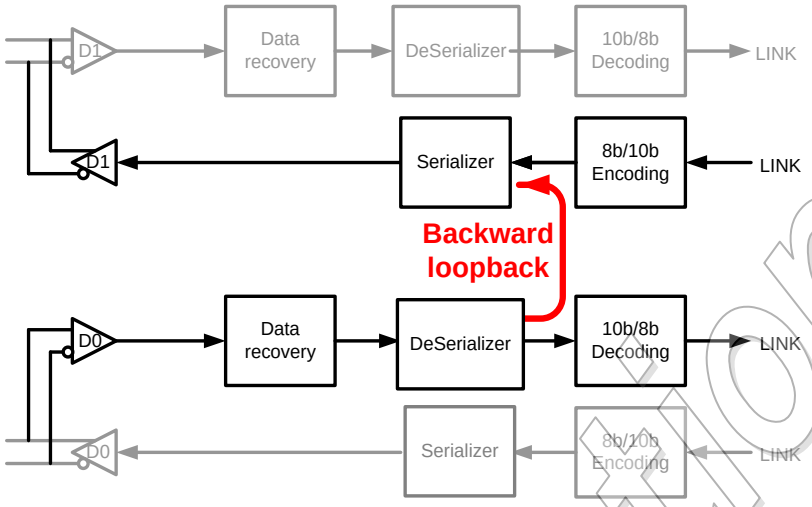


Figure 4-16: Location of Backward Loopback in PHY of the Host

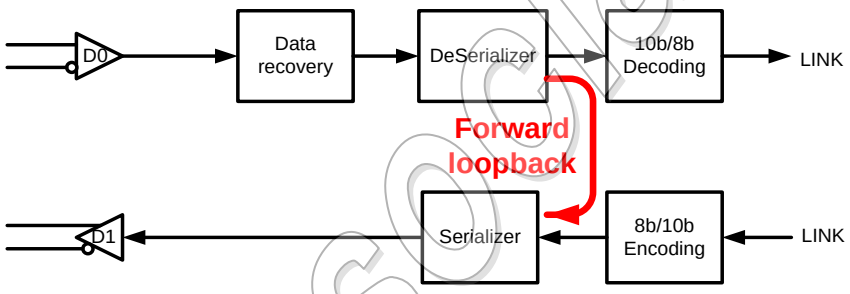


Figure 4-17: Location of Forward Loopback in PHY of the Device

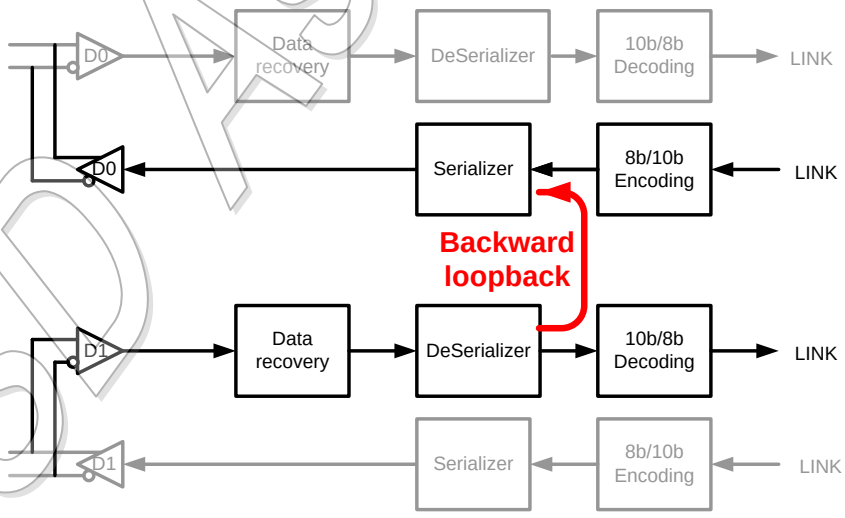


Figure 4-18: Location of Backward Loopback in PHY of the Device

4.7 PHY Test Mode

For the Compliance test of UHS-II PHY, Re-Sync state and following method are defined to UHS-II PHY in order to configure PHY for the specific test condition.

In PHY Test mode, Dormant state and Re-Sync state are used in case of changing PLL multiplier.

Dormant state used in PHY Test mode is the same state as in UHS-II normal operation, which is applied to the Rx which has Amplitude Detector (for example, Device D0.Rx), Therefore in the Dormant state during PHY Test mode, all PHY circuitry are powered off except Amplitude Detector. When exiting Dormant state, Amplitude Detector is used to detect STB.L.

Re-Sync state is applied to the Rx which has no Amplitude Detector (for example, Device D1.Rx). In the Re-Sync state PHY circuitry keeps power on (except for PLL while changing its multiplier) because Rx having no Amplitude Detector shall be able to receive symbols from Test equipment.

The difference between Dormant state and Re-Sync state is whether PHY is powered off or still powered on. Exiting Dormant state and Re-Sync state take the same sequences (Sequence to exit Dormant or Re-Sync; refer to Fig 4-19). When exiting these states, re-synchronization of CDR is performed.

Items to be configured in Test mode are as follows.

- Disconnect and Normal (Non-Disconnect) mode
  - **Disconnect mode**:
    Device and Host keep current test mode for any input levels.
    That means Device and Host do not enter Dormant state even if the connection change happens between the Device/Host and test equipment. It is possible to exit Disconnect mode by using Power cycle, or transfer to Normal mode by using "Sequence to Set Test Mode".

  - **Normal (Non-Disconnect) mode**:
    This mode is capable to enter the Dormant state. This mode is useful to perform multiple test items automatically.

- Loop Back Direction
  - **Forward Loopback**:
    Default loopback direction for all Devices and Hosts.

  - **Backward Loopback**:
    Device and Host which support 2L-HD mode support Backward Loopback.

    For Detailed Definition of Loopback modes, refer to Section 4.6 Loop Back mode.

Notes:

1. To enter Backward Loopback test mode, the sequence to set Test Mode (refer to Figure 4-19) shall be provided on Device D0 Rx and Host D1 Rx.
2. To enter Forward Loopback test mode retrieved from Backward Loopback test mode, the sequence to set Test Mode (refer to Figure 4-19) shall be provided on Device D1 Rx and Host D0 Rx.
3. Dormant state shall be used on Device D0 Rx (Forward Loopback) for testing an Amplitude Detector.

4. Which state Dormant or Re-sync should be used is dependent on implementation of Amplitude Detector especially on Device D1 Rx (Backward Loopback), Host D0 Rx (Backward Loopback) and Host D1 Rx (Forward Loopback).
5. Device and Host may transmit a few broken symbols instead of COM+SYN symbols expected, on switching Loopback direction.

- PLL Multiplier factor
  PLL Multiplier factor may be set by the test mode entry method without setting configuration Register. Change of PLL Multiplier is effective only when exiting Dormant or Re-Sync state.

- Future Test Mode Expandability
  Additional vendor specific Test Modes may be defined.

4.7.1 The Sequences used in PHY Test Mode

Figure 4-19 shows the sequences used in PHY Test Mode. Test mode configuration is done by setting the TMD1 and TMD2 in the symbol named "TEST-MODE" (which is constructed by COM (K28.5) + K-code (K30.7) + TMD1 + TMD2 as described in Figure 4-19). To avoid entering a test mode by mistake, TEST-MODE symbol is sent 4 times continuously.

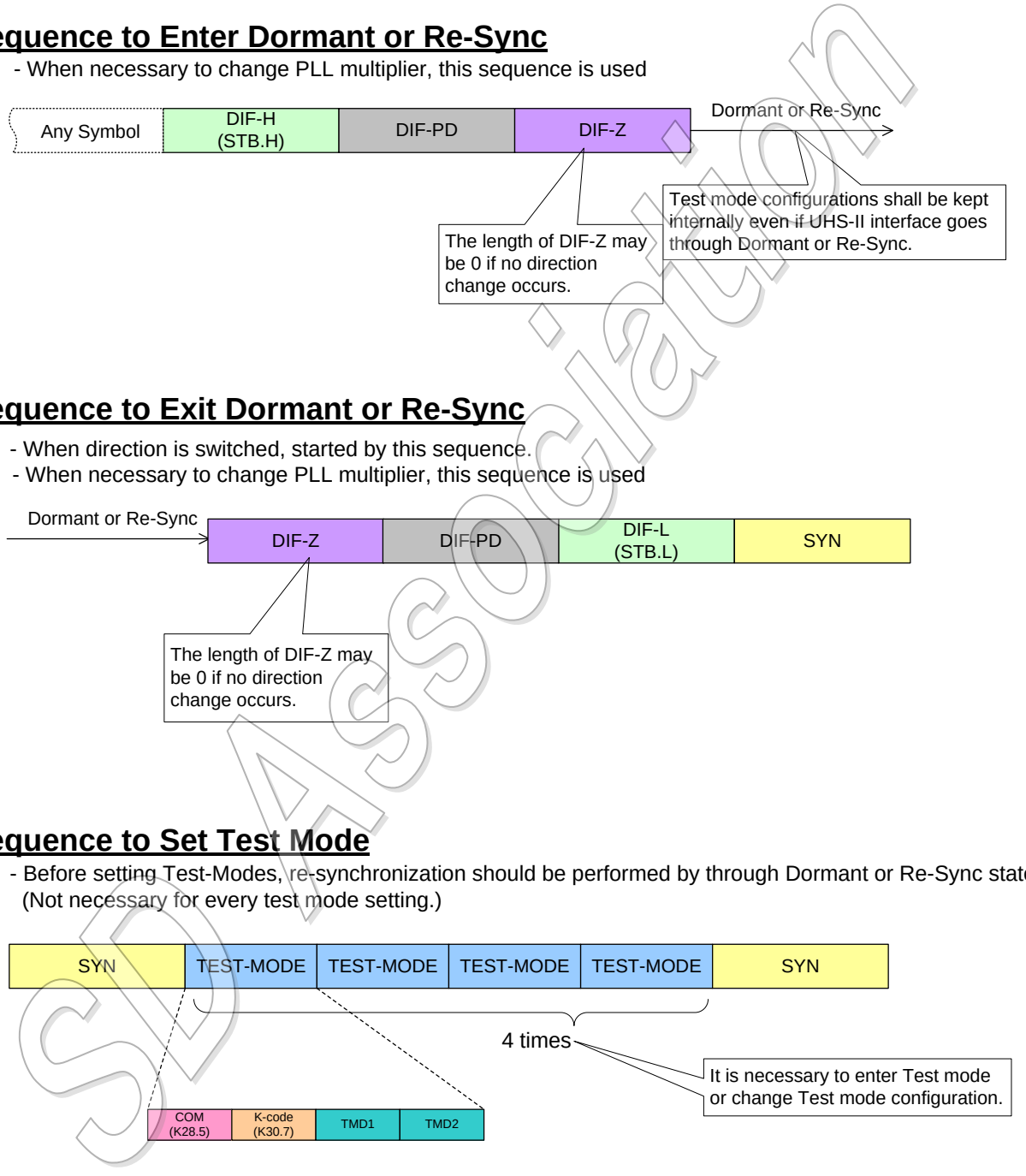


Figure 4-19: Sequences used in PHY Test Mode

4.7.2 Definition of TMD1 and TMD2

The structure of TMD1 and TMD2 are defined as follows and in Figure 4-20. Device maintains setting of TMD1 and TMD2 during PHY test mode until Host changes setting of TMD1 and TMD2, even if going through Dormant or Re-Sync mode.

4.7.2.1 TMD1

TMD1 is used for configuring Main mode and Sub mode.

Upper 4-bit is used to assign Main Mode:

- **0h** : assigned for Loop Back Test Modes
- **Fh** : assigned for vendor specific test modes (Vendor may define TMD1 and TMD2 to control vendor specific test modes)

Lower 4-bit is used to assign Sub Mode:

- **"Timing"(Sub Mode 00)**: determines the timing when Sub-Mode 03-01 is effective.
- **"Disconnect"(Sub Mode 01)**: determines whether Disconnected mode or Normal (Non-Disconnect mode).

4.7.2.2 TMD2

TMD2 is specified by each Main Mode.

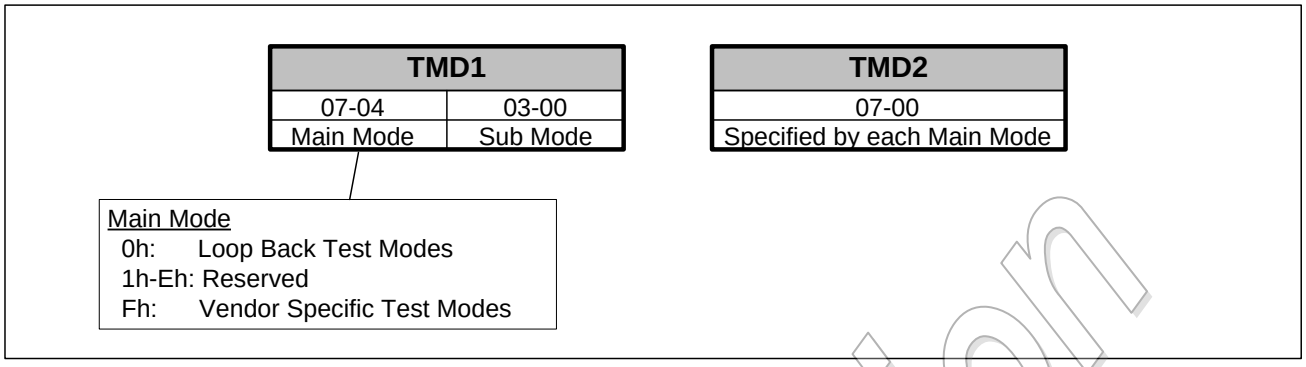
- **"Loop Back Direction"(07)**: determines whether Forward Loop back or Backward Loop back. When this bit is changed, the change of Loop Back Direction is done immediately.
  Everytime Loopback direction is changed, both D0 and D1 are set to input at first in order to re-connect Test tool.

  After re-connecting Test tool to Device/Host:
  <In case Loop Back Direction bit is changed 0 to 1>
  - After Device detects SYN from D1, D0 is enabled as output, and then the change of Loopback direction is done.
  - After Host detects SYN from D0, D1 is enabled as output, and then the change of Loopback direction is done.

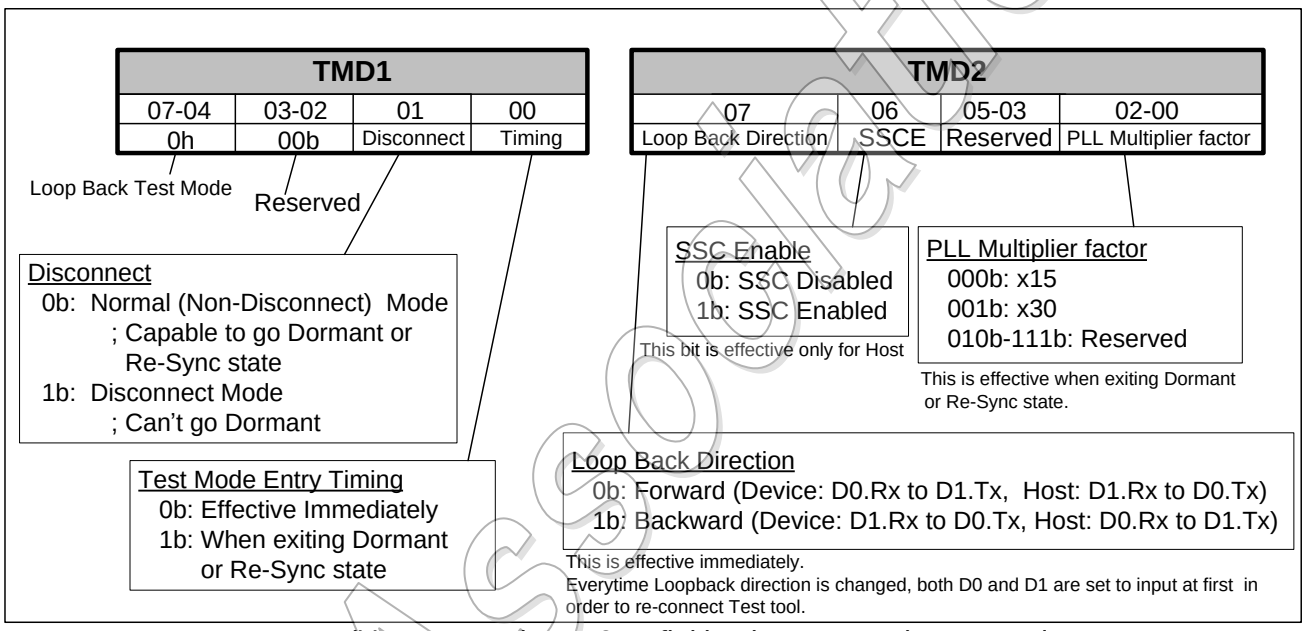
  <In case Loop Back Direction bit is changed 1 to 0>
  - After Device detects SYN from D0, D1 is enabled as output, and then the change of Loopback direction is done.
  - After Host detects SYN from D1, D0 is enabled as output, and then the change of Loopback direction is done.

- "**SSCE"(06)**: controls Host SSC On/Off if Host supports SSC function. This bit is not effective to Device.

- **"PLL Multiplier factor"(02-00)**: determines PLL Multiplier (x15 or x30). The actual change of PLL Multiplier is done after exiting Dormant or Re-Sync state.



(a) General Definition



(b) TMD1 and TMD2 Definition in Loop Back Test Mode

Note: Symbols are described in 8-bit domain for the convenience of explanation. Actual symbols to enter and exit test mode are transferred from test equipment after 8b/10b encoding.

Figure 4-20: Structure of TMD1 and TMD2

4.7.3 Test Modes

Parameters for entering each Test mode are described as follows. The sequences for entering each test mode are shown in Figure 4-21 and Figure 4-22.

TMD1 Modes:

- 00h: Normal Mode At Once
  Setting in Sub Modes 03-01(Normal Mode) is effective immediately.
  After entering a test mode, it is possible to go back to Dormant state.

- 01h: Normal Mode Through Dormant state
  Setting in Sub Modes 03-01(Normal Mode) is effective when exiting Dormant state.
  After entering a test mode, it is possible to go back to Dormant state.

- 02h: Disconnect Mode At Once
  Setting in Sub Modes 03-01 (Disconnect Mode) is effective immediately.
  After entering a test mode, the Device cannot go Dormant state.

- 03h: Disconnect Mode Through Dormant state
  Setting in Sub Modes 03-01 (Disconnect Mode) is effective when exiting Dormant state.
  After entering a test mode, the Device cannot go Dormant state.

TMD2 Modes:

PLL Multiplier (Bit 02-00)

- 000b: x15
- 001b:x30
- 010b-111b: Reserved

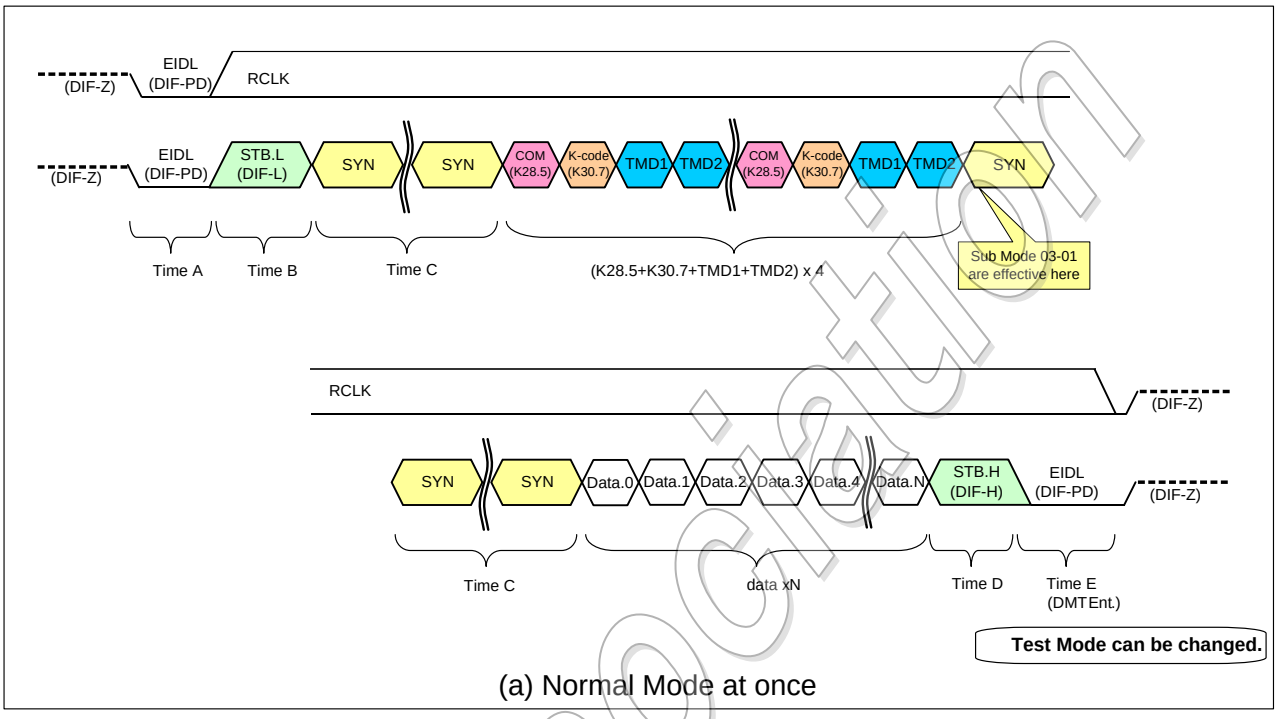
Change of this field is effective when exiting Dormant or Re-Sync state. Clock frequency may be changed only during Dormant or Re-Sync state.

Loop Back Direction (Bit 07)

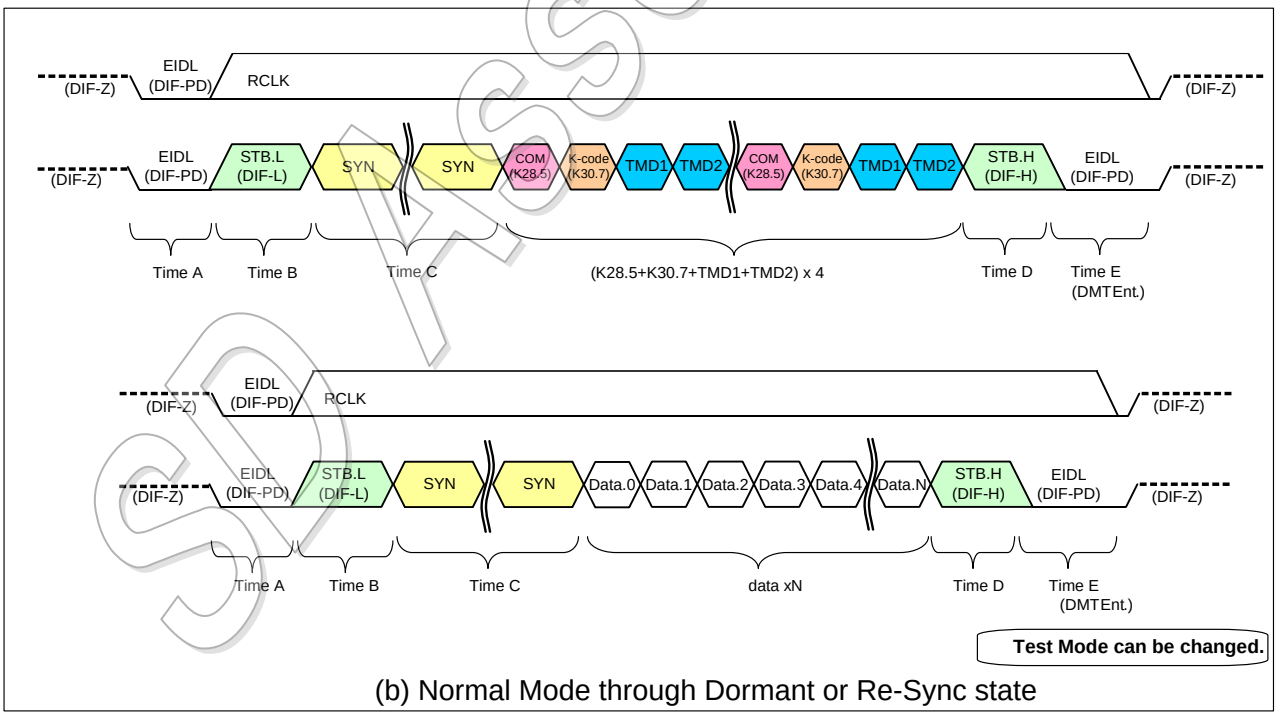
- 0b: Forward Loop Back (means from D0.Rx to D1.Tx)
- 1b: Backward Loop Back (means from D1.Rx to D0.Tx)

When this bit is changed, both D0 and D1 are set to input mode immediately.

Time A = EIDL Length = After Power up 100ms (min.) (Manual Start) and after that 200us.
Time B = Teidl_stb = 200us(min.)
Time C = Tactivate = After Power up 100ms (min.) and after that 2ms (min.)
Time D = T_EIDL_ENTRY = 4SI (min.) PHY Spec. defines as fixed but test mode defines as min.
Time E = T_DMT_ENTRY = 750RCLK (min.)



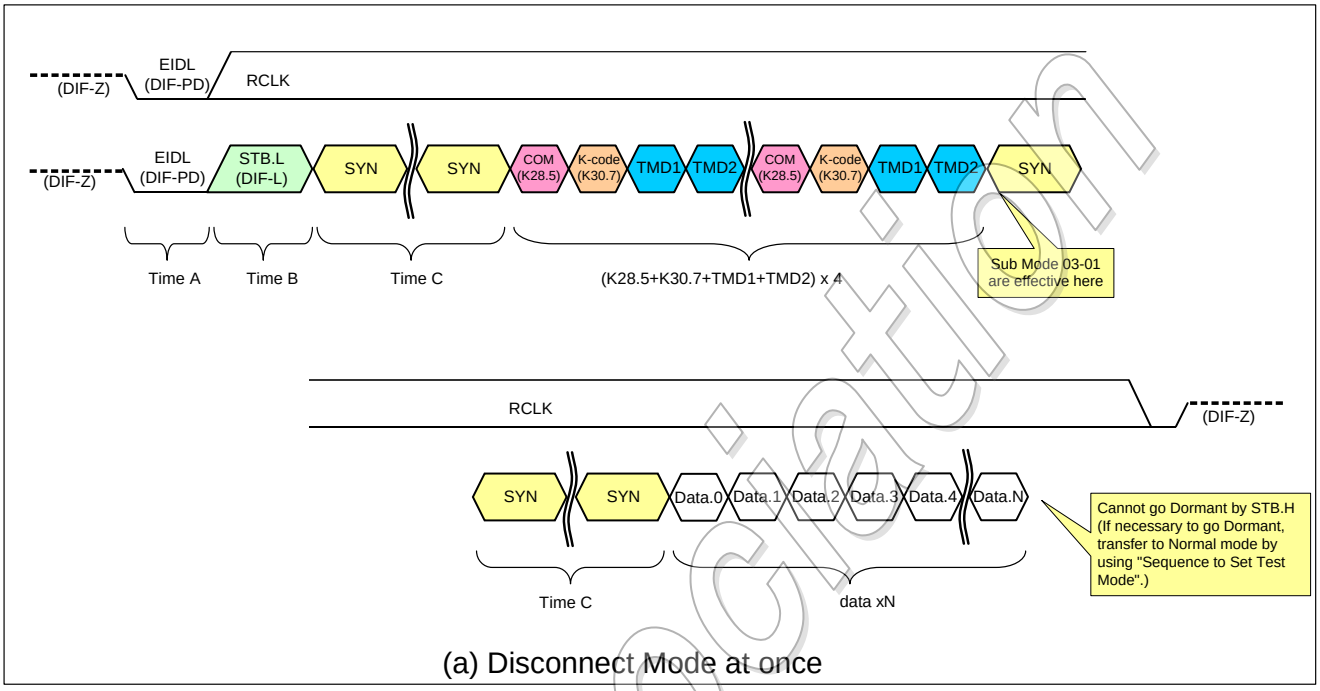
(a) Normal Mode at once



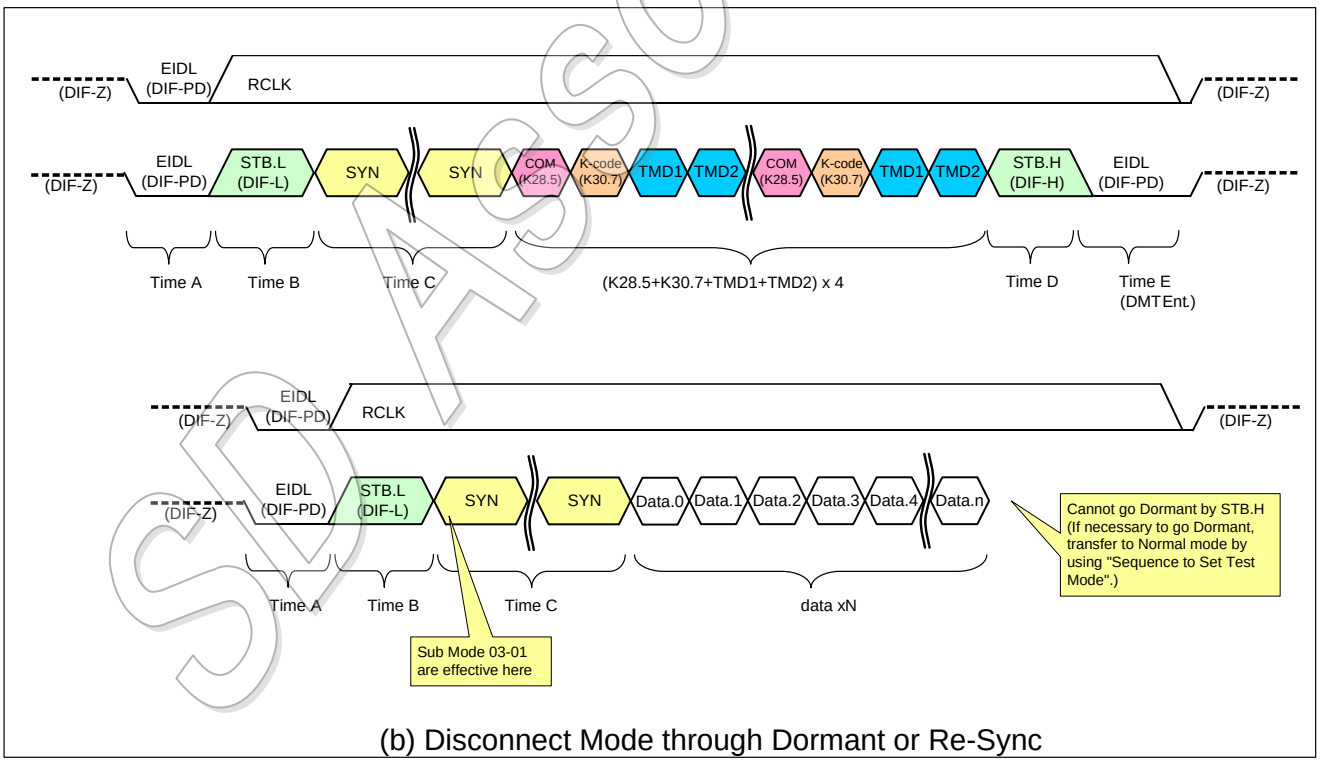
(b) Normal Mode through Dormant or Re-Sync state

Figure 4-21: Normal Modes Sequence

Time A = EIDL Length = After Power up 100ms (min.) (Manual Start) and after that 200us.
Time B = Teidl_stb = 200us(min.)
Time C = Tactivate = After Power up 100ms (min.) and after that 2ms (min.)
Time D = T_EIDL_ENTRY = 4SI (min.) PHY Spec. defines as fixed but test mode defines as min.
Time E = T_DMT_ENTRY = 750RCLK (min.)



(a) Disconnect Mode at once



(b) Disconnect Mode through Dormant or Re-Sync

Figure 4-22: Disconnect Mode Sequence

4.7.4 An Example Procedure

An example procedure for entering test mode is shown in Figure 4-23. This procedure is about Backward Loop Back test under the condition that PLL Multiplier is x30.

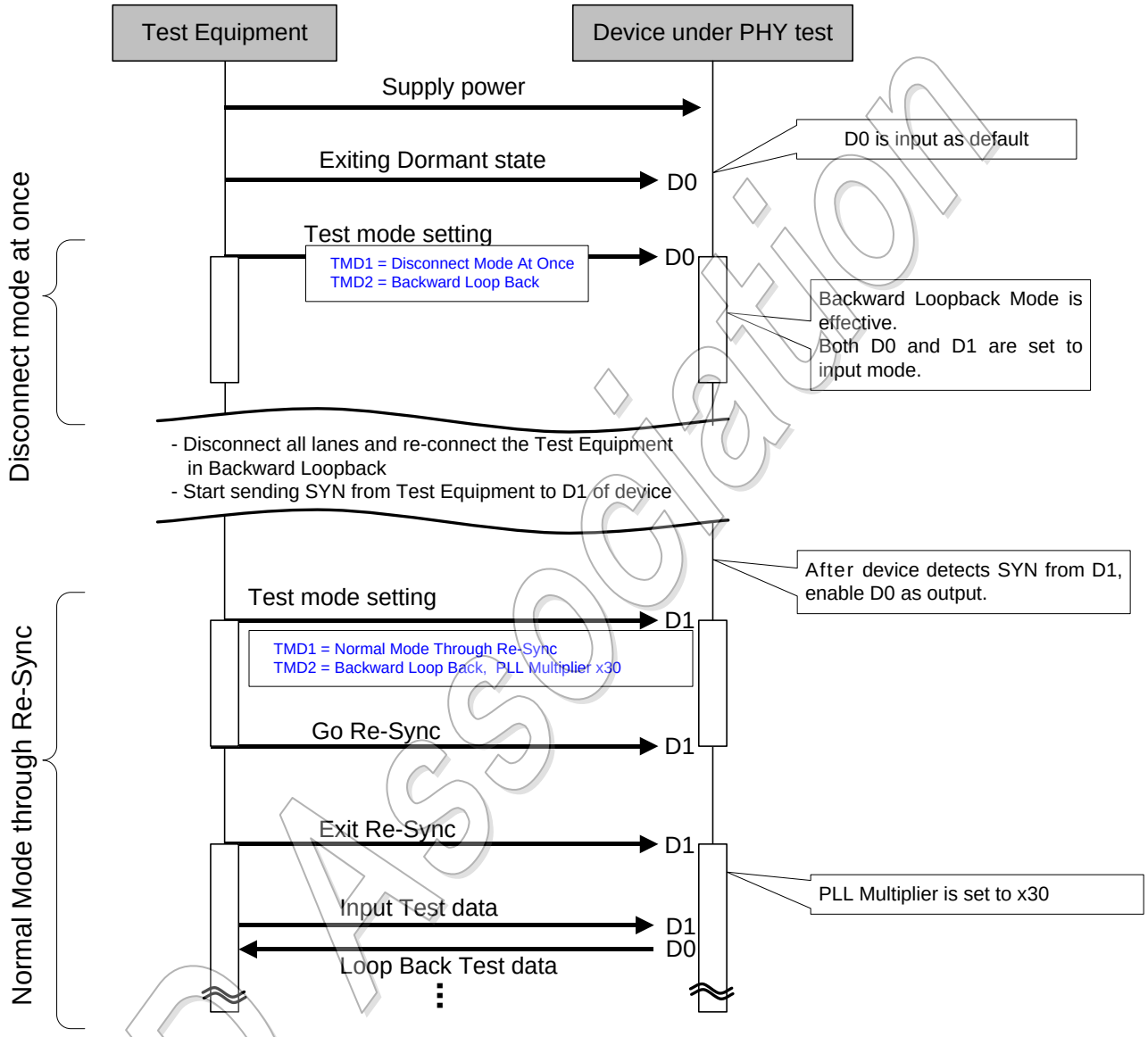


Figure 4-23: An Example Procedure (Backward Loop Back Test with PLL Multiplier is x30)

4.7.5 Test Mode for Host

Host shall have "Slave Mode" and enter this mode for Host PHY test. The Slave Mode is correspondent to Dormant state of a Device. The method to enter the Slave Mode depends on Host implementation. Figure 4-24 shows the states regarding Host PHY Test.

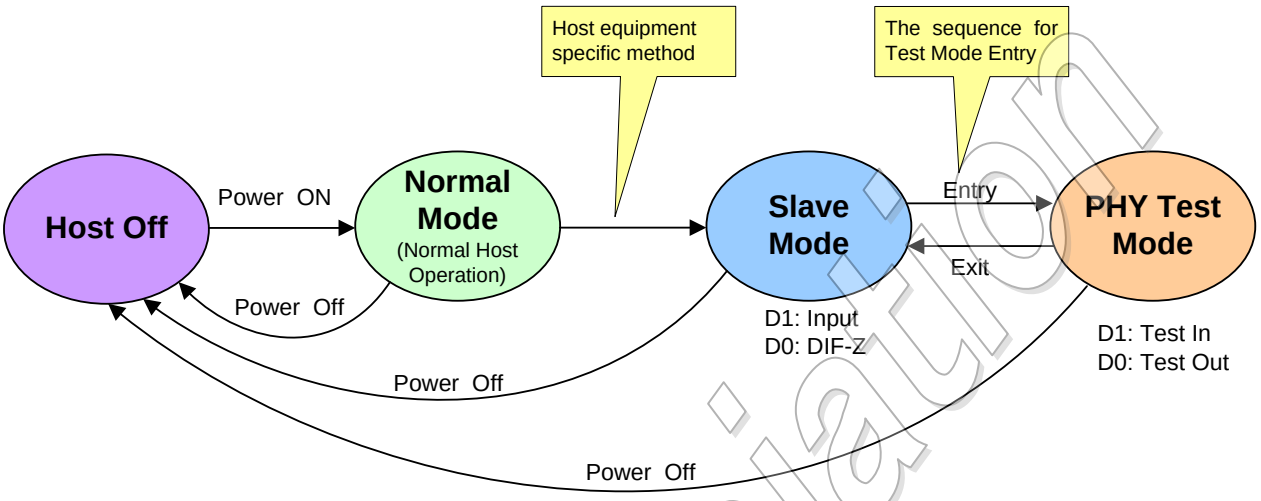


Figure 4-24: States Regarding Host PHY Test

In Slave Mode,
- Host watches D1 Line to detect the sequence for Test Mode entry.
- Host continuously provides RCLK at any frequency selected by itself.
- Disable SSC when entering Slave Mode as a default.

When entering PHY test mode from Slave mode,
- PLL Multiplier may be changed by TMD2
- Backward Loop Back mode may be selected by TMD2
- SSC Enable may be changed by TMD2

When the Slave Mode and PHY Test Mode, test equipment may be connected to Host.

The following is recommended for Host:
- Disable all timeout detectors when the sequence for Test Mode entry is detected

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5. Link Layer Specification

5.1 Link Layer Overview

Figure 5-1 shows the overview of Link Layer.

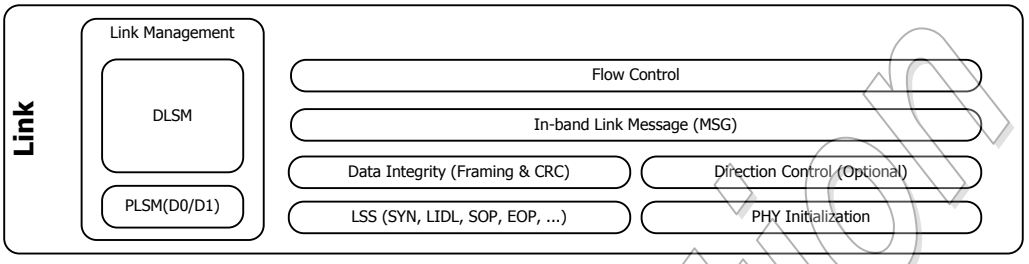


Figure 5-1 : Link Layer Overview

Link Layer is in charge of controlling data flow and making management for LINK and PHY. The key features of Link Layer are defined as follows.

- **PHY Initialization Control**
- **Data Integrity:** Packet framing with SOP and EOP, CRC generation and checking.
- **Flow Control:** Fixed window flow control only for Data packet transfer.
- **Direction Control:** Duplex mode switching between FD mode and 2L-HD mode (Optional).
- **Power Management (PM):**
  Lane level power saving state (EIDL: Electrical Idle)
  Link level power saving state (Dormant)
- **PHY and LINK error handling**
- **Packet Bypassing**

5.2 Link Layer Protocol

5.2.1 Protocol Overview

Link Layer generates Link Symbol Set (LSS) to control PHY (synchronization, direction control, etc.), frames UHS-II packet (refer to Section 3.4.1 for more details) in terms of packet separation and data integrity. When Link accepts outgoing packets from upper layer (CM-TRAN), it generates CRC for each packet and the packet accompanied by its CRC is framed with SOP and EOP LSS. The framed UHS-II packets are transmitted through UHS-II bus via PHY. Each byte of original packet and CRC is encoded to 8b/10b Data symbol (D) in PHY. Refer to Chapter 4 for the 8b/10b encoding scheme.

5.2.2 Link Symbol Set (LSS)

Section 5.2.2 is a blank in the Simplified Addendum.

5.2.3 Header for UHS-II Packet

Figure 5-2 illustrates header structure for UHS-II packet that is compliant to UHS-II Addendum Version 1.00. First, Node ID whose range is from 0 to 15 denotes a value to identify the individual Hosts and Devices. Node ID = 0 is set aside for Host. For Devices, number 15 is set as the initial value for Node ID after I/F power cycle or FULL_RESET, and one of numbers from 1 to 15 is assigned to each Device by Enumeration process described in Section 0. Note that Node ID of Boot Device is temporarily assigned for Boot Code Loading at first, then one of numbers from 1 to 15 is assigned by Enumeration.
Considering future extension, header format is allowed to be changed linked to LINK/TRAN Major Revision in CFG_REG (refer to Table 6-9).

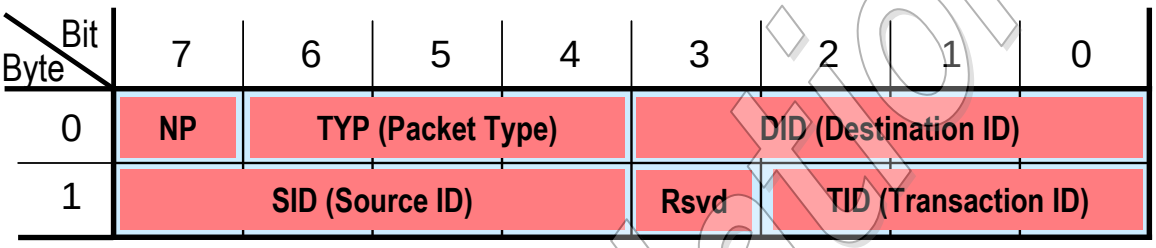


Figure 5-2 : Header Format

UHS-II Packet Header shall be composed of the following fields;

- **NP (Native Packet):** Indicator whether the packet follows native protocol or not
  - 0: not native protocol (application specific protocol)
  - 1: native protocol
  - NP field in MSG shall be set to '1'. (MSG packet transaction is defined on native protocol.)
- **TYP[2:0] (Packet Type):** Packet type described in Table 5-3.
- **DID[3:0] (Destination ID):** Node ID of destination Device or Host.
- **SID[3:0] (Source ID):** Node ID of source Device or Host.
- **TID[2:0] (Transaction ID):** Identification number of outstanding transactions
  - The TID field is defined in order to manage outstanding transactions for multiple command execution. (Details of multiple command execution will be defined in the future specification.)
- **Rsvd (Reserved):** Reserved bits. Initiator shall set them to '0', and receiver shall ignore them.

TYP [2:0]	Packet Type	Description	Note
000b	CCMD	Control Command packet	TLP
001b	DCMD	Data Command packet	TLP
010b	RES	Response packet	TLP
011b	DATA	Data payload packet	TLP
111b	MSG	Message packet	Handled in LINK
Others	Reserved	Reserved	--

Table 5-3 : Packet Type Encodings and Descriptions

DID and SID are used as routing information. If SID = DID, the packet is handled as broadcast. For UHS-II Addendum Version 1.00, broadcast packet is applicable only for CCMD. Details of broadcast CCMD are described in Section 6.2.2.3.
Basically, Host or Device processes a packet with the same DID as its own Node ID. In case of receiving a packet with different DID from own Node ID, Host or Device does not process it except broadcast packet and bypasses it to the next Host or Device on the bus. If Host or Device receives broadcast packet (SID = DID), it shall process even when DID is not equal to its own Node ID, and transmit to the next Host or Device.

5.2.4 Message Packet (MSG)

5.2.4.1 Overview

Message Packet (MSG) is introduced to realize flow control, error or interrupt handling instead of hard-wired signals.

Figure 5-3 illustrates a structure of MSG packet. Note that NP in Header shall be set to 1.

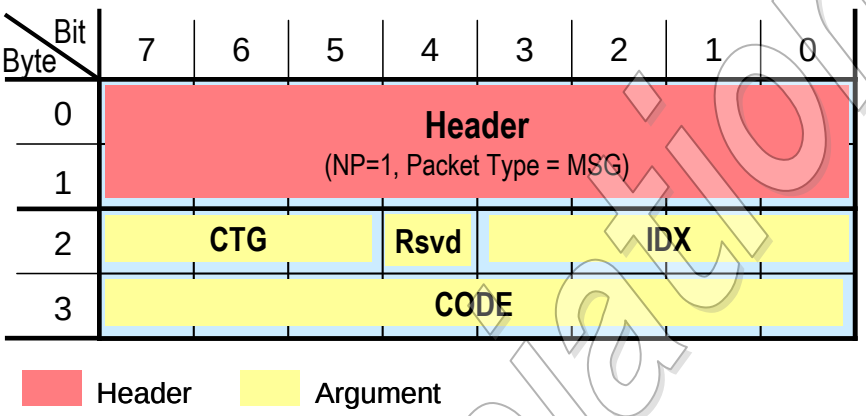


Figure 5-3 : MSG Format

- **CTG[2:0] (Message Category):** indicates category of MSG.
  - Refer to Table 5-4 for more details.
- **IDX[3:0] (Message Index):** indicates message Index related to CTG. Refer to Table 5-4 for more details.
- **CODE[7:0] (Message Code):** indicates code to define message detail.
- **Rsvd (Reserved):** Reserved bits. Initiator shall set them to '0', and receiver shall ignore them.

CTG		IDX		CODE	Description
Bits	**Name**	**Bits**	**Name**		
000b	LMSG (See Note (1))	0000b	FCREQ	Refer to Table 5-5	Flow Control Request from initiator of DATA
		0001b	FCRDY	Refer to Table 5-5	Flow Control Ready from receiver of DATA
		0010b	STAT	Refer to Table 5-6	Status of DATA Burst transfer notified from receiver of DATA
		others	Reserved	Reserved	Reserved
011b	INT	all	Reserved	Reserved	Reserved for interrupt
100b	AMSG	See Note (2)			Application specific message. It depends on application defined in CFG_REG.
Others	Reserved	all	Reserved	Reserved	Reserved

Note:
(1) LMSG is handled within LINK.

Table 5-4 : Detailed Definition of MSG

Also refer to Section 6.2.2.8 for operating reserved bits in the packet.

5.2.4.2 CODE Definition for Each IDX

Table 5-5 describes the CODE definition of FCREQ and FCRDY.

Bits	Identifier	Value	Description
7	UNRECOVERABLE_ERROR	'0' = no error '1' = error	Error occurs that it cannot be recovered by DATA Burst Retry.
6:0	Reserved	Reserved	Reserved

Table 5-5 : Code Definition of FCREQ and FCRDY

If Host receives an FCREQ, FCRDY or STAT MSG with UNRECOVERABLE_ERROR = 1, it needs to abort the data transaction by issuing TRANS_ABORT CCMD or encapsulated CMD12 (in case of SD-TRAN). This bit is not cleared until the transaction is aborted or completed. And once this bit is set, the transaction cannot be completed successfully.

Table 5-6 describes the CODE definition of STAT. Refer to Section 5.2.6 for framing rules or CRC.

Bits	Identifier	Value	Description
7	UNRECOVERABLE_ERROR	'0' = no error '1' = error	Error occurs that it cannot be recovered by DATA Burst Retry.
6:1	Reserved	Reserved	Reserved
0	RECOVERABLE_ERROR	'0' = no error '1' = error	Error occurs that it can be recovered by DATA Burst Retry. This bit is set as a request for DATA Burst Retry.

Table 5-6 : Code Definition of STAT

UHS-II has two types of error identifiers, one is UNRECOVERABLE_ERROR and the other is RECOVERABLE_ERROR. Refer to Section 5.2.5 for more details.
If LINK of DATA initiator side receives a STAT MSG with RECOVERABLE_ERROR = 1 and UNRECOVERABLE_ERROR = 0 just after a DATA Burst transmission, it needs to start performing DATA Burst Retry. Note that RECOVERABLE_ERROR in STAT MSG represents status of preceding DATA Burst..

5.2.4.3 MSG Duplication

For the purpose of getting transaction robustness, the MSG initiator shall send the same MSG packets twice for one message transmission. There are no gaps between the duplicated MSG packets.
Receiver shall recognize the MSG reception successful if at least one of MSG packets is recognized as a valid MSG. In other word, if the receiver detects the first MSG packet as a valid MSG, it can ignore the second one. Else if it fails the first MSG but succeeds to get the second one, it shall be considered as a valid MSG reception. Otherwise, it is recognized as MSG reception error.
From now on, "MSG" means the duplicated MSG packets if not otherwise specified.

5.2.5 Error Identifier

Details of error identifiers in UHS-II are as follows.

- **UNRECOVERABLE_ERROR:** includes ILLEGAL_HEADER_ERROR, DEVICE_SPECIFIC_ERROR and RETRY_EXPIRE_ERROR as follows.
  - **ILLEGAL_HEADER_ERROR:** indicates error detection in UHS-II Header on the condition of no CRC errors.
  - **DEVICE_SPECIFIC_ERROR:** is defined as a general error occurred in outside of UHS-II interface. For example, memory write error is treated as a DEVICE_SPECIFIC_ERROR. That

kind of error is indicated from outside of UHS-II (backend, for example) in receiver side internally.

- **RETRY_EXPIRE_ERROR:** indicates the retry counter reaches to its own "MAX_RETRY_NUM".

- **RECOVERABLE_ERROR:** includes FRAME_ERROR and CRC_ERROR as follows.
  - **FRAME_ERROR:** indicates detection of framing error. In other words, a control packet or DATA Burst violates the framing rules described in Section 5.2.6.
  - **CRC_ERROR:** indicates that CRC error is detected from a control packet or at least one of Framed DATA packet in the previous DATA Burst.

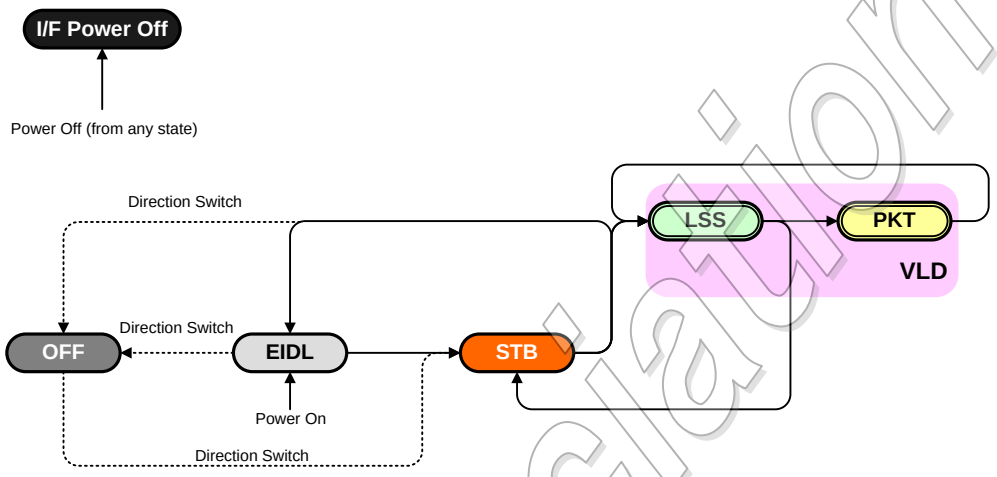
Basically these error identifiers are indicated in Status Register (ST_REG) described in Section 6.2.10. Moreover, when Device detects these errors during DATA Burst transmission, it should notify them to Host by STAT, FCREQ, or FCRDY MSG. Host can detect such errors by those MSGs or timeout.

Section 5.2.6 to Section 5.2.7 is a blank in the Simplified Addendum.

5.2.8 Physical Lane State Machine (PLSM)

5.2.8.1 Overview

Physical Lane State Machine (PLSM) denotes transmitting / receiving status for each data Lane. Figure 5-13 shows a top level state diagram of PLSM. PLSM is defined for both Tx and Rx of each data Lane and those are synchronously managed between Host and Device. For example, when D0.Tx of Host transits to EIDL, D0.Rx of Device shall also transit to EIDL soon afterward.



Note 1: It is allowed to go through EIDL before transiting to OFF.
Note 2: PLSM shall go through STB.H when transiting from VLD to EIDL, and STB.L when transiting from EIDL to VLD. Also refer to Figure 5-22 for the detailed PLSM transitions.

Figure 5-13 : Physical Lane State Machine (PLSM)

- **I/F Power Off state:** State indicating that I/F power supply (e.g. VDD2 in SD Memory) is off. Both Tx and Rx transit to this state from any state only when I/F power supply is off.
- **OFF state:** State indicating Tx or Rx is disabled. Both Tx and Rx transit to this state when direction switch occurs. In this state, both Tx driver and Rx termination resistor of a Lane are turned off. So, the Line between them becomes high impedance and floating state (DIF-Z).
- **EIDL state:** Electrical-Idle state with DIF-PD (pull-down) as a Lane level power saving state. In this state, the Lane state is kept to DIF-PD.
- **STB state:** Lane standby state with DIF-L (STB.L) or DIF-H (STB.H) required for transition from or to EIDL state. STB.L and STB.H are used as a prefix and postfix of a group of valid symbols respectively. Physically, Tx side keeps sending DIF-L during STB.L and DIF-H during STB.H, respectively. Rx side can receive (sample) serial data as a series of bit clocked data symbol at Deserializer after its PLL is locked. During wakeup from Dormant state, Rx side can transit from EIDL to STB.L when Amplitude Detector on Rx detects the amplitude difference between DIF-PD and DIF-L.
- **VLD state:** State for valid 8b/10b symbols including LSS sub-state and PKT sub-state.
  - **LSS sub-state:** State for Link layer symbol set including multiple symbol states.
  - **PKT sub-state:** State for packet including multiple symbol states.

Table 5-7 : PLSM State Definition for Tx and Rx

Following of Section 5.2.8 is a blank in the Simplified Addendum.

5.2.9 Data Link State Machine (DLSM)

5.2.9.1 Overview

Data Link State Machine (DLSM) is responsible for LINK Management such as LINK synchronization, direction control, PM and so on. Figure 5-15 shows a state diagram of DLSM.

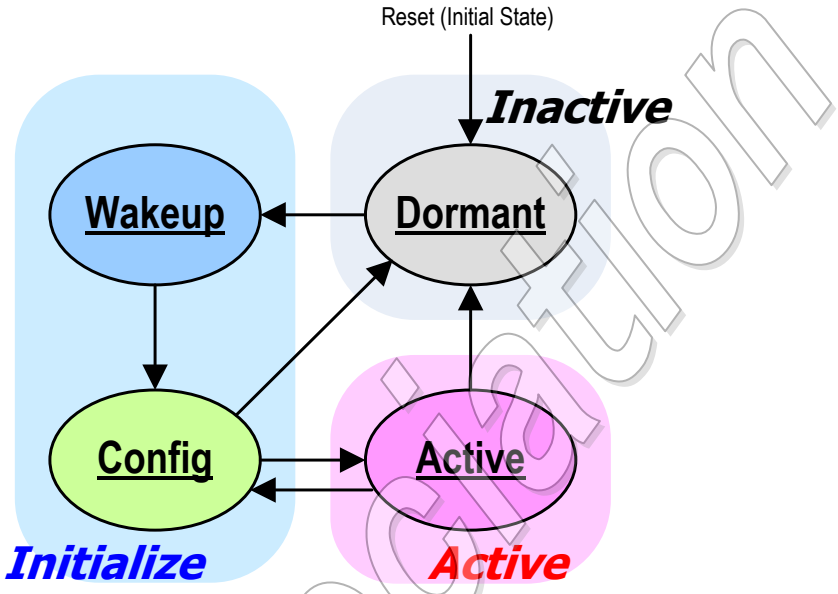


Figure 5-15 : Data Link State Machine (DLSM)

- **Dormant:** Link level power saving state. All Lanes are EIDL and PLL can be powered off.
- **Wakeup:** PHY initialization state with two sub-states.
- **Config:** Device configuration state in which Device is initialized, enumerated and functions are configured to be available at Active state.
- **Active:** Normal operation state with four sub-states.

Following of Chapter 5 is a blank in the Simplified Addendum.

6. Transaction Layer Specification

The details of UHS-II protocol including packet format, Configuration, state machine, initialization and flow control are described in this chapter.

6.1 Transaction Layer Overview

Figure 6-1 shows the overview of Transaction Layer.

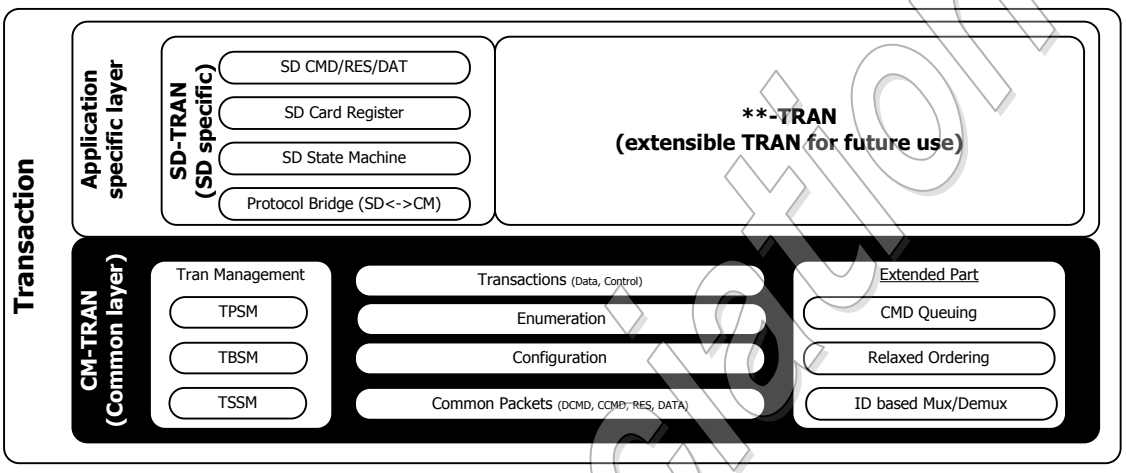


Figure 6-1 : Transaction Layer Overview

The key features of Transaction Layer are defined as follows:

- **New packet based protocol considering Legacy SD compatibility**
  - ID based routing for multiple device connectivity
  - CM-TRAN for common architecture between Host and Device

Transaction Layer consists of two sub-layers called CM-TRAN (lower sub-layer) and application specific layer including SD-TRAN (upper sub-layer). This layering is intended to define the common part of TRAN (CM-TRAN) between Host and Device. As a result, the same CM-TRAN can be used in both Host and Device side.
CM-TRAN provides basic functions to realize transactions on UHS-II native protocol.
CM-TRAN components are the following;

- **Generating UHS-II common packets and processing**
  - Configuration mechanism
  - Transaction management supporting multiple device connection
  - Future extension support (e.g. CMD Queuing)

CM-TRAN is also defined to be the common sub-layer between all application specific layers in order to realize UHS-II specific functions (e.g. multiple device connection, CMD Queuing, etc.) with application specific protocol.
For example, in Figure 6-1, CM-TRAN can provide SD protocol with a CMD Queuing feature as a future extension.

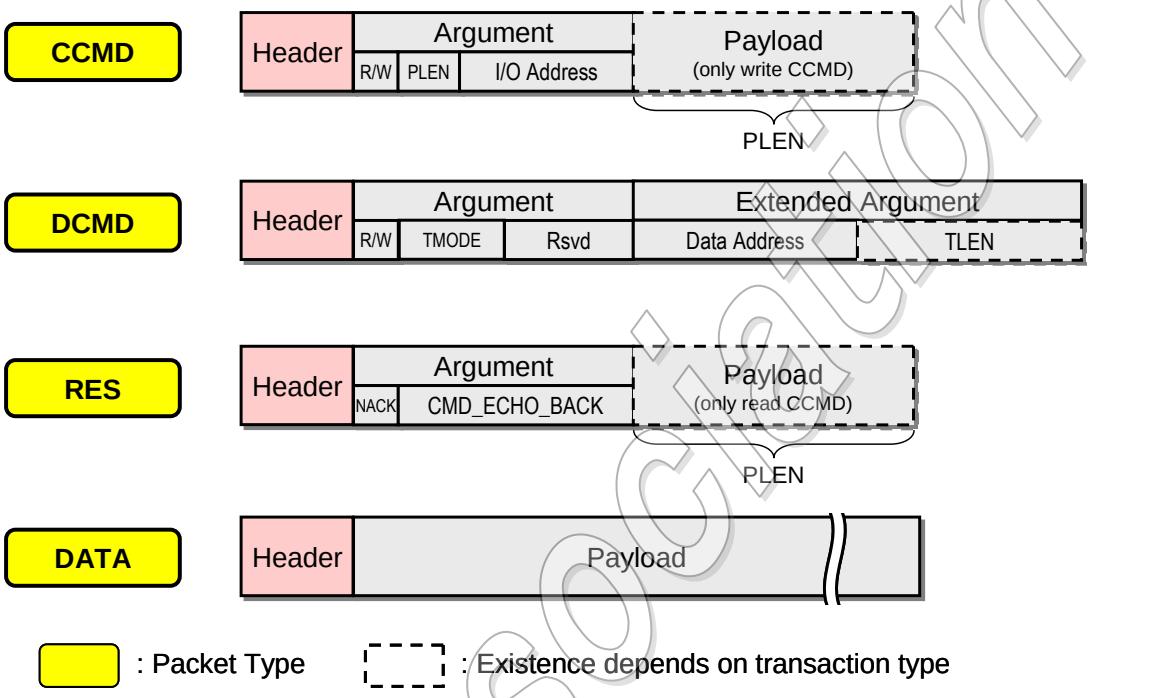
SD-TRAN is an application specific layer for compatibility with SD protocol and preserves the same state machine and registers as Legacy SD protocol. SD-TRAN works as a protocol bridging between Legacy SD and UHS-II native protocol. (Refer to Chapter 7 for details of SD-TRAN.)

Other application specific layers (**-TRAN) can be defined for future extension.

In Chapter 6, the details of CM-TRAN are presented.

6.1.1 Packet Types and Format Overview

Figure 6-2 illustrates the Transaction Layer Packet (TLP) types and format overview.



Notes
PLEN : Length of payload field in CCMD or RES
TMODE : Transfer mode to represent detailed transfer settings
TLEN : Transfer Length (total length of data transmitted during a transaction)
CMD_ECHO_BACK : Argument of the preceding CMD is copied

Figure 6-2 : TLP Format Overview

In Transaction Layer, four TLP types are defined to realize Legacy SD-compatible protocol and new functions of UHS-II native protocol.

- CCMD (Control CMD): control command packet for accessing to control registers in I/O space
- DCMD (Data CMD): data command packet for transferring data
- RES (Response): response packet associated with CCMD or DCMD
- DATA (Data payload): packet for data transmission

TLP consists of Header, Argument and Payload.
Each type of TLP shall have a common "Header". Header includes ID fields for packet identification and routing information. "Argument" is used for setting supplementary information such as data length (PLEN, TLEN), address information (I/O address, data address) and other information exchanged between Host and Device (TMODE). Only DCMD has "Extended Argument" for setting more information about data length and address. "Payload" is the field for setting data payload to be transmitted.

Argument in CCMD includes read/write flag, I/O address and payload length (PLEN) field. In the case of write CCMD, PLEN represents the length of write data which is assigned in Payload of CCMD. In the case of read CCMD, PLEN basically represents the length of read data which is assigned in Payload of the following RES.
Argument in DCMD includes read/write flag and transfer mode (TMODE) for representing detailed transfer settings such as Length Mode (TLEN is specified or not), TLEN Unit Mode (Block Mode or Byte Mode), etc.
Extended Argument includes transfer length (TLEN) field if Length Mode in TMODE is set to "TLEN is specified". TLEN represents the total length of data to be transmitted by a DCMD.
Extended Argument in DCMD also includes data address (DADR). The unit of data address is specified in Data Access Mode (DAM) in TMODE field. DAM also specifies which address space is to be accessed (refer to DAM explanation in Section 6.2.2.4).
Argument in RES is set to the same value as Argument in the corresponding CMD except read/write flag (command echo back). NACK field shows whether the associated CMD has an error or not. Only the case of CCMD read transaction, Payload field in RES exists and its size is shown by PLEN.

Figure 6-3 shows the basic concept of control transaction and data write/read transaction sequence.

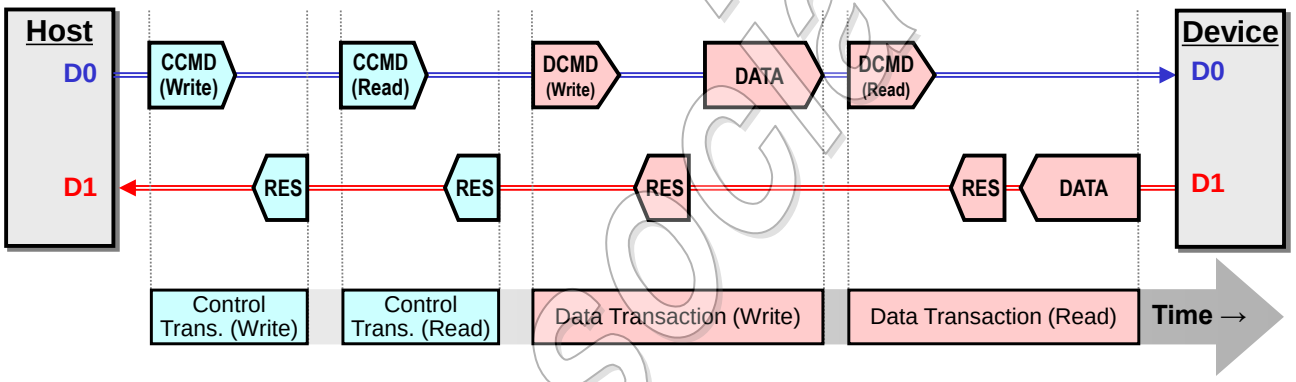


Figure 6-3 : Control Transaction and Data Transaction Sequence

The sequences of control transaction and data transaction are defined as follows;

- Control Transaction: CCMD -> RES (without DATA packet)
  - Broadcast control transaction does not bring RES.
- Data Transaction: DCMD -> RES -> DATA

Control transaction is performed for accessing to UHS-II I/O Registers such as Configuration Register, Command Register and so on, and consists of CCMD from Host and RES from Device. Note that broadcast control transaction does not accompany RES, and the transaction completes when Host receives broadcast CCMD. Special CCMDs such as FULL_RESET or TRANS_ABORT are defined in Command Register (refer to Section 6.2.12).
Data transaction is performed for transferring data, and consists of DCMD from Host, RES from Device and DATA from Host or Device. Flow control shall be executed during data transaction.
After issuing a CMD, Host shall not issue all types of packet until RES is received

6.2 Transaction Layer Protocol

6.2.1 UHS-II I/O Space and Memory Address Space

Two types of address spaces are defined.

- **UHS-II I/O space:** Address space for UHS-II I/O Registers expressed by 14bit address number.
- **Memory address space:** Logical address for the memory Device.

Figure 6-4 shows the layout of UHS-II I/O space.

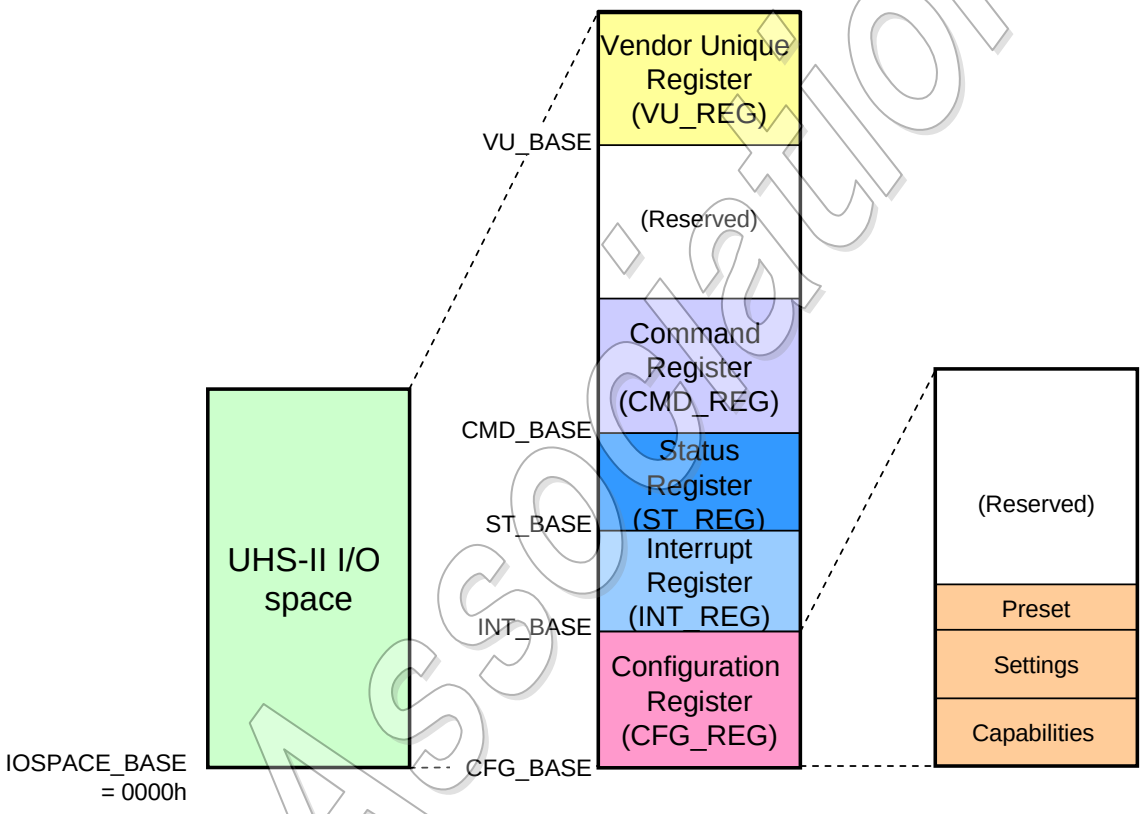


Figure 6-4 : UHS-II I/O Space Layout for Device

UHS-II I/O space consists of Configuration Register (CFG_REG), Interrupt Register (INT_REG), Status Register (ST_REG), Command Register (CMD_REG) and other areas including Vendor Unique Register (VU_REG). Host can access to the registers described below only by a CCMD.

- Configuration Register (CFG_REG): Register to assign device-dependent capabilities and determined operating settings during Configuration.
- Interrupt Register (INT_REG): Register for realizing interrupt.
- Command Register (CMD_REG): Register to assign UHS-II CCMDs (e.g. reset, abort, etc.)
- Vendor Unique Register (VU_REG): Register to be defined by vendors individually.

Register area indicated by "Reserved" means that it is initialized to zero and writing operation to them is ignored. The followings are Device behavior when accessed to its Reserved bit including bits inside CMD_REG.

- **P2P CCMD Read:** Device shall issue RES with NACK=0 and its Payload field corresponding to the reserved bit is set to 0.
- **P2P CCMD Write:** Device shall issue RES with NACK=0 and value of reserved bit is not changed.

- **Broadcast CCMD Write:** Device shall forward broadcast CCMD to the next node, and value of reserved bit is not changed.

Table 6-1 shows the map of UHS-II I/O space. Offset means the relative address based on IOSPACE_BASE = 0000h.

Offset		Register
Byte address	IOADR	
0000h : 03FFh	000h : 0FFh	Configuration Register (CFG_REG)
0400h : 05FFh	100h : 17Fh	Interrupt Register (INT_REG)
0600h : 07FFh	180h : 1FFh	Status Register (ST_REG)
0800h : 0BFFh	200h : 2FFh	Command Register (CMD_REG)
0C00h : 3BFFh	300h : EFFh	Reserved
3C00h : 3FFFh	F00h : FFFh	Vendor Unique Register (VU_REG)

Table 6-1 : I/O Address Space Map

During Configuration, CFG_REG values are negotiated between Host and Device by CCMDs. Refer to Section 0 for details of Configuration procedure.

6.2.2 Packet Format Details

In this section, msb denotes "most significant bit", lsb denotes "least significant bit" respectively. (Notice that they are different from MSB or LSB.) Moreover, smaller byte in a packet is transmitted first

6.2.2.1 Header

Refer to Section 5.2.3 for details of Header structure.

6.2.2.2 CCMD

Figure 6-5 illustrates CCMD structure.

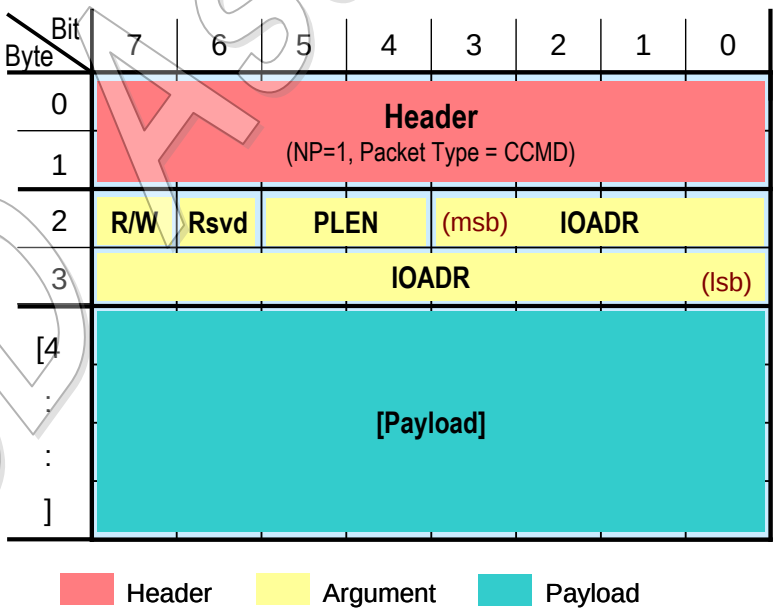


Figure 6-5 : CCMD Format

- **R/W (Read/Write):** Indicator for representing read or write command.
  - 0: Control read command
  - 1: Control write command
- **PLEN[1:0] (Payload Length):** Length of payload field in CCMD or RES.
  - PLEN field represents the length of payload field in CCMD or RES (Definition of PLEN is shown in Table 6-2)
  - In the case of write CCMD (R/W = 1), PLEN represents the length of write data which is assigned in Payload of CCMD.
  - In the case of read CCMD (R/W = 0), PLEN represents the length of read data which is assigned in Payload of the following RES.
- **IOADR[11:0] (I/O Address):** Address of register in UHS-II I/O space accessed by CCMD.
  - The unit of IOADR is 4 bytes. So quadruple of IOADR represents the absolute address in UHS-II I/O space.
  - It is transmitted in msb first, lsb last.
- **Payload:** Write data included with CCMD.
  - The length of payload field is assigned in PLEN.
  - In the case of read CCMD (R/W = 0), Payload field does not exist.
  - In the case that PLEN is set to "00b" (payload length is 0 byte), Payload field does not exist.
  - The Payload field is divided into a unit of DWORD (4byte data), and the transmission order within a DWORD is big endian. Refer to Figure 6-6 and Figure 6-7 for details of the transmission order of Payload. In these figures, bracketed numbers denote the bit order within a DWORD.
- **Rsvd (Reserved):** Reserved bits. Initiator shall set them to '0', and receiver shall ignore them.

PLEN[1:0]	Payload Length
00b	0 byte
01b	4 bytes
10b	8 bytes
11b	16 byte

Table 6-2 : Definition of PLEN

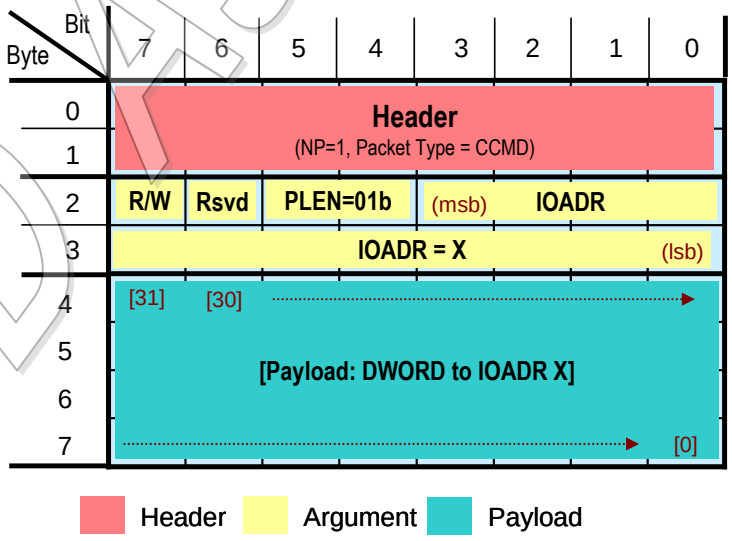


Figure 6-6 : Transmission Order of Payload in CCMD (PLEN = 01b)

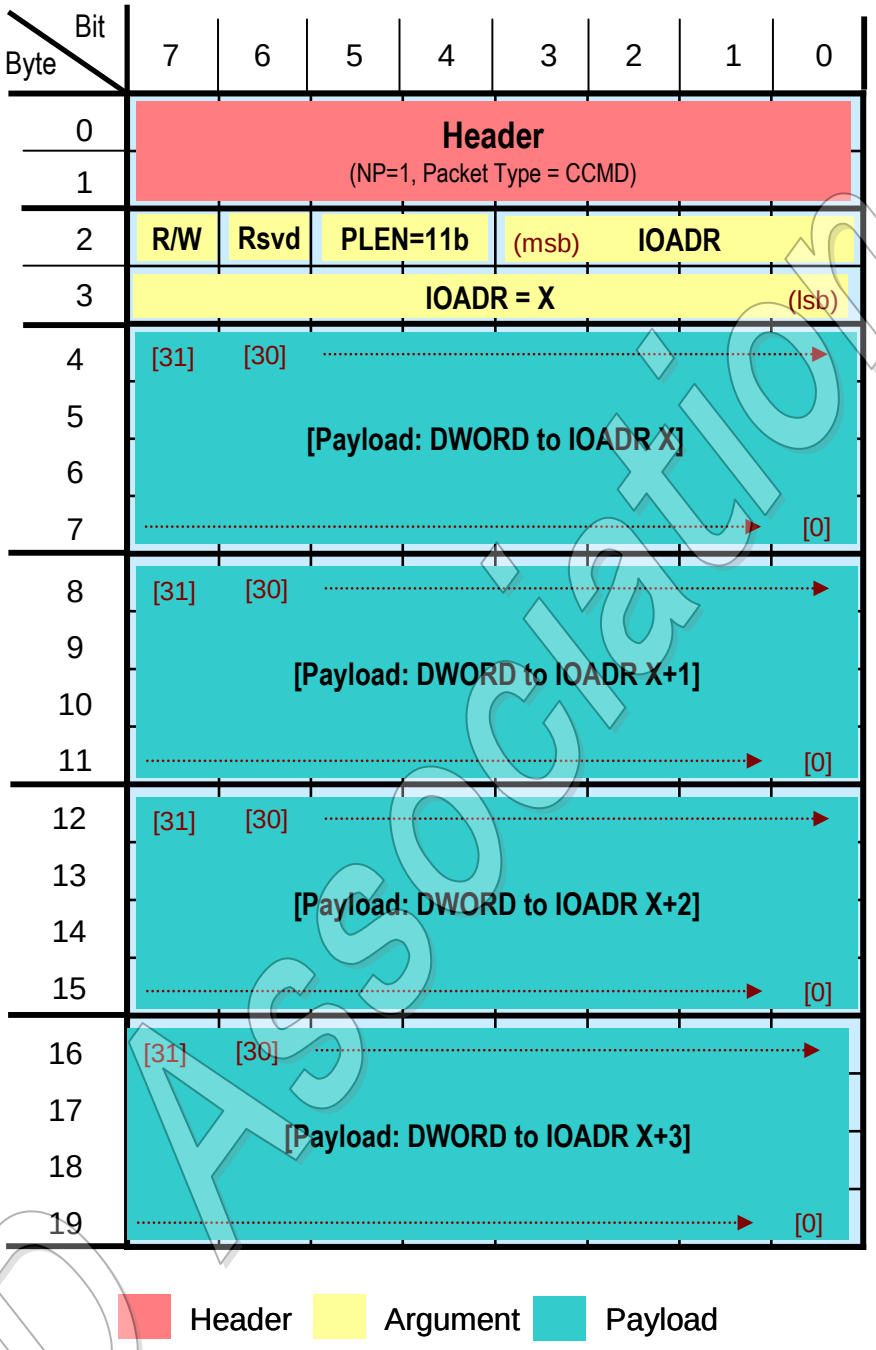


Figure 6-7 : Transmission Order of Payload in CCMD (PLEN = 11b)

In the case of application specific protocol (NP = 0), the definition of payload field existence may be different from the case of native protocol (NP = 1). Refer to Section 7.2.1.1 for details of CCMD format for SD application.

6.2.2.3 Broadcast CCMD

Broadcast CCMD operates to all Devices on the bus. On the other hand, CCMD that operates to a specified Device shown by DID is P2P CCMD.
In case of broadcast commands each Device may either transfer commands transparently (e.g. GO_DORMANT_STATE) or make some modifications to the continuing command to the following Node (e.g. ENUMERATE).
Features of broadcast CCMD are as follows.

- Broadcast CCMD issued by Host is represented as DID = SID = 0. In UHS-II Addendum Version 1.XX, broadcast packet is only permitted whose TYPE is CCMD and DID = SID = 0.
- If R/W = 1, broadcast CCMD writes content in its payload to the address in UHS-II I/O space calculated from IOADR for all connected Devices.
- Basically, broadcast CCMD with R/W = 0 is not available, but INQUIRY_CONFIG described in Section 6.2.8.3 is admitted as a special case of broadcast read CCMD. In this case, PLEN represents its payload length even if R/W = 0.
- Each Device shall process broadcast CCMD though DID is not equal to its own Node ID, and transmit it to the next Device or Host.
- Broadcast CCMD does not accompany RES. So if Host receives broadcast CCMD, Host shall terminate its transaction.
- If a Device detects some error from broadcast CCMD, it shall not transmit to the next Device or Host. In this case, Host can detect the error by timeout.

Note that the broadcast command behavior is the same for all topologies. In case of Hub topology the Hub shall emulate a Ring topology in a way that the CCMD shall be transferred in a serial manner passing the CCMDs between the Devices through the Hub.

6.2.2.4 DCMD

Figure 6-8 illustrates DCMD structure.

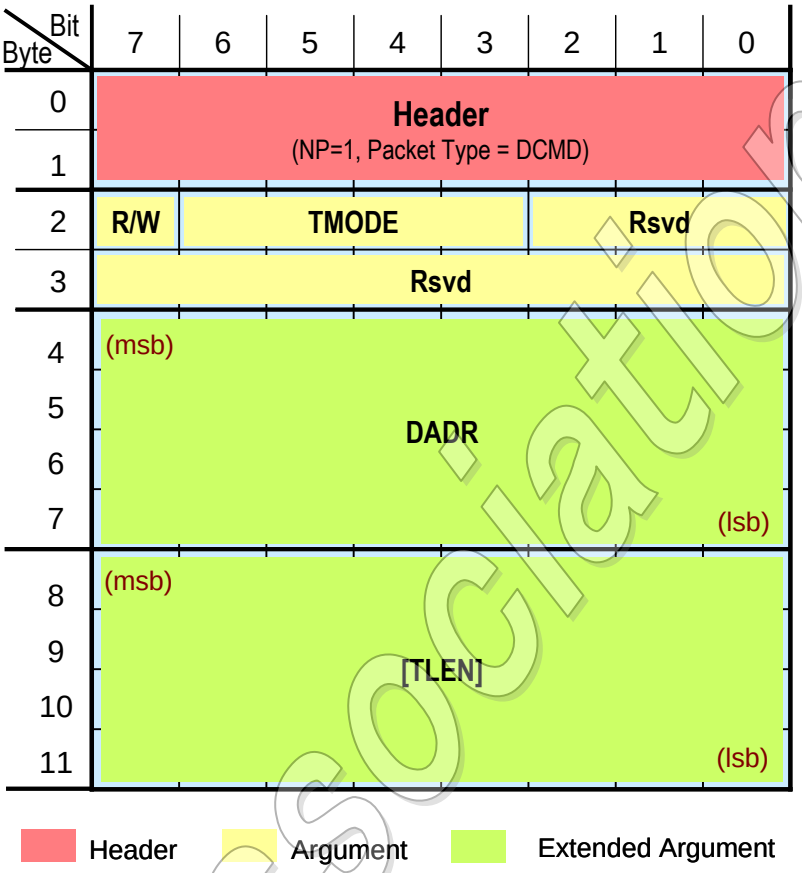


Figure 6-8 : DCMD Format

- **R/W (Read/Write):** Indicator for representing read or write command.
  - 0: Data read command
  - 1: Data write command
- **TMODE[3:0] (Transfer Mode):** Parameter settings for data transaction. (Refer to Figure 6-9 and Table 6-3.)
  - DM (Duplex Mode): Duplex mode selection of data transfer associated with DCMD
  - LM (Length Mode): Indicator whether TLEN is specified or not
  - TLUM (TLEN Unit Mode): Indicator for unit of TLEN
  - DAM (Data Access Mode): Data access mode selection.

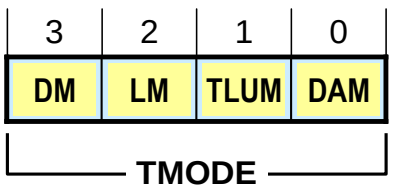


Figure 6-9 : TMODE Parameters

- **DM (Duplex Mode):**
  - 0: FD mode
  - 1: 2L-HD mode
  - If Host issues DCMD with DM = 1 to Device which does not support 2L-HD mode, Device returns RES with NACK = 1.
- **LM (Length Mode):**
  - 0: Data transfer length is not specified (TLEN field does not exist).
  - 1: Data transfer length is specified (TLEN field exists).
- **TLUM (TLEN Unit Mode):**
  - 0: Block Mode
  - 1: Byte Mode
  - In case of TLUM = 1, LM shall be equal to 1. If TLUM = 1 and LM = 0, the DCMD shall be handled as an illegal command and RES (NACK = 1) with ARG_ERR is responded (refer to Section 6.2.2.6).
  - In case of DM = 1, TLUM shall be equal 0. If DM = 1 and TLUM = 1, the DCMD shall be handled as an illegal command and RES (NACK = 1) with ARG_ERR is responded.
- **DAM (Data Access Mode):**
  - 0: Data access with incrementing the address by 1. In this case, DADR represents address in memory space address and unit of DADR is a block.
  - 1: Data access to fixed address, which is used in multiple data transfer to the same address like FIFO memory access. In this case, DADR represents address for specified UHS-II I/O address space to support FIFO memory access and unit of DADR is a byte.
  - In the case that DAM = 1 and DADR is not for FIFO memory access, the DCMD shall be handled as an illegal command and RES (NACK = 1) with ARG_ERR is responded. On UHS-II Addendum Version 1.00, as there are no fields to support FIFO memory access in the UHS-II I/O space, DCMD cannot access to UHS-II I/O space.
- **DADR[31:0] (Data Address):** data address in memory address space or I/O address space accessed by DCMD according to DAM.
  - In the case of DAM=0, DADR is for memory address space and its unit is a block.
  - In the case of DAM=1, DADR is for UHS-II I/O address space and its unit is a byte.
  - It is transmitted in msb first, lsb last.
- **TLEN[31:0] (Transfer Length):** Total length of data transmitted during a data transaction (unit depends on TLUM field setting).
  - In the case that LM = 0 (data transfer length is not specified), TLEN field does not exist.
  - In the case of TLUM = 0 (Block Mode):
    TLEN field represents the data length within the range of 1 to (4G – 1) blocks.
    If TLEN = 0000000h, it does not affect the data transaction (same as LM = 0).
  - In the case of TLUM = 1 (Byte Mode):
    TLEN field represents the data length.
    Note that TLEN shall be smaller than or equal to Block Length.
    If TLEN = 0000000h, it is regarded same as LM = 0, and becomes ARG_ERR as a result.
  - It is transmitted in msb first, lsb last.
- **Rsvd (Reserved):** Reserved bits. Initiator shall set them to '0', and receiver shall ignore them.

Table 6-3 shows availability of TMODE. Marks in 'Availability' column mean as follows.

- **X:** TMODE is available.
- **-:** TMODE is not available.
- **-(1):** TMODE is not available in UHS-II Addendum Version 1.00. (It is subject to change in the future specification.)

TMODE				Avail-ability	Remark
DM	LM	TLUM	DAM		
0	0	0	0	X	FD mode, No TLEN, Block Mode, Memory Access
0	0	0	1	-(1)	DCMD cannot access I/O space in Version 1.00
0	0	1	0	-	TLEN shall be specified in Byte Mode
0	0	1	1	-	TLEN shall be specified in Byte Mode
0	1	0	0	X	FD mode, TLEN, Block Mode, Memory Access
0	1	0	1	-(1)	DCMD cannot access I/O space in Version 1.00
0	1	1	0	X	FD mode, TLEN, Byte Mode, Memory Access
0	1	1	1	-(1)	DCMD cannot access I/O space in Version 1.00
1	0	0	0	X	2L-HD mode, No TLEN, Block Mode, Memory Access
1	0	0	1	-(1)	DCMD cannot access I/O space in Version 1.00
1	0	1	0	-	TLEN shall be specified in Byte Mode
1	0	1	1	-	TLEN shall be specified in Byte Mode
1	1	0	0	X	2L-HD mode, TLEN, Block Mode, Memory Access
1	1	0	1	-(1)	DCMD cannot access I/O space in Version 1.00
1	1	1	0	-	Byte Mode is not available in 2L-HD mode
1	1	1	1	-	Byte Mode is not available in 2L-HD mode

Table 6-3 : Availability of TMODE

6.2.2.5 RES (NACK = 0)

Figure 6-10 illustrates the RES (NACK = 0) structure.

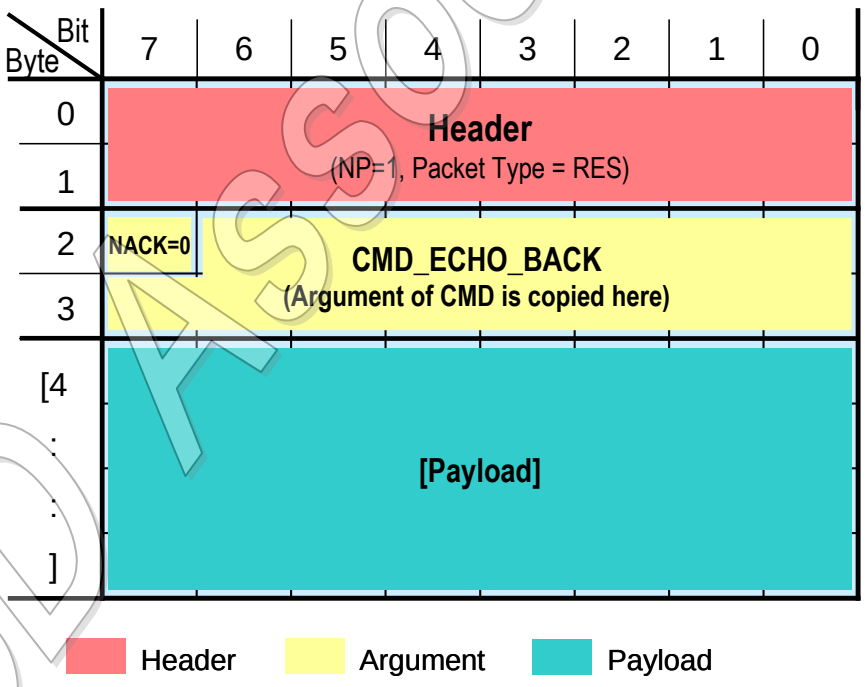


Figure 6-10 : RES (NACK = 0) Format

- **NACK (Negative Acknowledgement):** Indicator whether the corresponding CMD is accepted or not.
  - 0: The corresponding CMD is accepted.
  - 1: The corresponding CMD is rejected.

- In the case of NACK = 0 (CMD is accepted), the requested operation is in execution or waiting for execution.
- In the case of NACK = 1 (CMD is rejected), the requested operation is not in execution (an error has occurred in the corresponding CMD).
- Refer to Section 6.2.2.6 for details of RES with NACK = 1.

- **CMD_ECHO_BACK[14:0] (Command Echo Back):** Copied field of CMD Argument.
  - The same values in Argument field are copied from the corresponding CMD (echo back). Specifically, [6:0] in the second byte, and [7:0] in the third byte of CMD packet are copied to the same location of RES packet.
- **Payload:** Read data for control read transaction.
  - The length of payload field is assigned in PLEN of the corresponding read CCMD.
  - In the case that PLEN of the CCMD is set to "00b" (payload length is 0 byte), Payload field does not exist.
  - In the case that write CCMD is issued, Payload field in RES does not exist.
  - In the case that DCMD is issued (data transaction), Payload field in RES does not exist.
  - The Payload field is divided into a unit of DWORD (4byte data), and the transmission order within a DWORD is big endian. Refer to Figure 6-11 and Figure 6-12 for details of the transmission order of Payload. In these figures, bracketed numbers denote the bit order within a DWORD.

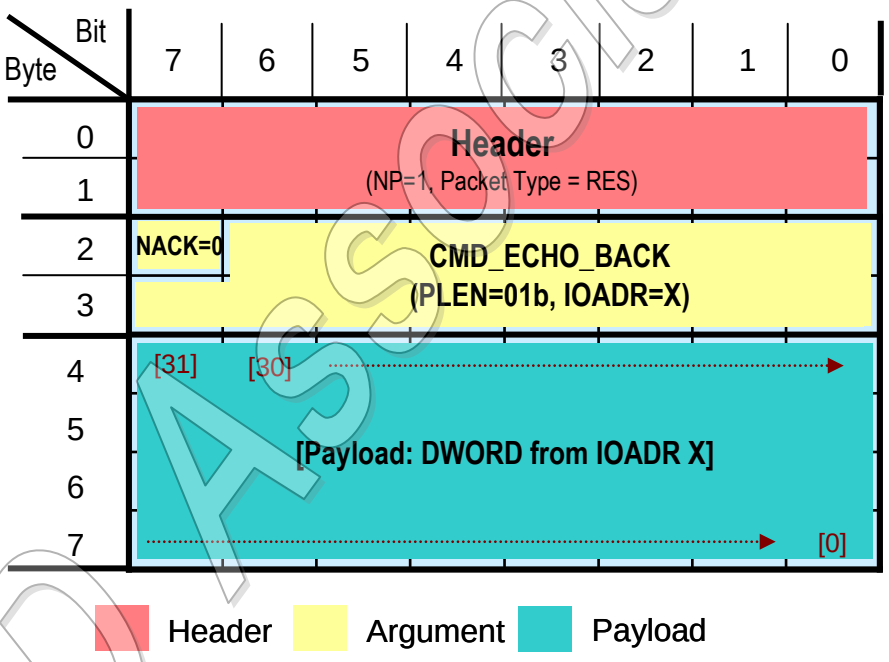


Figure 6-11 : Transmission Order of Payload in RES (NACK = 0, PLEN = 01b)

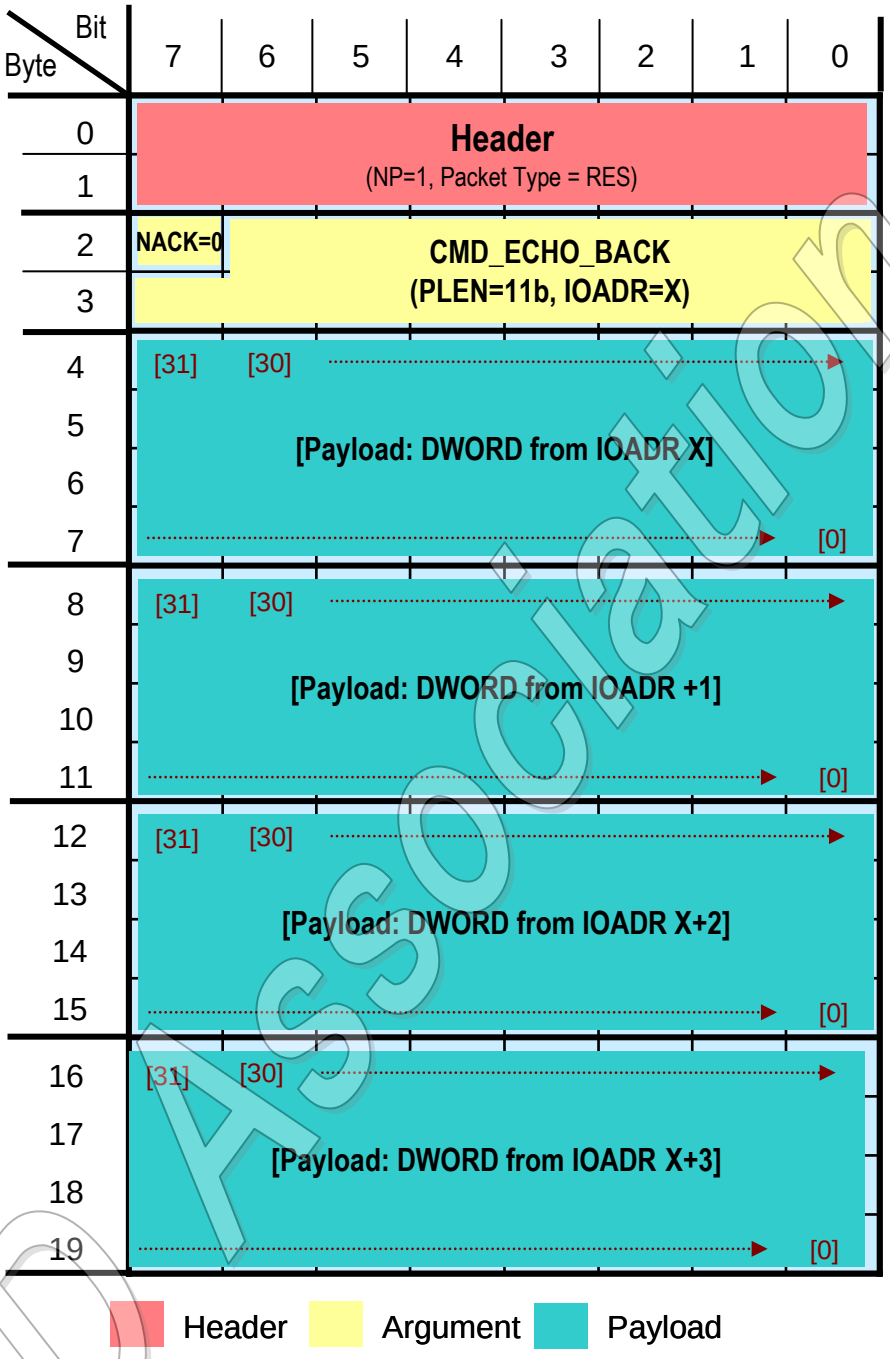


Figure 6-12 : Transmission Order of Payload in RES (NACK = 0, PLEN = 11b)

DID field in Header of RES is set to the same value as SID field in Header of the corresponding command. TID field in Header is set to the same value as TID field in Header of the corresponding command.
In the case of application specific protocol (NP = 0), the definition of payload field existence may be different from the case of native protocol (NP = 1). Refer to Section 7.2.1.3 for details of RES format for SD application.

6.2.2.6 RES (NACK = 1)

Figure 6-13 illustrates RES (NACK = 1) structure.

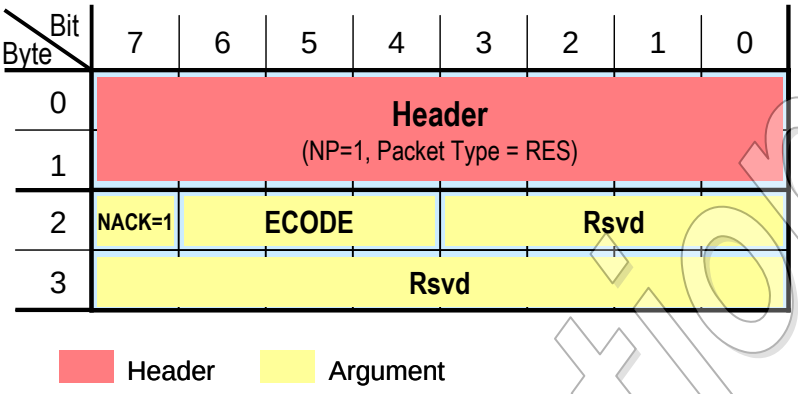


Figure 6-13 : RES (NACK = 1) Format

- **NACK (Negative Acknowledgement):** Indicator whether the corresponding CMD is accepted or not.
  - NACK = 1 means the corresponding CMD is rejected.
  - In the case of NACK = 1 (CMD is rejected), the requested operation is not in execution (an error has occurred in the corresponding CMD).
- **ECODE[2:0] (Error Code):** Error code to represent error descriptions (refer to Table 6-4).
- **Rsvd (Reserved):** Reserved bits. Initiator shall set them to '0', and receiver shall ignore them.

Table 6-4 shows the error descriptions represented by ECODE. If CMD includes multiple errors, RES with NACK = 1 is generated with the error whose ECODE value is the smallest. For example, when some command is issued at improper state with illegal argument (e.g. illegal address), the ECODE of its RES with NACK = 1 is COND_ERR.

ECODE		Description
Value	Name	
001b	COND_ERR	Command is issued in any improper states defined in all layers in this specification.
010b	ARG_ERR	At least one of parameters in any of Argument field, Extended Argument field, or Payload field is improper in the CMD.
011b	GEN_ERR	Other errors not belonging to the errors above.
others	Reserved	Reserved

Table 6-4 : Error Categories and Descriptions

6.2.2.7 DATA

Figure 6-14 illustrates a basic DATA structure.

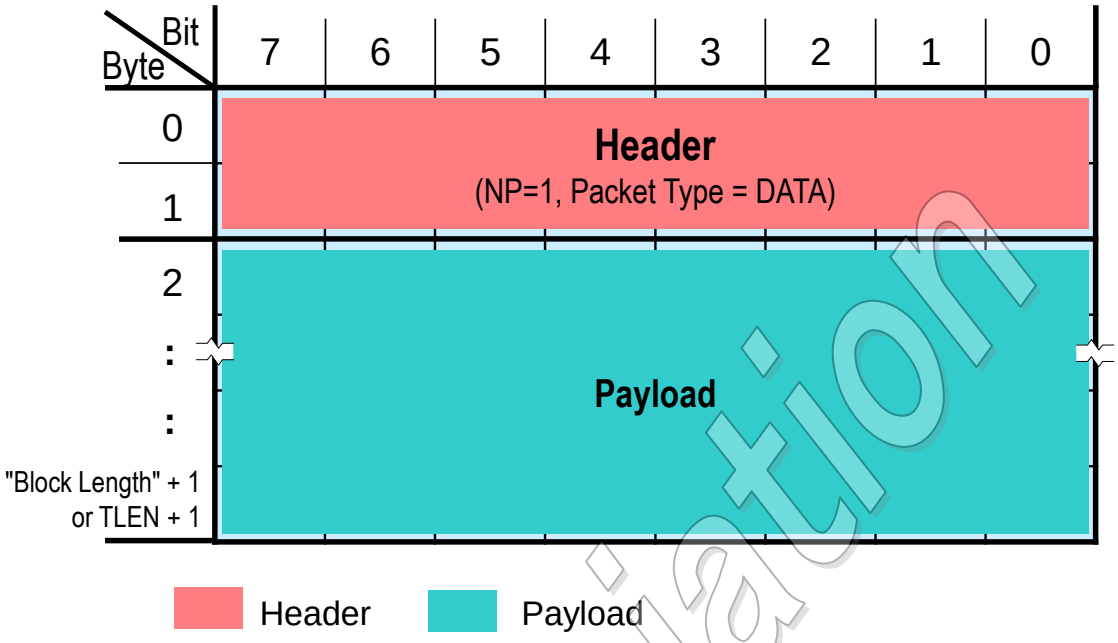


Figure 6-14 : Basic DATA Format

- **Payload:** Data included with DATA.
  - The length of payload is equal to Block Length in Block Mode and TLEN in Byte Mode.
  - It is transmitted in LSB first, MSB last. For the individual byte, it is msb first, lsb last.

6.2.2.8 Operation of Reserved Bits in the Packet

The following table indicates how each Node operates reserved bits in the packet.

Node	Operation
Initiator (both Host and Device)	Reserved bits shall be set to '0' other than in CMD_ECHO_BACK field
Device bypassing control packet	Reserved bits shall be ignored upon reception, and not to be set or cleared upon transmission.
Device handling broadcast packet	Reserved bits shall be ignored upon reception, and not to be set or cleared upon transmission.

Table 6-5 : Operation for the Reserved Bits in the Packet

Host should use Reserved bits considering the specification versions that all devices that exist in the ring topology.

6.2.3 Supplements of UHS-II Initialization

In this section, supplements of UHS-II Initialization are described. Refer to Section 3.5 for the basic specifications.

Figure 6-15 shows UHS-II Initialization flow in case of recovery from Dormant state.

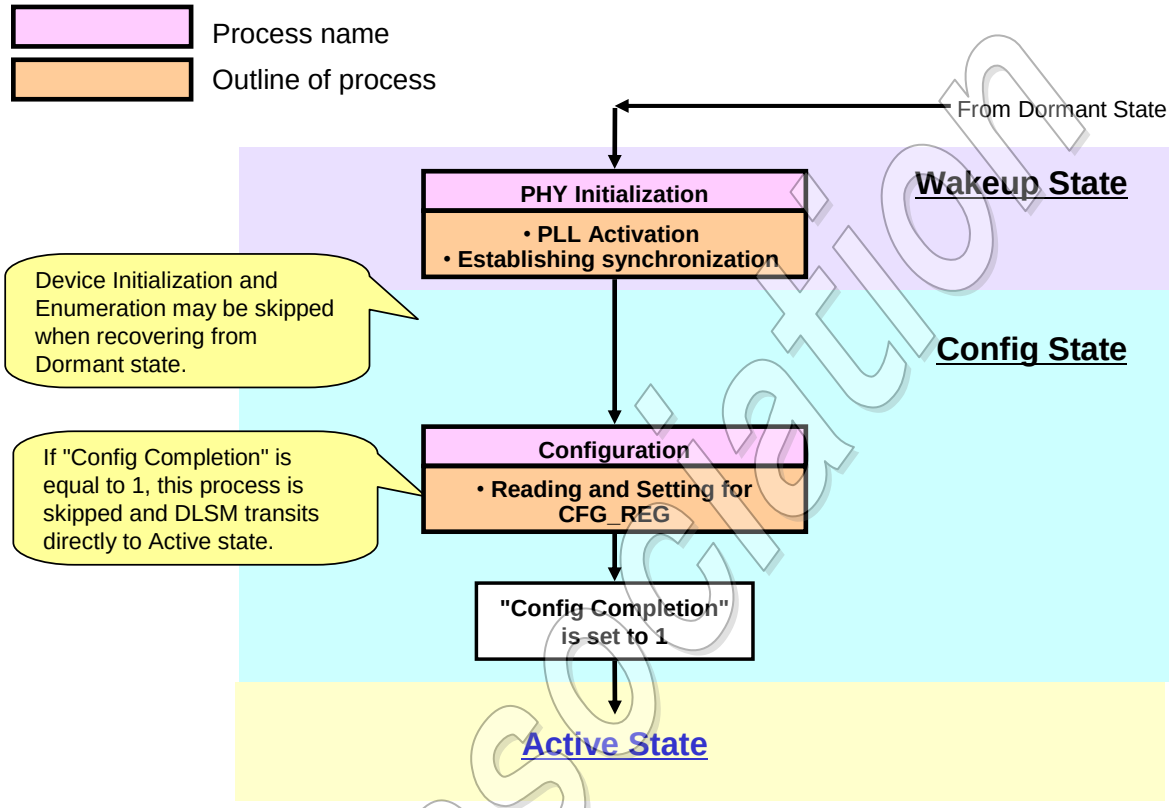


Figure 6-15 : UHS-II Initialization Flow When Recovery from Dormant State

If Device receives BSYN LSS after recovering from Dormant State, Device behavior is up to implementation. Note that Host shall not transmit BSYN LSS after recovering from Dormant State.

Both Device Initialization process and Enumeration process may be skipped when recovering from Dormant state, for whole functions of each Device and Node ID. If "Config Completion" is equal to 0, Configuration process can be done, but otherwise, that process is skipped and DLSM transits to Active state.

Figure 6-16 shows an example of Initialization flow in case of using Range B as a transmission speed range (refer to Section 6.2.9.2.5 for more details).

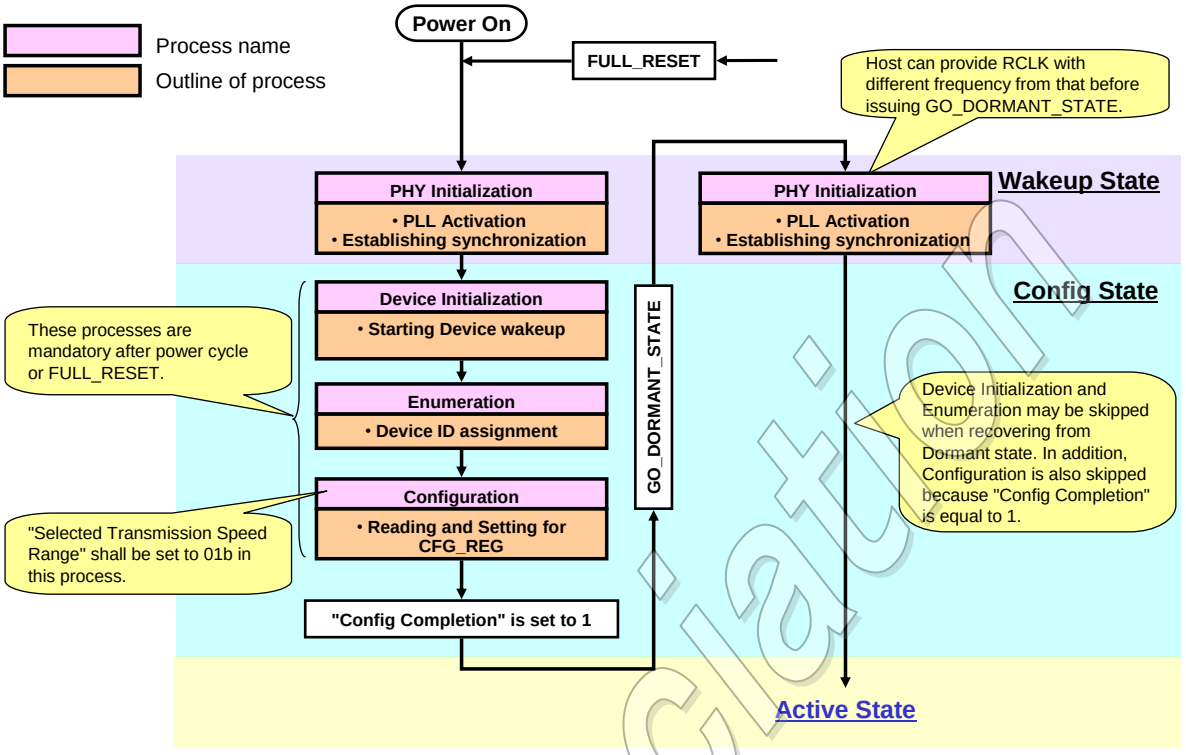


Figure 6-16 : An Example of UHS-II Initialization Flow (in Case of Using Higher Speed Range)

Host shall set "Selected Transmission Speed Range" in CFG_REG to the desire range (01b, in this case) at the Configuration process. After setting "Config Completion" to 1, Host issues GO_DORMANT_STATE in order to enable "Selected Transmission Speed Range". Afterwards, it provides RCLK to do PHY Initialization again. Note that frequency of RCLK may be changed during Dormant state only. At the end of PHY Initialization, DLSM transits to Active State where higher speed range is available because "Config Completion" has been already set to 1.

6.2.4 Transition to Dormant State

6.2.4.1 General

When Device receives GO_DORMANT_STATE CCMD, it makes its DLSM transit to Dormant state for interface power saving. During Dormant state, state machines defined in Chapter 6 get back to the initial state. On the other hand, all registers defined in Chapter 6 are kept and some Settings Registers in CFG_REG are reflected by transiting to Dormant state (refer to Section 6.2.9.2).

Figure 6-17 illustrates a format of GO_DORMANT_STATE CCMD.

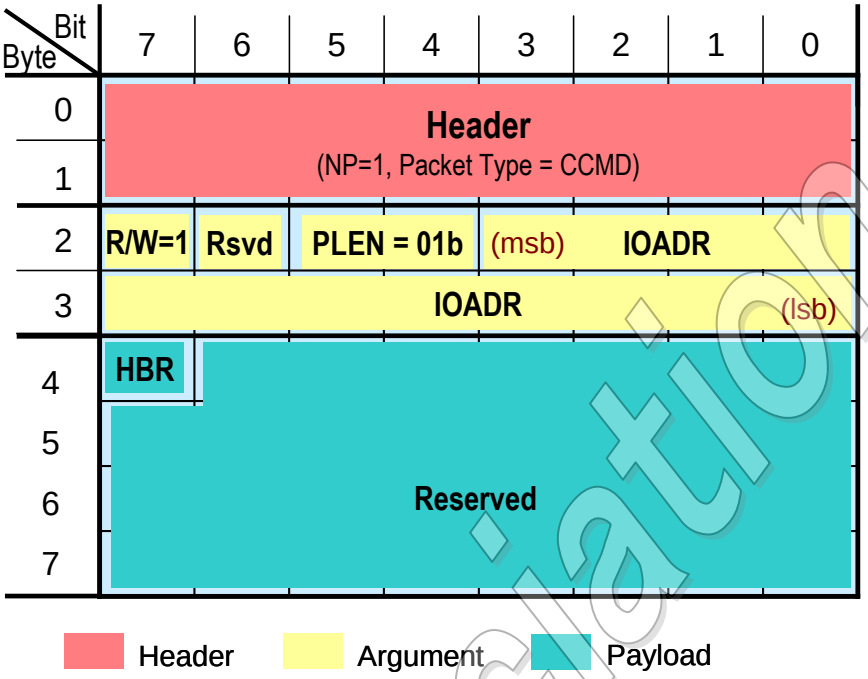


Figure 6-17 : GO_DORMANT_STATE CCMD Format

- **HBR (Entry to Hibernate Mode):** This value indicates entry to Hibernate mode (refer to Section 6.2.4.2 for more details). If Host intends to enter to Hibernate mode during Dormant state, it issues GO_DORMANT_STATE CCMD with HBR = 1. If Device not supporting Hibernate mode receives GO_DORMANT_STATE CCMD with HBR = 1, Device shall handle it as an illegal CMD.

6.2.4.2 Hibernate Mode

6.2.4.2.1 Overview

Hibernate mode is an enhanced power saving mode by turning off VDD1 (refer to Chapter 4 for the details) during Dormant state, and optional by UHS-II Device. Time for recovering from Hibernate mode is much shorter than that in case of power cycle. To realize Hibernate mode, Device will indicate if Hibernate mode is supported through "Supporting Hibernate Mode" field located in PHY Capabilities Register, bit position #15 (refer to Table 6-8 for more details).

Host shall inquire if Device or system is capable of Hibernate mode. In case that Hibernate mode is supported, Host may activate this mode. Activation of Hibernate mode is done through setting HBR bit in GO_DORMANT_STATE CCMD payload.

Note that in case of Multi-device connection such as Ring, the condition to operate Hibernate mode is that all connected Devices support Hibernate mode. If Device not supporting Hibernate mode is turned off VDD1 during Dormant state, its behavior is not guaranteed.

Following of Section 6.2.4.2 is a blank in the Simplified Addendum.

Section 6.2.5 is a blank in the Simplified Addendum.

6.2.6 Device Initialization Mechanism

6.2.6.1 General

Device initialization mechanism enables Host system to optimize initialization time considering power consumption. Under Multi-device connection Host may perform initializations for multiple Devices at the same time with in a range of a Host's power supply capability. Device Initialization takes place by issuing the broadcast CCMD called DEVICE_INIT iteratively, and the Host's power supply capability is provided by the argument of DEVICE_INIT to each Device.
Figure 6-21 illustrates a format of DEVICE_INIT CCMD.

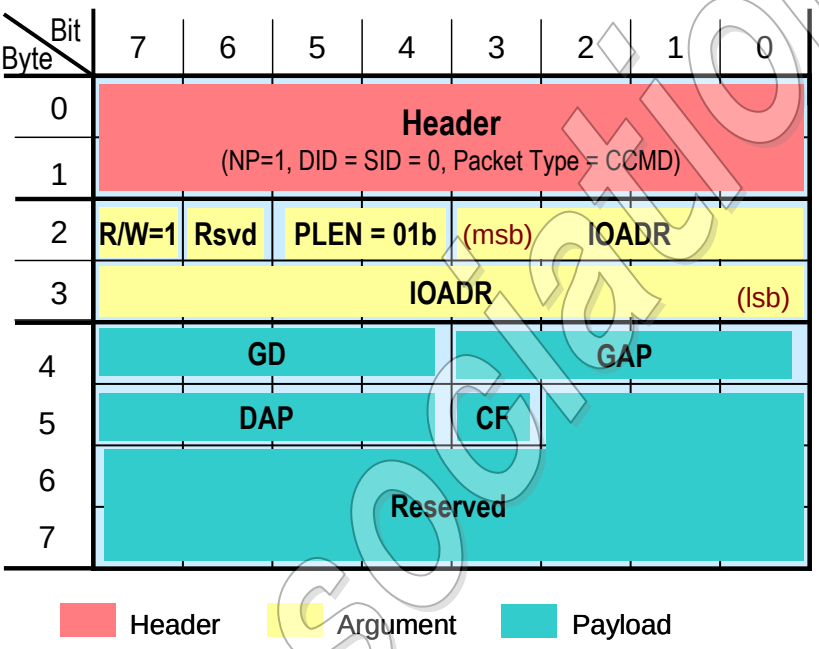


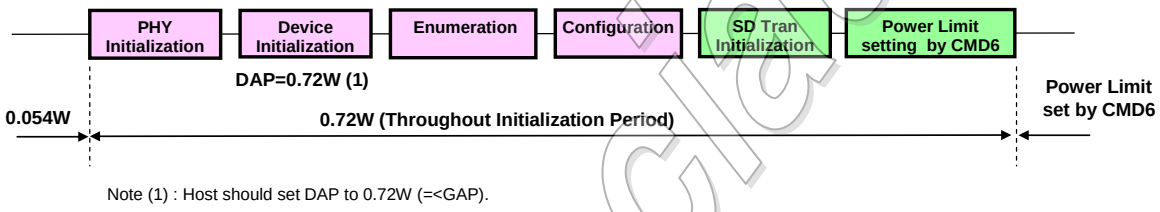
Figure 6-21 : DEVICE_INIT CCMD Format

- **GD[3:0] (Group Descriptor):** This value indicates the group number to be initialized. The start value is 0 and incremented when all Devices in the group are initialized.
- **GAP[3:0] (Group Allocated Power):** This value indicates the maximum Host's power supply capability that is allowed to certain group. A Device which starts initialization updates this value by subtracting own power consumption from this value. In such a way this field represents the currently remained power resource for a given group.
  - 0: Reserved
  - 1: 360 [mW] (3.6Vx100mA)
  - 2: 720 [mW]
  - 3: 1080 [mW]
  - :
  - n: 360n [mW] (n ≤ 15)
- **DAP[3:0] (Device Allocated Power):** This value is the maximum Host's power supply capability that is allowed to a certain Device.
  - 0: 360 [mW] Default (Host does not know own power capability)
  - 1: 360 [mW] (3.6Vx100mA)
  - 2: 720 [mW]
  - 3: 1080 [mW]
  - :
  - n: 360n [mW] (n ≤ 15)

- **CF (Completion Flag):** Device shall clear this bit to "0" if it is not initialized yet. Host uses this value to check whether all Devices are initialized in the system. If Host detects CF = 0 (not all Devices are initialized) from the received DEVICE_INIT, Host continues to issue DEVICE_INIT CCMD.
    - 0: Not all Devices complete initialization.
    - 1: All Devices complete initialization.

Device can accept DEVICE_INIT CCMD only in Config state. So Device shall regard it as an illegal CMD and shall not transmit it to the next Node in case of other than Config state.

Application Note:
Host should estimate at least 0.72W power supply capability for a UHS-II SD memory card until Power Limit is set, including settings of DAP and GAP.
When DAP or GAP is set to 0.36W, whether device can be initialized or not is dependent on implementation.



Note (1) : Host should set DAP to 0.72W (=<GAP).

Figure 6-22 : Power Consumption during Initialization

In case of embedded devices, device manufacturer should provide detail power consumption specification to host system vendor if necessary so that host system vendor can calculate required power budget.

(1) Power consumption during PHY Initialization (Ppi).
(2) Power consumption during packet bypassing (Ppb).
(3) Power consumption in Dormant State (Pds)

Host system calculates required power budget by using device information for all embedded devices and reserves additional power 0.72W for a UHS-II memory card.

Following of Section 6.2.6 is a blank in the Simplified Addendum.

6.2.7 Enumeration Mechanism

6.2.7.1 General

After initialization, Enumeration process takes place.
Figure 6-28 illustrates a format of ENUMERATE CCMD.

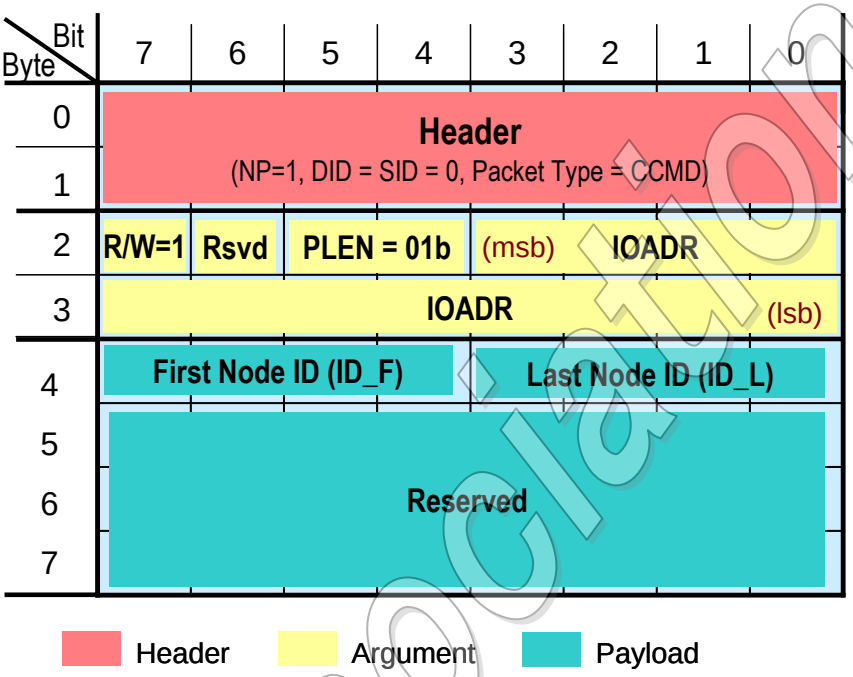


Figure 6-28 : ENUMERATE CCMD Format

There are two parameters in Payload area named First Node ID (abbreviated to ID_F) and Last Node ID (abbreviated to ID_L) to perform Enumeration.

Following of Section 6.2.7 is a blank in the Simplified Addendum.

6.2.8 Configuration Mechanism

6.2.8.1 Basic Specification

After Enumeration, Configuration process takes place.
All UHS-II Host and Device shall have their own Configuration Register (CFG_REG). Its details are described in Section 6.2.9.
CFG_REG consists of the following fields;

- **Capabilities:** Device-dependent initial capabilities are set to this field.
- **Settings:** Negotiated operating values are assigned to this field.
- **Preset:** Preset values are indicated to this field.

In Capabilities field, device-specific initial capabilities or properties are set, and this field is referred for deciding operating conditions during Configuration.
In Settings field, negotiated values between Host and Device are assigned as operating conditions after Configuration.
Moreover, some parameters can be preset by system manufactures or so, and these are indicated in Preset field.

Following of Section 6.2.8.1 is a blank in the Simplified Addendum.

6.2.8.2 Determination of Block Length

Block Length is determined as follows.

(1) Host reads "Device-specific MAX_BLKLEN" from LINK/TRAN Capabilities Registers in Device.
(2) Host determines the feasible value for "MAX_BLKLEN" and writes to LINK/TRAN Settings Registers in Device.
(3) If Device has an application specific layer, Block Length is finally determined by the setting in the application specific layer. Note that Block Length shall be set smaller than or equal to "MAX_BLKLEN" in the application specific layer.
(4) Otherwise, Block Length is equal to "MAX_BLKLEN". Only in this case, Block Length is immediately changed even in Active State when Host writes the value of "MAX_BLKLEN" by CCMD.

If the application is SD-memory, both "Device-specific MAX_BLKLEN" and "MAX_BLKLEN" shall be 512 bytes.

6.2.8.3 Quick Configuration

The basic Configuration mentioned above takes place for one Device. So it takes much time for Configuration if there are many Devices connected to Host, because Host shall repeat the process.
In order to make Configuration more efficient, Quick Configuration mechanism is introduced.
Quick Configuration can be established by the following two broadcast CCMDs, one is INQUIRY_CONFIG and the other is SET_COMMON_CONFIG. Note that these two commands are not defined in CMD_REG, because IOADR for these commands are set the address for CFG_REG.
Figure 6-35 illustrates a format of INQUIRY_CONFIG.

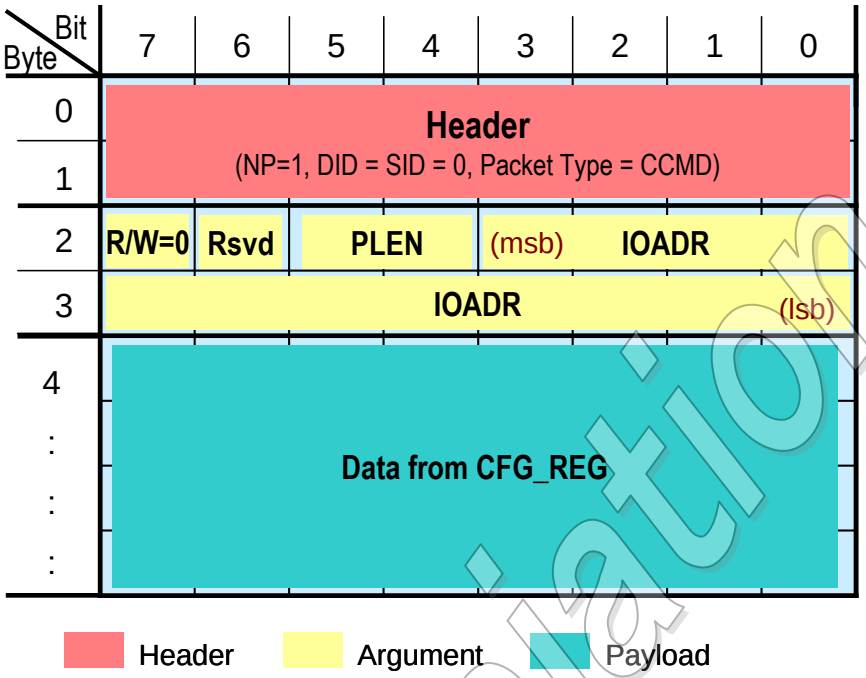


Figure 6-35 : INQUIRY_CONFIG Format

INQUIRY_CONFIG queries to each Device and returns the values that all Devices satisfy for their settings. IOADR is set the quarter of the absolute address to access in CFG_REG. The target field of INQUIRY_CONFIG specified by PLEN and IOADR shall consist entirely of Capabilities registers. Otherwise, INQUIRY_CONFIG commands are discarded.

A part of Section 6.2.8.3 is a blank in the Simplified Addendum.

Host sets the payload including the parameter and issues INQUIRY_CONFIG. When Device receives the broadcast CCMD, it compares the parameter in the input CMD payload and that in CFG_REG in its own, selects appropriate value between them, and overwrites the selected parameter to the broadcast CCMD. Then Device sends the updated broadcast CCMD from its Tx Port. The comparison conditions may be different for each parameter and are described in Section 6.2.9.2. No operations take place for some parameters specified in Section 6.2.9.2, and Reserved field.

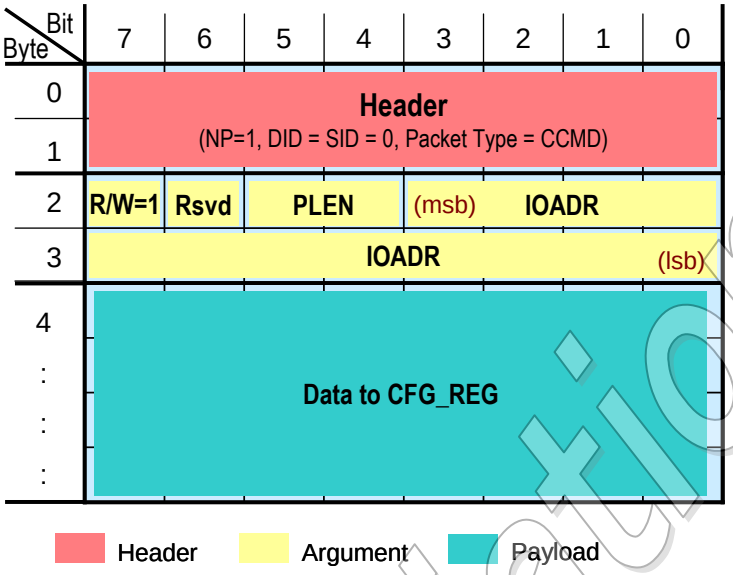


Figure 6-37 : SET_COMMON_CONFIG CCMD Format

Figure 6-37 illustrates a format of SET_COMMON_CONFIG. This broadcast CCMD writes content of Payload area to CFG_REG specified by IOADR and PLEN. So Host can set the same parameters to all Devices by issuing this broadcast CCMD.

6.2.9 Configuration Register (CFG_REG)

Parameters related to Configuration are assigned to CFG_REG. CFG_REG can be accessed by CCMD, not DCMD.

6.2.9.1 Register Map

Table 6-6 shows the map of CFG_REG. Offset means the relative address based on CFG_BASE. The parenthetic values indicate bit location in each register. In case of writing to Settings Register, SET_COMMON_CONFIG (broadcast CCMD) shall be used for Generic Settings Register and PHY Settings Register in case of Ring connection. In other words, common values shall be set for the two registers among all Devices.

Offset		Register
Byte address	IOADR	
0000h : 0007h	000h : 001h	Generic Capabilities Register (63) (00)
0008h : 000Fh	002h : 003h	PHY Capabilities Register (63) (00)
0010h : 0017h	004h : 005h	LINK/TRAN Capabilities Register (63) (00)
0018h : 001Fh	006h : 007h	Reserved for Capabilities Register
0020h : 0027h	008h : 009h	Generic Settings Register (63) (00)
0028h : 002Fh	00Ah : 00Bh	PHY Settings Register (63) (00)
0030h : 0037h	00Ch : 00Dh	LINK/TRAN Settings Register (63) (00)
0038h : 00FFh	00Eh : 03Fh	Reserved
0100h : 0107h	040h : 041h	Preset Register (63) (00)
0108h : 03FFh	042h : 0FFh	Reserved

Table 6-6 : CFG_REG Map

6.2.9.2 CFG_REG Description

The details of CFG_REG fields are described below. Refer to Appendix D for the details of registers, and in addition, refer to Table D- 1 for the description of "Attrib" in this specification.

It is recommended for Host to use INQUIRY_CONFIG (whose initial values are set to Host's capabilities) and SET_COMMON_CONFIG regardless of topology (P2P or Ring). Refer to Section 6.2.8.3 for the details of INQUIRY_CONFIG and SET_COMMON_CONFIG. For each Capabilities register, the operation is defined when receiving INQUIRY_CONFIG. Note that no operations take place to the Capabilities field whose "Attrib" is Rsvd when receiving INQUIRY_CONFIG.

The followings are Device behavior when written to the register whose "Attrib" is RO or HwInit.

- **P2P_CCMD Write:** Device shall issue RES with NACK=0 and bit value of such register is not changed.
- **Broadcast CCMD Write:** Device shall forward broadcast CCMD to the next node, and bit value such register is not changed.

A part of Section 6.2.9.2 is a blank in the Simplified Addendum.

6.2.9.2.1 Generic Capabilities Register

The table shown below describes Generic Capabilities Register.

Location	Attrib	Register Field Name and Explanation	CMD category
63-24	Rsvd	--	Broadcast /P2P
23-16	RO	**Application Type** This field indicates a type of Application. Bit 16: 0 = Non-SD memory, 1 = SD Memory Bit 17: 0 = Non-SDIO, 1 = SDIO Bit 18: 0 = Card, 1 = Embedded Others = reserved No operations take place when receiving INQUIRY_CONFIG.	
15	Rsvd	--	
14	RO	**DADR Length** This field indicates the length of DADR. 0b = 4 bytes 1b = Reserved for the future use No operations take place when receiving INQUIRY_CONFIG. (See Note (1)).	
13-08	RO	**Device-specific Number of Lanes and Functionality** This field indicates capabilities of number of Lanes and 2L-HD mode. As Device shall support FD mode, the following table shows the optional capabilities. If functionality mentioned below is available, the corresponding bit is set to 1, and otherwise 0. Device can indicate pluralities of options.	
07-00	Rsvd	--	

Bit Location	Mode	D0	D1	D2	D3
08	2L-HD	Bi	Bi	NA	NA
09	2D1U-FD	Dn	Up	Dn	NA
10	1D2U-FD	Dn	Up	NA	Up
11	2D2U-FD	Dn	Up	Dn	Up
12, 13	Reserved	-	-	-	-

Legends:
Bi = Lane is bidirectional
Dn = Lane is fixed to downstream
Up = Lane is fixed to upstream
NA = Not available

Refer to Chapter 8 and 9 for more details.
No operations take place when receiving INQUIRY_CONFIG.

Note:
(1) Host which handles 4 bytes address cannot access to the Device whose DADR Length is other than 0b.

Table 6-7 : Generic Capabilities Register

6.2.9.2.2 PHY Capabilities Register

The table shown below describes PHY Capabilities Register.

Location	Attrib	Register Field Name and Explanation	CMD category
63-40	Rsvd	--	Broadcast /P2P
39-36	RO	**Device-specific N_LSS_DIR** This field indicates the device-specific number of "DIR" LSS in order that Rx can recognize to have switched 2L-HD mode. It is indicated in unit of eight (8), and 0000b means 128 (16x8). Larger value is set on the command payload field when receiving INQUIRY_CONFIG. (Note that 0000b is regarded as the largest value.)	
35-32	RO	**Device-specific N_LSS_SYN** This field indicates the device-specific number of "SYN" LSS in order that Rx can recognize as a trigger of synchronization. It is indicated in unit of four (4), and 0000b means 64 (16x4). Larger value is set on the command payload field when receiving INQUIRY_CONFIG. (Note that 0000b is regarded as the largest value.)	
31-16	Rsvd	--	
15	RO	**Supporting Hibernate Mode** This field indicates whether Device supports Hibernate Mode (refer to Section 6.2.4.2) or not. 0b = Not supporting Hibernate Mode 1b = Supporting Hibernate Mode Smaller value is set on the command payload field when receiving INQUIRY_CONFIG.	
14-06	Rsvd	--	
05-04	RO	**PHY Major Revision** This field indicates PHY major revision. 00b = UHS156 (Maximum speed of a Lane is 1.56Gbps) Others = Reserved. Smaller value is set on the command payload field when receiving INQUIRY_CONFIG	
03-00	RO	**PHY Minor Revision** It is defined incrementally from 0 to 15 and reset to 0 if PHY Major Revision is updated. No operations take place when receiving INQUIRY_CONFIG.	

Table 6-8 : PHY Capabilities Register

Application Note:
Host shall accept Device with any PHY Major Revision. And Host shall use PHY functions which defined by minimum capability of PHY Major Revision.
e.g. Host whose PHY Major Revision is 00b shall accept Device whose PHY Major Revision is 00b or more. In this case, Host can use PHY functions which are defined in Revision 00b regardless of Device's Major Revision.

6.2.9.2.3 LINK/TRAN Capabilities Register

The table shown below describes LINK/TRAN Capabilities Register.

Location	Attrib	Register Field Name and Explanation	CMD category
63-40	Rsvd	--	Broadcast /P2P
39-32	RO	**Device-specific N_DATA_GAP** This field indicates device-specific number of DIDL between DATA packets. N_DATA_GAP is finally determined with reference to this parameter and set in LINK/TRAN Settings Register during Configuration. Larger value is set on the command payload field when receiving INQUIRY_CONFIG	
31-20	RO	**Device-specific MAX_BLKLEN** This field indicates maximum payload length of one block in byte supported by the Device (000h is reserved). Block Length is finally determined with reference to this parameter (refer to Section 6.2.8.2 for more details). If bit 16 in Generic Capabilities Register is equal to 1 ("Application Type" is SD-memory), this field shall be 200h (512 bytes). Smaller value is set on the command payload field when receiving INQUIRY_CONFIG.	
19	Rsvd	--	
18-16	RO	**Device Type** This field indicates a type of Device as follows. 001b = Host 010b = Device 011b = Reserved for CMD issuable Device Others = Reserved. No operations take place when receiving INQUIRY_CONFIG.	
15-08	RO	**Device-specific N_FCU** This field indicates maximum block number in a flow control unit (FCU) supported by the Device. 00h means 256. N_FCU is finally determined with reference to this parameter and set in LINK/TRAN Settings Register during Configuration. Smaller value is set on the command payload field when receiving INQUIRY_CONFIG.	
07-06	Rsvd	--	
05-04	RO	**LINK/TRAN Major Revision** This field indicates LINK/TRAN major revision. 00b = Compliant to UHS-II Addendum Version 1.00 01b = Reserved for the future extension Others = Reserved. Smaller value is set on the command payload field when receiving INQUIRY_CONFIG.	
03-00	RO	**LINK/TRAN Minor Revision** It is defined incrementally from 0 to 15 and reset to 0 if LINK/TRAN Major Revision is updated. No operations take place when receiving INQUIRY_CONFIG.	

Table 6-9 : LINK/TRAN Capabilities Register

Application Note:
Host shall accept Device with any LINK/TRAN Major Revision.
e.g. Host whose LINK/TRAN Major Revision is 00b shall accept Device whose LINK/TRAN Major Revision is 00b or more.

6.2.9.2.4 Generic Settings Register

The table shown below describes Generic Settings Register.

Location	Attrib	Register Field Name and Explanation	Writable State	Effective Timing	CMD category
63	RW	**Config Completion** This field is used for DLSM transition between Config and Active state. In Config state, DLSM transits to Active state immediately when this field is set to 1. In Active state, there are two cases of DLSM transitions when this field is set to 0. DLSM transits to Config state immediately after completing of Boot Code Loading. In other cases, DLSM does not transit to Config state (See Note (1)).	Config/ Active	(See Note (2))	Broadcast /P2P (See Note (3))
62-32	Rsvd	--		--	
31-12	Rsvd	--	Config only	--	
11-08	RW	**Number of Lanes and Functionality** This field indicates the number of Lanes determined through Configuration (See Note (4) and (5)). The default setting is 0000b. 0000b = 2 Lanes – operated by FD mode or 2L-HD mode (if supported) 0010b = 3 Lanes – operated by 2D1U-FD mode. 0011b = 3 Lanes – operated by 1D2U-FD mode. 0100b = 4 Lanes – operated by 2D2U-FD mode. Others = reserved		After exiting from Dormant	
07-01	Rsvd	--		--	
00	RW	**Power Control Mode in Active.Control State** This field indicates the mode for power control in Active state. In other words, it indicates symbols to be filled in the gaps on VLD state 0b = Fast mode (filled with LIDL) 1b = Low power mode (filled with EIDL, STB, and SYN)		In Active	

Note:
(1) In case of synchronization by BSYN LSS, it is automatically set to 1 for executing Boot Code Loading and DLSM transits to Active state. After the Boot Code Loading, Host shall set the parameter to 0 in order to make DLSM Config state.
(2) "Config Completion" becomes effective immediately if it is written in Config state. On the other hand, it becomes effective after exiting from Dormant if it is written in Active State except the case of Boot Code Loading described in Note (1).
(3) In Ring connection, Host shall issue broadcast CCMD for writing Generic Settings Register.
(4) "Number of Lanes and Functionality" becomes valid by transiting to Dormant state. So if more than 2 Lanes are used, Host shall issue GO_DORMANT_STATE after setting appropriate value to "Number of Lanes and Functionality". On the other

hand, transition to Dormant state is not necessary in case of using only 2 Lanes.

(5) Even Device supports 2D1U-FD mode, it is impossible to configure 1D2U-FD mode if it does not support 1D2U-FD mode, and vice versa

(6) In case of synchronization by BSYN LSS, it is automatically set to 0.

Table 6-10 : Generic Settings Register

6.2.9.2.5 PHY Settings Register

The table shown below describes PHY Settings Register.

Location	Attrib	Register Field Name and Explanation	Writable State	Effective Timing	CMD category
63-40	Rsvd	--	Config only	--	Broadcast /P2P (See Note (1))
39-36	RW	**N_LSS_DIR** This field indicates minimum number of "DIR" LSS to be sent from Tx. This value is set during Configuration with reference to "Device-specific N_LSS_DIR" field in other side, and becomes valid in Active state. It is indicated in unit of eight (8), and 0000b means 128 (16x8).		In Active	
35-32	RW	**N_LSS_SYN** This field indicates minimum number of "SYN" LSS to be sent from Tx when starting to synchronize. This value is set during Configuration with reference to "Device-specific N_LSS_SYN" field in other side, and becomes valid in Active state. It is indicated in unit of four (4), and 0000b means 64 (16x4).		In Active	
31-08	Rsvd	--	Config/ Active	--	
07-06	RW	**Selected Transmission Speed Range** This field indicates the range of transmission speed. 00b = Range A (default) 01b = Range B Others = Reserved (See Note (2))		After exiting from Dormant	
05-04	Rsvd	**Selected PHY Major Revision** This field is reserved for future use.		--	
03-00	Rsvd	--		--	

Note:

(1) In Ring connection, Host shall issue broadcast CCMD for writing PHY Settings Register.

(2) Detailed definitions of Transmission Speed Range are shown in Table 6-12. Host may support only Range A and it may support an arbitrary RCLK frequency from 26 MHz to 52 MHz. On the other hand, Device shall support both Range A and B, and all RCLK frequency from 26 MHz to 52 MHz.

Table 6-11 : PHY Settings Register

Range	Speed Range [Mbps]		RCLK Frequency Range [MHz]		RCLK:D0/D1 Ratio
	Min	Max	Min	Max	
A	390	780	26	52	1:15
B	780	1,560	26	52	1:30

Table 6-12 : Detailed Definitions of Transmission Speed Range

6.2.9.2.6 LINK/TRAN Settings Register

The table shown below describes LINK/TRAN Settings Register.

Location	Attrib	Register Field Name and Explanation	Writable State	Effective Timing	CMD category
63-40	Rsvd	--	Config/ Active	--	Broadcast /P2P
39-32	RW	**N_DATA_GAP** This field indicates minimum number of DIDL between DATA packets determined through Configuration. Initiator shall send DIDL at least N_DATA_GAP between EOP and SOP with in the DATA Burst. It is common for both read and write transaction.		In Active (See Note (1))	
31-20	RW	**MAX_BLKLEN** This field indicates maximum payload length of one block in byte determined through Configuration (000h is reserved). Block Length shall be smaller or equal to this value (refer to Section 6.2.8.2 for more details). If bit 16 in Generic Capabilities Register is equal to 1 ("Application Type" is SD-memory), this field shall be 200h (512 bytes). Default value is 200h.		In Active (See Note (2))	
19-18	Rsvd	--		--	
17-16	RW	**MAX_RETRY_NUM** This field indicates maximum retry times of DATA Burst Retry. If MAX_RETRY_NUM = 00b, DATA Burst Retry becomes disable. Default value is 11b.		In Active (See Note (1))	
15-08	RW	**N_FCU** This field indicates maximum number of blocks in a flow control unit (FCU) determined through Configuration. 00h means 256. Default value is 01h. (See Note (3) and (4).)		In Active (See Note (1))	
07-00	Rsvd	--		--	

Note:
(1) It is immediately effective in Active State.
(2) It is immediately effective in Active State if there are no application specific layers. With any application specific layers, this parameter is not reflected immediately if it is written in Active State.
(3) If bit 16 in Generic Capabilities Register is equal to 1 ("Application Type" is SD-memory), its possible settings are 01h, 02h, 04h, 08h, 10h, 20h, 40h, and 80h.
(4) The length of a DATA Burst obtained by Block Length and N_FCU shall be smaller than or equal to 64K (65,536) bytes

Table 6-13 : LINK/TRAN Settings Register

6.2.9.2.7 Preset Register

The table shown below describes Preset Register.

Location	Attrib	Register Field Name and Explanation
63-08	Rsvd	
07-04	HwInit	**CDCP** This field indicates the value of CDCP (Candidate DCP) for Device Initialization. Refer to Section 6.2.6 for more details.
03-00	HwInit	**GN** This field indicates the value of GN (Group Number) for Device Initialization. Refer to Section 6.2.6 for more details.

Table 6-14 : Preset Register

6.2.10 Status Register (ST_REG)

Status Register indicates detecting error and states of CM-TRAN. ST_REG can be accessed by CCMD, not DCMD.

6.2.10.1 Register Map

Table 6-15 shows the map of ST_REG. Offset means the relative address based on ST_BASE.

Offset		Register
Byte address	IOADR	
0000h : 0003h	000h : 000h	(00) Status in TRANS_ABORT (31)
0004h : 01FFh	001h : 07Fh	Reserved

Table 6-15 : Status Register

6.2.10.2 ST_REG Description

The details of ST_REG fields are described below. Refer to Table D- 1 for the description of "Attrib" in this specification.

6.2.10.2.1 Status in TRANS_ABORT Register

The table shown below describes Status in TRANS_ABORT Register. After I/F power cycle or FULL_RESET, all bits in this field are set to 0.

Fields of TBSM, TPSM and TSSM are updated only when Device accepts TRANS_ABORT CCMD, and reflected the last status of each state machine before accepting TRANS_ABORT CCMD.

On the other hand, fields of error identifier (refer to Section 5.2.5) are updated when each error is detected, and cleared after Device issues RES of the corresponding any P2P commands for that Device other than TRANS_ABORT. Different from RECOVERABLE_ERROR in MSG (STAT), RECOVERABLE_ERROR in ST_REG shall be accumulated until its clear condition described above is satisfied.

This Register can be read by CCMD, but it makes sense only when Host can get RES of the previous TRANS_ABORT.

Location	Attrib	Register Field Name and Explanation
31-25	Rsvd	
24	RO	**RECOVERABLE_ERROR** It indicates whether RECOVERABLE_ERROR occurs or not. (See Note (1).) 0b = no error 1b = error
23-19	Rsvd	
18	RO	**RETRY_EXPIRE_ERROR** It indicates whether RETRY_EXPIRE_ERROR occurs or not. (See Note (1).) 0b = no error 1b = error
17	RO	**DEVICE_SPECIFIC_ERROR** It indicates whether DEVICE_SPECIFIC_ERROR occurs or not. (See Note (1).) 0b = no error 1b = error
16	RO	**ILLEGAL_HEADER_ERROR** It indicates whether ILLEGAL_HEADER_ERROR occurs or not. (See Note (1).) 0b = no error 1b = error
15-12	Rsvd	
11-08	RO	**TSSM** It indicates the last TSSM when receiving TRANS_ABORT. 0000b = TS_INIT 0001b = TS_STNBY 0011b = TS_SCBSY 0010b = TS_SCRDY Others = Reserved
07-04	RO	**TPSM** It indicates the last TPSM when receiving TRANS_ABORT. 0000b = TP_IDLE 0001b = TP_WAIT 0110b = TP_INTERVAL 0010b = TP_DIN 0100b = TP_DOUT 1000b = TP_C_WAIT Others = Reserved
03-00	RO	**TBSM** It indicates the last TBSM when receiving TRANS_ABORT. 0000b = TB_BUSY 0001b = TB_IN_REQ 0011b = TB_IN_PREP 0010b = TB_IN_RDY 0100b = TB_OUT_PREP 1100b = TB_OUT_REQ 1000b = TB_OUT_RDY Others=Reserved

Note:
(1) Refer to Section 5.2.5 for the definition of each error identifier.

Table 6-16 : Status in TRANS_ABORT Register

6.2.11 Interrupt Register (INT_REG)

Interrupt can be operated through INT_REG. INT_REG can be accessed by CCMD, not DCMD.
If the application is SD-memory, it is not necessary to implement INT_REG.

6.2.11.1 Register Map

Table 6-17 shows the map of INT_REG. Offset means the relative address based on INT_BASE.

Offset		Register	
Byte address	IOADR		
0000h : 0003h	000h : 000h	INT Enable (31)	(00)
0004h : 0007h	001h : 001h	INT Status (31)	(00)
0008h : 01FFh	002h : 07Fh	Reserved	

Table 6-17 : Interrupt Register

6.2.11.2 INT_REG Description

The details of INT_REG fields are described below. Refer to Table D- 1 for the description of "Attrib" in this specification.

6.2.11.2.1 INT Enable

The table shown below describes INT Enable Register. Up to eight kinds of interrupt factors (from Factor#0 to Factor#7) can be defined in UHS-II. In this specification, all interrupt factors are not defined and reserved for the future specifications.

Location	Attrib	Register Field Name and Explanation
31-08	Rsvd	
07-00	RW	**INT Enable** This field indicates enables of each interrupt factors. Location X (0 ≤ X ≤ 7) corresponds to the enable bit for Factor#X. 0b = Interrupt disable 1b = Interrupt enable

Table 6-18 : INT Enable Register

6.2.11.2.2 INT Status

The table shown below describes INT Status Register. Up to eight kinds of interrupt factors (from Factor#0 to Factor#7) can be defined in UHS-II. In this specification, all interrupt factors are not defined and reserved for the future specifications.

Location	Attrib	Register Field Name and Explanation
31-08	Rsvd	
07-00	RO	**INT Status** This field indicates status for each interrupt factors. Location X (0 ≤ X ≤ 7) corresponds to the status bit for Factor#X. 0b = Interrupt is not pending 1b = Interrupt is pending

Table 6-19 : INT Status Register

6.2.12 Command Register (CMD_REG)

UHS-II native commands are executed by "writing" to the specific address in CMD_REG by CCMD, not DCMD.
Table 6-20 shows CMD_REG. Offset means the relative address based on CMD_BASE.

Offset		Register Field Name and Explanation	PLEN	CMD category
Byte address	IOADR			
0000h	000h	**FULL_RESET** - To reset all components in Device (same situation before I/F power up). - Refer to Section 6.2.5 for more details.	00b	Broadcast/ P2P
0004h	001h	**GO_DORMANT_STATE** - To make DLSM transit to Dormant state for power saving including Hibernate Mode. - Refer to Section 6.2.4 for more details.	01b (4 bytes)	Broadcast/ P2P
0008h	002h	**DEVICE_INIT** - To start Device Initialization according to the payload settings. - Refer to Section 6.2.6 for more details.	01b (4 bytes)	Broadcast
000Ch	003h	**ENUMERATE** - To perform Device Enumeration. - Refer to Section 0 for more details.	01b (4 bytes)	Broadcast
0010h	004h	**TRANS_ABORT** - To abort outstanding transaction. - In case of UHS-II native protocol, this command also terminates the DATA Burst transmission. - TRANS_ABORT shall terminate all existing transactions regardless of its TID. - Refer to Section 3.4.5 for more details.	00b	P2P
Others		Reserved	---	---

Table 6-20 : Command Register

Application Note:
In case of Ring connection, Host shall not issue P2P FULL_RESET CCMD or P2P GO_DORMANT_STATE CCMD.

Following of Chapter 6 is a blank in the Simplified Addendum.

7. SD-TRAN Specification

SD-TRAN rides over CM-TRAN and acts as bridge between Legacy SD protocol and UHS-II common protocol for SD-compatibility. This chapter presents encapsulated SD packet formats, transaction sequences, initialization for SD-TRAN, state machine, error handling and timing rules. These are based on CM-TRAN specification, but SD-memory is applied to some specific rules described in this chapter. In this case, the specific rules in SD-TRAN are effective instead of those in CM-TRAN.
In this section, UHS-II specifications for SD-memory are described, not included for SDIO.

7.1 SD-TRAN Overview

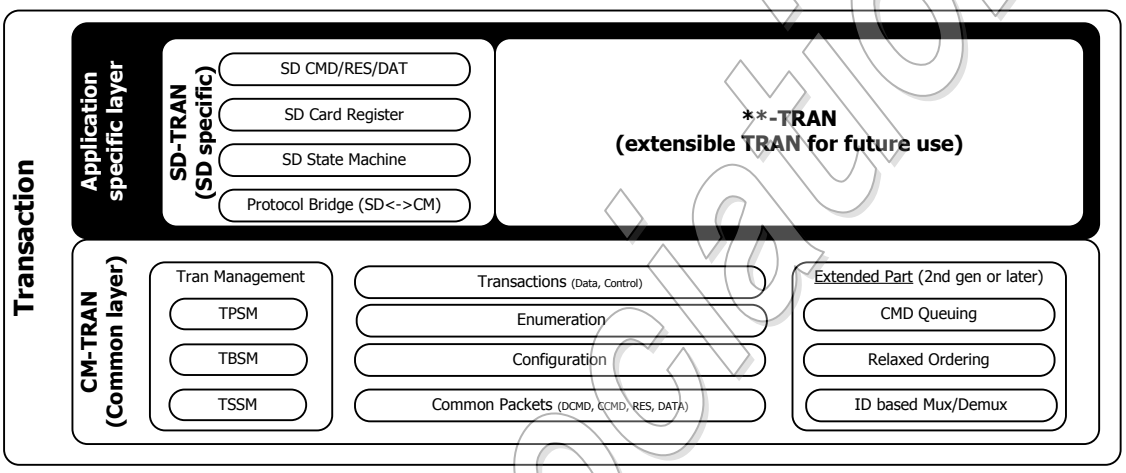


Figure 7-1 : SD-TRAN Overview

The features of SD-TRAN are shown below;

- Preserving Legacy SD infrastructures (CMD, RES, status, errors and etc.)
- Bridging between Legacy SD protocol (e.g. Host/Device register interface) and UHS-II common protocol (CM-TRAN)

7.1.1 Packet Types and Format Overview

Encapsulated SD packets are defined in SD-TRAN in order to ensure Legacy SD compatibility and preserve Legacy SD infrastructures.
Conceptual diagram of SD-encapsulation is shown in Figure 7-2.

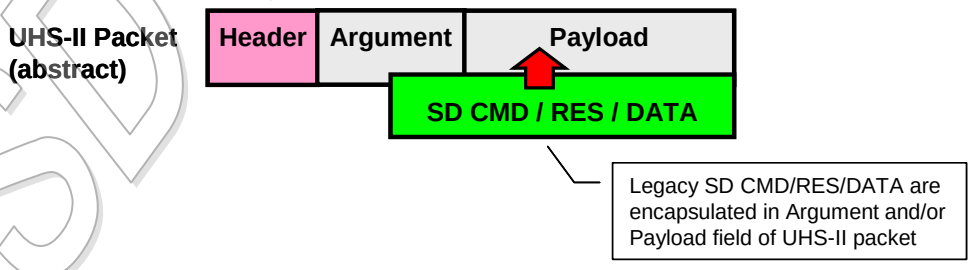


Figure 7-2 : Conceptual Diagram of SD-encapsulation

SD-encapsulation formats in each types of TLP are shown in Figure 7-3.

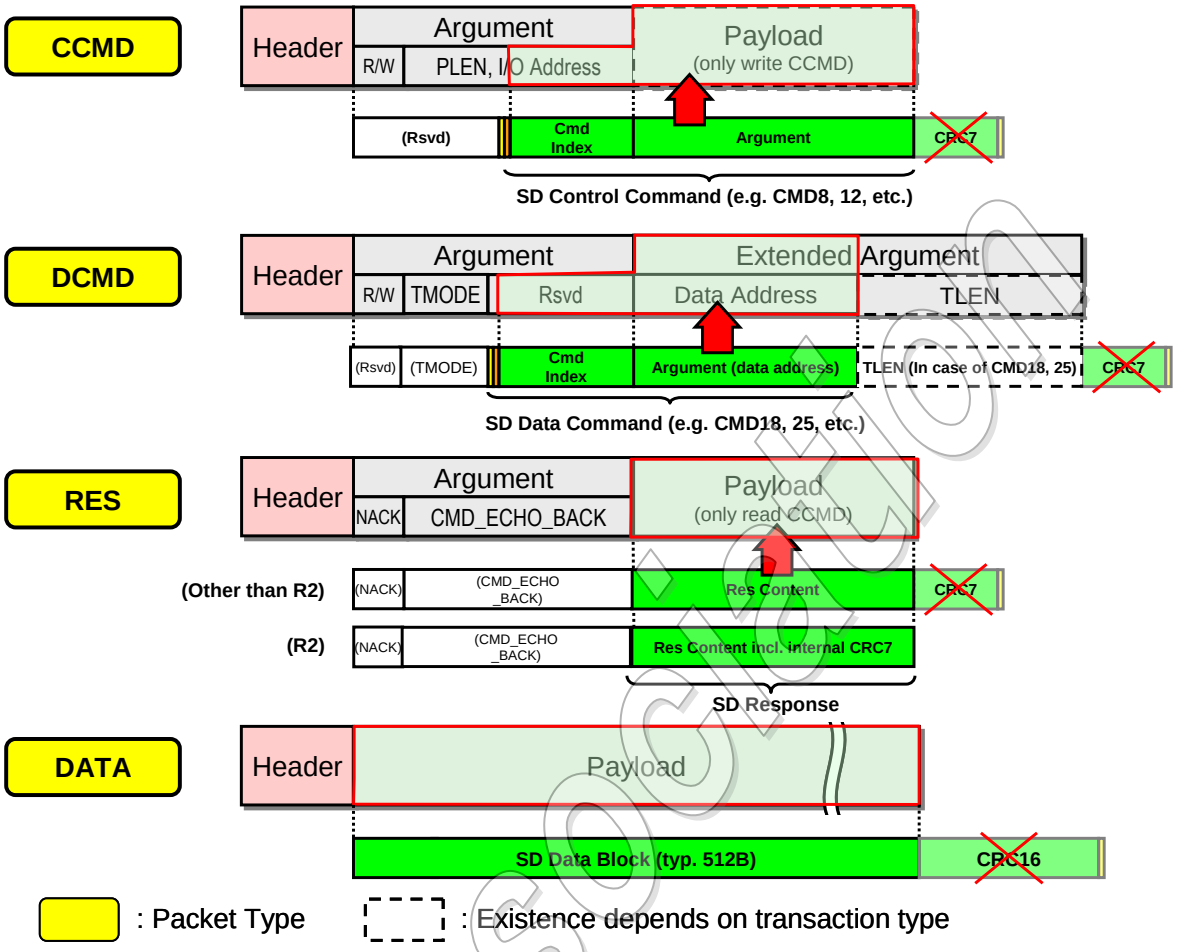


Figure 7-3 : Encapsulation of Legacy SD Format

Basically, CRC7 or CRC16 for Legacy SD are not overridden in SD-encapsulation format because all TLPs are added CRC16 in Link Layer.
Details are described in next section.

7.1.2 Registers for Legacy SD

Registers for Legacy SD such as CID or CSD can be accessed only by SD encapsulated CMD. For example, when Host wants to get CID, Host sends an encapsulated CMD2 (ALL_SEND_CID).

7.2 SD-TRAN Protocol

7.2.1 Packet Format Details

In this section, the bracketed number in the figures denotes the bit position in Legacy SD command or response format. Note that broadcast packet is not permitted in SD-TRAN.

7.2.1.1 CCMD

Figure 7-4 illustrates CCMD on SD-TRAN.

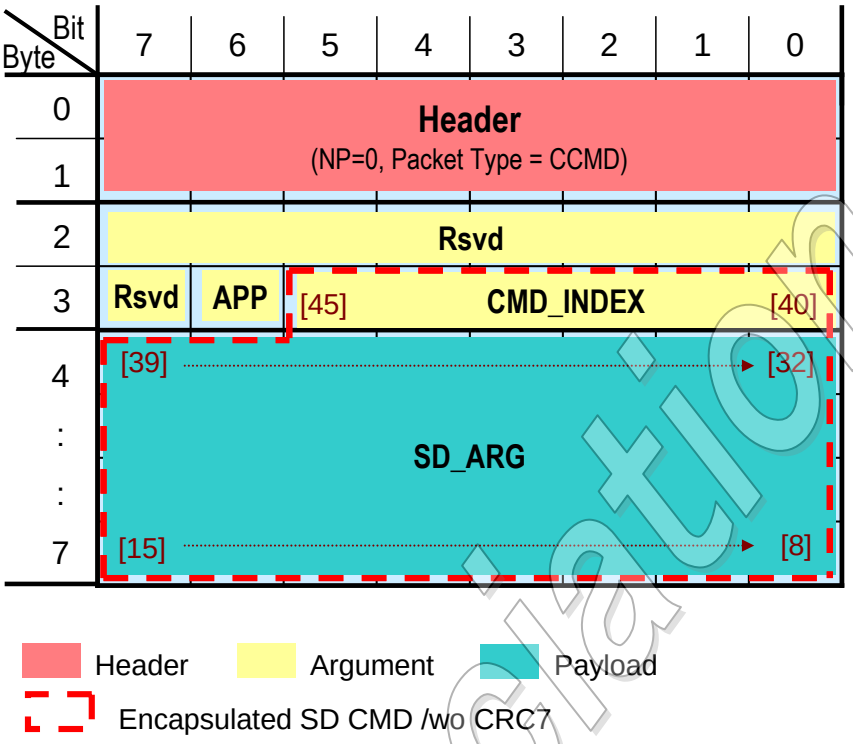


Figure 7-4 : CCMD Format on SD-TRAN

- **APP:** Indicator for application command. APP = 1 means application command, otherwise regular command. Device shall regard as application command if APP = 1.
- **CMD_INDEX[5:0]:** CMD Index in Legacy SD Command to be issued.
- **SD_ARG:** Corresponding argument for the Legacy SD Command.
  - Notice the bit order of Payload field.
- **Rsvd (Reserved):** Reserved bits. Initiator (Host) shall set them to '0', and receiver (Device) shall ignore them.

7.2.1.2 DCMD

Figure 7-5 illustrates DCMD on SD-TRAN.

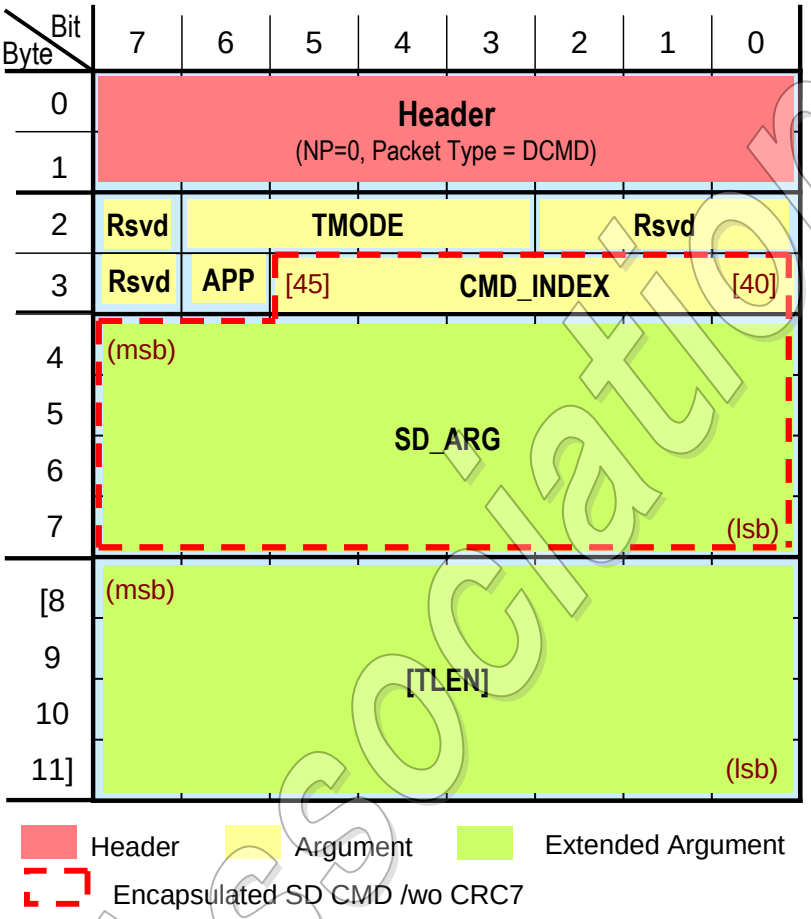


Figure 7-5 : DCMD Format on SD-TRAN

- **TMODE[3:0] (Transfer Mode):** Parameter settings for data transaction.
  - Host may set DM to 1 for DCMD which supports multi-block read / write regardless of data transfer length (e.g., CMD18, CMD25). Otherwise, it shall not set DM to 1. (e.g. CMD6, CMD17, CMD24). These rules are also applied to other multi-block read / write commands defined in other Part of SD specifications (for example, Host may set DM to 1 for ACMD18 or ACMD25).
  - LM is alternative only for CMD18 and 25, and it shall be set to 0 for other DCMDs.
  - Both DAM and TLUM shall be set to 0.
  - If Host issues DCMD with DM = 1 to Device which does not support 2L-HD mode, Device returns RES with NACK = 1.
- **APP:** Indicator for application command. APP = 1 means application command, otherwise regular command. Device shall regard as application command if APP = 1.
- **CMD_INDEX[5:0]:** CMD Index in Legacy SD Command to be issued.
- **SD_ARG:** Corresponding argument for the Legacy SD Command.
- **TLEN[31:0] (Transfer Length):** Total length of data transmitted during a data transaction
  - This field exists only for CMD18 or CMD25 with LM = 1, and unit of TLEN is a block (512 bytes in SD-memory). It is strongly recommended for Host to be set LM = 1 and TLEN > 0 in case of CMD18 and CMD25.

- If TLEN = 0000000h, it does not affect the data transaction (same as LM = 0).
- It is transmitted in msb first, lsb last.

- **Rsvd (Reserved):** Reserved bits. Initiator (Host) shall set them to '0', and receiver (Device) shall ignore them.

7.2.1.3 RES

Figure 7-6 illustrates the generic structure of RES associated with CCMD and DCMD on SD-TRAN.

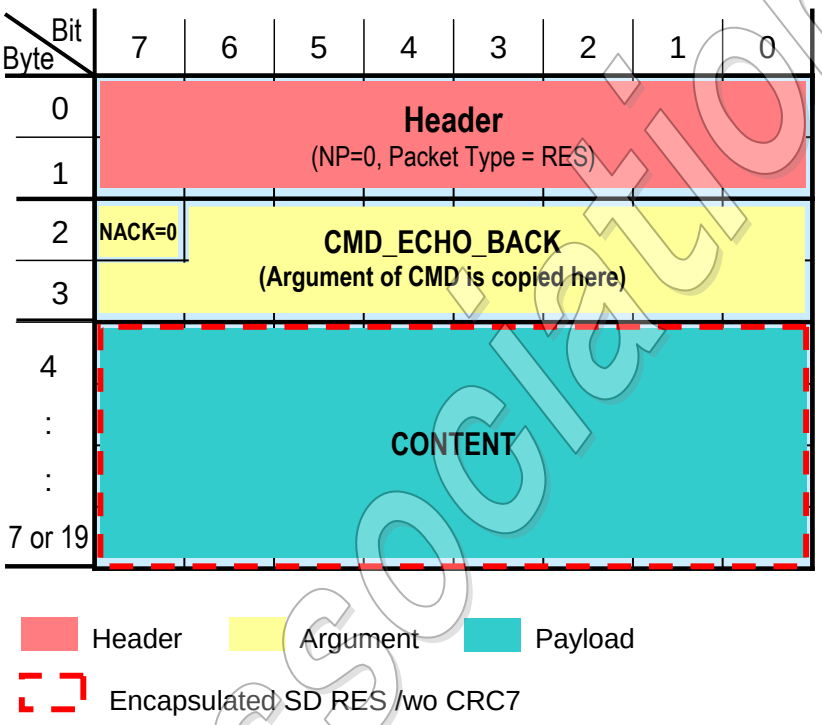
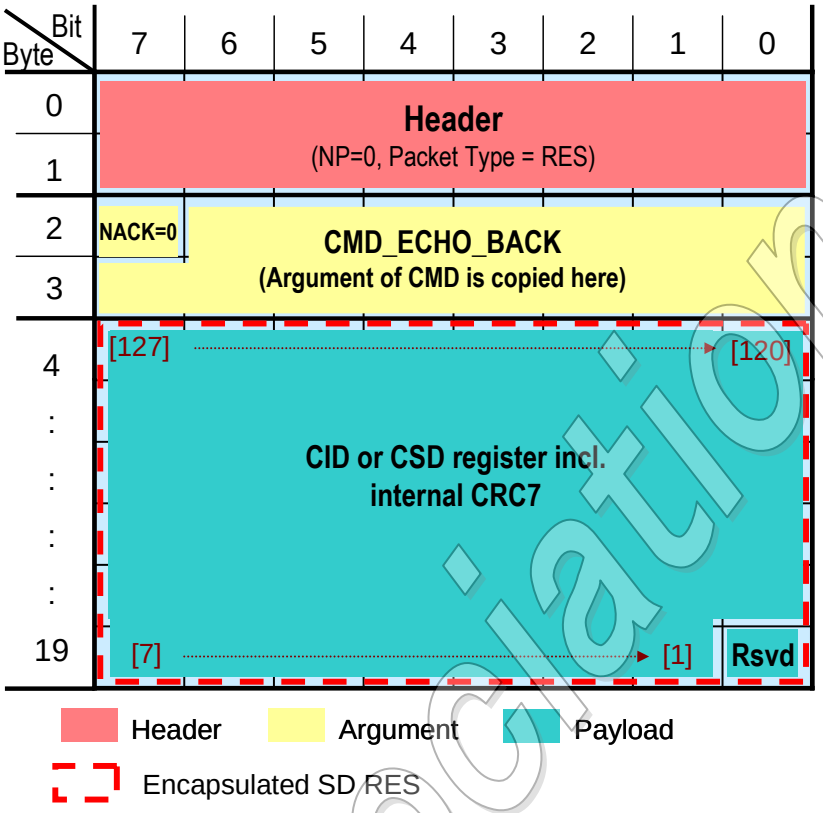


Figure 7-6 : RES Format on SD-TRAN (Generic)

- **NACK (Negative Acknowledgement):** Indicator whether the corresponding CMD is accepted or not.
- **CMD_ECHO_BACK[14:0] (Command Echo Back):** Copied field of CMD Argument.
  - The same values in Argument field such as CMD_INDEX or TMODE are copied from the corresponding CMD (echo back). Specifically, [6:0] in the second byte, and [7:0] in the third byte of CMD packet are copied to the same location of RES packet.
- **CONTENT:** Content of Response. Refer to Figure 7-7 for R2, and Figure 7-8 for other than R2 for more details. Rsvd in Figure 7-7 is reserved bits, so initiator (Device) shall set it to '0' and receiver (Host) shall ignore them.

DID field in Header is set to the same value as SID field in Header of the corresponding command. TID field in Header is set to the same value as TID field in Header of the corresponding command.



Note: In UHS-II mode, field of CRC7 in R2 response is not used to check CRC, and may be set any value

Figure 7-7 : RES Format on SD-TRAN (R2)

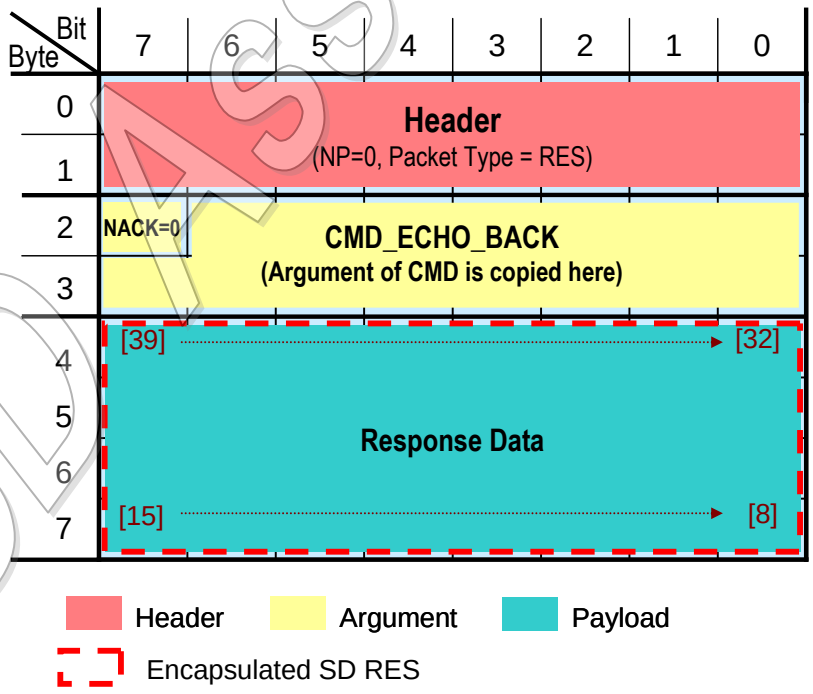


Figure 7-8 : RES Format on SD-TRAN (Other than R2)

7.2.1.4 RES (NACK = 1)

Unlike the Legacy SD protocol, Device shall respond RES with NACK = 1 if it receives illegal CMD. Figure 7-9 illustrates the RES with NACK = 1 on SD-TRAN.

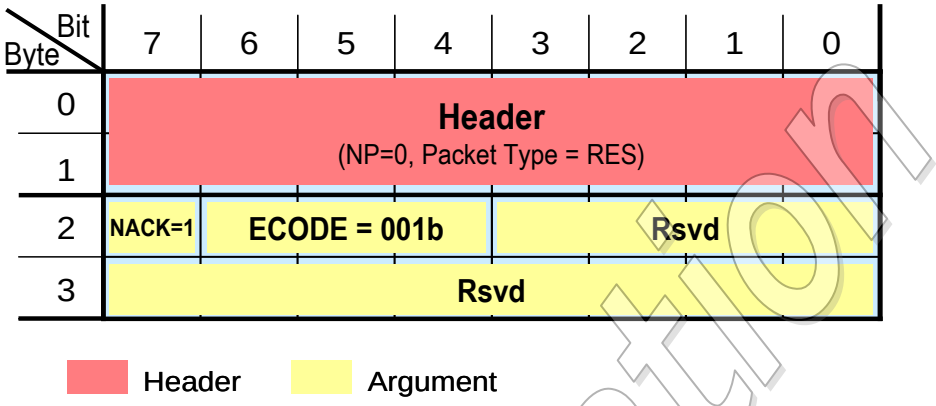


Figure 7-9 : RES (NACK = 1) Format on SD-TRAN

- **NACK (Negative Acknowledgement):** indicator whether the corresponding CMD is accepted or not.
  - NACK = 1 means the corresponding CMD is rejected.
  - In the case of NACK = 1 (CMD is rejected), Device shall not execute the requested operation (an error has occurred in the corresponding CMD).
- **ECODE[2:0] (Error Code):** Error code to represent error descriptions. It shall be set to 001b in SD-TRAN.
- **Rsvd (Reserved):** Reserved bits. Initiator shall set them to '0', and receiver shall ignore them.

7.2.1.5 DATA

Figure 7-10 illustrates DATA on SD-TRAN.

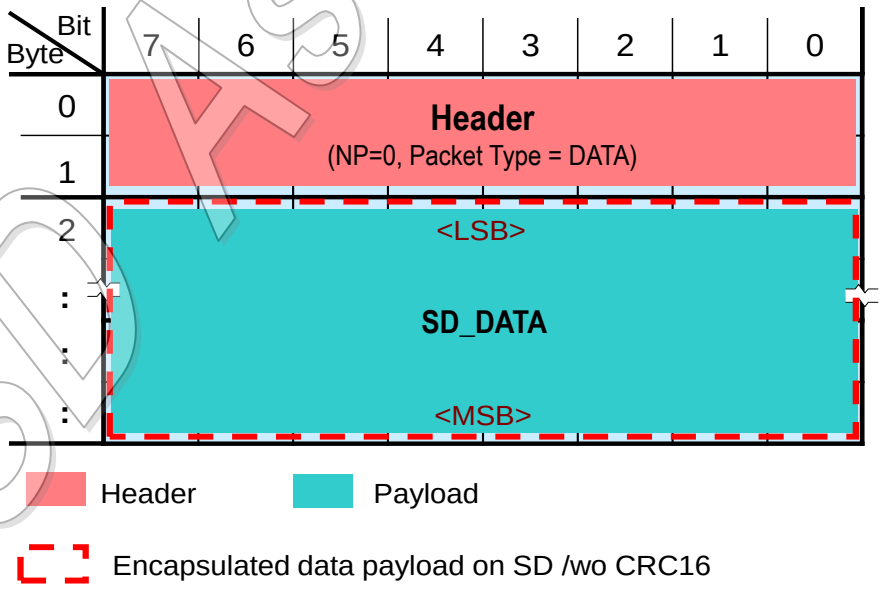


Figure 7-10 : DATA Format on SD-TRAN

- **SD_DATA:** Data included with DATA
  - The length of Payload field depends on CMD_INDEX. Refer to Section 7.2.2 for more details.
  - It is transmitted in LSB first, MSB last.

Following of Section 7.2.1 is a blank in the Simplified Addendum.

7.2.2 DATA Burst Framing Rules in SD-TRAN

Section 7.2.2 is a blank in the Simplified Addendum.

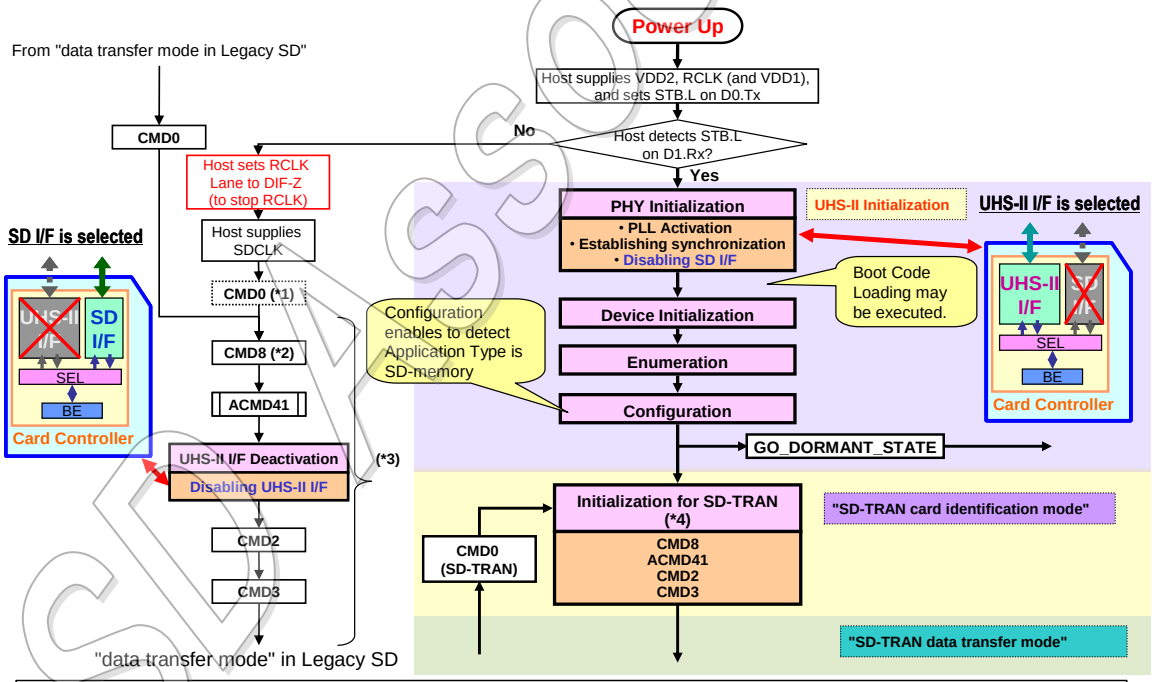
7.2.3 Interface Selection for UHS-II Card and Initialization

7.2.3.1 Overview

As Hosts and Devices supporting UHS-II interface shall also support SD Legacy interface, Host supporting UHS-II (simply described as "Host") interface may select either UHS-II interface or Legacy SD interface after power up. Only in Section 7.2.3, "CMD" denotes the command described in SD Physical Simplified Specification Version 4.10, and SD command on UHS-II is described as "encapsulated CMD".

7.2.3.2 Interface Selection after Power Up

Figure 7-11 shows a concept diagram of initialization flow after power up.



Note:
(*1) CMD0 can be issued before CMD8.
(*2) CMD8 is mandatory because UHS-II Card is not available over SDSC.
(*3) Refer to SD Specifications Part 1 Physical Layer Specification Version 4.00.
(*4) All CMDs are executed on SD-TRAN.

Figure 7-11 : Initialization Flow after Power Up

If Host intends to use UHS-II interface, it supplies VDD2, RCLK and VDD1 after power up, and sets STB.L on D0.Tx. Device connects termination resistors of RCLK Lanes after power up. Device starts PHY Initialization when receiving STB.L and responds STB.L if it succeeds.
The method for Host to distinguish whether Device fails to start PHY initialization is through detecting timeout from Host's setting STB.L on D0.Tx to receiving it on D1.Rx, which can be estimated from Teidl_stb and UHS-II bus topology.
If Host detects timeout, Host sets RCLK Lane to DIF-Z to stop supplying RCLK, and then Host supplies SDCLK and issues CMD8 and ACMD41 for Legacy SD protocol to initialize SD interface. Then, Host proceeds card identification and the card status transits to "data transfer mode" in Legacy SD (same as data transfer mode defined in SD Specifications Part 1 Physical Layer Simplified Specification Version 4.10) as a result. When Legacy SD interface is selected, UHS-II interface that is activated by power up is disabled before ACMD41 is completed. Moreover, termination resistors of RCLK Lanes in Device are disconnected when disabling UHS-II interface. As the sequence to "data transfer mode" in Legacy SD in Figure 7-11 is simplified, refer to SD Specifications Part 1 Physical Layer Simplified Specification Version 4.10 for detailed specifications of Legacy SD initialization. Note that if CMD0 is issued in Legacy SD card state transits to 'idle'. (Note that it is impossible to execute (UHS-II) PHY Initialization.)
On the other hand, if Device succeeds PHY Initialization, UHS-II interface is available and then, Device Initialization, Enumeration and Configuration take place in this order. If Host detects "Application Type" is "SD memory" or "SDIO" during Configuration, it can issue the encapsulated SD CMD. Host shall execute card identification described in Section 7.2.4.1 by encapsulated SD CMDs in case of detecting "SD memory". If encapsulated CMD0 is issued, card state transits to 'idle' in SD-TRAN. On the other hand, if FULL_RESET CCMD is issued, Device waits STB.L for PHY Initialization.

If Host intends to use only Legacy SD interface or detects that Legacy SD Card is inserted, it is allowed to supply only VDD1 and SDCLK, and issue CMD8 in order to accelerate initialization of Legacy SD interface. Note that once UHS-II I/F is disabled, Host requires power cycle to enable UHS-II again. Refer to Section 3.10.4 in SD Specification Part 1 Version 4.00 for more details about VDD2 supply.
Note that Device's power consumption during Device Initialization is not regulated by Power Limit specified by CMD6, but parameters specified by DEVICE_INIT CCMD.

7.2.3.3 Interface Selection after FULL_RESET or GO_DORMANT_STATE

Figure 7-12 shows a concept diagram of initialization flow after executing FULL_RESET or GO_DORMANT_STATE CCMD.

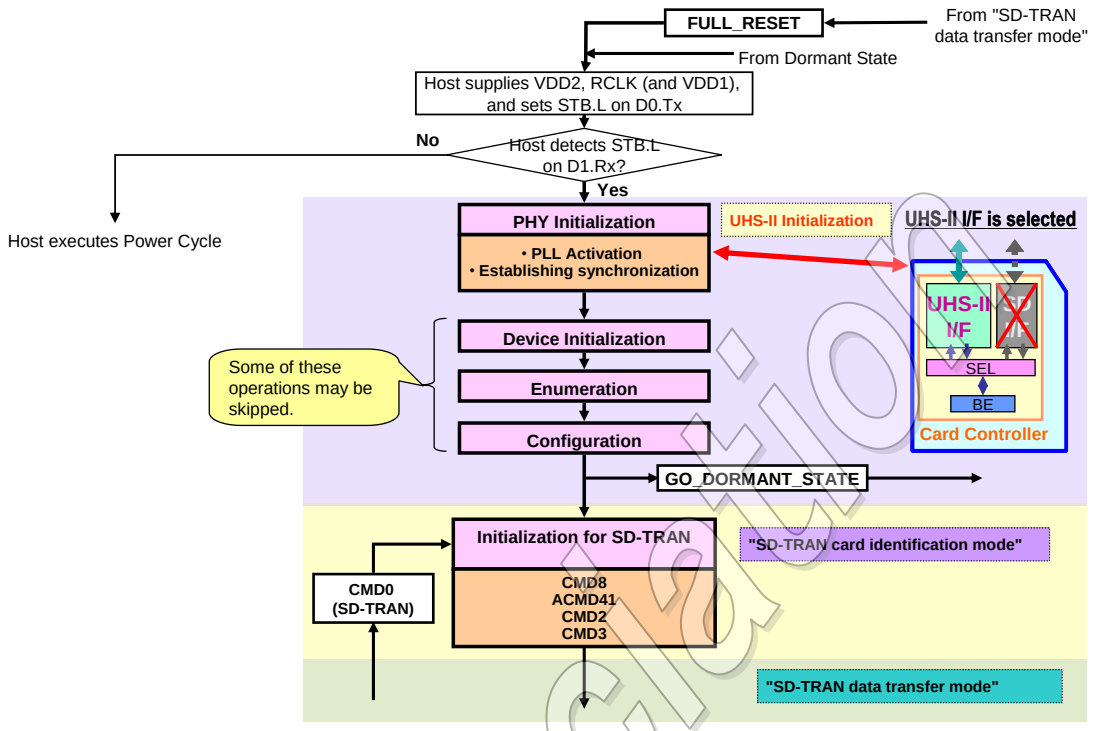


Figure 7-12 : Initialization Flow after FULL_RESET or GO_DORMANT_STATE

Host shall not select Legacy SD interface after issuing these CMDs. Then if Host detects that Device fails to start PHY Initialization, Host requires power cycle to recover this illegal situation.
Setting of Power Limit specified by CMD6 is kept after recovering from Dormant State. After exiting Dormant State and until going into Active state, power consumption of Device is up to 0.72W. Setting of Power Limit which has been specified by CMD6 is effective in Active state again.

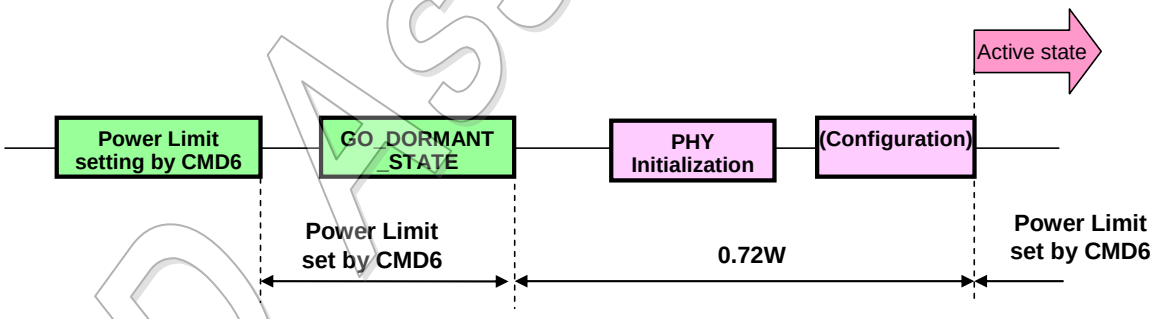


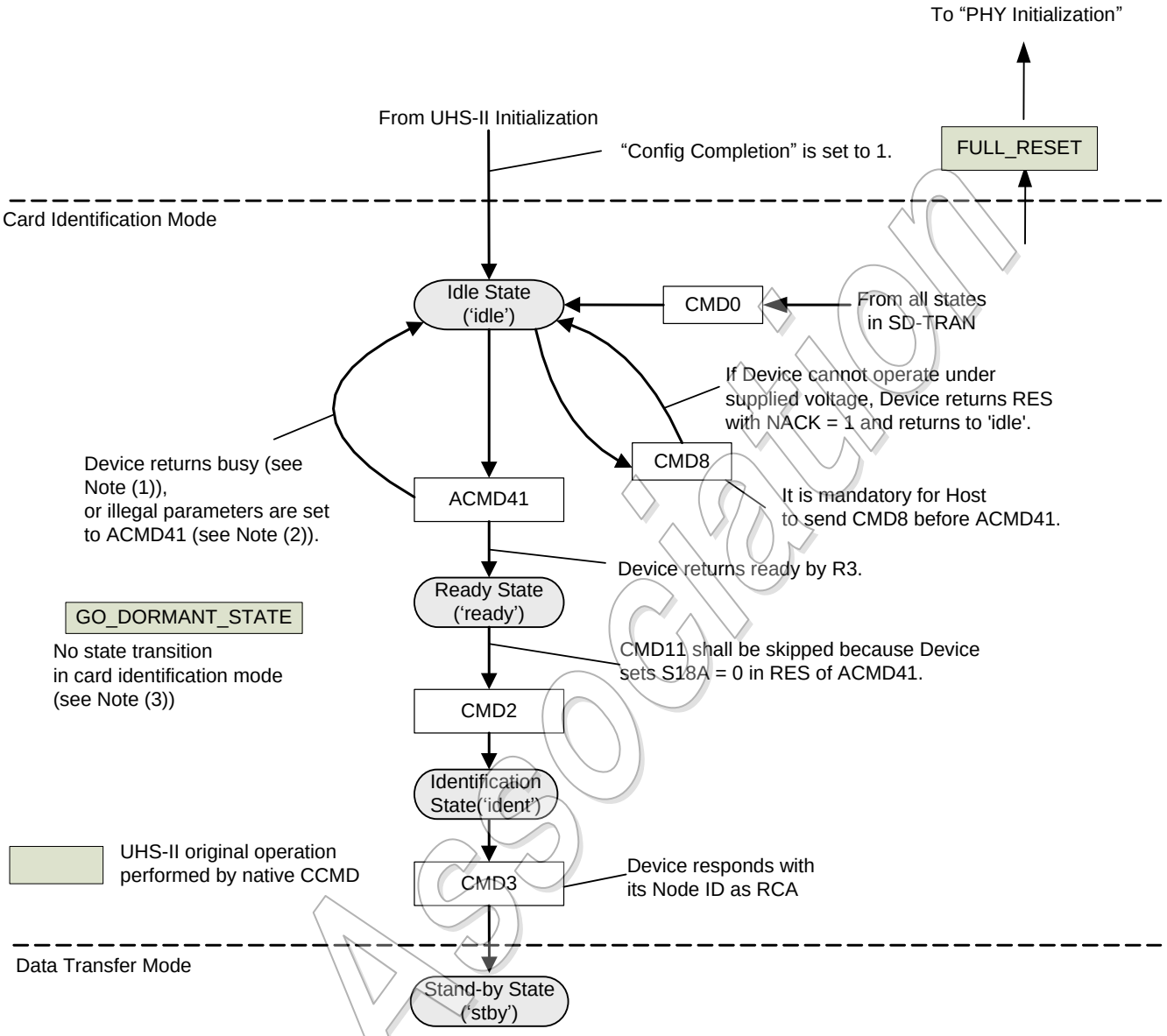
Figure 7-13 : Power Consumption after Exiting from Dormant State

7.2.4 Transaction Control and Management State Machine

From this section, an "encapsulated CMD" is described as just a "CMD" for simplicity (e.g. "encapsulated CMD0" is described as "CMD0"). In this section, state diagrams in card identification mode and data transfer mode for SD-TRAN are shown. They are based on those in Legacy SD, but some differences exist as described below.

7.2.4.1 Card Identification Mode

Figure 7-14 shows a state diagram for card identification mode on SD-TRAN.



Note:
(1) Device returns busy when Device executes internal initialization process
(2) Device always returns RES with NACK = 1 when illegal parameters are set to the CMD
e. g.)
- CMD8 with improper VHS.
- ACMD41 with HCS = 0.

(3) Card status is kept after recovering from Dormant state.

Figure 7-14 : State Diagram on SD-TRAN (Card Identification Mode)

Differences from the Legacy SD are as follows.

- Like Legacy SD, Host shall issue CMD8 and then ACMD41 in order to transit from 'idle' to 'ready'.
- If Device receives CMD with illegal parameters, Device shall return RES with NACK = 1 on SD-TRAN.
    - RES with NACK = 1 is transmitted in illegal CMD8.

    - Device never returns ready in illegal ACMD41, and the state transits to 'idle' state.
- CMD11 shall be skipped. Related to this Device shall set '0' to S18A field in RES of ACMD41.
- If Device receives CMD3, Device responds with its own Node ID as new RCA. As each Device's Node ID is guaranteed to be distinctive even in case of multiple-Device connection, Host does not need to reissue CMD3 for avoiding RCA duplication.
- The 'ina' state and its related transition are removed from SD-TRAN.

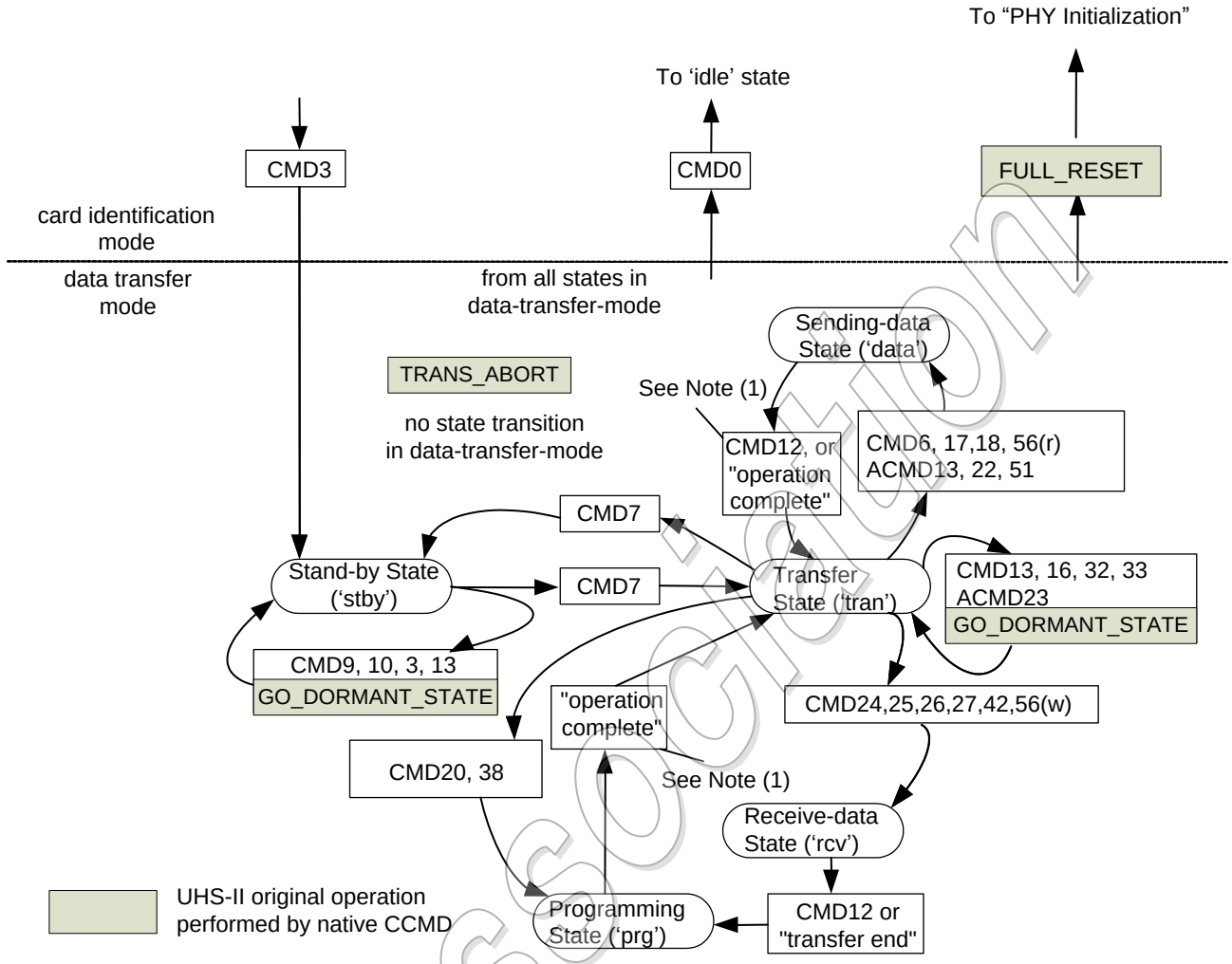
During card identification mode, Device operation when receiving native CMD is same as that in Active state. Host cannot issue arbitrary DCMD during this mode. Note that card status is kept when receiving GO_DORMANT_STATE CCMD. So Device directly transits to the appropriate card status after UHS-II Initialization in case of recovery from Dormant state. For example, if card status was 'ready' before transiting to Dormant state, it is still 'ready' after recovering from Dormant state. This rule is same as for 'idle' and 'ident' (and also same as 'stby' and 'tran' in Data Transfer Mode).

7.2.4.2 Data Transfer Mode

Figure 7-15 shows a state diagram for data transfer mode of SD-TRAN. Differences from the Legacy SD are as follows.

- Common CMDs with Legacy SD shall be executed through SD-TRAN.
- The 'dis' state and its related transitions are abandoned for simplicity. And transition from 'data' state to 'stby' state is also removed.
- Transitions by CMD7 are defined as follows.
    - Transits to 'tran' if RCA in CMD7 is equal to Device's Node ID.
    - Transits to 'stby' if RCA in CMD7 is not equal to Device's Node ID.
- RCA in the argument shall be ignored other than CMD7.
- If Device receives illegal command in 'stby' state, Device shall return RES with NACK = 1.
- CMD13 can be issued only in 'stby' or 'tran' state. In other words, CMD13 cannot be issued during CTS in case of SD memory.
- When Device receives CMD3 in 'ident' state or 'stby' state, Device shall always return its Device ID as RCA.

For read transaction, state transits from 'data' to 'tran' at transmission of MSG (EBSY). For write transaction, state transits from 'rcv' to 'prg' when Device receives all DATA packets specified by TLEN on write DCMD, or it transmits RES (R1b) of CMD12 corresponding to write DCMD. In addition, state transits from 'prg' to 'tran' at transmission of MSG (EBSY).



Note:
(1) In fact, this state transition occurs at transmission of MSG(EBSY) in UHS-II.

Figure 7-15 : State Diagram on SD-TRAN (Data Transfer Mode)

Following of Chapter 7 is a blank in the Simplified Addendum.

8. 2L-HD Mode (optional)

8.1 Overview

Lower operating frequency generally provides applicability to a variety of hosts due to easy implementation of whole system. Duplex mode switching between FD mode and 2L-HDmode achieves a good balance between easy controllability and higher bus efficiency under I/O pin count restriction as in SD Memory.

FD mode provides easy controllability by setting D0 and D1 to different directions, because handshake between Host and Device can be performed anytime. It is the default mode in UHS-II. On the other hand, 2L-HD mode realizes higher speed data transfer than FD mode by setting D0 and D1 to the same direction. 2L-HD mode is optional in UHS-II specification.

Basically, CCMD, DCMD, RES and MSG are transmitted in FD mode. Only DATA can be transmitted in both FD mode and 2L-HD mode. If Host intends to read or write data in 2L-HD mode, duplex mode switching shall be executed after DCMD and RES handshake.

On the way of data transmission in 2L-HD mode, it suspends data transmission and switches to FD mode temporarily in order to keep room for sending CCMD or MSG. Then it switches to 2L-HD mode again and continue data transmission.

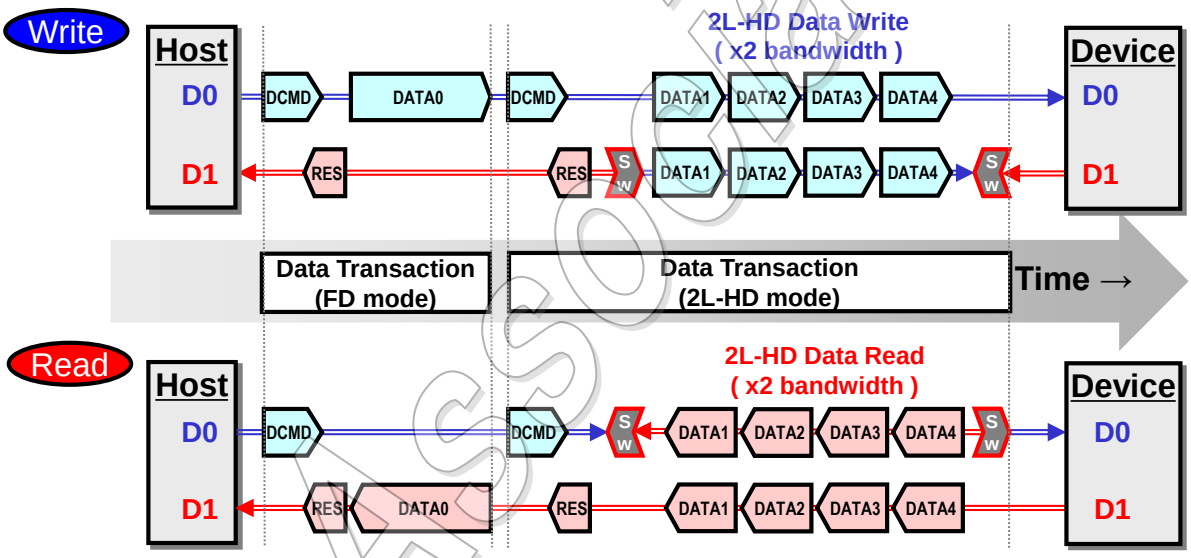


Figure 8-1 : Overview of FD Mode and 2L-HD Mode

Following of Chapter 8 is a blank in the Simplified Addendum.

9. Additional Lanes Support (optional)

9.1 Overview

Lower operating frequency generally provides applicability to a variety of Hosts due to easy implementation of whole system. Adding more Lanes can give a good balance between performance and complexity.

The basic idea is to extend to concept of FD mode and 2L-HD mode for DATA packets. Host and Device can have one additional Lane (D2 or D3) or two additional Lanes (D2, D3), both are optional.

Device reports its capabilities in Generic Capabilities Register.

Figure 9-1 shows the entire possible Lane configuration.

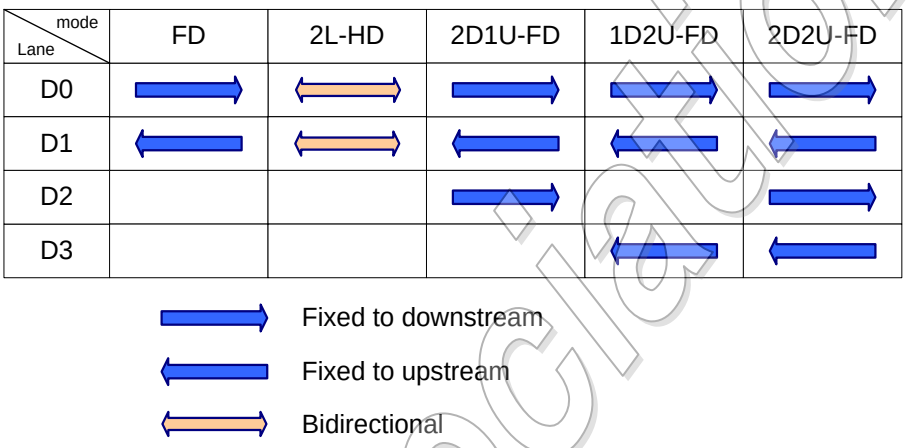


Figure 9-1 : Possible Lanes Configurations in FD / 2L-HD Mode

Following of Chapter 9 is a blank in the Simplified Addendum.

Appendix A (Normative) : Reference

A.1 Related Documentation

- SD Specifications Part 1 Physical Layer Simplified Specification Version 4.10 or later
- ANSI X3.230-1994, clause 11 (and also IEEE 802.3z, 36.2.4)

Appendix B (Normative) : Special Terms

B.1 Terminology

2L-HD mode	Half Duplex with 2 Lanes mode
8b/10b	One of line coding that maps 8-bit symbols to 10-bit symbols to achieve DC-balance and bounded disparity.
Block	Data unit to be transmitted by one DATA packet
Block Length	Data length for one Block
Boot Code	Code including initial set of operations using bootstrapping process
Boot Code Loading	Transmitting Boot Code from Boot Device to Host immediately after PHY Initialization
Boot Device	Device that stores Boot Code
broadcast	Operating to all connecting nodes (Devices)
BUSY period	Period that Host cannot access to backend (flash memory for SD-memory)
Card	SD memory card
CM	Common Mode
CM-TRAN	Common transaction layer in UHS-II
Command Time Slot	Time period that FULL_RESET, TRANS_ABORT, and arbitrary read CCMD are allowed to be issued on the way of data transmission
Configuration	An arrangement of functional unit or parameters according to capabilities of Host and Devices
DATA Burst	A unit that consists of one or more DATA packets and related LSS and can be sent in one flow control unit
DATA Burst Streaming	Bypassing DATA Bursts to the next Node without passing through LINK.
De-embedding	Removing the effect of unwanted component from the measurement result
Device	The electrical equipment which transmit/receive data to/from Host and communication is controlled by Host. Device includes Card and Embedded Device
Device Initialization	Process to make Device enable its all functions
downstream	Transmission from Host to Device
Embedded Device	Non-removable SD Device without form factor
Enumeration	Assigning Node ID for each connecting Device
FD mode	Full Duplex mode
Flow Control	Process of managing the data transmission to prevent data overflow or underflow.
Flow Control Unit	A unit of period for data transmission accompanied by FCREQ-FCRDY handshake. Also refer to DATA Burst.
Fractional DATA Burst	A DATA Burst which consists of Framed DATA packet less than N_FCU
Framing	Prefixing SOP and postfixing EOP for packets, and prefixing SDB and postfixing EDB for DATA Burst.
Full Duplex mode	Communication mode that the direction of two Lanes is opposite each other.
Half Duplex with 2 Lanes mode	Communication mode that the direction of two Lanes is same. It is optional in UHS-II.
Host	The electrical equipment which transmit/receive data to/from Device (e. g. SD Card) and control the communication. Only Host can issue commands.
Hub	Device that allows many Devices to be connected to a single port on a Host
I/F power cycle	Act of turning whole UHS-II interface off and then on again by I/F power

	supply
I/F power supply	Power supplement for UHS-II interface (e.g. VDD2 for SD-memory)
Inter skew	The skew between differential Lanes transmitting in same direction.
Intra skew	The skew between Positive Line signal and Negative Line signal of one differential pair.
Jitter	Jitter is undesirable time variation of a periodic signal, which is caused by ISI and some fluctuations such as voltage supply and temperature etc.
Lane	Each set which consists of Tx Port, transmission Line and Rx Port. For example, D0 consists of D0.Tx in Host, D0 Line and D0.Rx in Device.
Legacy SD	SD card not supporting UHS-II interface
Line	Component for connecting a Tx (Transmitter) Port and an Rx (Receiver) Port and realizing differential transmission
LINK	The interface layer above PHY Layer. LINK is in charge of controlling data flow and making management for LINK and PHY.
Loopback	Method or procedure of routing electronic signals from their originating facility quickly back to the same source entity without intentional processing or modification
Node	Host or Device
Node ID	Number to identify Nodes
Packet bypassing	Sending packets to the next Node without any operations in TRAN
Parallel termination	Termination connecting positive and negative Lines of a differential Lane
PHY	Physical Interface Layer
Return loss	Reflection ratio of signal power in a transmission Line
Rx	Receiver Circuit, which is responsible for outputting differential signal
SD-TRAN	One of application specific layers in UHS-II. It bridges CM-TRAN and Legacy SD applications or drivers.
Serializer/Deserializer	A pair of functional blocks to compensate for limited input/output. These blocks convert data between serial data and parallel interfaces in each direction.
skew	Time difference of transmission delay between two transmission Lines
TRAN	The interface layer above LINK. It is divided into CM-TRAN and an application specific TRAN.
transaction	A unit of communication that takes place by one command
Tx	Transmitter circuit, which is responsible for outputting differential signal
UHS-II Card	SD card supporting UHS-II Interface
UHS-II native	UHS-II without (or not considering) application specific layers
upstream	Transmission from Device to Host
Wakeup	PHY initialization state
X5R,X7R	Symbol for dielectric material of capacitors

B.2 Abbreviations

BSYN	Synchronization for Boot Code Loading
CCMD	Control Command
CDCP	Candidate DCP
CF	Completion Flag of Device Initialization
CFG_REG	Configuration Register

CMD	Command
CMD_REG	Command Register
COM	Comma Symbol
CPR	Control Packet Reception
CRC	Cyclic Redundancy Check
CTS	Command Time Slot
DAM	Data Access Mode
DAP	Device Allocated Power
DATA	DATA packet
DBR	DATA Burst Reception
DCMD	Data Command
DCP	Device Consumed Power
DFL	Direction Fixed Lane
DID	Destination ID
DIDL	Data Idle
DIF-H	Differential High state
DIF-L	Differential Low state
DIF-PD	Pull-down state
DIF-Z	High-Z (high impedance)
DIR	Direction
D_J	Deterministic jitter
DLSM	Data Link State Machine
DM	Duplex Mode
DSL	Direction Switched Lane
EDB	End of DATA Burst
EIDL	Electrical Idle
EMI	Electromagnetic interference
EOP	End Of Packet
ESD	Electrostatic Discharge
FC	Flow Control
FCRDY	Flow Control Ready
FCREQ	Flow Control Request
FCU	Flow Control Unit
GAP	Group Allocated Power
GD	Group Descriptor
GN	Group Number
INT	Interrupt
INT_REG	Interrupt Register
IP	Intellectual Property
ISI	Inter Symbol Interference
LFSR	Linear Feedback Shift Register
LIDL	Logical Idle
LM	Length Mode
LPM	Low Power Mode
LPS	Low Power State
lsb	Least Significant Bit
LSB	Least Significant Byte

LSI	Large Scale Integration
LSS	Link Symbol Set
MAX_BLKLEN	Maximum payload length of one block
MLCC	Multi-Layer ceramic capacitor
msb	Most Significant Bit
MSB	Most Significant Byte
MSG	Message
NACK	Negative-acknowledge
N_FCU	Number of blocks in a FCU
P2P	Point to Point
PAD	Padding Symbol
PLEN	Payload Length
PLL	Phase-Locked Loop
PLSM	Physical Lane State Machine
PM	Power Management
RCLK	Referential Clock
RES	Response
R_J	Random jitter
SDB	Start of DATA Burst
SI	Symbol Interval, equal to 10 * UI
SID	Source ID
SOP	Start Of Packet
SSC	Spread Spectrum Clocking
STAT	Status Message
STB	Standby
ST_REG	Status Register
SYN	Synchronization
TBD	To Be Determined
TBSM	Transaction Buffer-management State Machine
TDR	Time Domain Reflection
TID	Transaction ID
T_J	Total jitter
TLEN	Transfer Length
TLP	Transaction Layer Packet
TLUM	TLEN Unit Mode
TPSM	Transaction Processing State Machine
TSSM	Transaction Scheduling State Machine
UI	Unit Interval or data bit time interval
VLD	Valid State
VU_REG	Vendor Unique Register

Appendix C (Normative) : Test Condition of Measuring Output Signals

C.1 Test Condition for Host Output Signal at TP2

By using Host test fixture, illustrated in Figure C- 1, a measurement for output waveform of Host transceiver is performed. The Test fixture is designed to be as ideal as possible (100ohm differential impedance and 25ohm common-mode impedance as the target). A detailed description of the test fixture and the test procedure is defined in UHS-II PHY Test Guideline document

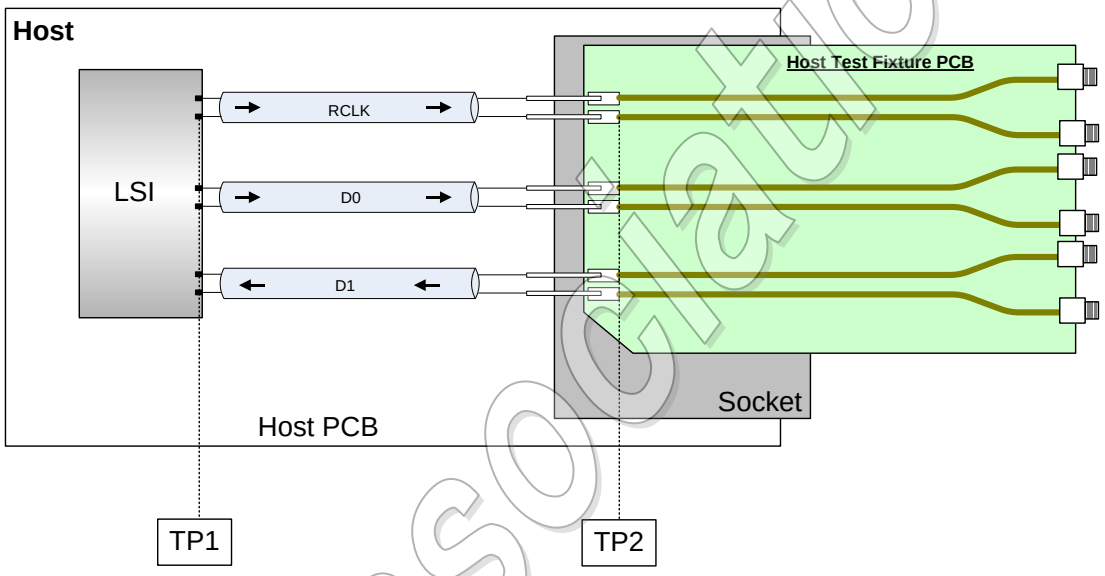


Figure C- 1: Host Test Fixture Illustration (Concept)

C.2 Test Condition for Card Output Signal at TP2

By using Card test fixture, illustrated in Figure C- 2, a measurement for output waveform of Card transceiver is performed. The test fixture is designed to be as ideal as possible (100ohm differential impedance and 25ohm common-mode impedance as the target). A detailed description of the test fixture and the test procedure is defined in UHS-II PHY Test Guideline document

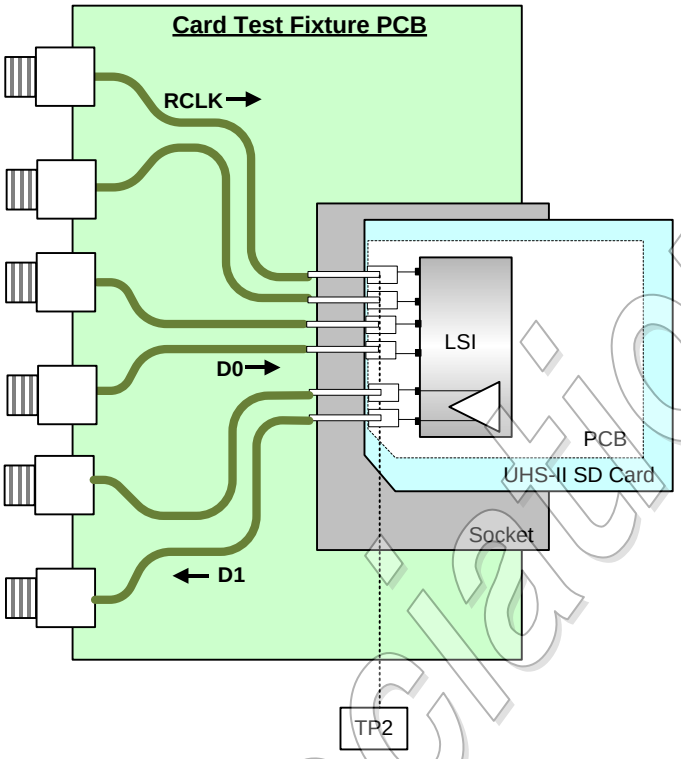


Figure C- 2: Card Test Fixture Illustration (Concept)

Appendix D (Normative) : Register

D.1 Register Summary

D.1.1 Register Types

Attribute of register field should be defined as an example shown below. It may help easy to understand register specification

Register fields are assigned one of the attributes described below:

Register Attribute	Description
RO	Read-only register: Register bits are read-only and cannot be altered by software or any reset operation. Writes to these bits are ignored.
ROC	Read-only status: These bits are cleared to zero at reset. Writes to these bits are ignored.
ROW1C	Read-only status, Write-1-to-clear status: Register bits indicate status when read, a set bit indicating a status event may be cleared by writing a 1. Writing a 0 to ROW1C bits has no effect.
RW	Read-Write register: Register bits are read-write and may be either set or cleared by software to the desired state. These bits are cleared to zero at reset.
RWAC	Read-Write, automatic clear register: Software requests an operation by setting the bit. The hardware shall clear the bit automatically when the operation completes. Writing a 0 to RWAC bits has no effect.
HwInit	Hardware Initialized: Register bits are initialized by firmware or hardware mechanisms. Bits are read-only after initialization, and writes to these bits are ignored.
Rsvd	Reserved. Device shall initialize to zero on reserved bits and ignore writes to these bits. Host shall ignore these bits. The bit can be defined for future use.

Table D- 1 : Register Attribute Table

D.1.2 Register Initial Values

Hardware should set registers to their initial values at power-on reset. Initial values for RO and HwInit are specified by each Device. Those for other types of register shall be set to zero except parameters used in Boot Code Loading.

Appendix E (Informative) : Design Guide

This appendix is a blank in the Simplified Addendum.

Appendix F (Informative) : PHY-LINK I/F

This appendix is a blank in the Simplified Addendum.

Appendix G (Informative) : Host's Operation in Detecting Timeout

This appendix is a blank in the Simplified Addendum.