**微算機系統**

**小組專案報告**

實驗一

組別： 18

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1. 實驗內容：

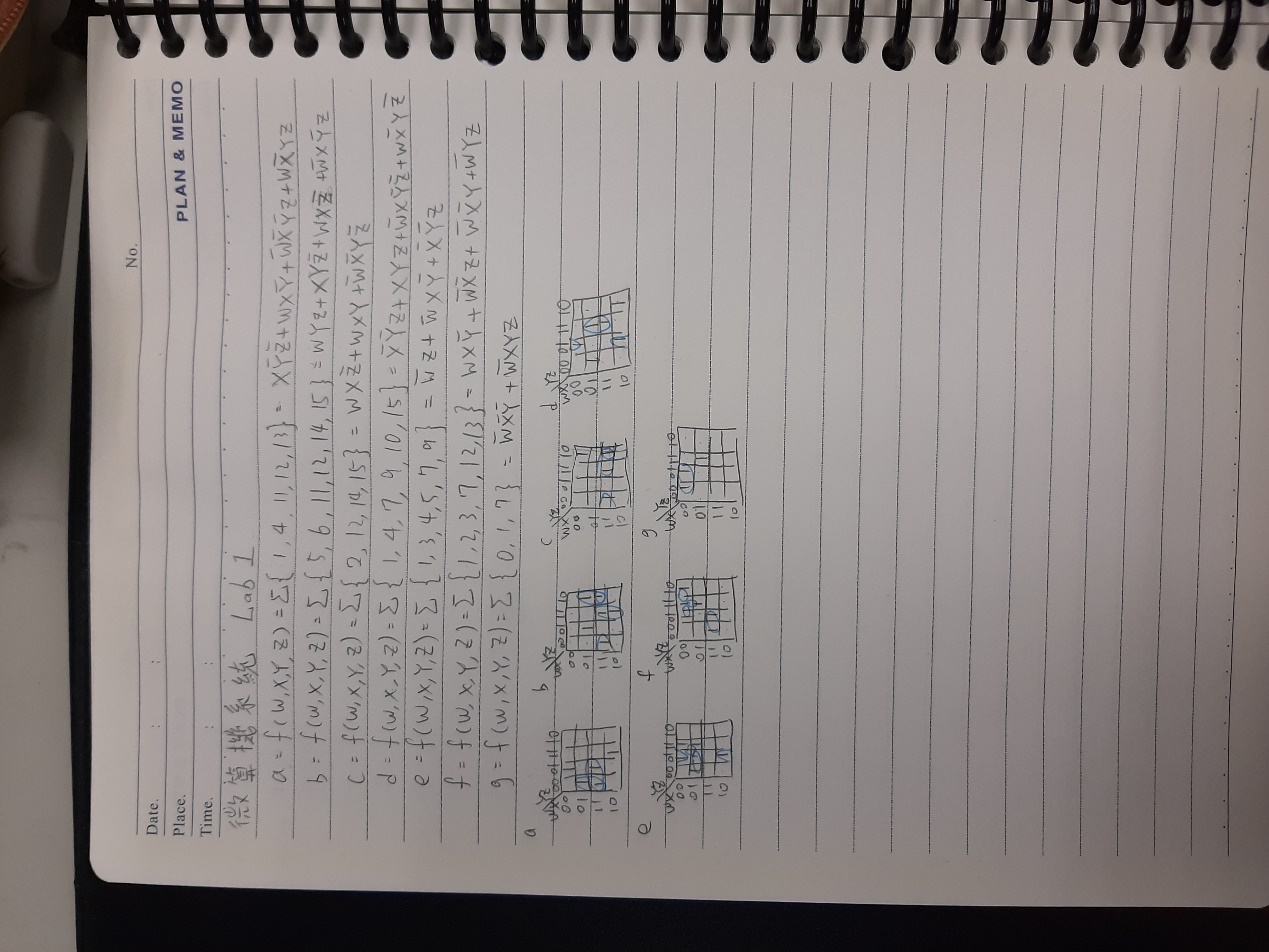
練習以VHDL邏輯函數方式實驗邏輯電路，使七段顯示器顯示出0~9,AbcdEF

1. 實驗過程及結果：

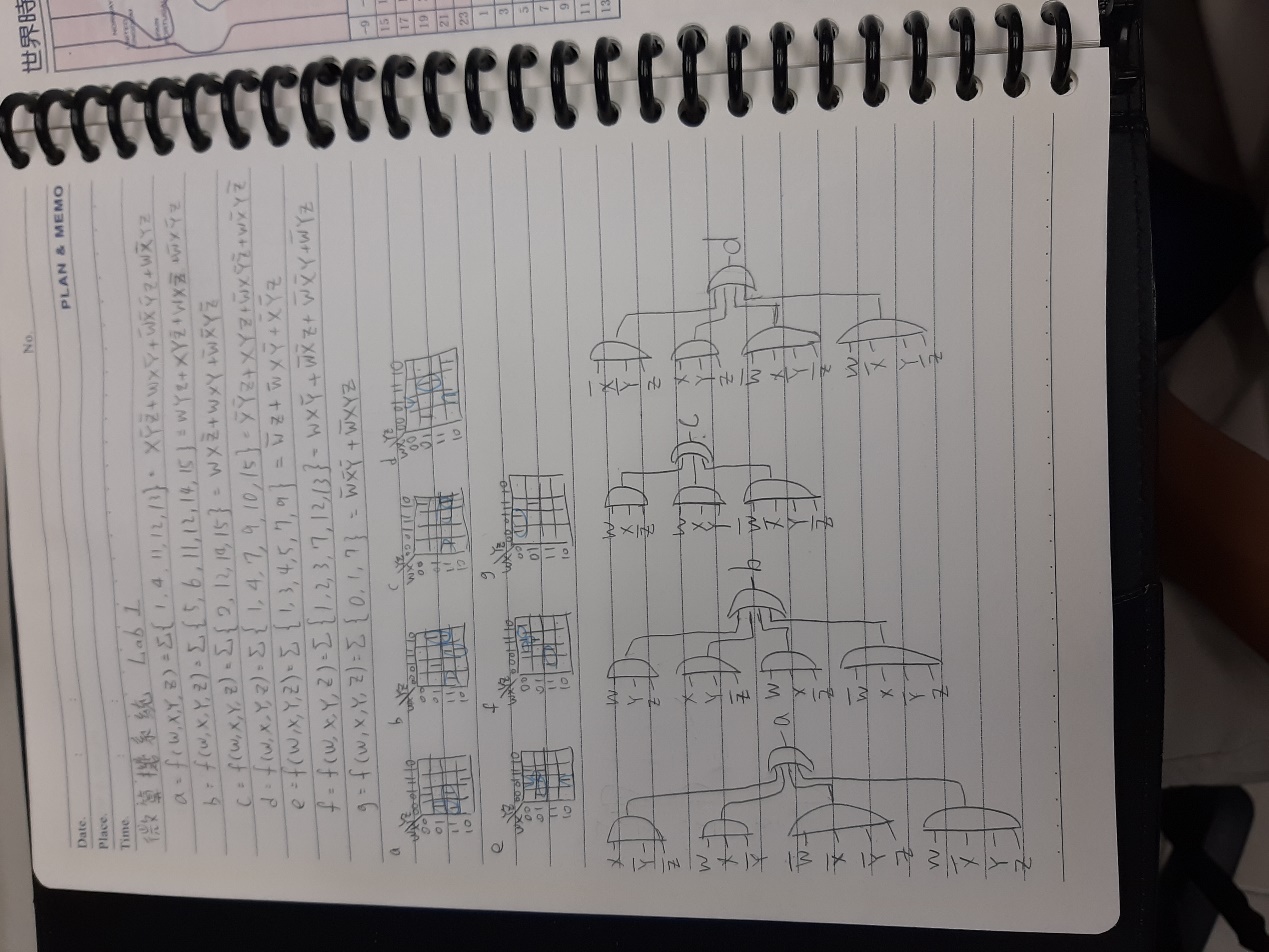
預期實驗結果的真值表

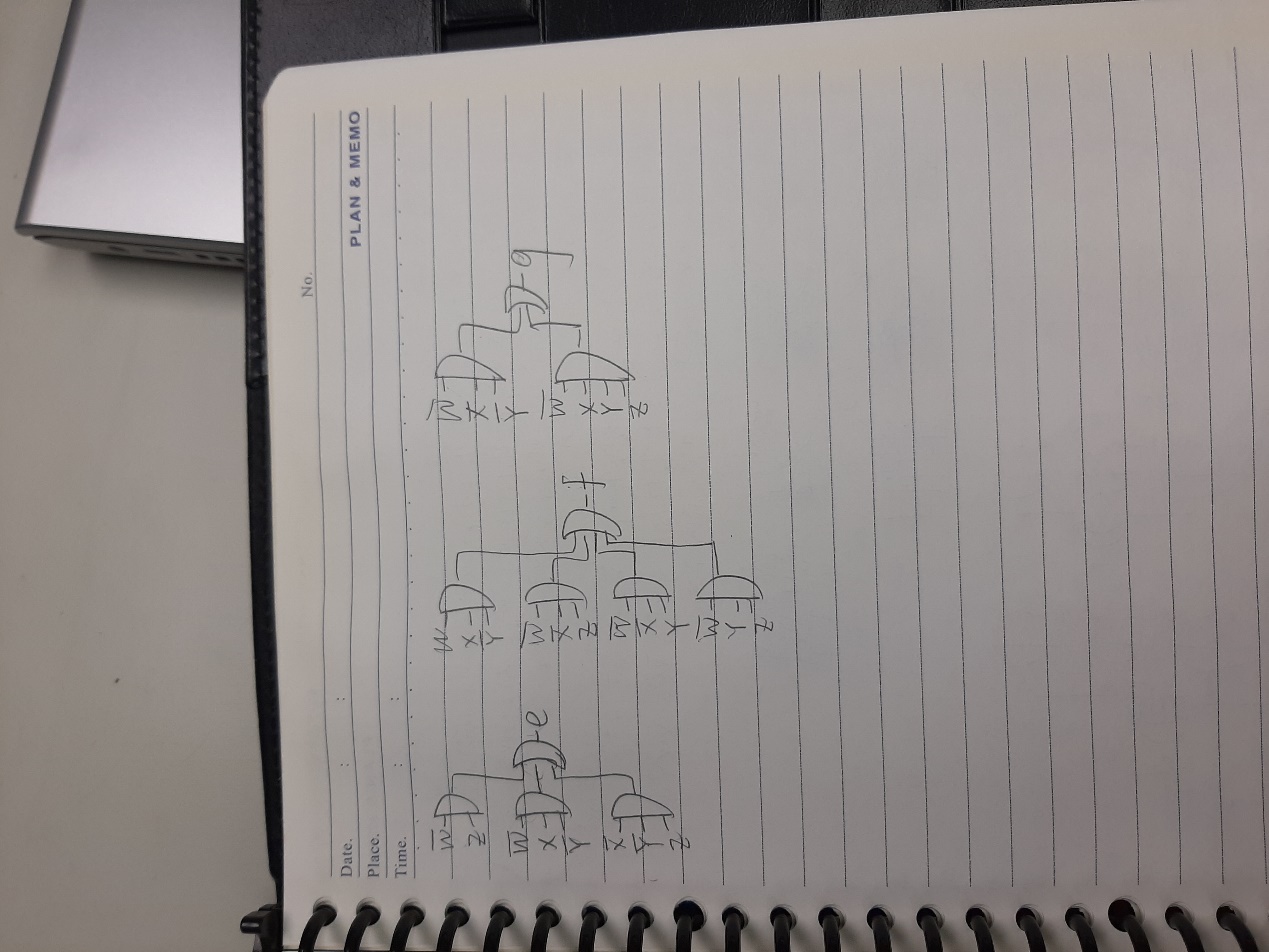


根據上方真值表使用卡諾圖來化簡



卡諾圖化簡後設計出的電路





實驗的結果

基本題

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1. 程式碼

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| 基本題 |
| library ieee;  use ieee.std\_logic\_1164.all;  entity Lab1\_1 is  port(  SW:in std\_logic\_vector(3 downto 0);  --SW(3)=W,SW(2)=X,SW(1)=Y,SW(0)=Z  HEX0:out std\_logic\_vector(6 downto 0)  );  end Lab1\_1;  architecture behavioral of Lab1\_1 is  --boolean  begin  --a  HEX0(0) <= (SW(2) and not(SW(1)) and not(SW(0))) or (SW(3) and SW(2) and not(SW(1))) or  (not(SW(3)) and not(SW(2)) and not(SW(1)) and SW(0)) or (SW(3) and not(SW(2)) and SW(1) and SW(0));  --b  HEX0(1) <= (SW(3) and SW(1) and SW(0)) or  (SW(2) and SW(1) and not(SW(0))) or  (SW(3) and SW(2) and not(SW(0))) or  (not(SW(3)) and SW(2) and not(SW(1)) and SW(0));  --c  HEX0(2) <= (SW(3) and SW(2) and not(SW(0))) or (SW(3) and SW(2) and SW(1)) or  (not(SW(3)) and not(SW(2)) and SW(1) and not(SW(0)));  --d  HEX0(3) <= (not(SW(2)) and not(SW(1)) and SW(0)) or (SW(2) and SW(1) and SW(0)) or (not(SW(3)) and SW(2) and not(SW(1)) and not(SW(0))) or (SW(3) and not(SW(2)) and SW(1) and not(SW(0)));  --e  HEX0(4) <= (not(SW(3)) and SW(0)) or  (not(SW(3)) and SW(2) and not(SW(1))) or  (not(SW(2)) and not(SW(1)) and SW(0));  --f  HEX0(5) <= (SW(3) and SW(2) and not(SW(1))) or (not(SW(3)) and not(SW(2)) and SW(0)) or  (not(SW(3)) and not(SW(2)) and SW(1)) or  (not(SW(3)) and SW(1) and SW(0));  --g  HEX0(6) <= (not(SW(3)) and not(SW(2)) and not(SW(1))) or  (not(SW(3)) and SW(2) and SW(1) and SW(0));  end behavioral; |

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| 加分題 |
| library ieee;  use ieee.std\_logic\_1164.all;  entity Lab1\_2 is  port(  SW2:in std\_logic\_vector(3 downto 0);  --SW(3)=W,SW(2)=X,SW(1)=Y,SW(0)=Z  HEX2:out std\_logic\_vector(6 downto 0);  SW1:in std\_logic\_vector(3 downto 0);  --SW(3)=W,SW(2)=X,SW(1)=Y,SW(0)=Z  HEX1:out std\_logic\_vector(6 downto 0);  SW0:in std\_logic\_vector(3 downto 0);  --SW(3)=W,SW(2)=X,SW(1)=Y,SW(0)=Z  HEX0:out std\_logic\_vector(6 downto 0)  );  end Lab1\_2;  architecture behavioral of Lab1\_2 is  --boolean  begin  --a  HEX2(0) <= (SW2(2) and not(SW2(1)) and not(SW2(0))) or (SW2(3) and SW2(2) and not(SW2(1))) or  (not(SW2(3)) and not(SW2(2)) and not(SW2(1)) and SW2(0)) or (SW2(3) and not(SW2(2)) and SW2(1) and SW2(0));  --b  HEX2(1) <= (SW2(3) and SW2(1) and SW2(0)) or (SW2(2) and SW2(1) and not(SW2(0))) or  (SW2(3) and SW2(2) and not(SW2(0))) or  (not(SW2(3)) and SW2(2) and not(SW2(1)) and SW2(0));  --c  HEX2(2) <= (SW2(3) and SW2(2) and not(SW2(0))) or (SW2(3) and SW2(2) and SW2(1)) or  (not(SW2(3)) and not(SW2(2)) and SW2(1) and not(SW2(0)));  --d  HEX2(3) <= (not(SW2(2)) and not(SW2(1)) and SW2(0)) or (SW2(2) and SW2(1) and SW2(0)) or  (not(SW2(3)) and SW2(2) and not(SW2(1)) and not(SW2(0))) or (SW2(3) and not(SW2(2)) and SW2(1) and not(SW2(0)));  --e  HEX2(4) <= (not(SW2(3)) and SW2(0)) or (not(SW2(3)) and SW2(2) and not(SW2(1))) or (not(SW2(2)) and not(SW2(1)) and SW2(0));  --f  HEX2(5) <= (SW2(3) and SW2(2) and not(SW2(1))) or (not(SW2(3)) and not(SW2(2)) and SW2(0)) or  (not(SW2(3)) and not(SW2(2)) and SW2(1)) or  (not(SW2(3)) and SW2(1) and SW2(0));  --g  HEX2(6) <= (not(SW2(3)) and not(SW2(2)) and not(SW2(1))) or  (not(SW2(3)) and SW2(2) and SW2(1) and SW2(0));  ----1  --a  HEX1(0) <= (SW1(2) and not(SW1(1)) and not(SW1(0))) or (SW1(3) and SW1(2) and not(SW1(1))) or (not(SW1(3)) and not(SW1(2)) and not(SW1(1)) and SW1(0)) or(SW1(3) and not(SW1(2)) and SW1(1) and SW1(0));  --b  HEX1(1) <= (SW1(3) and SW1(1) and SW1(0)) or (SW1(2) and SW1(1) and not(SW1(0))) or  (SW1(3) and SW1(2) and not(SW1(0))) or  (not(SW1(3)) and SW1(2) and not(SW1(1)) and SW1(0));  --c  HEX1(2) <= (SW1(3) and SW1(2) and not(SW1(0))) or (SW1(3) and SW1(2) and SW1(1)) or  (not(SW1(3)) and not(SW1(2)) and SW1(1) and not(SW1(0)));  --d  HEX1(3) <= (not(SW1(2)) and not(SW1(1)) and SW1(0)) or (SW1(2) and SW1(1) and SW1(0)) or  (not(SW1(3)) and SW1(2) and not(SW1(1)) and not(SW1(0))) or (SW1(3) and not(SW1(2)) and SW1(1) and not(SW1(0)));  --e  HEX1(4) <= (not(SW1(3)) and SW1(0)) or (not(SW1(3)) and SW1(2) and not(SW1(1))) or (not(SW1(2)) and not(SW1(1)) and SW1(0));  --f  HEX1(5) <= (SW1(3) and SW1(2) and not(SW1(1))) or (not(SW1(3)) and not(SW1(2)) and SW1(0)) or (not(SW1(3)) and not(SW1(2)) and SW1(1)) or  (not(SW1(3)) and SW1(1) and SW1(0));  --g  HEX1(6) <= (not(SW1(3)) and not(SW1(2)) and not(SW1(1))) or  (not(SW1(3)) and SW1(2) and SW1(1) and SW1(0));  ----0  --a  HEX0(0) <= (SW0(2) and not(SW0(1)) and not(SW0(0))) or (SW0(3) and SW0(2) and not(SW0(1))) or  (not(SW0(3)) and not(SW0(2)) and not(SW0(1)) and SW0(0)) or (SW0(3) and not(SW0(2)) and SW0(1) and SW0(0));  --b  HEX0(1) <= (SW0(3) and SW0(1) and SW0(0)) or (SW0(2) and SW0(1) and not(SW0(0))) or  (SW0(3) and SW0(2) and not(SW0(0))) or (not(SW0(3)) and SW0(2) and not(SW0(1)) and SW0(0));  --c  HEX0(2) <= (SW0(3) and SW0(2) and not(SW0(0))) or (SW0(3) and SW0(2) and SW0(1)) or  (not(SW0(3)) and not(SW0(2)) and SW0(1) and not(SW0(0)));  --d  HEX0(3) <= (not(SW0(2)) and not(SW0(1)) and SW0(0)) or (SW0(2) and SW0(1) and SW0(0)) or  (not(SW0(3)) and SW0(2) and not(SW0(1)) and not(SW0(0))) or (SW0(3) and not(SW0(2)) and SW0(1) and not(SW0(0)));  --e  HEX0(4) <= (not(SW0(3)) and SW0(0)) or (not(SW0(3)) and SW0(2) and not(SW0(1))) or (not(SW0(2)) and not(SW0(1)) and SW0(0));  --f  HEX0(5) <= (SW0(3) and SW0(2) and not(SW0(1))) or (not(SW0(3)) and not(SW0(2)) and SW0(0)) or (not(SW0(3)) and not(SW0(2)) and SW0(1)) or  (not(SW0(3)) and SW0(1) and SW0(0));  --g  HEX0(6) <= (not(SW0(3)) and not(SW0(2)) and not(SW0(1))) or (not(SW0(3)) and SW0(2) and SW0(1) and SW0(0));  end behavioral; |

1. 本次實驗過程說明與解決方法:

實驗過程:

基本題是先利用老師給的真值表，並用卡諾圖化簡出七段顯示器每一個接腳的布林代數式(包含開關)，再使用VHDL寫出這些接腳的布林代數式完成這次實作。

進階題是利用基礎題的VHDL的寫法套用到3個開關和3個七段顯示器上面，然後改變一些變數，完成此次實作。

我們遇到的困難是我們一開始的做法是用if去實作這次實驗，沒有用到布林函數去實作。

解決方法:

在發現使用錯誤的方法實作之後，即時利用老師給的真值表去用卡諾圖化到最簡布林代數式，再用最簡的布林代數式去寫VHDL實作這次電路。