Analog to Digital Converter and Digital to Analog Converter

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***Abstract*— The student was instructed to create an Analog-to-Digital converter circuit by using nonzero reference comparators. A series of fifteen op amp comparators were used to create the needed voltage quantization steps as voltage reference points for each comparator. This was possible by implementing a voltage divider circuit onto the supply voltage source and connecting it to the negative inputs of the op amps. In addition to creating an ADC, the student was instructed to create a Digital-to-Analog converter circuit by using a summing amplifier. It takes each input and converts it into a proportional voltage value before it is combined to create a final voltage output.**

I. INTRODUCTION

Operational amplifiers (op amps) are one of the most basic components in an analog circuit or analog application. Op amps can perform under a variety of circumstances where a high voltage gain is needed or a wide frequency range is needed. Implementing just a differential input, a negative feedback, or a positive feedback can create these circumstances. An op amp with no feedback loop will cause the op amps output to be driven to either positive or negative saturation; this characteristic is most desired for comparator circuits. An op amp with a negative feedback is desirable for applications that need a stable gain and creates either high or low impedance for the op amps input or output. An op amp that has a positive feedback is used in applications of comparators with hysteresis, which helps to block noise on an input signal. In this lab, op amps were used as comparators in order to utilize them in converter applications [1].

II. PRE-LAB

The student was instructed to research the mechanics of comparators and how they can be a component to an Analog to Digital converter application. Some of the basic mechanics of comparators involve differential inputs, which can lead to desired saturation outputs, and positive feedback loops, which are used for blocking input signal noise. For the conversion, the student needs to know the operational voltage range for the application and how much digital memory is allowed for quantization.

III. LAB

A. Comparators

Comparator circuits are used in applications to detect if an input signal is larger or smaller to the voltage reference. This causes the op amp circuit to have a two-state output, either high or low. This characteristic makes this circuit a great interface for analog to digital circuits [1].

B. Zero Reference

The simplest comparator circuit is an op amp without a feedback loop and grounding one of the inputs. This allows the high open-loop gain to create positive saturation if the input is positive and negative saturation if the input is negative. This circuit has its output switch from low to high, or vice versa, whenever the input signal crosses zero volts. The output swing of this comparator will be V_{CC} to V_{EE}. In this case, the zero volts is the trip point of a comparator, this is where the input causes the output to switch between states of high and low [1].

C. Non-Zero Reference

In some applications, a zero volt trip point may not be preferred. In order to have a voltage reference, or trip point, other than zero volts, a voltage divider is implemented on one of the op amps inputs. Therefore the output states switch when the input crosses the voltage reference point, instead of zero. Equation (1) is used to find the desired voltage reference for a comparator circuit [1].

$$V_{ref} = \frac{R_2}{R_1 + R_2} V_{CC} \tag{1}$$

D. Single Supply Comparator

A single supply comparator is very similar to the circuit design of a non-zero reference comparator, except that V_{EE} pin on the op amp is connected to ground. This cause the output to swing from zero volts to V_{CC}, which can be seen as giving the output a positive polarity. One can ground V_{CC} instead in order to give the output a negative polarity, but for digital applications, a positive polarity output is preferred in order to make the circuit more cost effective by implementing less hardware within the circuit [1].

E. Comparators with Hysteresis

One issue with some comparator applications is that noise will effect how much the comparator will switch between output states. By implementing a positive feedback, the circuit will be able to use two separate trip points into order to reduce the amount of false transitions from a noisy input [1].

F. Analog to Digital Converter

This converter circuit implements nonzero reference comparators with dual supply sources. Each comparator represents a quantization step needed for the analog to digital conversion. This circuit is one of the main components in the modern-day communication system.

One such application is for radio communication. These circuits must be able to take a high rate of sampling due to a wide range of frequencies utilized. The sampling size can be determined by the quantization step. To do these applications' high sampling rate, there are several imposed distortion signals sent through the circuit. One approach to help reduce the distortion is to interleave several analog to digital converters together to produce a more effective sampling. Another approach is to transform the signal into the wavelet domain and implement linear least-mean-squares estimation techniques to recover the original signal. [2]

In this labs analog to digital converter design, the voltage reference points are fixed. The quantization step can only be used in one particular case of voltage ranges. This can be a bit of an issue with todays technology, where there are many different functions and operations that need to be performed that require different amounts of power and frequencies. A new generation of comparators under the research of Yoo and his colleagues are making a flash analog to digital converter where its architecture can change the resolution of the quantization for comparison operations. It has better speed, low power consumption, and can satisfy the system-on-chip trends in today's technology. [3]

1) Quantization: Quantization represents a range of voltage input that a binary value can represent. For this value can represent a smaller range of voltages based on the pretense that one has enough hardware to keep track of many quantization steps. Equation (2) is used to determine a quantization step for an analog to digital converter. R is the voltage range values one needs to quantize and N is the number of bits available to use for the binary representation.

$$Q = \frac{R}{2^N} \tag{2}$$

2) Error: With a quantization step, there will always be a positive error. This error can be determined by equation (3). The quantization that is easily and commonly used is the full step quantization, which is what was implemented in this lab and depicted in the Results section. In order to help reduce the error, one can implement half step quantization. This has the first quantization value be half of the full step value, but each sequential range of values are at full step intervals.

$$Err = Analog - Digital \tag{3}$$

3) Voltage Divider: To implement the full step in the circuit, a voltage divider breaks the supply voltage into the necessary quantization steps in order for them to be transferred properly to an encoder. Equation (1) was used to break the supply voltage, V_{CC}, into the desired quantized steps [1].

G. Encoder

An encoder circuit takes the quantized voltage from the analog-to-digital converter and puts it into a binary value representation. One way to convert 16 quantization steps to 4-bit digital values is to implement two 74LS481 8-to-3 chips and connecting additional digital logic gates to create the final desired 4-bit value.

In many applications, an analog to digital converter is used in many microprocessors, which have to intake analog signals and create a translated digital value that it can use for the chip's operations. However, with todays technology, microprocessor speeds are rapidly increasing with each new technological advancement in hardware. The analog to digital converter implemented in this lab was a serial combination logic, when many current and future applications will require that the logic be in a parallel design. Within these applications, the accuracy and speed of an analog to digital converter circuit can be improved with the help of an encoder. Many output errors from an analog to digital converter circuit are due to babble errors on the chips inputs. Additional digital logic gates may need to be implemented in order to prevent the babble error from being related to a logical boundary. Additional methods for encoding designs have been created in Tsukamotos research in order to help reduce the effects of babble errors after trying to create a parallel analog to digital converter design [5].

H. Digital to Analog Converter

This circuit takes a binary input/value and converts it into a voltage or current. This conversion will make a proportional voltage or current from the binary value. Two common converters are the binary-weighted digital-to-analog converter and the R/2R digital-to-analog converter. For this lab, the binary-weighted digital to analog converter was implemented, which produces an output voltage that is equal to the weighted sums of the input. This is possible due the implementation of a summing amplifier [1].

In order to test some analog to digital converter and digital to analog circuit designs for accuracy, these circuits are generally tested in pairs to create a built-in-self-test. High clock frequencies and shortened test times are used in various testing schemes to ensure that these circuits on IC chips are in high functioning capability before being released to the industry. The amount of analog to digital converter and digital to analog circuits being tested are not required to be the same, which can allow an analog to digital converter to be tested with more than one digital to analog and vice versa in order to determine where a fault might occur within a cell on a chip. [4]

1) Summing Amplifier: A digital to analog circuit is one application in where a summing amplifier is utilized. The basic mechanics of a summing amplifier is that it combines two for more analog signals into a single output. In many of the students previous lab sections, summing amplifiers had at most two inputs, for the sake of simplicity. For this lab the amount of inputs were expanded to require to handle four inputs. The gain for each input is given by the ratio of the

negative feedback resistance to the input resistance. Equation (4) shows the mathematical representation of this amplifier circuit.

$$V_{out} = \frac{-R_f}{R_1}V_1 + \frac{-R_f}{R_2}V_2 \tag{4}$$

2) Dual Input Summing Amplifier: The previously mentioned summing amplifier typically only utilizes the inverting input. However there are applications were it is necessary to use both the inverting and non-inverting inputs of the op amp. Within this circuit, the gain of the inverting inputs is the ratio of the feedback resistor to the input resistor, and the gain for non-inverting inputs is a voltage-divider factor multiplied to the ratio of the feedback resistor to a compensating resistor equal to the inverting resistors in parallel. Equation (5) is a mathematical depiction of the gain for one of the non-inverting inputs. Figure 1 shows the general circuit layout for the dual input implementation [6].

$$A_{v4} = (\frac{R_f}{R_1||R_2}||R_3 + 1)(\frac{R_7||R_6||R_5}{R_7||R_6||R_5 + R_4}) \tag{5}$$

3) Subtracter: There are other applications were a summing amplifier will be utilized as a subtracter. In this circuit, the input that needs to result in a positive value will be driven into an inverter circuit first, which is an op amp with a negative feedback resistance that is equal to the input resistance. Then, this inverted input will be combined with the secondary input into a summing amplifier in order to produce an output that results in the first output subtracting the second, as depicted in equation (6).

$$V_{out} = V_1 - V_2 \tag{6}$$

IV. RESULTS

In the first part of this lab, the student was required to quantize a voltage range of 0v to 4v into 4 bits. By using equation (2), the quantization step was 0.125v. Refer to table I to see the mapping of the quantization step to the desired digital 4-bit value.

After this mapping was computed, the circuit was designed with fifteen op amps as non-zero reference comparators. This allows the analog voltage values to be converted into a quantifiable voltage value for the encoder

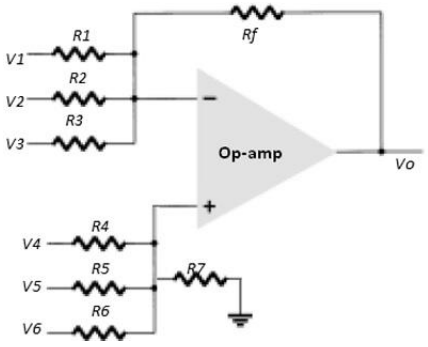

Fig. 1. Summing amplifier with inverting and non-inverting inputs

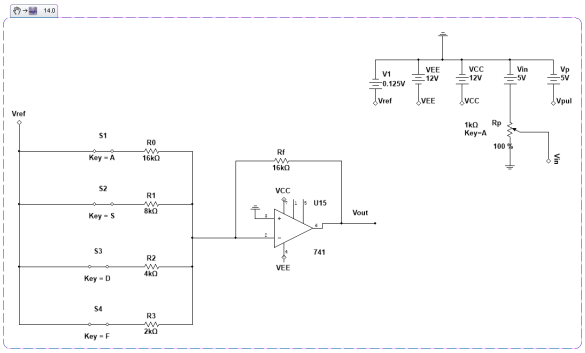

Fig. 2. Converts a 4-bit input into an output voltage

TABLE I
ANALOG TO DIGITAL MAPPING

Analog Input Value Range (V)	Quantized Input (V)	Digital Value
$0 \leq$ VIN < 0.125	0	0000
$0.125 \leq$ VIN < 0.25	0.125	0001
$0.25 \leq$ VIN < 0.375	0.25	0010
$0.375 \leq$ VIN < 0.5	0.375	0011
$0.5 \leq$ VIN < 0.625	0.5	0100
$0.625 \leq$ VIN < 0.75	0.625	0101
$0.75 \leq$ VIN < 0.875	0.75	0110
$0.875 \leq$ VIN < 1.0	0.875	0111
$1.0 \leq$ VIN < 1.125	1	1000
$1.125 \leq$ VIN < 1.25	1.125	1001
$1.25 \leq$ VIN < 1.375	1.25	1010
$1.375 \leq$ VIN < 1.5	1.375	1011
$1.5 \leq$ VIN < 1.625	1.5	1100
$1.625 \leq$ VIN < 1.75	1.625	1101
$1.75 \leq$ VIN < 1.875	1.75	1110
$1.875 \leq$ VIN < 2.0	1.875	1111

to compute a 4-bit value. Refer to figure 3 for the analog to digital converter circuit. This figure can be found at the end of the report.

For the second part of the lab, the student was required to take the digital 4-bit value and convert it back into an analog voltage value. To do this, a summing op amp has each input multiplied by the binary weight gain and then added together to create a final value. Equation (7) below mathematically represents the how this circuit can create the desired value.

$$V_{\text{out}} = (B_0 * 2^0) + (B_1 * 2^1) + (B_2 * 2^2) + (B_3 * 2^3) \tag{7}$$

Table II displays how each 4-bit input will result in the calculated corresponding output value.

From these calculations, the summing amplifier can be constructed. The gain for each input is needed to be a binary weight. To do this, the ratio of the negative feedback resistance to the input resistance needed to be a power of two. The circuit design used for the lab can be seen in figure 2.

V. CONCLUSION

This lab enhanced the students understanding of how to apply a non-zero reference comparator to create an analog to

TABLE II
DIGITAL TO ANALOG MAPPING

Digital Value	Ideal DAC Output (V)	Measured DAC Output (V)
0000	0	0.000245
0001	0.125	0.122
0010	0.25	0.245
0011	0.375	0.369
0100	0.5	0.495
0101	0.625	0.617
0110	0.75	0.741
0111	0.875	0.865
1000	1	1.54
1001	1.125	1.53
1010	1.25	1.24
1011	1.375	1.36
1100	1.5	1.46
1101	1.625	1.61
1110	1.75	1.73
1111	1.875	1.85

digital converter and a summing amplifier to create a digital to analog converter. The amount of error for the analog to digital converter is positive due to the fact that the input voltage is compared to the lower value of the quantization step. The digital to analog converter had a negative error due the fact that the output voltage had a lower value than the desired value.

APPENDIX

The figure 3 was too large to insert in the Results section. Therefore figure 3 is appended to the end of this report for the reader's benefit.

ACKNOWLEDGMENT

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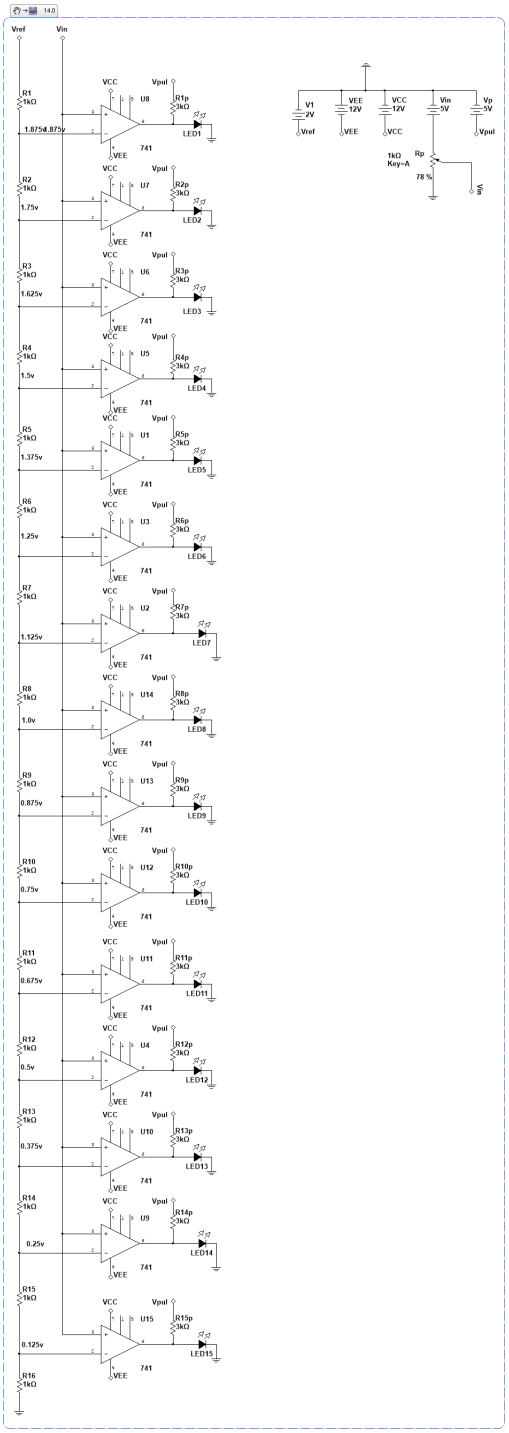

Fig. 3. Converts a voltage range of 0v to 4v into 4-bits