Analog and Digital Electronics syllabus for CS 3 Sem 2017 scheme | VTU CBCS 17CS32 Syllabus

VTU Syllabus CS 2017 Scheme 3 SEM Analog and Digital Electronics

Module-1	Field Effect Transistors	10 hours

Field Effect Transistors: Junction Field Effect Transistors, MOSFETs, Differences between JFETs and MOSFETs, Biasing MOSFETs, FET Applications, CMOS Devices. Wave-Shaping Circuits: Integrated Circuit(IC) Multivibrators.

Introduction to Operational Amplifier: Ideal v/s practical
Opamp, Performance Parameters,

Operational Amplifier Application Circuits: Peak Detector
Circuit, Comparator, Active Filters, Non-Linear Amplifier, Relaxation Oscillator, Current-To-Voltage Converter, Voltage-To-Current Converter.

Module-2	The Basic Gates	10 hours

The Basic Gates: Review of Basic Logic gates, Positive and Negative Logic, Introduction to HDL.

Combinational Logic Circuits: Sum-of-Products Method, Truth Table to Karnaugh Map, Pairs Quads, and Octets, Karnaugh Simplifications, Don't-care Conditions, Product-of-sums Method, Product-of-sums simplifications, Simplification by Quine-McClusky Method, Hazards and Hazard covers, HDL Implementation Models.

Module-3	Data-Processing Circuits	10 hours

Data-Processing Circuits: Multiplexers, Demultiplexers, 1-of-16 Decoder, BCD to Decimal Decoders, Seven Segment Decoders, Encoders, Exclusive-OR Gates, Parity Generators and Checkers, Magnitude Comparator, Programmable Array Logic, Programmable Logic Arrays, HDL Implementation of Data Processing Circuits. Arithmetic Building Blocks, Arithmetic Logic Unit

FLIP-FLOPs, Edge-triggered JK FLIP-FLOPs.

Module-4	Flip- Flops	10 hours

Flip- Flops: FLIP-FLOP Timing, JK Master-slave FLIP-FLOP, Switch Contact Bounce Circuits, Various Representation of FLIP-FLOPs, HDL Implementation of FLIP-FLOP. Registers: Types of Registers, Serial In - Serial Out, Serial In - Parallel out, Parallel In - Serial Out, Parallel In - Parallel Out, Universal Shift Register, Applications of Shift Registers, Register implementation in HDL.

Counters: Asynchronous Counters, Decoding Gates, Synchronous Counters, Changing the Counter
Modulus.

Module-5	Counters	10 hours

Counters: Decade Counters, Presettable Counters, Counter Design as a Synthesis problem, A Digital Clock, Counter Design using HDL.

D/A Conversion and A/D Conversion: Variable,
Resistor Networks, Binary Ladders, D/A Converters, D/A Accuracy and Resolution, A/D Converter-
Simultaneous Conversion, A/D Converter-Counter Method, Continuous A/D Conversion, A/D Techniques, Dual-slope A/D Conversion, A/D Accuracy and Resolution.