	ID	Name	End
August	Start	Teaching starts	21.08.2023
	Intro	Course introduction	24.08.2023
	P1	Introductory lab lecture & Chisel lecture	31.08.2023
September	T1	Trends and performance	01.09.2023
	T2	Instruction sets	07.09.2023
	E1	Trends and performance exercise	07.09.2023
	P2	RISC-V CPU project introduction	14.09.2023
	T3	Single-cycle datapath and pipelining	15.09.2023
	E2	Instruction set exercise	15.09.2023
	V1	E1 evaluation	15.09.2023
	D1	Chisel warm-up delivery	20.09.2023
	E3	Single-cycle datapath and pipelining exercise	21.09.2023
	V2	E2 evaluation	22.09.2023
	T4	Out-of-order execution	28.09.2023
	V3	E3 evaluation	29.09.2023
October	E4	Out-of-order execution exercise	05.10.2023
	D2	CPU functionality milestone 1	11.10.2023
	T5	Branch prediction	12.10.2023
	V4	E4 evaluation	13.10.2023
	D3	CPU functionality milestone 2	18.10.2023
	T6	The memory system	19.10.2023
	E5	Branch prediction exercise	19.10.2023
	T7	Bringing it all together -- the interval model	26.10.2023
	E6	Memory system exercise	26.10.2023
	V5	E5 evaluation	27.10.2023
November	D4	CPU functionality milestone 3	01.11.2023
	T8	Microarchitectural design options	02.11.2023
	E7	Interval model exercise	02.11.2023
	V6	E6 evaluation	03.11.2023
	E8	Microarchitectural design options exercise	09.11.2023
	M1	Research presentation	09.11.2023
	V7	E7 evaluation	10.11.2023
	D5	CPU project final delivery	15.11.2023
	V8	E8 evaluation	17.11.2023
	End	Teaching ends	24.11.2023
December	QA	Q/A session on selected topics	07.12.2023
	Exam	Final exam	14.12.2023

ID	Name	End	Weekday	Max points	Description	Type	Responsible
Intro	Course introduction	24.08.2023	Thu	0		Lecture	Joseph
T1	Trends and performance	01.09.2023	Fri	10	Chapter 1	Lecture	Joseph
T2	Instruction sets	07.09.2023	Thu	10	Appendix A	Lecture	Joseph
T3	Single-cycle datapath and pipelining	15.09.2023	Fri	10	Appendix C	Lecture	Joseph
T4	Out-of-order execution	28.09.2023	Thu	10	Appendix C and Chapter 3	Lecture	Joseph
T5	Branch prediction	12.10.2023	Thu	10	Chapter 3	Lecture	Joseph
T6	The memory system	19.10.2023	Thu	10	Appendix B, Chapter 2 and Chapter 3	Lecture	Joseph
T7	Bringing it all together -- the interval model	26.10.2023	Thu	10	Chapter 3 and Eyerman et al. TECS'09	Lecture	Joseph
T8	Microarchitectural design options	02.11.2023	Thu	10	Appendix C.7, Chapter 3, and Carlson et al., ISCA'15	Lecture	Joseph
QA	Q/A session on selected topics	07.12.2023	Thu	0		Lecture	Joseph
E1	Trends and performance exercise	07.09.2023	Thu	10		Theory exercise	Joseph
E2	Instruction set exercise	15.09.2023	Fri	10		Theory exercise	Joseph
E3	Single-cycle datapath and pipelining exercise	21.09.2023	Thu	10		Theory exercise	Joseph
E4	Out-of-order execution exercise	05.10.2023	Thu	10		Theory exercise	Joseph
E5	Branch prediction exercise	19.10.2023	Thu	10		Theory exercise	Joseph
E6	Memory system exercise	26.10.2023	Thu	10		Theory exercise	Joseph
E7	Interval model exercise	02.11.2023	Thu	10		Theory exercise	Joseph
E8	Microarchitectural design options exercise	09.11.2023	Thu	10		Theory exercise	Joseph
V1	E1 evaluation	15.09.2023	Fri	5		Peer evaluation	Joseph
V2	E2 evaluation	22.09.2023	Fri	5		Peer evaluation	Joseph
V3	E3 evaluation	29.09.2023	Fri	5		Peer evaluation	Joseph
V4	E4 evaluation	13.10.2023	Fri	5		Peer evaluation	Joseph
V5	E5 evaluation	27.10.2023	Fri	5		Peer evaluation	Joseph
V6	E6 evaluation	03.11.2023	Fri	5		Peer evaluation	Joseph
V7	E7 evaluation	10.11.2023	Fri	5		Peer evaluation	Joseph
V8	E8 evaluation	17.11.2023	Fri	5		Peer evaluation	Joseph
P1	Introductory lab lecture & Chisel lecture	31.08.2023	Thu	20		Lecture	David/Babis
D1	Chisel warm-up delivery	20.09.2023	Wed	20	Demonstrate functionality to the TA	Practical deliverable	David/Babis
P2	RISC-V CPU project introduction	14.09.2023	Thu	20		Lecture	David/Babis
D2	CPU functionality milestone 1	11.10.2023	Wed	30	Demonstrate functionality to the TA	Practical deliverable	David/Babis
D3	CPU functionality milestone 2	18.10.2023	Wed	30	Demonstrate functionality to the TA	Practical deliverable	David/Babis
D4	CPU functionality milestone 3	01.11.2023	Wed	30	Demonstrate functionality to the TA	Practical deliverable	David/Babis
D5	CPU project final delivery	15.11.2023	Wed	100	Implementation will be checked for correctness	Practical deliverable	David/Babis
Exam	Final exam	14.12.2023	Thu			External	Joseph
Start	Teaching starts	21.08.2023	Mon			External	
End	Teaching ends	24.11.2023	Fri			External	
M1	Research presentation	09.11.2023	Thu		Contemporary Problems in Computer Architecture	Lecture	Joseph