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Department of Computer Science

Examination paper for TDT4258 Low-Level Programming

Examination date: 15-Dec-2022
Examination time (from-to): 15:00 – 18:00

Permitted examination support material: **D** (No printed or hand-written support material is allowed. A specific basic calculator is allowed).

Academic contact during examination:
Phone:

Important information: This exam includes 20 multiple choice. Only one alternative is correct. You get 2 points for each correct answer and 0 points for no answer. A wrong answer results in -0.66 points.
Furthermore, this exam includes 5 text question. You can achieve up to 5 points in each text questions. If applicable a more fine-grained distribution of points is stated in the text question. Your answers should stay concise and within the task!

Read the questions and answer choices carefully. If a question is unclear/vague, you can ask an invigilator to contact the academic contact. Write down what you want to ask in advance.

Notifications: If there is a need to send a message to the candidates during the exam (e.g. if there is an error in the question set), this will be done by sending a notification in Inspera. A dialogue box will appear. You can re-read the notification by clicking the bell icon in the top right-hand corner of the screen.

Withdrawing from the exam: If you become ill or wish to submit a blank test/withdraw from the exam for another reason, go to the menu in the top right-hand corner and click “Submit blank”. This cannot be undone, even if the test is still open.

Access to your answers: After the exam, you can find your answers in the archive in Inspera. Be aware that it may take a working day until any hand-written material is available in the archive.

1 ARM Assembly

In ARM ISA, “bl” (branch and link) instruction is used to jump to a function/procedure. Where does this instruction store the return address? (The return address is PC of “bl” + 4.)

Select one alternative:

- The programmer needs to specify a general-purpose register to store the return address.
- It stores the return address on stack.
- It stores the return address in LR (Link Register) ✔
- It stores the return address in SP (Stack Pointer)

Maximum marks: 2

2 ARM Assembly Programming

What will be the value in register r3 after executing the following code?

```
.global _start
.section .text
_start:
        ldr     r0, =vars
        ldr     r1, [r0]
        ldr     r2, [r0, #4]
        mov     r3, #0
        cmp     r1, r2
        bge     else
        mov     r3, #1
        b       exit
else:
        mov     r3, #2
exit:
        b exit

.section .data
vars:
        .word 10
        .word 20
```

Note: "bge" stands for "branch if greater than or equals to".

Select one alternative:

- 2
- 10
- 0
- 1 ✔

Maximum marks: 2

3 ARM Assembly (Stack operations)

“push” and “pop” instructions are used to load and store data from stack region of memory. What is the correct way to specify memory address for these instructions?

Select one alternative:

- Just like load/store instructions, push/pop instructions can have their address in any general-purpose register.
- Push/pop instructions always have their address in Stack Pointer (SP) register and the programmer needs to update SP after each push/pop instruction.
- Push/pop instructions always have their address in Stack Pointer (SP) register and SP is updated automatically as a consequence of executing push/pop instructions. ✔
- Push/pop instructions can have their address in either Stack Pointer (SP) or Link Register (LR), but not in a general-purpose register.

Maximum marks: 2

4 RISC vs CISC ISA

Which of the following statements is TRUE regarding RISC (Reduced Instruction Set Computer) and CISC (Complex Instruction Set Computer) ISA?

Select one alternative:

- If we write a program in both CISC and RISC, the CISC version is likely to use fewer instructions.
- All instructions in a RISC ISA are typically same length (i.e., number of bits required to represent instructions is fixed) while CISC instructions are variable length.
- Arithmetic instructions in CISC can have their operands in memory, whereas arithmetic instructions in RISC must have their operands in registers.
- All of above are TRUE. ✔

Maximum marks: 2

5 Direct Memory Access (DMA)

Direct Memory Access (DMA) frees up CPU from managing the data transfer between memory and Input/Output devices. What does CPU have access to while DMA is in progress, i.e., when the data is actually being transferred between memory and an Input/Output device by the DMA controller?

Select one alternative:

- CPU can access registers and memory, but cannot access caches.
- CPU can access registers, but cannot access caches and memory.
- CPU can access registers and caches, but cannot access memory. ✔
- CPU can access register, caches, and memory.

Maximum marks: 2

6 Processor Design

Consider two processors, Processor A and Processor B, that implement the same instruction set architecture (ISA). Which of the following statements is TRUE?

Select one alternative:

- Both processors are guaranteed to operate at same frequency.
- Both processors are guaranteed to have same CPI (Clocks Per Instruction) while running the same program (Assume that the program is compiled with same compiler with same optimizations enabled).
- Both processors are guaranteed to execute same number of instructions while running the same program (Assume that the program is compiled with same compiler with same optimizations enabled). ✔
- All of above are TRUE

Maximum marks: 2

7 Cache Addressing

How many bits are needed for Tag, Index, and Byte Offset in an 32KB 8-way set associative cache with 32-byte block size, assuming 32-bit addresses?

Note: Cache size refers only to the size of data portion, not including tags and valid bits. So, a 32KB cache can store 32KB of data.

Select one alternative:

- Tag: 17, Index: 10, Byte Offset: 5
- Tag: 12, Index: 15, Byte Offset: 5
- Tag: 20, Index: 7, Byte Offset: 5 ✔
- None of the above.

Maximum marks: 2

8 Writing to Caches

Among write-back and write-through caches, which one is likely to write more data to memory?

Select one alternative:

- Write-back
- Write-through ✔
- Both will always write the same amount of data to memory

Maximum marks: 2

9 Virtual Memory

What does a TLB (Translation Lookaside Buffer) miss indicate?

Select one alternative:

- The requested data is not in memory and needs to be brought from disk.
- The requested data is not in the cache but is present in the memory.
- The virtual to physical translation for this address does not exist in the page table.
- None of the above. ✔

Maximum marks: 2

10 Virtual Memory

What is the advantage of multi-level page table over one-level page table?

Select one alternative:

- Multi-level page table requires less memory than one-level page table for applications that do not use full virtual address space. ✔
- Multi-level page table enables faster virtual to physical address translation.
- Both of the above.
- One-level page table is used while executing a single application, whereas multi-level page table is required while executing multiple applications simultaneously.

Maximum marks: 2

11 C Programming

What will the following C code print?

```
#include <stdio.h>
void conditional_sum (int a, int b, int c, int condition)
{
    if (condition)
    {
        c = a + b;
    }
    else
    {
        c = a - b;
    }
}
void main()
{
    int a = 10;
    int b = 4;
    int c = 0;
    int condition = 1;
    conditional_sum(a, b, c, condition);
    printf("%d",c);
}
```

Select one alternative:

- 6
- 14
- 1
- 0 ✔

Maximum marks: 2

12 C Programming

Consider a C array declared as:

int arr[20];

Which array element will be written by the following statement?

**(arr + 4) = 10;*

Note: Assume that an integer takes 4 bytes in memory.

Select one alternative:

- arr[4] ✔
- arr[0]
- arr[1]
- arr[16]

Maximum marks: 2

13 Dynamic memory allocation in C

Which of the following statements is TRUE regarding dynamic memory allocation/deallocation in C?

Select one alternative:

- “malloc” allocates memory dynamically at run time; however, the amount of memory to be allocated using “malloc” must be known at compile time.
- Dynamically allocated memory must be explicitly freed by programmer using “free”. ✔
- Both of above are TRUE.

Maximum marks: 2

14 Bit Operations in C

Which of the following C statements toggles bit 7 of a variable declared as:

int var;

Select one alternative:

- var = var ^ ~(7 << 7);
- var = var ^ ~(7);
- var = var ^ (1 << 7); ✔
- var = var ^ 7;

Maximum marks: 2

15 Debugging

You have a simple microcontroller, and all of its pins have been used to connect to the power supply and other external components. Your code running inside the microcontroller does not work as expected. Which of the following mechanisms can be used to debug the issue?

Select one alternative:

- Use JTAG
- Include a stub debugger in your code
- Run it in a simulator ✔
- All of the above can be used

Maximum marks: 2

16 Compilers

What is the advantage of using an intermediate representation (IR) in a compiler?

Select one alternative:

- Same compiler frontend can be used to translate any source language to IR
- IR code is ISA independent. Therefore, it can directly be executed on any processor
- IR enables easier optimizations ✔
- All of the above

Maximum marks: 2

17 Compilers

Which of the following statements is TRUE regarding register allocation?

Select one alternative:

- The aim of register allocation is to use as few registers as possible
- Register allocation does not provide any benefit in CISC architectures because CISC instructions can directly operate on data stored in memory
- Register allocation attempts to minimize memory accesses ✔
- All of the above

Maximum marks: 2

18 Operating Systems

Which of the following first two statements is TRUE regarding process state transition? If Both are true, choose the third option. If both are false, choose the fourth option.

Select one alternative:

- A process can go from "ready" to "blocked" state.
- A process can go from "blocked" to "running" state.
- Both of the first two statements are TRUE.
- Both of the first two statements are FALSE. ✔

Maximum marks: 2

19 Operating Systems

Which of the following statements is TRUE regarding processes in operating systems?

Select one alternative:

- Each process has its own heap and stack. ✔
- Each process has its own heap, but all processes share the same stack.
- Each process has its own stack, but all processes share the same heap.
- All processes share the same heap and stack.

Maximum marks: 2

20 Power

Which of the following parameters affects the static (also called leakage) power consumption?

Select one alternative:

- Supply voltage (Vdd) ✔
- Frequency (F)
- Activity factor (α)
- All of these affect static power consumption

Maximum marks: 2

21 Direct-Mapped vs. Fully-Associative Cache

Consider a fully-associative cache and a direct-mapped cache.

First describe one advantage and one disadvantage of each cache type. (2 Points)

For the following, you will be working with a data cache which has a cache block size of 8 bytes and the total cache size is 32 bytes. The fully-associative cache uses the LRU (least recently used) replacement policy. The cache is empty in the beginning. You are given the following 16 data addresses.

0x00, 0x04, 0x08, 0x0c,
0x10, 0x14, 0x18, 0x1c,
0x20, 0x24, 0x28, 0x2c,
0x30, 0x34, 0x38, 0x3c

Construct two access patterns each containing at most 6 accesses to any of the addresses above. One access pattern in which the direct-mapped cache has has a higher hit rate over the fully-associative cache (1 point) and one access pattern in which the fully-associative cache has a higher hit rate (1 point). Explain shortly why this access pattern favors the direct-mapped or fully-associative cache type (0.5 each, up to 1 point).

Example access pattern (favors no type):
0x00 0x04 0x08 0x0c 0x10 0x14

Fill in your answer here

Maximum marks: 5

22 Coorporative Scheduling & Preemptive scheduling

Describe the difference between cooperative scheduling and preemptive scheduling (4 points)? State advantages and disadvantages of both scheduling methods (1 points).

Fill in your answer here

Maximum marks: 5

23 An energy limited IoT device

You are designing a device that needs to periodically take pictures, compresses them and transmits them wireless to a cloud backend. The device has 512 MB of volatile main memory and the CPU can run up to 2 GHz. Your persistent flash memory only barely fits the operating system and software needed in the field.

Your contractor currently contemplates about enrolling the device in an environment with a limited energy supply. You are tasked to discuss potential measures to save energy while keeping up the operation of the device.

Describe dynamic voltage and frequency scaling (DVFS) and sleep modes in the context of energy and latency (3 points).

What would be the impact of a temporary power loss considering the described memory system of the device (1 point)?

The design of your device is not finalized yet. What would you propose to improve the system with these concepts in mind? (1 point)?

Volatile -- State is lost on power loss.

Persistent -- Keeps state on power loss.

Fill in your answer here

Maximum marks: 5

24 Calling convention

Describe what one understands under a function call convention (for caller and the callee) which is defined in an Instruction Set Architecture like ARM-v7 (4 points).

How can one handle nested function calls (1 points).

Fill in your answer here

Maximum marks: 5

25 Memory Mapped I/O

Describe the concept of memory mapped I/O and how it is used in software to communicate with I/O devices (3 points).

What advantage and disadvantage does it have when compared to isolated address spaces (1 point)?

Describe the process of memory mapping a file or device I/O into a process' virtual address space in Linux systems (1 point).

Fill in your answer here

Maximum marks: 5