

23-April-2003

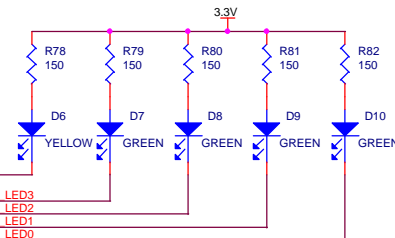
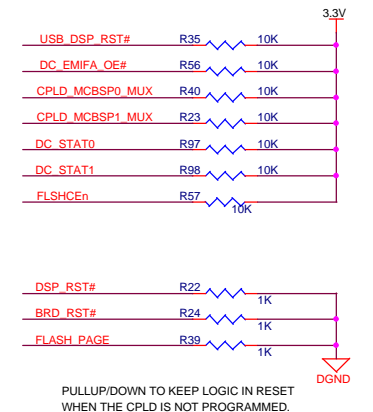
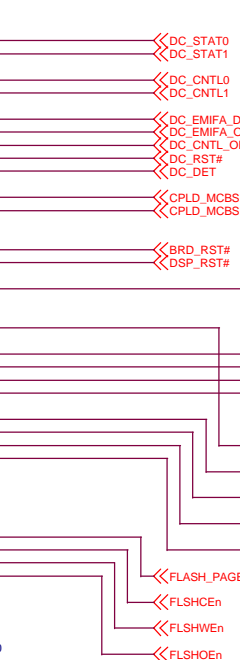
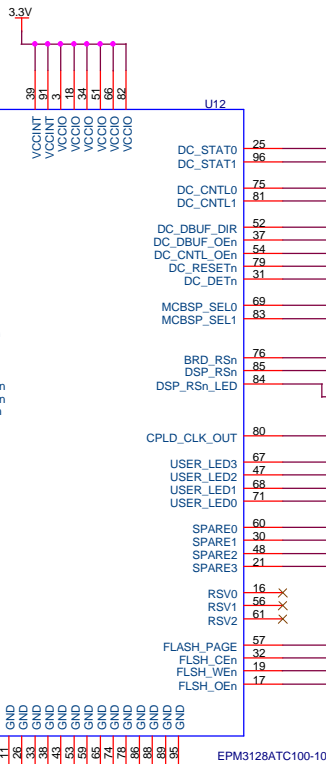
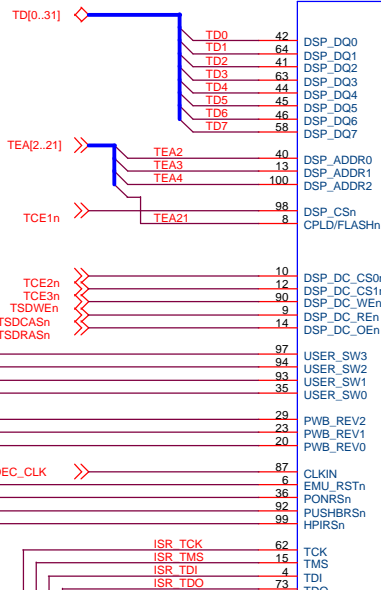
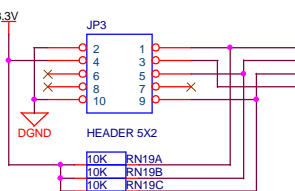
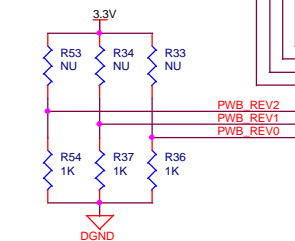
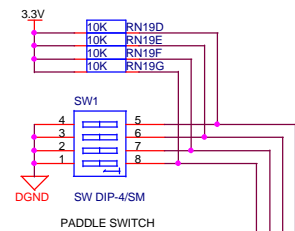
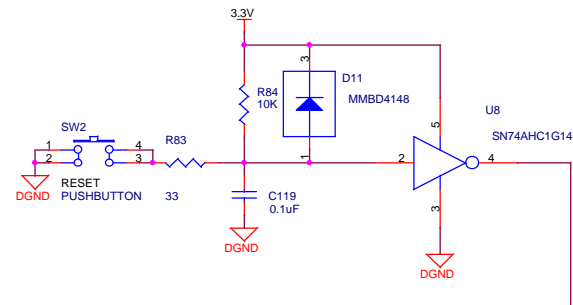
The TMS320C6713DSK design is based on
TMS320C6713 device data sheet
SPRS186B and errata SPRZ173E. This
schematic is subject to change without notification.
Spectrum Digital Inc. assumes no liability for
applications assistance, customer product design
or infringement of patents described herein.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	BETA	23-Jan-2003	

REVISION STATUS OF SHEETS										OWN	DATE
REV										CHK	DATE
SH										ENGR	DATE
REV	A	B	A	A	A	A	A			ENGR-MGR	DATE
SH	8	9	10	11	12	13	14			QA	DATE
REV	B	A	A	A	A	A	B	NEXT ASSY	USED ON	MFG	DATE
SH	1	2	3	4	5	6	7	APPLICATION		ELSE	DATE

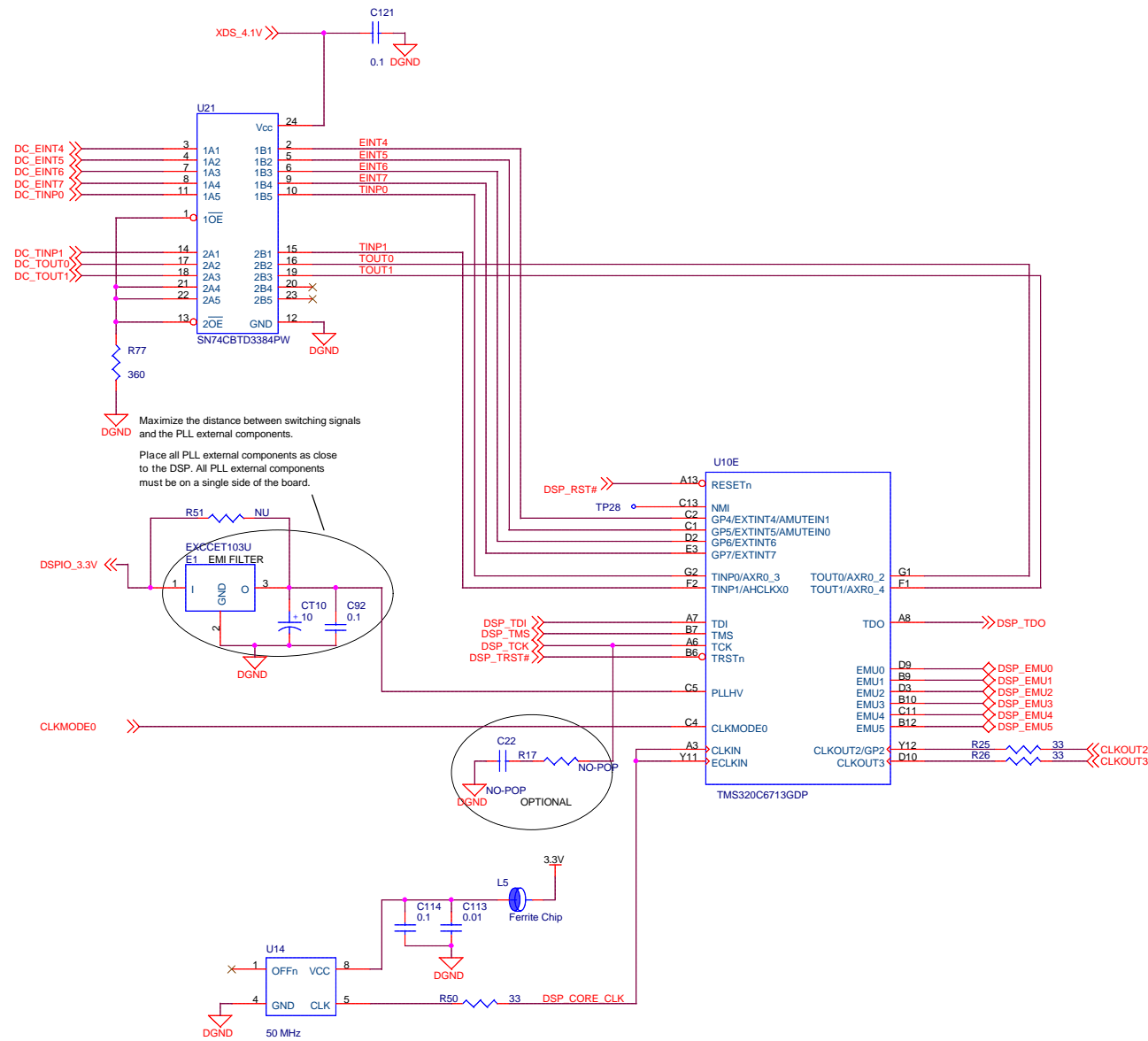
SPECTRUM DIGITAL INCORPORATED

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CPLD

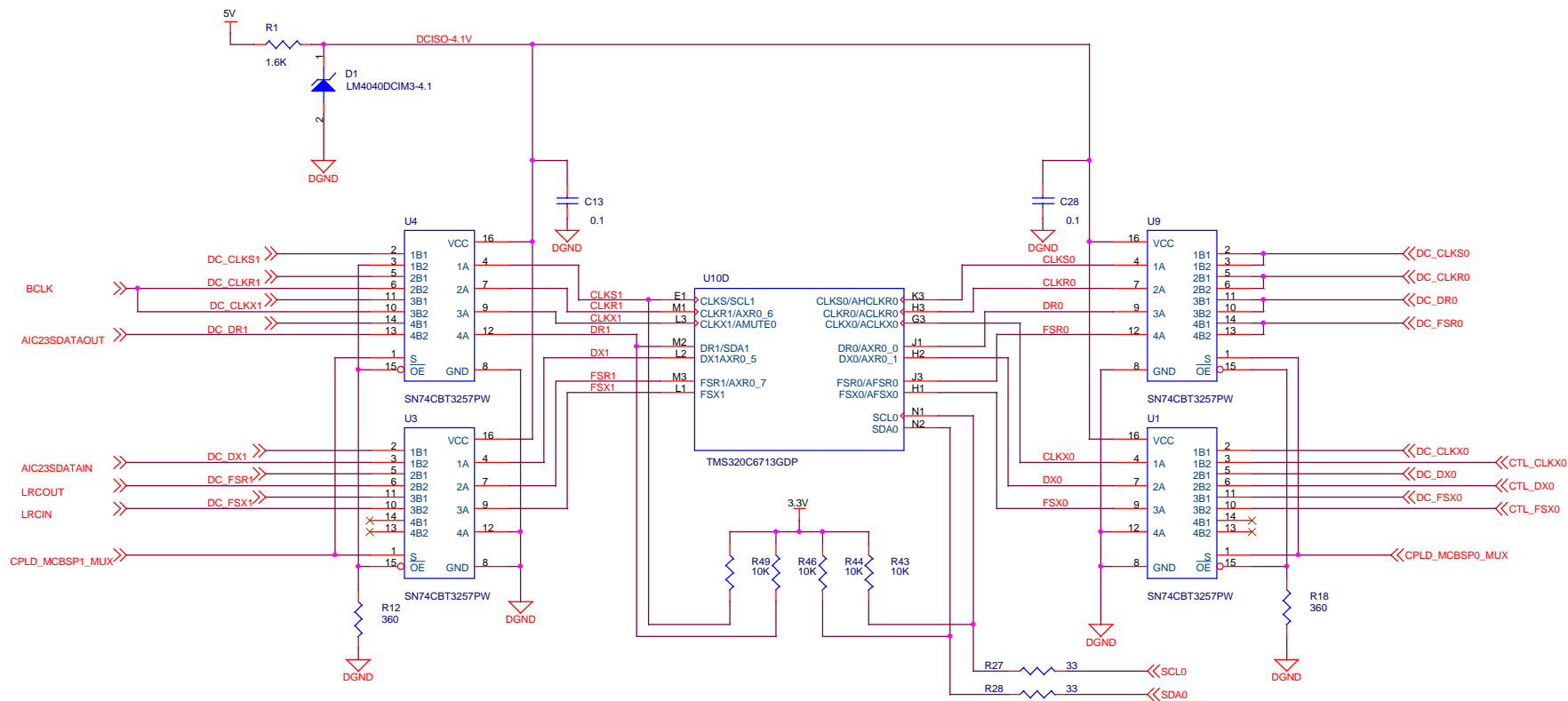
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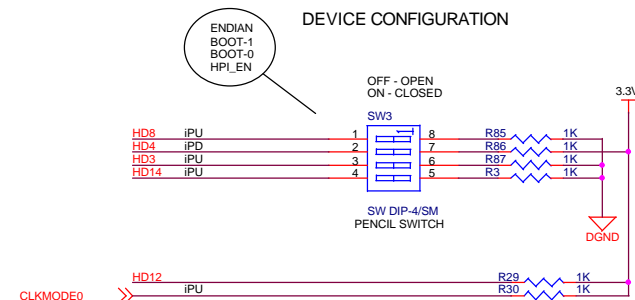
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MCBSP

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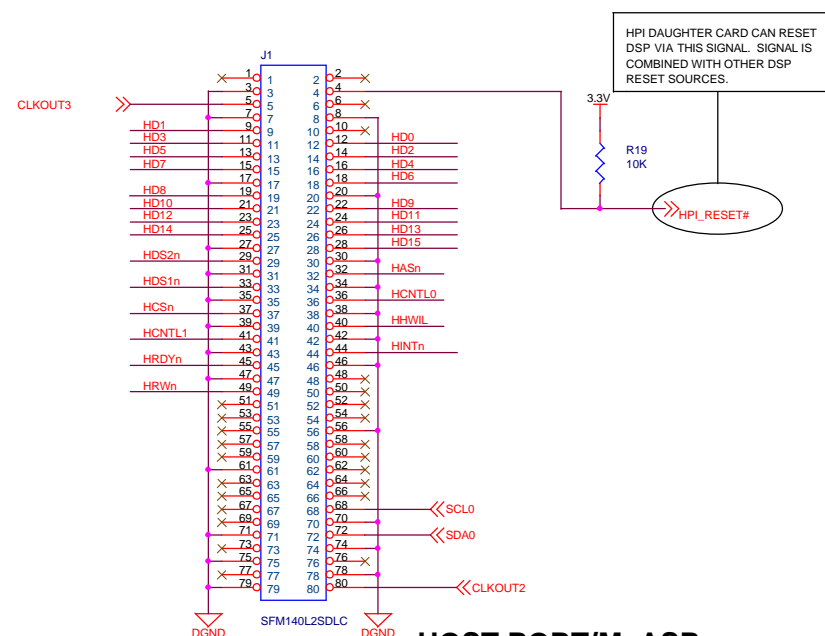
DEVICE CONFIGURATION



U10C

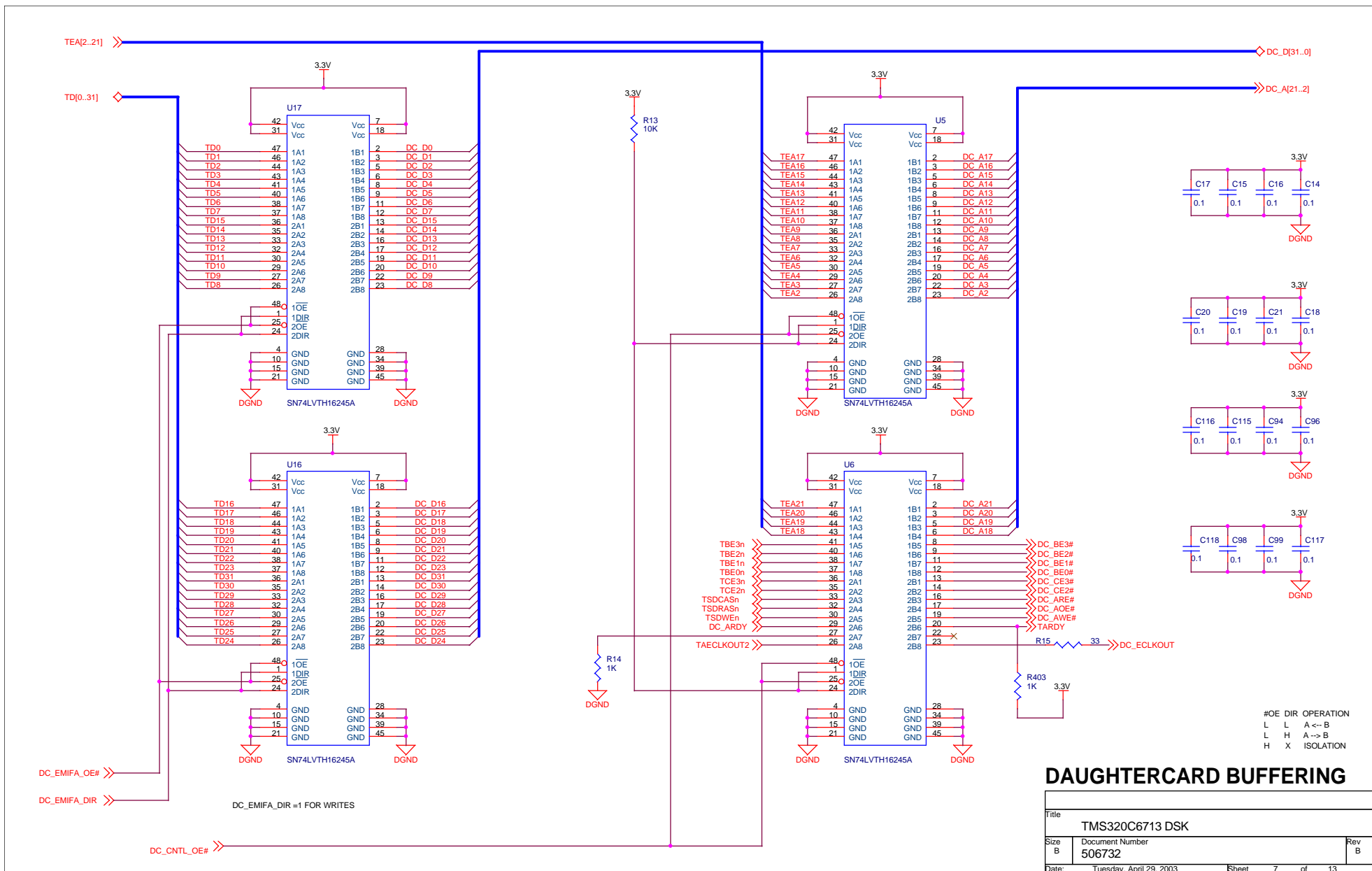
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HD14/GP14	C14	HD14
HD13/GP13	A15	HD13
HD12/GP12	C15	HD12
HD11/GP11	A16	HD11
HD10/GP10	B16	HD10
HD9/GP9	C16	HD9
HD8/GP8	B17	HD8
HD7/GP3	A18	HD7
HD6/AHCLKR1	C17	HD6
HD5/AHCLKX1	B18	HD5
HD4/GP0	C19	HD4
HD3/AMUTE1	C20	HD3
HD2/AFSX1	D18	HD2
HD1/AXR1_7	D20	HD1
HD0/AXR1_4	E20	HD0
HINTn/GP1	J20	HINTn
HCNTL1/AXR1_1	G19	HCNTL1
HCNTL0/AXR1_3	G18	HCNTL0
HHWIL/AFSR1	H20	HHWIL
HRWn/AXR1_0	G20	HRWn
HASn/ACLKX1	E18	HASn
HCSn/AXR1_2	E19	HCSn
HDS1n/AXR1_6	F18	HDS1n
HDS2n/AXR1_5	F18	HDS2n
HDRYn/ACLKX1	H19	HDRYn

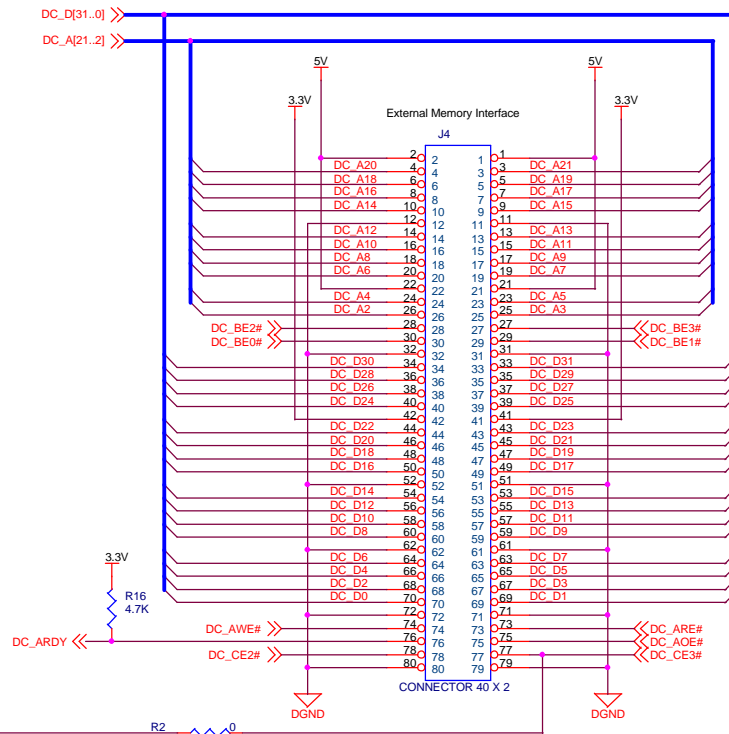
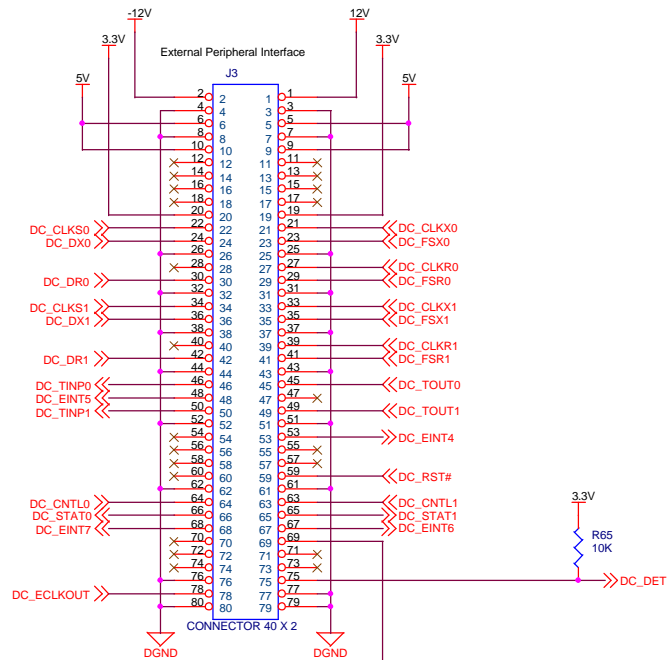
TMS320C6713GDP



HOST PORT/McASP

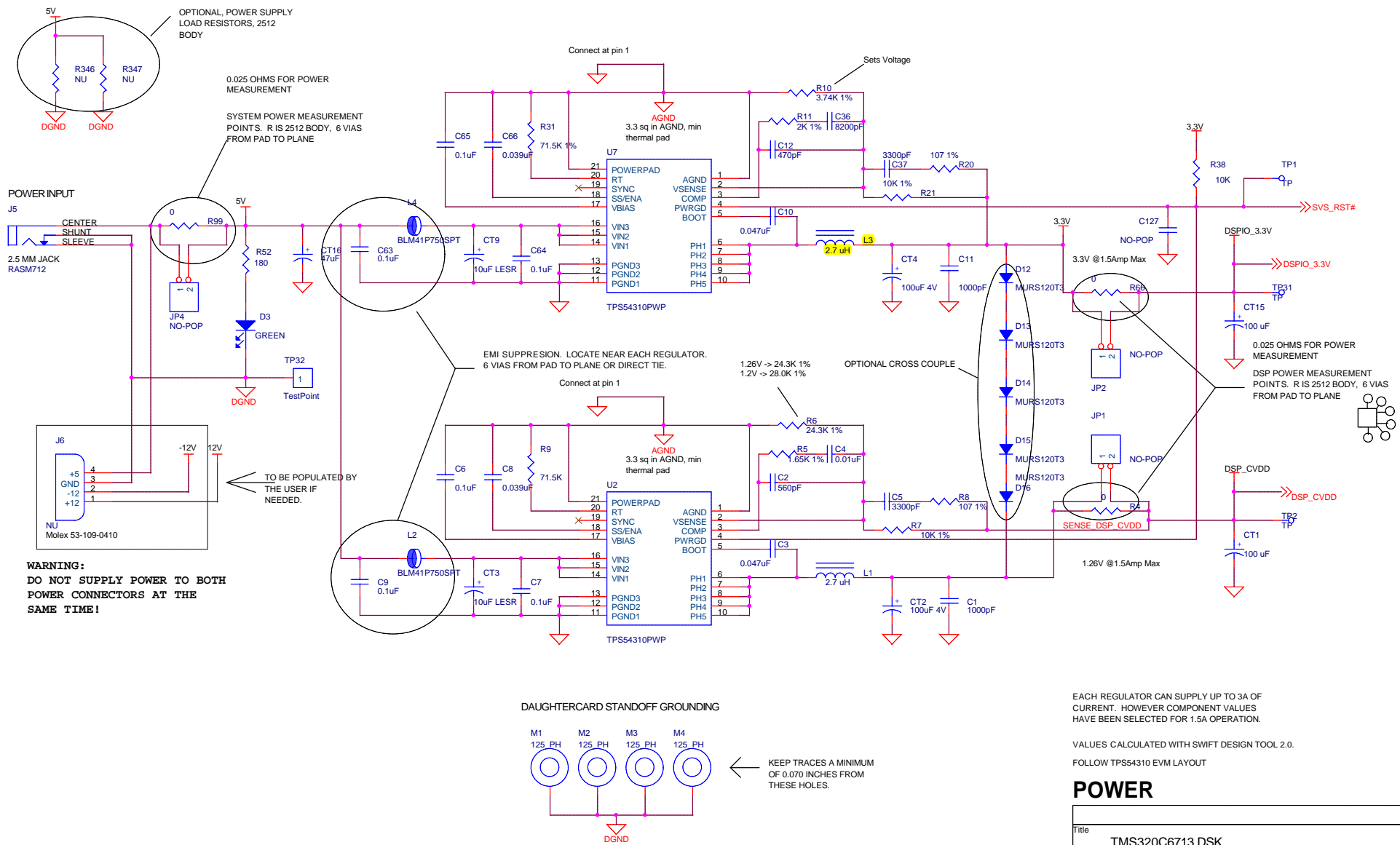
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DAUGHTERCARD I/F

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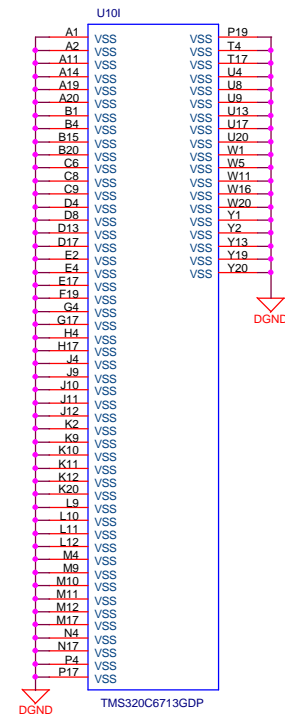
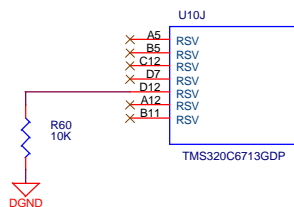
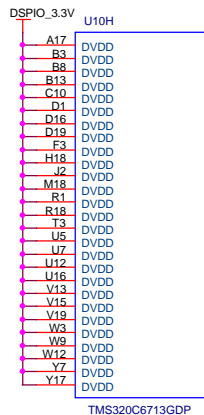
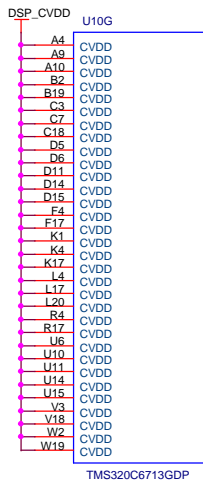


EACH REGULATOR CAN SUPPLY UP TO 3A OF CURRENT. HOWEVER COMPONENT VALUES HAVE BEEN SELECTED FOR 1.5A OPERATION.

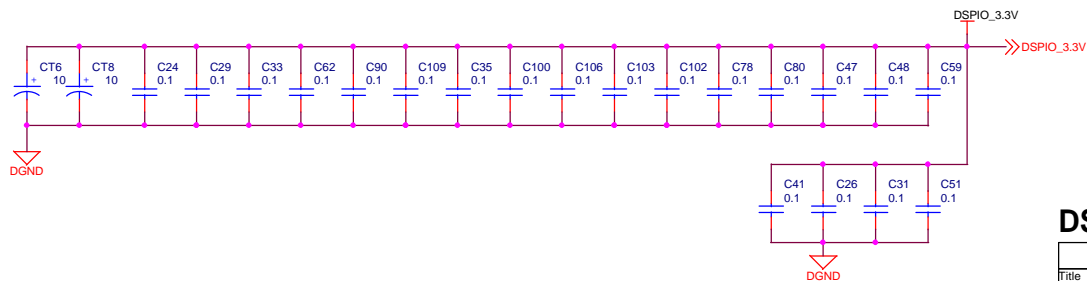
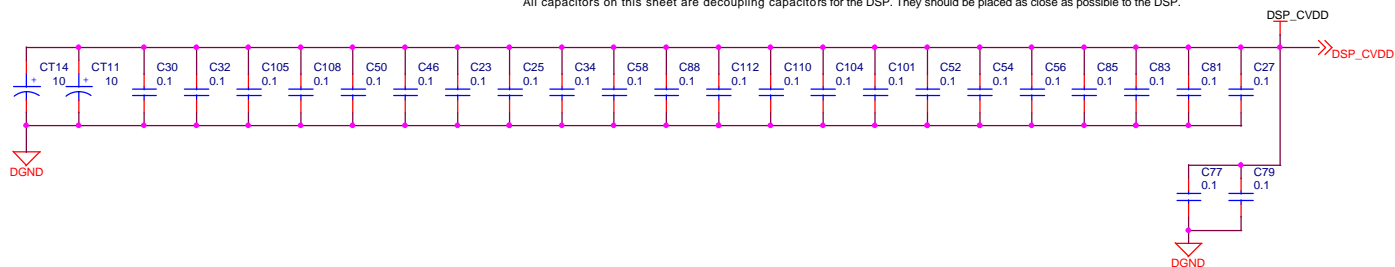
VALUES CALCULATED WITH SWIFT DESIGN TOOL 2.0.
FOLLOW TPS54310 EVM LAYOUT

POWER

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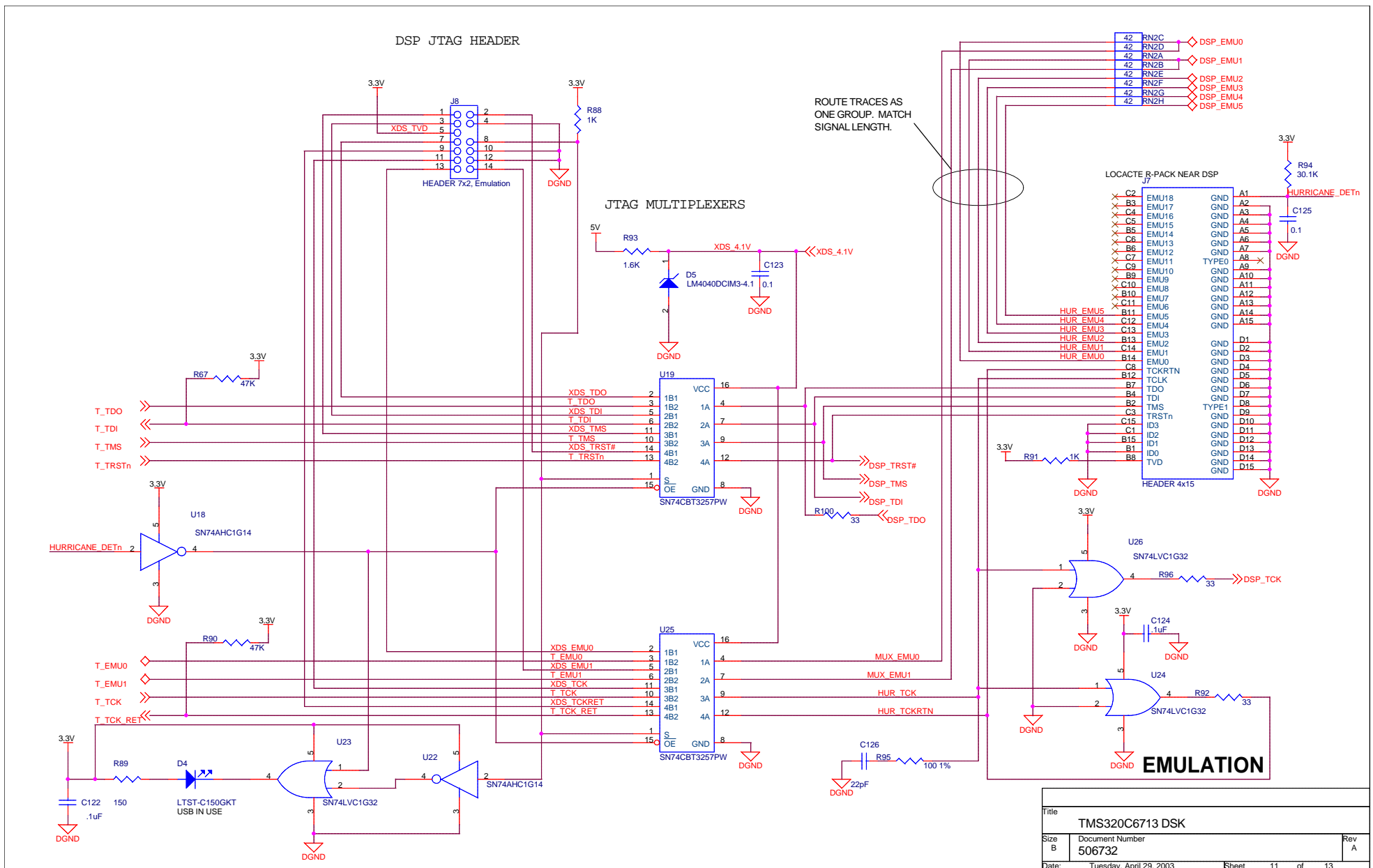


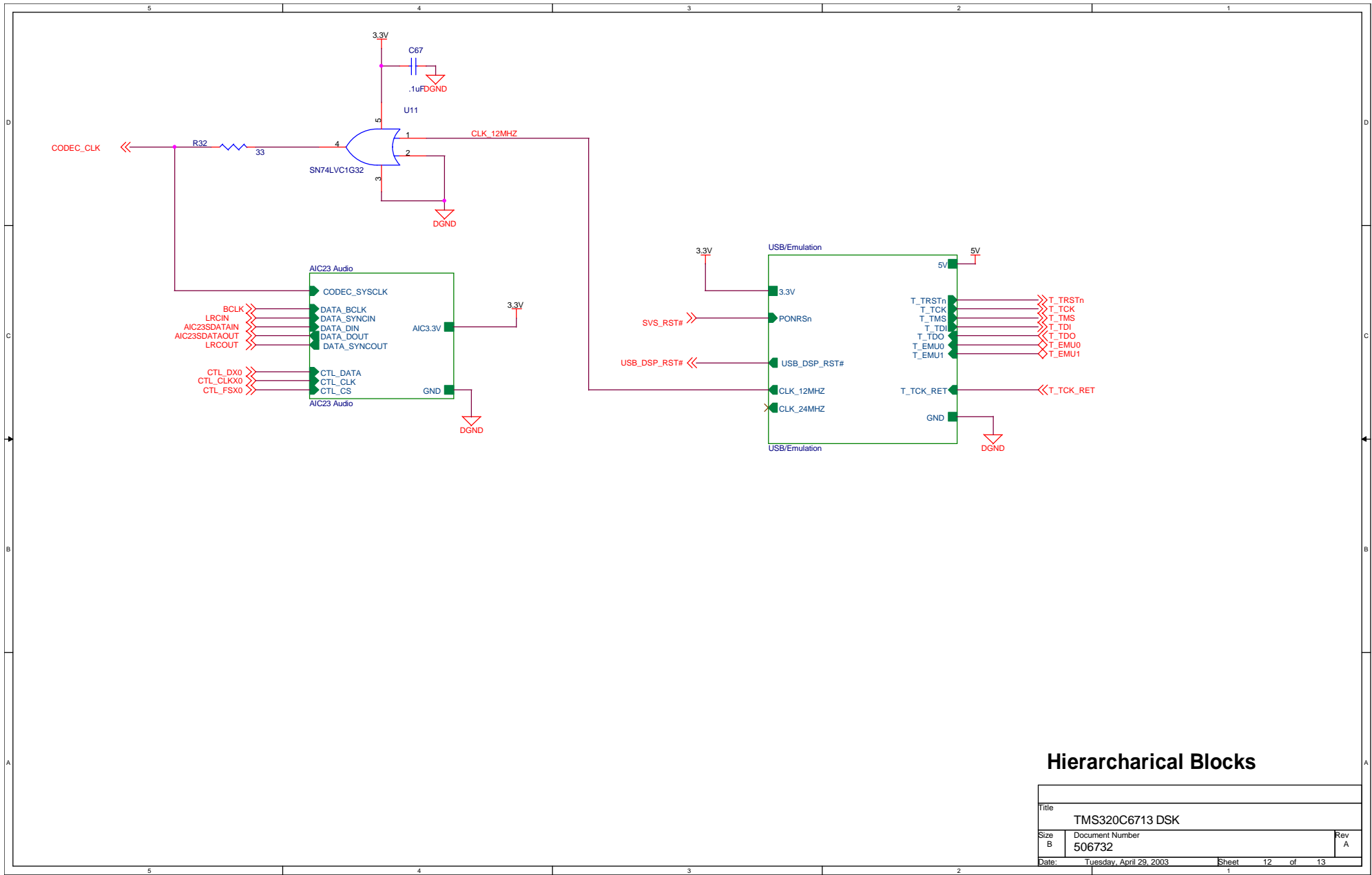
All capacitors on this sheet are decoupling capacitors for the DSP. They should be placed as close as possible to the DSP.



DSP POWER & DECOUPLING

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Hierarchical Blocks

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