DIGITAL SYSTEM

7th PRACTICUM: FLIP - FLOP BASIC

Writed by :

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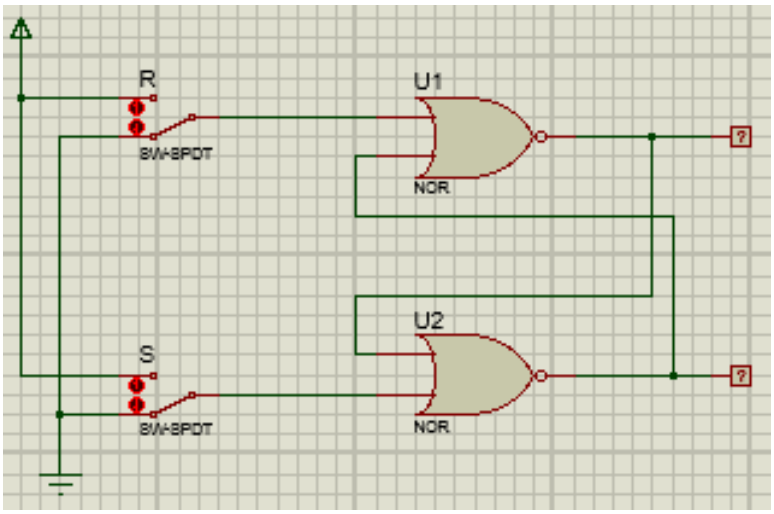
PRACTICUM ACTIVITIES

1st Experiment. NOR Latch

1. Create and simulate NOR latch as shown! And then click the SW-SPDT switch to operate Latch.



2. Based on your simulation, fill in the points in the following table!

	S (Set)	R (Reset)	Output	
			Q	Q’
1	0	1	0	1
2	0	0	0	1
3	1	0	1	0
4	0	0	1	0
5	1	1	0	0

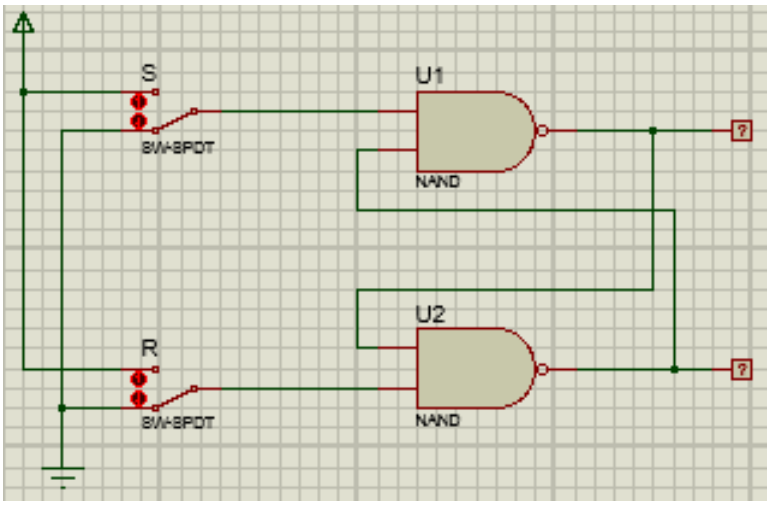
3. Answer the following question!

a. What will happen if we give the condition S = R = 0?
The output will be same with before, so it can be memory

b. Why is the condition S = R = 1 not allowed?
Because the output between Q and Q’ is same

2nd Experiment. NAND Latch

1. Create and simulate NAND latch as shown! And then click the SW-SPDT switch to operate Latch.



2. Based on your simulation, fill in the points in the following table!

	S (Set)	R (Reset)	Output	
			Q	Q’
1	0	1	1	0
2	1	1	1	0
3	1	0	0	1
4	1	1	0	1
5	0	0	1	1

3. Answer the following question!

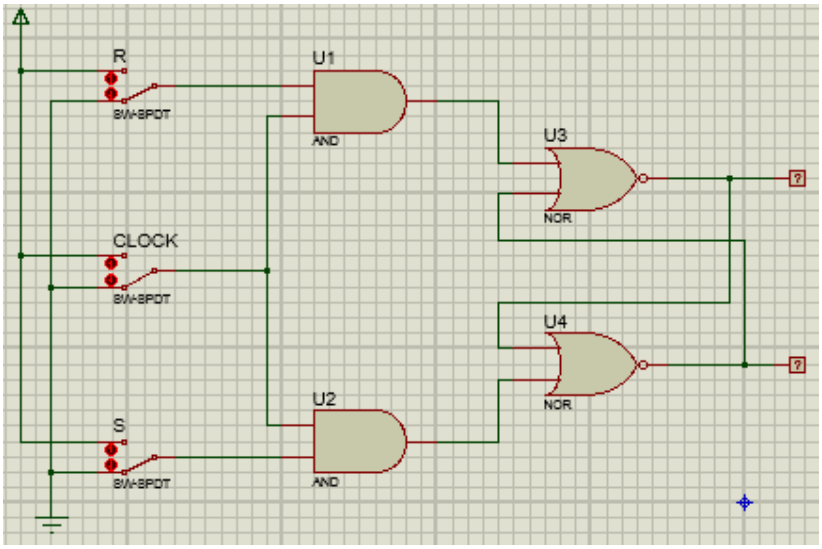
   a. What will happen if we give the condition S = R = 1?
   The output will be same with before, so it can be memory
   b. Why is the condition S = R = 0 not allowed?
   Because the output between Q and Q’ is same

4. Based on the flip-flop analysis above, what is your opinion about the statement "Flip-flop and latch are used as data storage elements":

   The output will be memory or not change data if S = R = 1 and will give new data or change data if change input 0 to 1 and 1 to 0. And the forbidden thing is S = R = 0 because it give Q and Q’ are same.

3rd Experiment. Flip-Flop RS

1. Create and simulate the Flip-Flop RS as shown! And then click the SW-SPDT switch to operate the Flip-Flop RS.



2. Based on your simulation, fill in the points in the following table!

	S (Set)	R (Reset)	CLOCK	Output	
				Q	$Q_{(t+1)}$
1	0	0	0	x	x
2	0	0	1	x	x
3	0	1	0	x	x
4	0	1	1	0	1
5	1	0	0	0	1
6	1	0	1	1	0
7	1	1	0	1	0
8	1	1	1	0	0

3. Answer the following question!

a. What will happen if we give the condition S = R = 1 and the clock changes from 1 to 0?
Logic race condition detected during transient analysis (simulation error).

b. How can the above conditions occur?
Because S = R = 1 is forbidden because Q and Q' will be same. So, if we change the clock will be error (S = R = 1 and the clock changes from 1 to 0).

4. Explain how the Flip-Flop RS works?

R S = 0 0 then lock the previous value

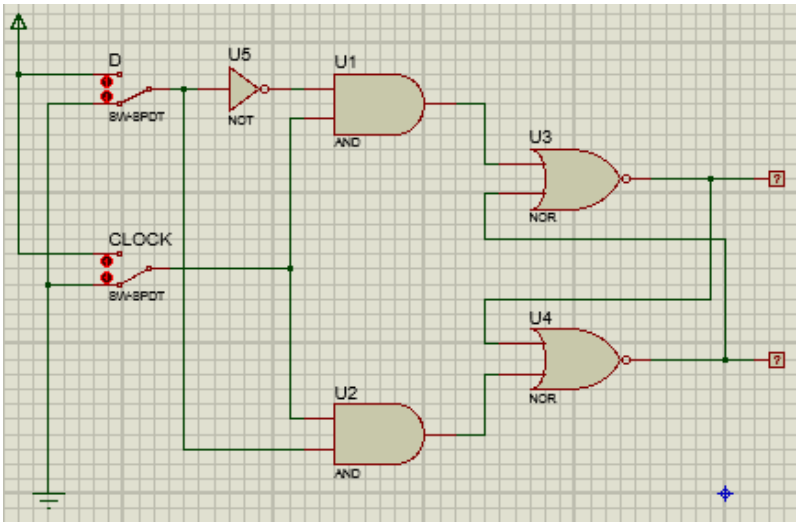
0 1 then change the value of Q to $Q_{(t+1)}$

1 0 then change the value

1 1 prohibited conditions that cause errors

4th Experiment. Flip-Flop D

1. Create and simulate the Flip-Flop D as shown! And then click the SW-SPDT switch to operate the Flip-Flop.



2. Based on your simulation, fill in the points in the following table!

	D	CLOCK	Output	
			Q	Q’
1	0	0	x	x
2	0	1	0	1
3	1	0	0	1
4	1	1	1	0
5	0	0	1	0
6	0	1	0	1
7	1	0	0	1
8	1	1	1	0

3. Explain how the Flip-Flop D works?

If the clock is off, it will lock the previous output value.

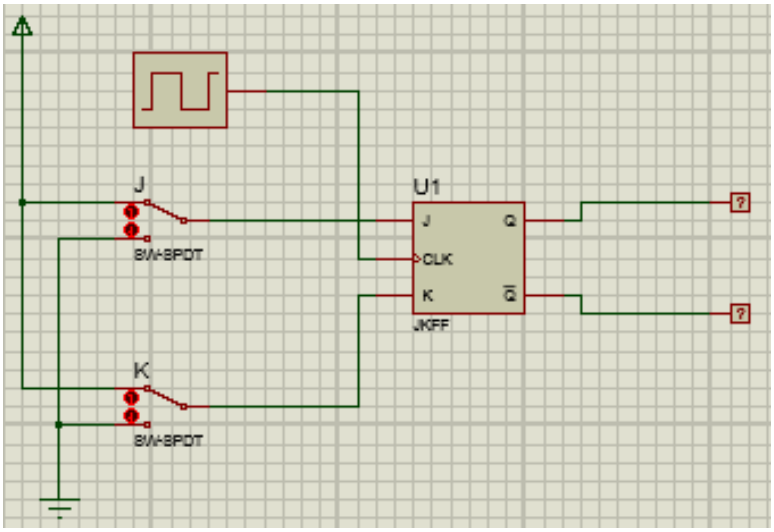
If the clock is on, it will change the previous Q value.

4. What is the function of the NOT gate on the Flip - Flop D compared to the Flip - Flop SR?

To overcome prohibited conditions

5th Experiment. Flip-Flop JK

1. Create and simulate the JK Flip-Flop as shown! And then click the SW-SPDT switch to operate the Flip-Flop.



2. Based on your simulation, fill in the points in the following table!

	J	K	CLOCK	Output	
				Q	$Q_{(t+1)}$
1	0	0	0	0	1
2	0	0	1	0	1
3	0	1	0	0	1
4	0	1	1	0	1
5	1	0	0	0	1
6	1	0	1	1	0
7	1	1	0	1	0
8	1	1	1	0	1

3. Answer the following question!
   a. What will happen if J = K = 0 and the clock rise up (change from 0 to 1)?
      Clock values change but do not change the value of Q and $Q_{(t+1)}$ (it be memory).
   b. What will happen if J = K = 1 and the clock rise up?
      If clock = 1, the value of Q and $Q_{(t+1)}$ will change.
      If clock = 0 it will store the values of Q and $Q_{(t+1)}$.

4. Explain how the Flip-Flop JK works!

   The principle works almost the same as the Flip-Flop RS, only the prohibited condition (J K = 1 1, clock up) has been removed.