浙江大学 2021－2022 学年秋冬学期

《计算机组成与设计》课程期末考试试卷

课程号：_67190020_，开课学院：_信息与电子工程学院_

考试试卷：√A 卷、B 卷（请在选定项上打√）

考试形式：√闭、开卷（请在选定项上打√），

允许带 1 张 A4 纸大小的手写资料和计算器入场

考试日期：_2022_年_1_月_9_日，考试时间：__120__分钟

诚信考试，沉着应考，杜绝违纪。

考生姓名：_____学号：_____所属院系（专业）：_____

题序	一	二	三	四	五	六	七	八	总 分
得分									
评卷人									

I. CHOICE (Only one correct answer, 60 points)

1. With the help of _____ we reduce the memory access time. (_____)

A. SDRAM

B. Cache

C. Heaps

D. Higher capacity RAMs

2. Two processors P1 and P2 have clock frequencies of 600 MHz and 900 MHz respectively. Suppose the average CPI (Clock cycle Per Instruction) of P1 is 2 and the CPI of P2 is 3. For the execution of the same instruction sequence which processor is faster? (_____)

A. P1

B. P2

C. Both take the same time

D. Insufficient information

3. Cache block size (B) can affect both miss rate and miss latency. Assume a machine with a base CPI of 1, and an average of 1.35 references (both instruction and data) per instruction, find the lock size that minimizes the total miss latency given the following miss rates for various block sizes. What is the optimal block size for a miss latency of 24 + B cycles? (_____)

8: 4%	16: 3%	32: 2%	64: 1.5%

A. 8

B. 16

C. 32

D. 64

4. A processor performing fetch or decoding of different instruction during the execution of another instruction is called (_____).

A. Super-scaling

B. Pipe-lining

C. Parallel Computation

D. None of the above

5. In memory-mapped I/O (_____).

A. The I/O devices and the memory share the same address space

B. The I/O devices have a separate address space

C. The memory and I/O devices have an associated address space

D. A part of the memory is specifically set aside for the I/O operation

6. The spatial locality of reference means (_____).

A. That the recently referenced memory location is referenced again next

B. That the recently referenced won't be referenced again

C. That the memory location referenced will be referenced at a later time

D. That the locations in nearby addresses of the memory location referenced will be referenced soon

7. Consider the following code:

```
lh x6, 0(x7)
sw x6, 4(x7)
```

Assume that the register x7 contains the address 0x10000000 and the data at address is 0x11223344. What value is stored in 0x10000005 on a little-endian machine? (_____)

A. 0x11

B. 0x22

C. 0x33

D. 0x44

8. When silicon chips are fabricated, a very common defect is for one signal wire to get "broken" and always register a logical 0. This is often called a "stuck-at-0" fault. Which instruction below operates correctly if the *RegWrite* wire is stuck at 0? (_____)

A. auipc

B. jal

C. addi

D. sw

9. A program originally takes 10 seconds to run. We manage to parallelize 80% of our code to be 10 times faster, at the cost of 1.2 seconds of overhead. How many times faster is our new code? (_____)

A. 2.5

B. 5

C. 10

D. None of the above

10. What is used to compute the offset of all branch instructions? (_____)

A. Compiler

B. Assembler

C. Linker

D. Loader

11. You have a two-way set-associative cache with 8B blocks and a total size of 64B. Suppose use a least-recently used replacement policy and begin from power on. Given this sequence of byte-addressed accesses, what is the hit rate? (_____)

0, 4, 16, 132, 208, 160, 130, 4

A. 12.5%

B. 25.0%

C. 37.5%

D. None of the above

12. The stalling of the processor due to the unavailability of the instructions is called as (_____).

A. Control hazard

B. Structural hazard

C. Data hazard

D. Input hazard

13. Consider the following C code.

```
int* func(){
    int* arr = malloc(10 * sizeof(int));
    return arr;
}

int main(){
    char* str = "hello world";
    int* a = func();
    return 0;
}
```

In what part of memory are each of the following values stored? (_____)

arr, arr[0], *str

A. stack, heap, stack

B. stack, heap, static

C. static, heap, stack

D. static, stack, static

14. In _____ protocol the data is directly written into the main memory. (_____)

A. Write through

B. Write back

C. Write first
D. Write allocate

15. Consider a normal 5-stage pipeline. If a unit in the pipeline completes its task before the time period, then (_____).
A. It will perform some other task in the remaining time
B. Its time gets reallocated to a different task
C. It will remain idle for the remaining time
D. None of the above

16. Consider a system with 64 MiB of physical memory, which runs programs that have 4 GiB of virtual memory. The page size is 4 KiB. How many bits long is a virtual page number? (_____)
A. 6
B. 12
C. 20
D. 26

17. What is the value of x10 for the following sequence of instructions? (_____)

```
lui x10, 0xABCDE
addi x10, x10, 0xDEF
```

A. 0xACACD
B. 0xABCDFDEF
C. 0xABCDEDEF
D. 0xABCDDDEF

18. What is the decimal sum of the binary number 1.001×2^{-1} and -1.110×2^{-2}? (_____)
A. 0.0625
B. 0.125
C. 0.25
D. None of the above

19. Assume a 5-stage pipelined RISC-V CPU. There are no pipelining optimizations (no forwarding, load delay slot, branch prediction, pipeline flushing, etc.). It cannot read and write from registers in the same clock cycle. An integer 100 is stored at memory address 0x60000000. How many cycles would the following sequence of instructions take to execute correctly? (_____)

```
lw t0, 0(a0)   // a0 = 0x60000000
srli s0, t0, 4
addi s1, t0, 4
beq a0, s1, Label
add a1, t2, t3
Label …
```

A. 9
B. 13
C. 15

D. 18

20. Assume a machine has 32-bit virtual address, 8 KiB page size, and 4-byte page table entry. What is the maximum possible page table size for a system running five processes? (_____)

A. 5 MiB

B. 10 MiB

C. 20 MiB

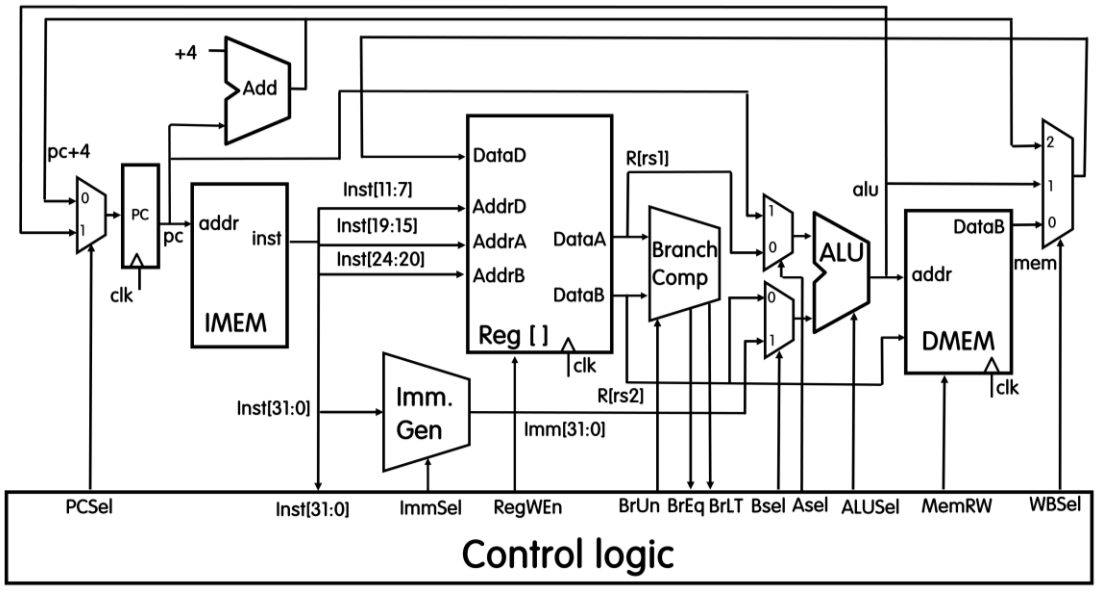
D. None of the above

II. TRUE OR FALSE (10 points)

1. ____The assembler produces an executable.
2. ____Two's complement in 8 bits for -127 is 1000 0000.
3. ____The penalty for a page fault is about the same as the penalty for a cache miss.
4. ____A linear page table takes up more memory as the process uses more memory.
5. ____The page table is stored in main memory.
6. ____Large block size of a cache may increase the average access time or the miss rate.
7. ____Capacity misses would not occur under perfect replacement policy.
8. ____Choice of hardware and software parallelism is independent.
9. ____A branch target buffer in the IF stage can cache the branch results that tell whether the branch was taken the last time it was execute.
10. ____Superscalar processors use multiple execution units for additional instruction level parallelism.

III. DATAPATH PIPELINING (10 points)

1. Given the single-cycle datapath for the following instruction, what control signals are provided for the datapath? Use 0, 1, or * for signals. (* means don't care.) For the ALU, assume 0 refers to the add operation and 1 to the sub operation. (4 points)



Instruction: bltu (not taken)

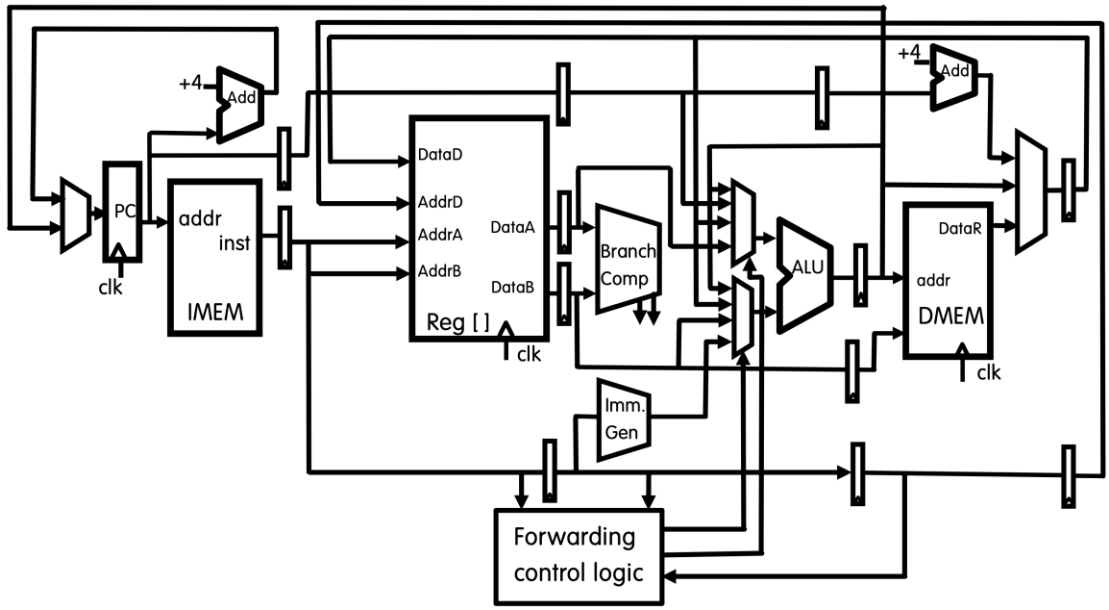
PCSel	RegWEn	BrUn	Bsel	Asel	ALUSel	MemRW	WBSel

2. Now consider the 5-stage pipelining with the combinational-read IMEM and DMEM and the forwarding paths as shown below. Assume you can write to and read from the same address in the register file in the same cycle. If there is a branch, assume that it is not taken, and there is no branch prediction. Consider two cases:

Case 1: Forwarding is not implemented;

Case 2: The forwarding muxes in the diagram are driven correctly by the forwarding logic.

For each case, write the number of NOPs needed between each instruction, and list the hazard that causes the stall. If no hazard occurs, write "None" and list the number of NOPs as 0. (6 points)




```
1       addi x1, x0, 0xFF
2       ori x2, x1, 0x7FF
3       bge x1, x2, label
4       xori x2, x2, 1
```

Instructions	Case 1 Hazard	Case 1 NOPs	Case 2 Hazard	Case 2 NOPs
1-2				
2-3				
3-4				

IV. CACHE (10 points)

For this question, assume `sizeof(int) == 4`. Assume a 4 KiB cache with 64B blocks, on a machine that has 4 GiB of physical memory.

1. Specify the size (in bits) of each field for the following cache types. (3 points)

i. Fully associative

Tag: _____ Index: _____ Offset: _____

ii. Four-way set associative
Tag: _____ Index: _____ Offset: _____

2. Consider the following C code.

```
int array_size = 1024;
void looptoy_loop(int *A, int *B) {
    for (int i = 0; i < array_size – 16; i += 16) {
       A[i] = A[i+16] + B[i];
    }
}
```

Recall that we have an 4KiB cache with 64B blocks, on a machine that has 4GiB of physical memory. For the following questions, assume the address of A[0] is 0x40000000 and the address of B[0] is 0x80000000.
i. If we have an 8-way set associative cache with an LRU replacement policy, a write allocate policy for write misses, and a write back policy for write hits, what is the hit rate? (2 points)
Hit rate: _____

ii. Assume the cache and block sizes are held constant. What is the minimum cache associativity that results in a hit rate no worse than the hit rate in question 2.i? (2 points)
Associativity: _____

iii. Assume now, with the current 8-way set associative cache, we add a second-level 64KiB Direct Mapped cache with 128B blocks, a write back policy for write hits, and a write allocate policy for write misses. Calculate the respective local hit rates for the L1 and L2 caches. (3 points)
L1: _____
L2: _____

V. VIRTUAL MEMORY (10 points)

Consider a RISC-V processor that include 2^{30} bytes of virtual memory, 2^{20} bytes of physical memory, and uses a page size of 2^{8} bytes.
1. Please calculate the following parameters relating to the size of the page table. You may assume each page entry contains a dirty bit and a resident bit. (3 points)
Number of entries in the page table: _____
Size of page table entry (in bits): _____
Size of the page table (in bits): _____

2. Now consider the same RISC-V processor, with a 4-element, fully-associative Translation Lookaside Buffer (TLB) with an LRU replacement policy. A program running on the processor is halted right before executing the following instruction located at address 0x5BA:

```
. = 0x5BA
sw x3, 0(x4) // x4 = 0xCAFE4
```

The first 8 entries of the page table are shown below. The page table uses an LRU replacement

policy. Assume that all physical pages currently in use.

TLB

	VPN	V	R	D	PPN
LRU→	0xD09	1	1	0	0x2
	0x1	1	1	0	0xFA
	0xCAF	1	1	1	0xEE
	0x3	1	1	0	0xB

Page Table

VPN	R	D	PPN
Next LRU→0	1	0	0x13
1	1	0	0xFA
2	0	0	0x3
3	1	0	0xB
4	1	0	0x1
5	0	--	--
6	0	--	--
LRU→7	1	0	0xF
	…		

For each virtual address in the chart below, please indicate the VPN, whether or not the access results in a TLB Miss, whether or not the access results in a page fault, the PPN, and the physical address. Please write all numerical values in hexadecimal. (5 points)

Virtual Address	VPN	TLB Miss (Yes/No)	Page Fault (Yes/No)	PPN	Physical Address
0x5BA					
0xCAFE4					

3. In question 2, please decide whether or not any physical page would be evicted upon a page fault, and whether or not any physical page would need to be written back to disk. (2 points)

Evicted page (Yes/No): _____

Writeback page (Yes/No): _____