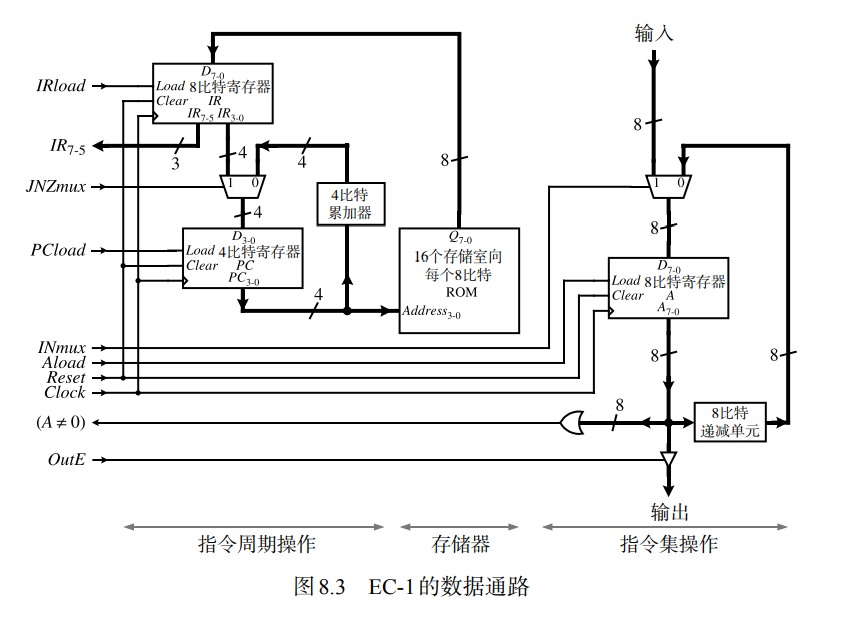
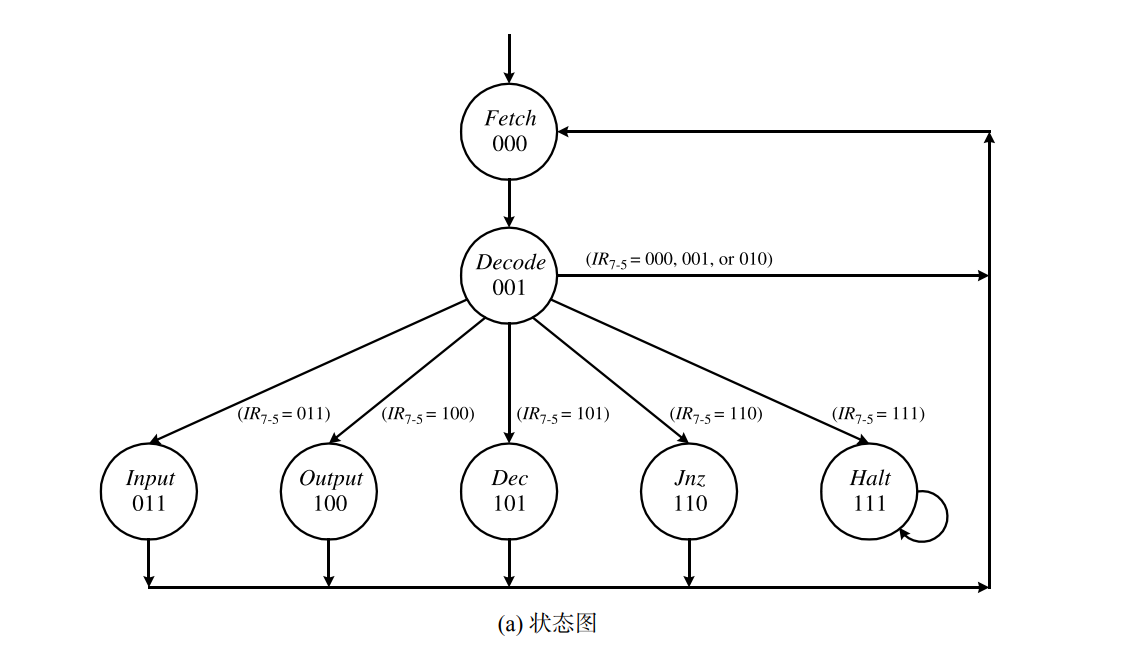
Lab7 实验报告

1. 实验原理



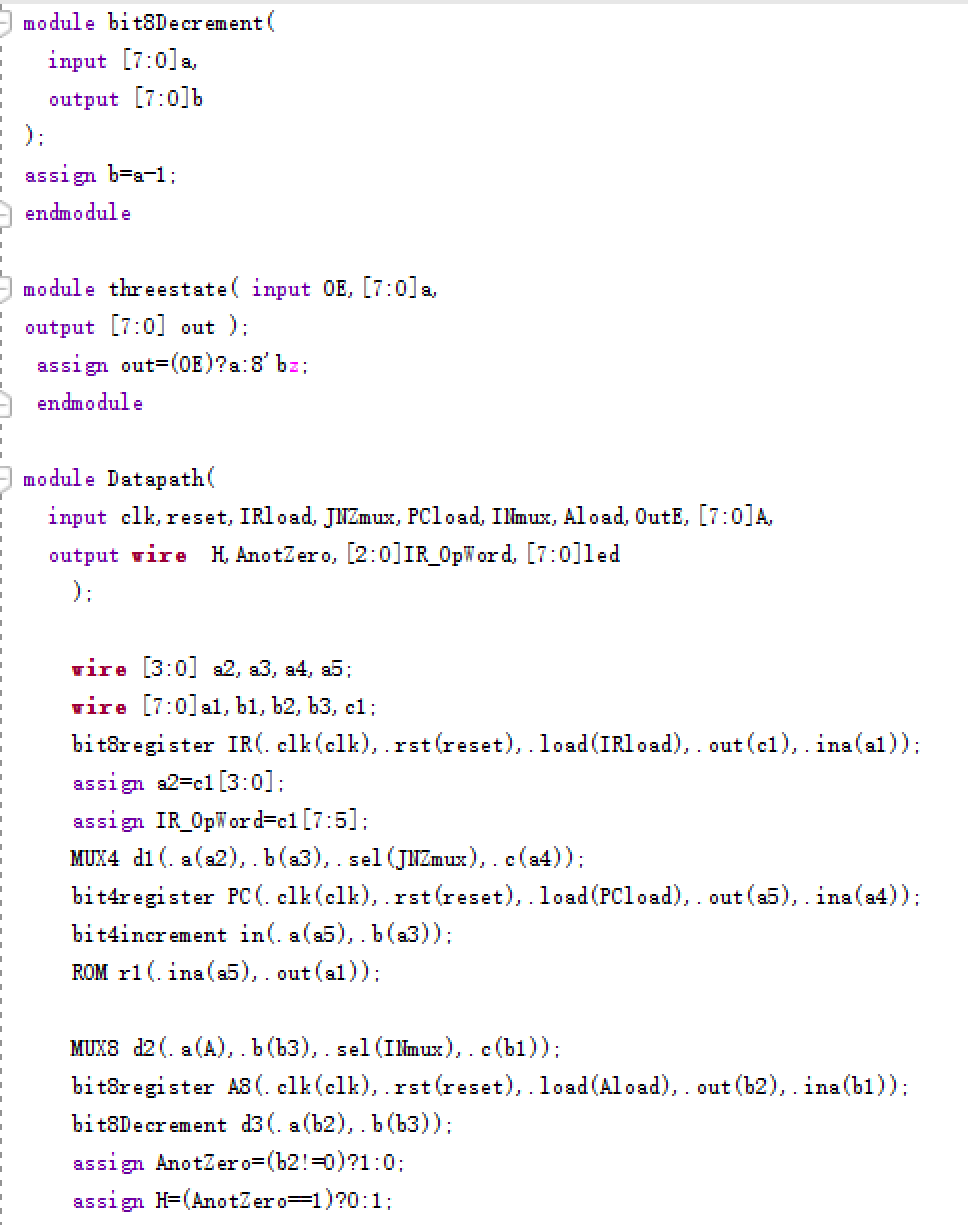
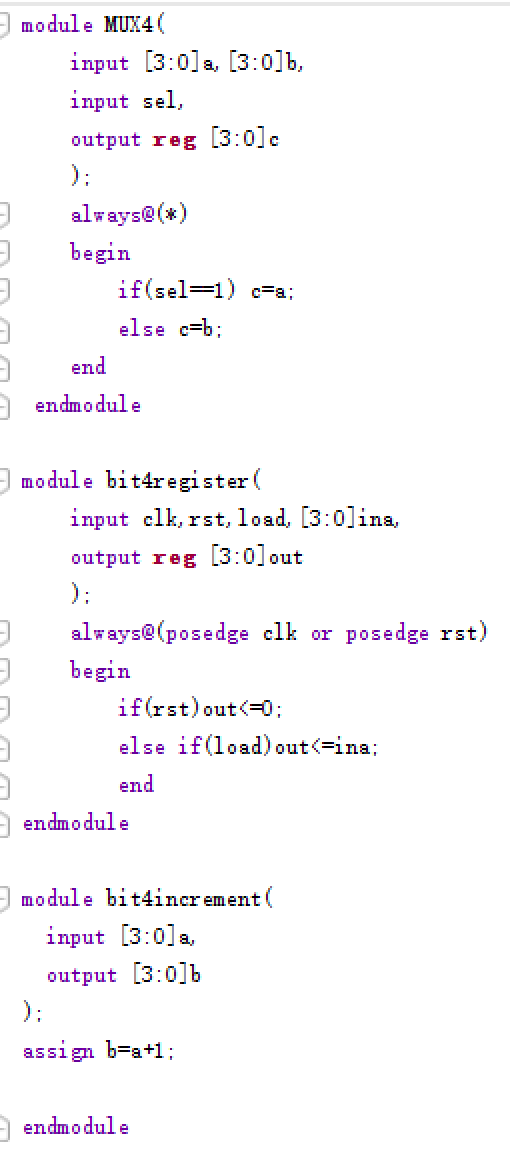
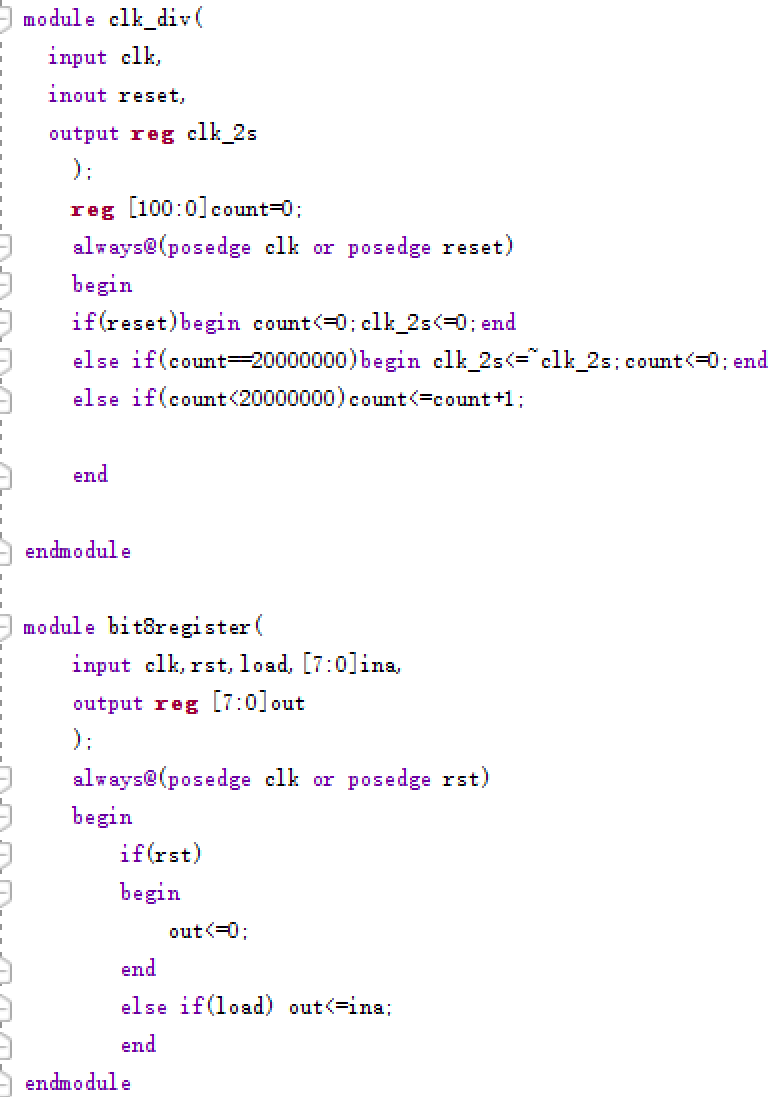


1. 状态图

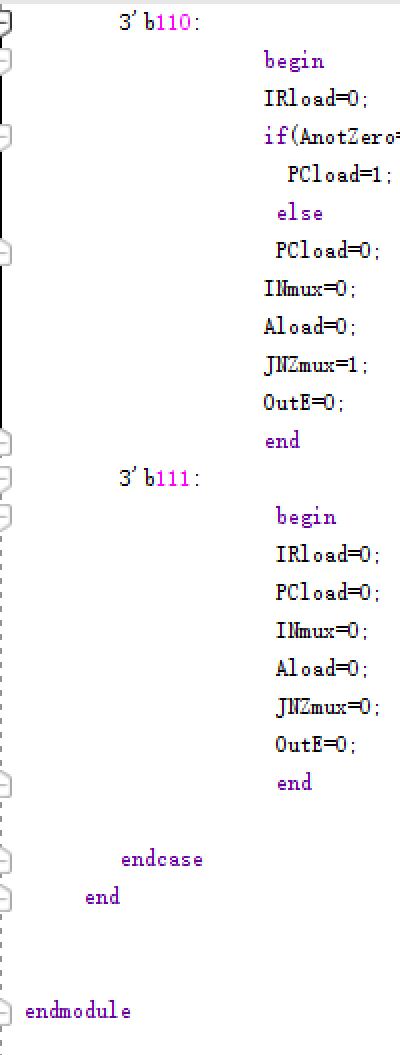
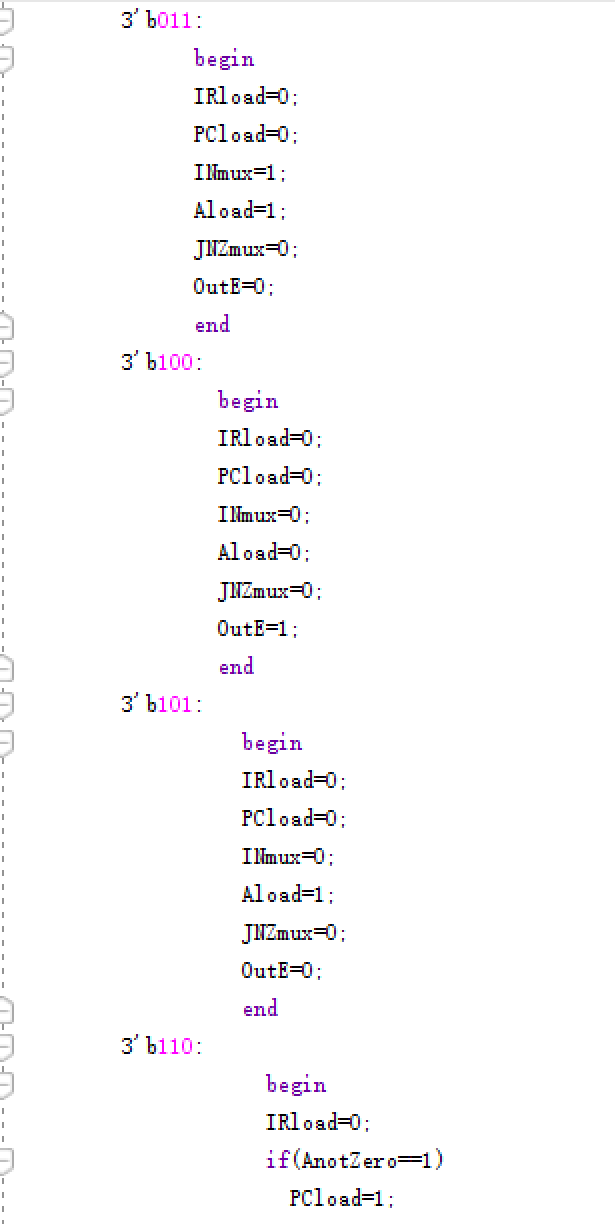
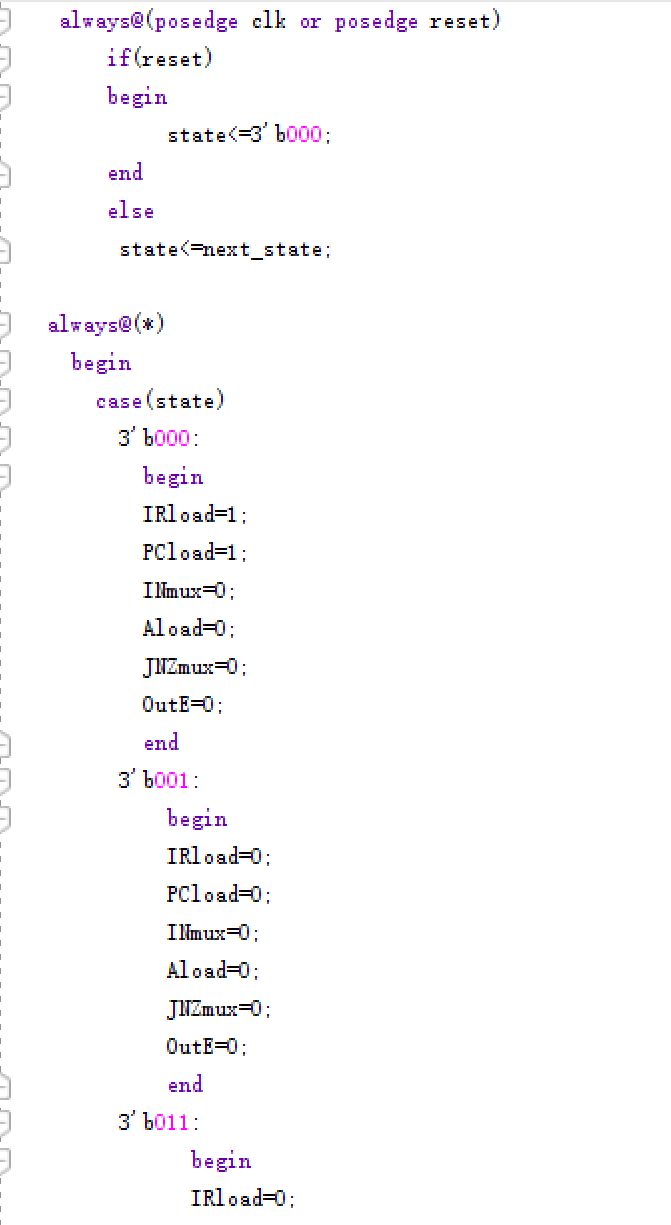
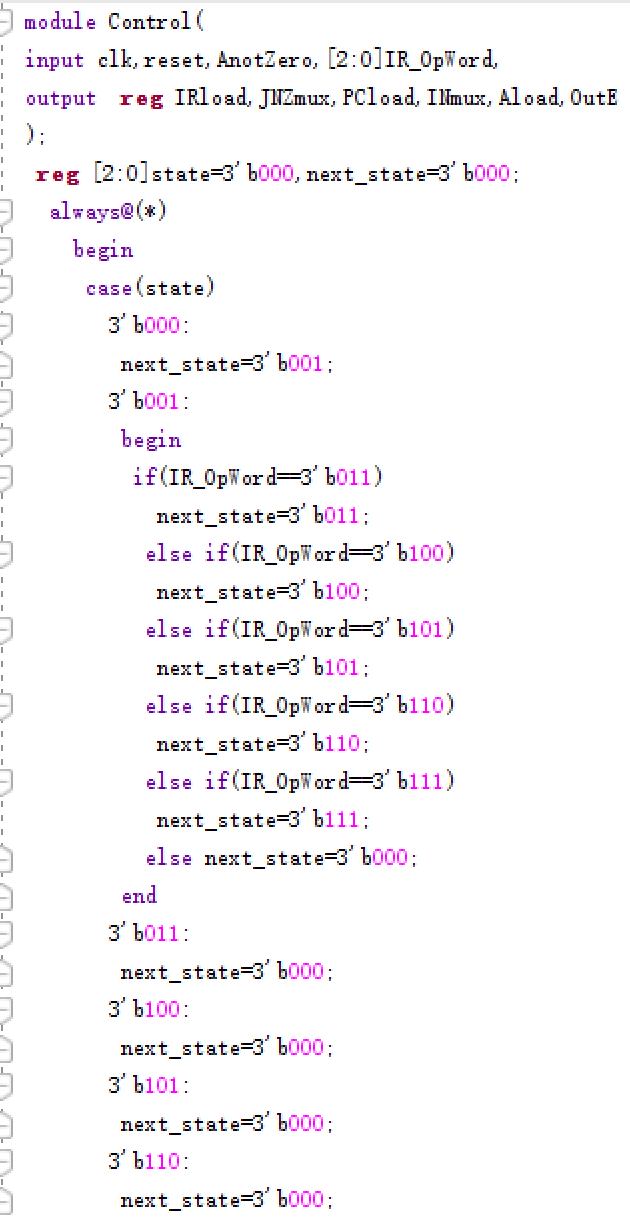


1. Verilog mode

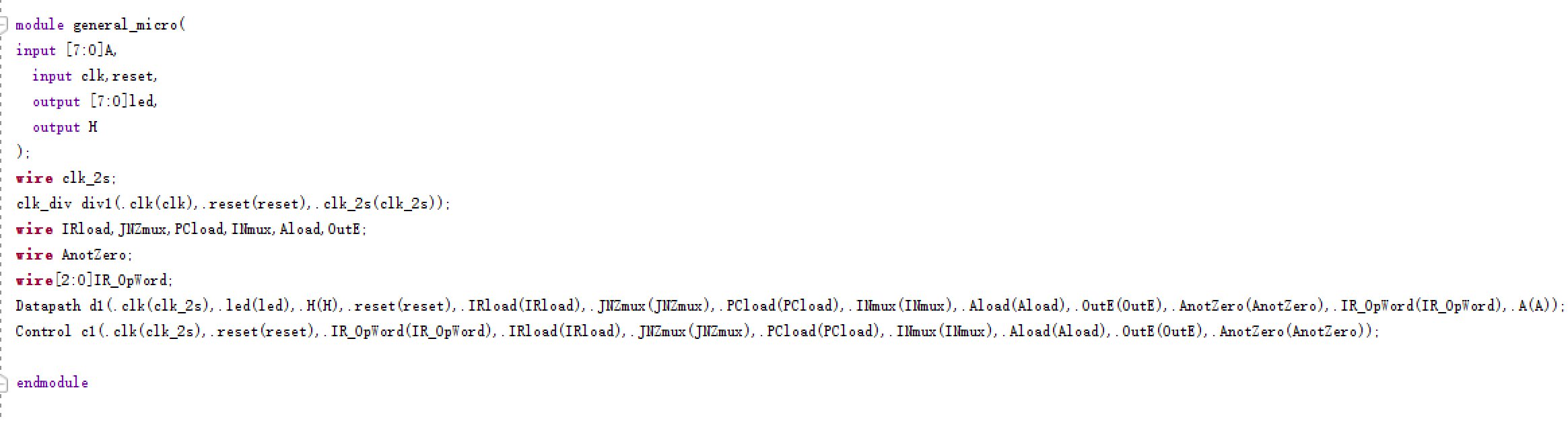
Datapath:



Control:



顶层：



1. 效果

