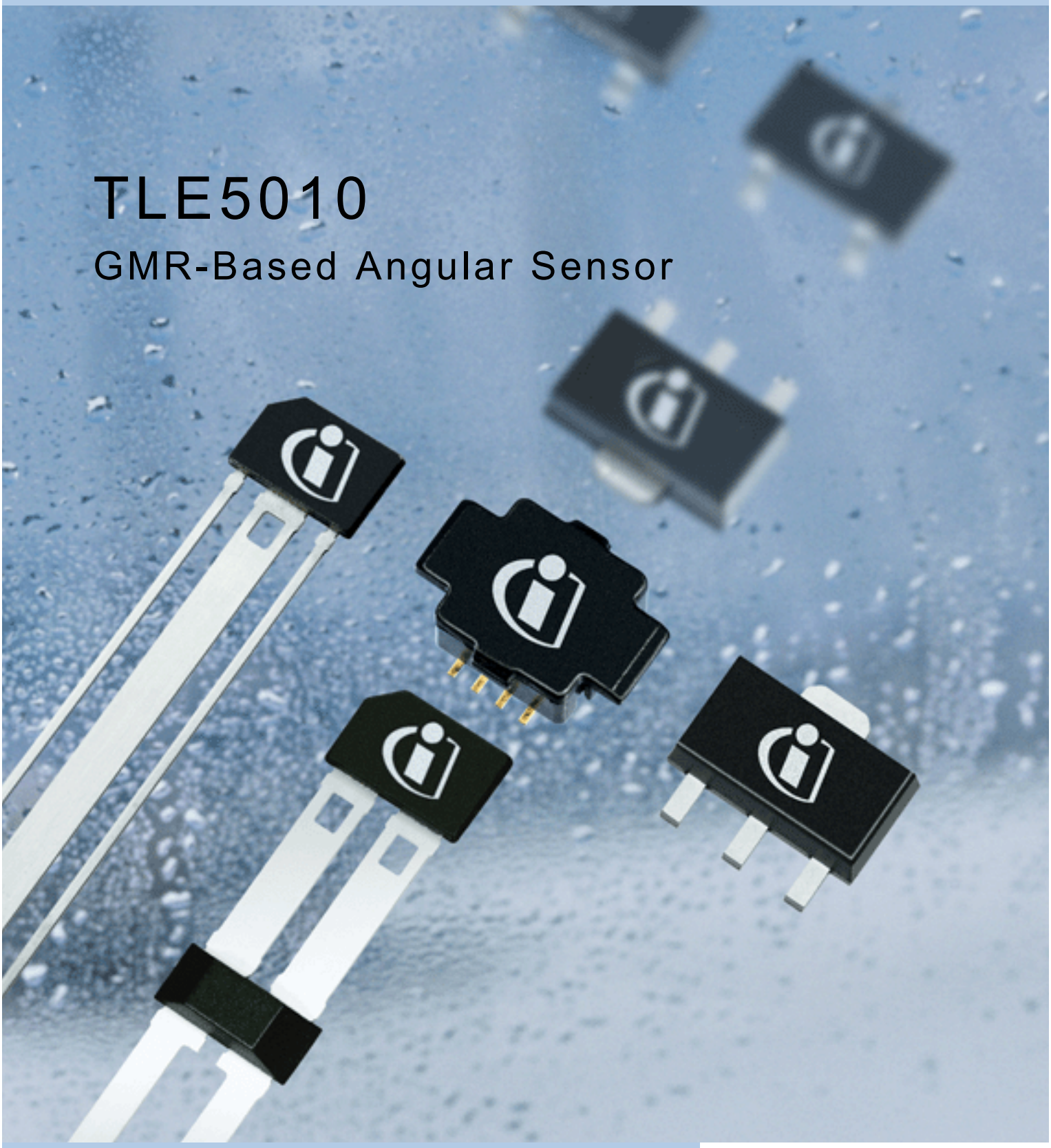
Preliminary Data Sheet, V 0.91, January 2008

TLE5010

GMR-Based Angular Sensor



Sensors

Never stop thinking

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TLE5010 Preliminary Data Sheet

Revision History:	**2008-01**	V 0.91
Previous Version:	V 0.9	

Page	Subjects (major changes since last revision)
General	Spelling and typing errors corrected
51	Molding Compound removed
52	Package Outline Figure modified
53	Marking changed

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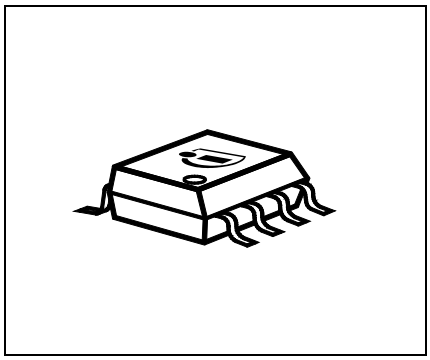
1 Overview



1.1 Features

- **G**iant **M**agneto **R**esistance (GMR)-based principle
- Integrated magnetic field sensing for angle measurement
- Full 0 - 360° angle measurement
- Highly accurate single bit SD-ADC
- 16 bit representation of sine / cosine values on the interface
- Bi-directional SSC Interface up to 2 Mbit/s
- 3-pin SSC Interface, SPI compatible with open drain
- ADCs and filters are synchronized with external commands via SSC
- Test resistors for simulating angle values
- Core supply voltage 2.5 V
- 0.25 µm CMOS technology
- Automotive qualified: -40°C to +150°C (Junction Temperature)
- Latch up immunity according JEDEC standard
- ESD > 2 kV (HBM)
- Green package with lead-free (Pb-free) plating

Type	Marking	Ordering Code	Package
TLE5010	5010-2	TBD	PG-DSO-8

1.2 Target Applications

The TLE5010 GMR-Based Angular Sensor is designed for angular position sensing in automotive applications, such as:

- Steering Angle
- Brushless DC Motor Commutation (e.g. EPS)
- Rotary Switch
- General Angular Sensing

1.3 Product Description

The TLE5010 is a 360° angle sensor that detects the orientation of a magnetic field. This is achieved by measuring sine and cosine angle components with monolithic integrated Giant Magneto Resistance (GMR) elements.

Data communications are accomplished with a bi-directional SSC Interface that is SPI compatible.

The sine and cosine values can be read out. These signals can be digitally processed to calculate the angle orientation of the magnetic field (magnet). This calculation can be done by using a cordic algorithm.

It is possible to connect more than one TLE5010 to one SSC Interface of a microcontroller for redundancy or any other reasons. If multiple TLE5010 devices are used, the synchronization of the connected TLE5010 is performed by a broadcast command. Each connected TLE5010 can be addressed by a dedicated Chip Select ($\overline{CS}$) pin.

Online diagnostic functions are provided to ensure reliable operation.

These diagnostics are

- Angle test (generated via test voltages feeding the ADC).
- Crossed signal paths (switchable for comparison)
- Inverted signs of bit streams
- Overvoltage and undervoltage detections

1.4 Pin Configuration

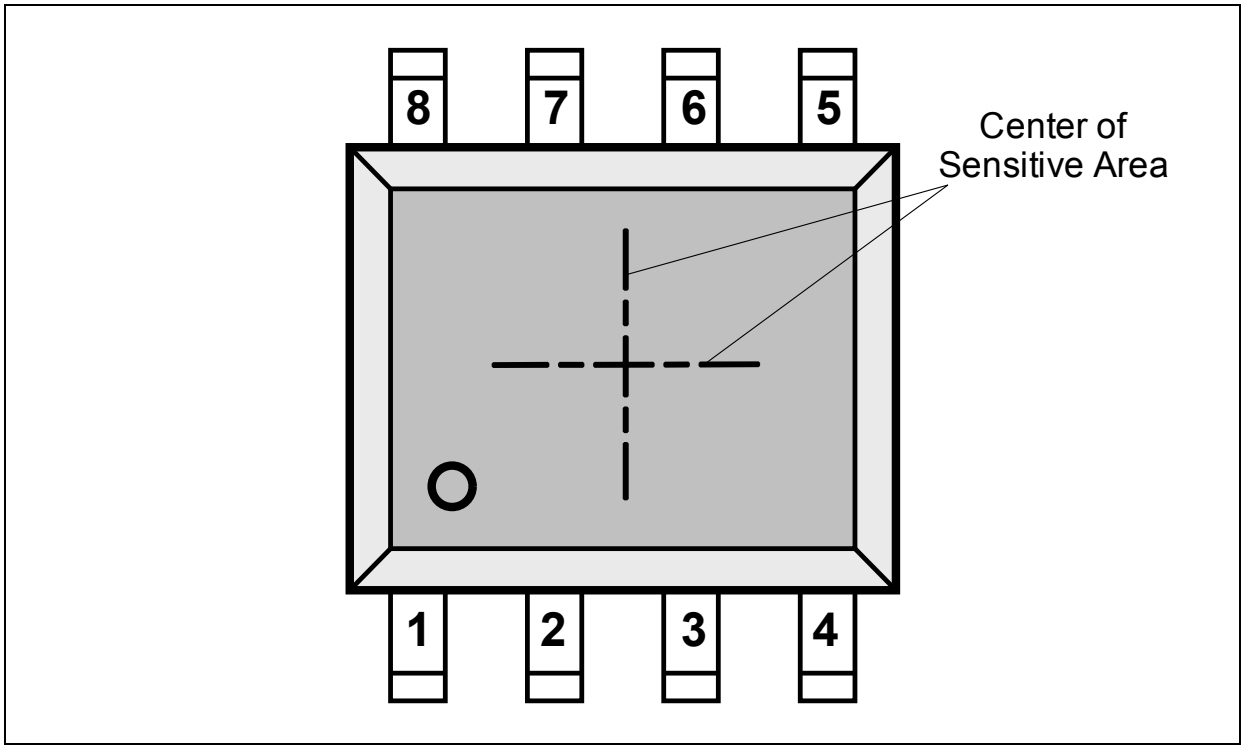


Figure 1 Pin Configuration (top view)

Table 1 Pin Definitions and Functions

Pin No.	Symbol	In/Out	Function
1	*CLK*	*I*	Chip Clock
2	*SCK*	*I*	SSC Clock
3	$\overline{CS}$	*I*	SSC Chip Select
4	*DATA*	*I/O*	SSC Data, open drain
5	*TST1*	*I/O*	Test Pin 1, must be connected to GND
6	V_{DD}	-	Supply Voltage
7	*GND*	-	Ground
8	*TST2*	*I/O*	Test Pin 2, must be connected to GND

2 General

2.1 Functional Description

The clock for the sensors is provided externally. This ensures a synchronously operation in case of multiple system participants.

The sensor has its own Phase Lock Loop (PLL) to generate the necessary clock frequency for the chip operation.

2.2 Block Diagram

The block diagram shows all switches in the reset position.

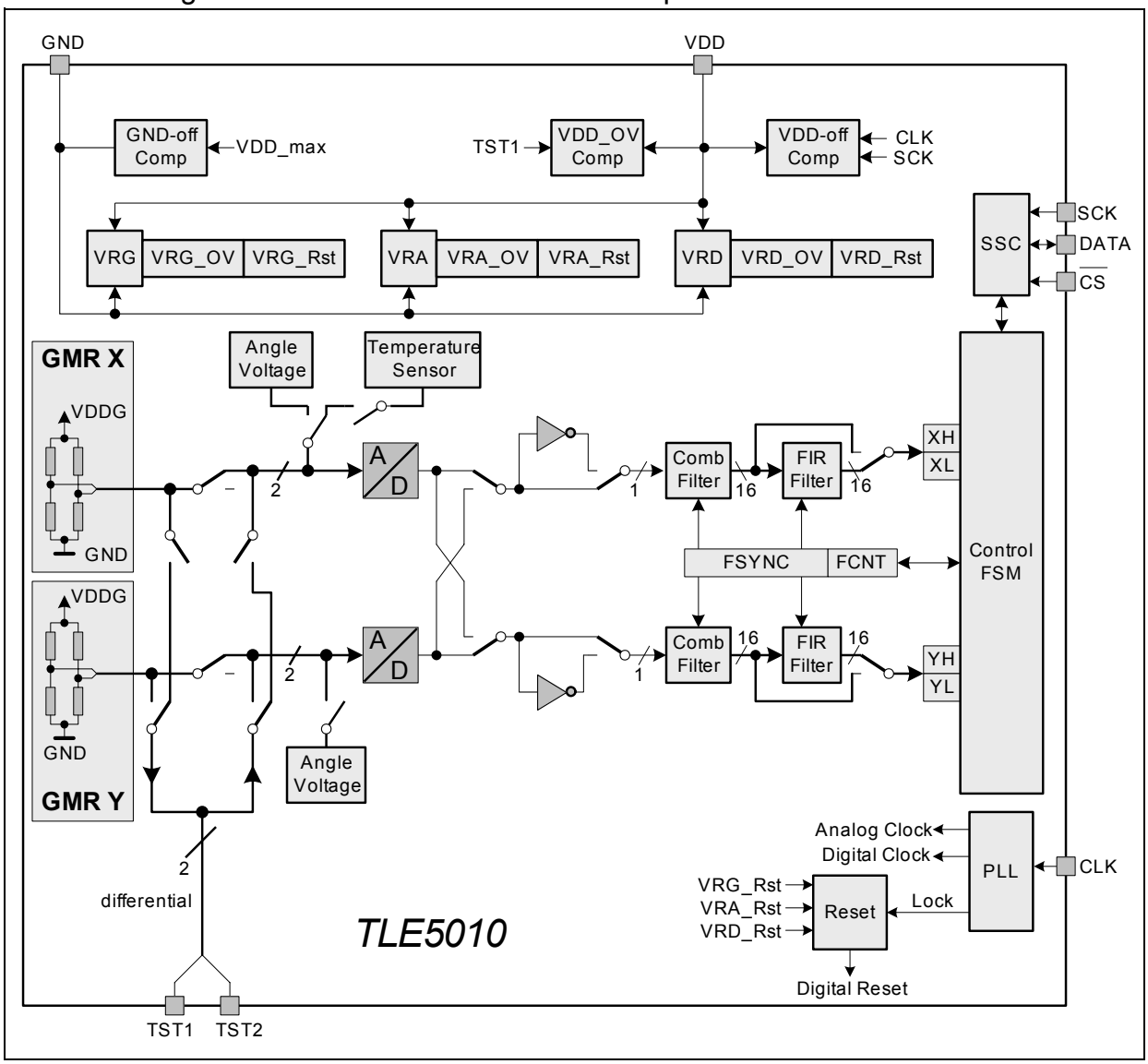


Figure 2 Block Diagram

2.3 Internal Power Supply

The internal stages of the TLE5010 are supplied with different voltage regulators.

- GMR Voltage Regulator VRG
- Analog Voltage Regulator VRA
- Digital Voltage Regulator VRD

Each voltage regulator has its own overvoltage and undervoltage detection circuits.

2.3.1 GMR Voltage Regulator VRG (VDDG-Voltage)

The GMR voltage regulator supplies all GMR parts.

- GMR Bridges
- Test Voltages for Angle Test
- ADC Reference Voltage

The voltages are monitored in the VRG overvoltage and undervoltage detectors.

2.3.2 Analog Voltage Regulator VRA (VDDA-Voltage)

The analog voltage regulator supplies the analog parts.

- ADCs
- PLL (analog)
- VDD-Off comparator
- GND-Off comparator
- V_{DD} Overvoltage detection

The voltages are monitored in the VRA overvoltage and undervoltage detectors.

2.3.3 Digital Voltage Regulator VRD (VDDD-Voltage)

The digital voltage regulator supplies all digital parts.

- Comb filters, FIR filters and Low Pass filter
- PLL (digital)
- Control FSM with Bitmap
- SSC Interface
- Counters (Reset, FSYNC, FCNT)

The voltages are monitored in the VRD overvoltage and undervoltage detectors.

2.4 GMR Functionality

The GMR sensor is implemented using vertical integration. This means that the GMR active areas are integrated above the logic portion of the TLE5010 device. GMR elements change their resistance depending on the direction of the magnetic field.

Four individual GMR elements are connected to one Wheatstone Sensor Bridge. These GMR elements sense one of two components of the applied magnetic field:

- X component, V_X (cosine) or the
- Y component, V_Y (sine)

The advantage of a full-bridge structure is that the amplitude of the GMR signal is doubled.

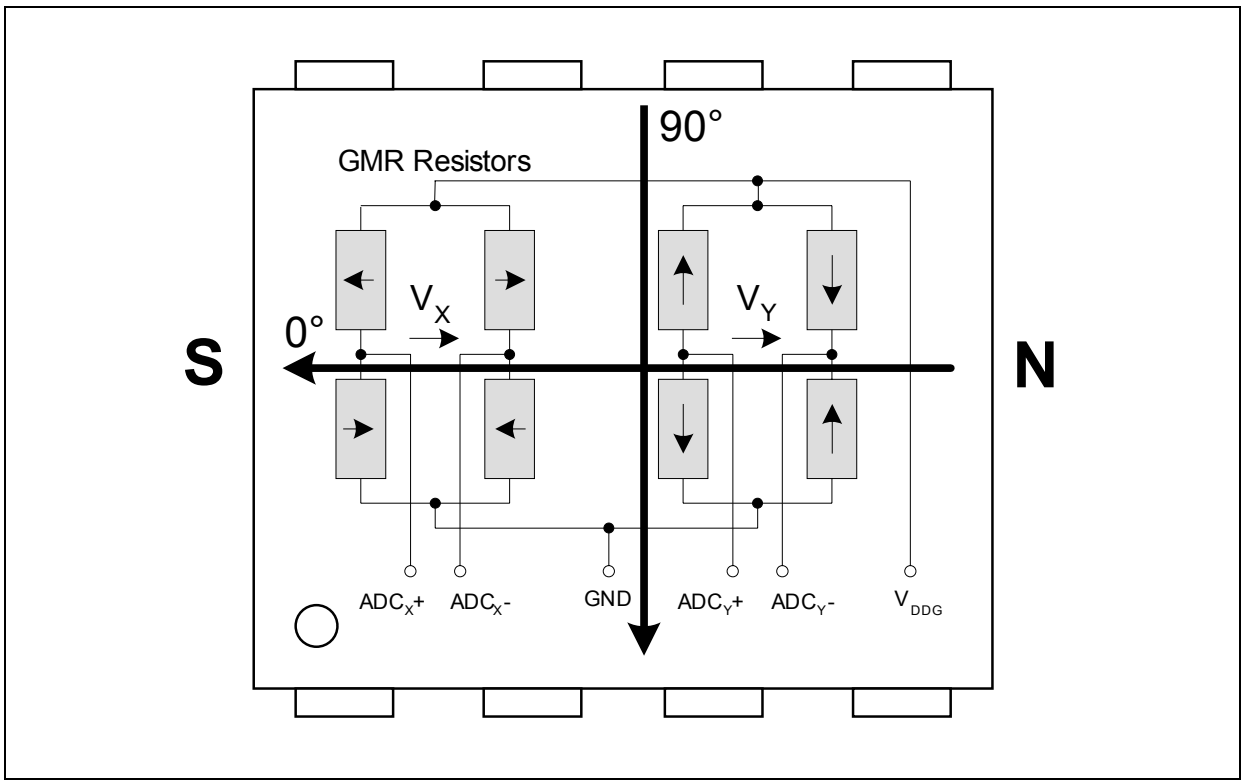


Figure 3 Sensitive Bridges of the GMR Sensor

*Note: In **Figure 3**, the arrows in the resistor symbols indicate the direction of the Reference Layer.*

The output signal of each bridge is only unambiguous over 180° between two maxima. Therefore two bridges are orientated orthogonally to each other.

Using the ARCTAN function, the true 360° angle value can be calculated that is represented by the relation of the X and Y signals.

Because only the relative values influence the result, the absolute size of the two signals is of minor importance. Therefore, most influences to the amplitudes are compensated.

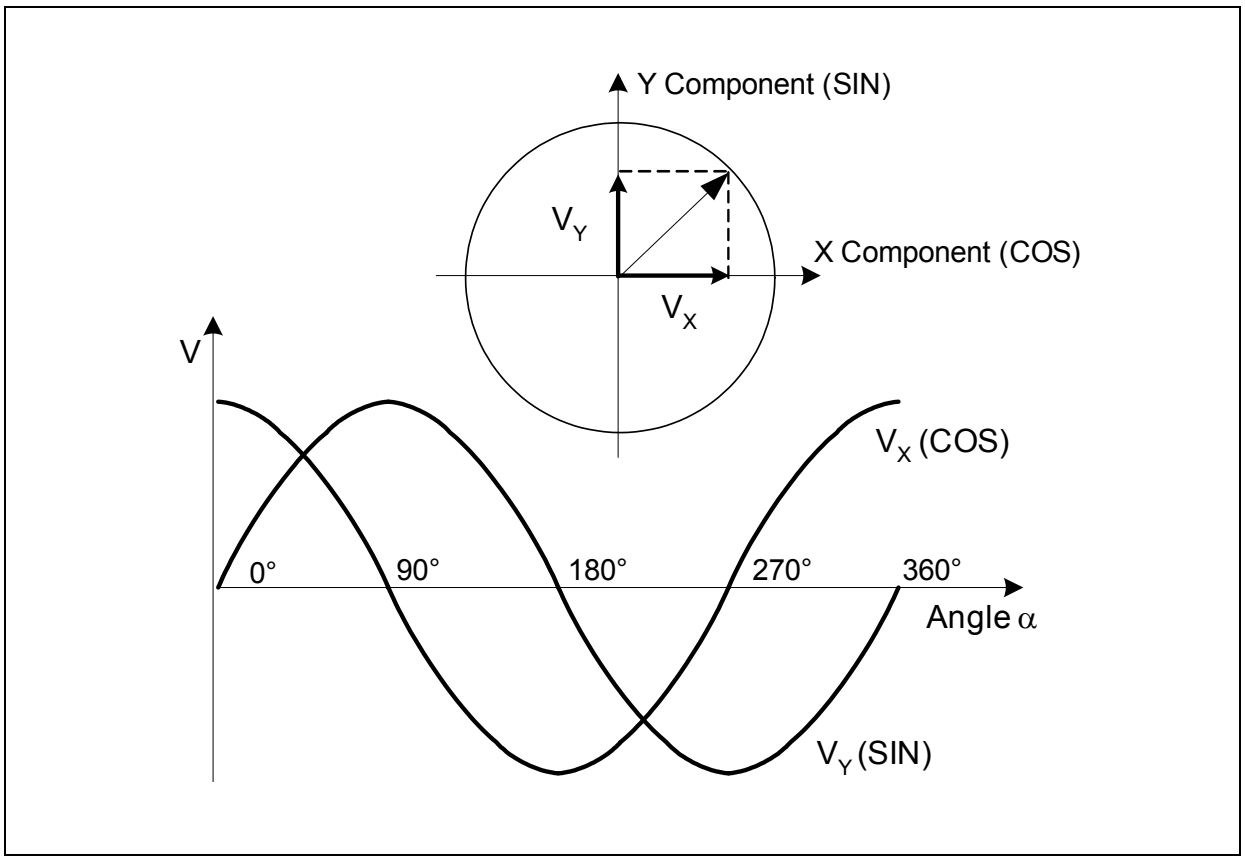


Figure 4 Ideal Output of the GMR Sensor

3 Absolute Maximum Ratings

Table 2 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Voltage on V_{DD} pin respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	max 40 h / lifetime
Voltage on any pin respect to ground (V_{SS})	V_{IN}	-0.5	6.5	V	V_{DD} + 0.35 V may not be exceeded
Junction Temperature	T_J	-40	150	°C	
Magnetic Field Induction	B	-	|125|	mT	max 5 min. @ t_A = 25°C
		-	|80|		max 5 h @ t_A = 25°C

Note: Stresses above the max. value listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit..

4 Operating Range

The operating conditions identified in **Table 3** must not be exceeded in order to ensure correct operation of the TLE5010. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 3 Operating Range

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Supply Voltage	V_{DD}	4.5	-	5.5	V	1)
Output Current	I_Q	-	-5	-10	mA	2) 3)
Input Voltage	V_{IN}	-0.3	-	5.5	V	V_{DD} + 0.5 V may not be exceeded
Magnetic Induction	B_{XY}	25	30	45	mT	In X / Y direction4)
Angle Range	Ang	0	-	360	°	sine / cosine
Storage Temperature	T_{ST}	-40	-	50	°C	
Overall Lifetime	t_{life}	-	-	15	Years	

1) Directly blocked with 100 nF ceramic capacitor.

2) Max current to GND over Open Drain Output.

3) The corresponding voltage levels are listed in **Table 5 "Electrical Parameters" on Page 16**.

4) Values refer to an homogenous magnetic field (Bxy) without vertical magnetic induction (Bz = 0 mT). By applying a vertical magnetic induction an additional error has to be considered.

*Note: The thermal resistances listed in **Table 20 "Package Parameters" on Page 51** must be used to calculate the corresponding ambient temperature.*
***Table 3** is valid for* - 40°C < T_J < 150°C.

5 Electrical and Magnetic Parameters

5.1 Electrical Parameters

The indicated electrical parameters apply to the full operating range, unless otherwise specified. The typical values correspond to a supply voltage V_{DD} = 5.0 V and 25°C, unless individually specified. All other values correspond to - 40°C < T_J < 150°C

Table 4 Electrical Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Supply Current [1]	I_{DD}	-	15	20	mA	V_{DD} = 4.5 to 5.5 V
		-	-	21		V_{DD} = 6.5 V
POR Level	V_{POR}	2.0	2.3	2.9	V	Power On Reset
POR Hysteresis	V_{PORhy}	-	30	-	mV	
Power On Time	t_{Pon}	50	100	200	µs	V_{DD} > V_{DDmin} & after first edge on f_{CLK}
PLL Jitter	t_{PLLjit_S}	-	1.3	2.0 [2]	ns	short term [3]
	t_{PLLjit_L}		3.0	3.9		long term [4]
ADC Noise [5]	N_{ADC}	-	1	2.2	digits	1 σ @ FIR_BYP = 0
		-	2	4.4 [2]		1 σ @ FIR_BYP = 1
Input Signal Low Level	V_L	-0.35	-	0.3 V_{DD}	V	Tested only at DATA pin as structures of all pins are identical
Input Signal High Level	V_H	0.7 V_{DD}	-	V_{DD} +0.35	V	
Capacitance of SSC Data Pin	C_{LDATA}	-	4	6 [2]	pF	Internal

[1] Without external pull-up resistor for SSC-Interface.

[2] Not tested.

[3] From pulse to pulse.

[4] Accumulated over 1 ms.

[5] ADC noise with respect to the peak ADC value specified in **"Signal Processing" on Page 23**.
Noise tested using 1 σ of 100 sample values from Angle Test "000"

Table 5 Electrical Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Input Hysteresis	V_{HY}	0.07 V_{DD}	-	-	V	
Pull-Up Current	I_{PU}	-10	-	-150	µA	$\overline{CS}$, DATA
Pull-Down Current	I_{PD}	15	-	225	µA	SCK, CLK
		15	-	225		TST1
		10	-	150		TST2
Output Signal Low Level	V_{OL}	- -	- -	0.7 0.4	V	I_Q = - 10 mA I_Q = - 5 mA [1]

[1] The value -5 mA is not tested

*Note: **Table 5** is valid for* 4.5 V < V_{DD} < 5.5 V

5.2 ESD Protection

Table 6 ESD Protection

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
ESD Voltage	V_{HBM}	-	± 2	kV	HBM [1]
	V_{CDM}	-	± 500	V	CDM [2]

[1] Human Body Model (HBM) according to: JEDEC EIA/JESD22-A114-B (R = 1.5 kΩ, C = 100 pF, T_A = 25°C)

[2] Charge Device Model (CDM) according to: ANSI ESD STM JEDEC JESD 22-C101-A Class III.

5.3 GMR Parameters

All parameters apply over the full operating range, unless otherwise specified.

Table 7 Basic GMR Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
X, Y Output range	RG_{ADC}	-	-	±23230	digits	
X, Y Amplitude [1]	A_X, A_Y	7402	12337	15781	digits	@ Calibration Conditions
		3922	-	20620		Operating Range
X, Y Synchronism [2]	k	80	100	120	%	@ Calibration Conditions
X, Y Offset [3]	O_X, O_Y	-3000	0	3000	digits	@ Calibration Conditions
X, Y Orthogonality Error	φ	-10.0	0	10.0	°	@ Calibration Conditions
X,Y without field	X_0, Y_0	-5000	-	5000	digits	without magnet[4]

1) See **Figure 4, Page 12**

2) k = 100 x (A_X / A_Y).

3) O_{SIN} = (Y_{MAX} + Y_{MIN}) / 2 ; O_{COS} = (X_{MAX} + X_{MIN}) / 2

4) Not tested.

5.3.1 Offset and Amplitude

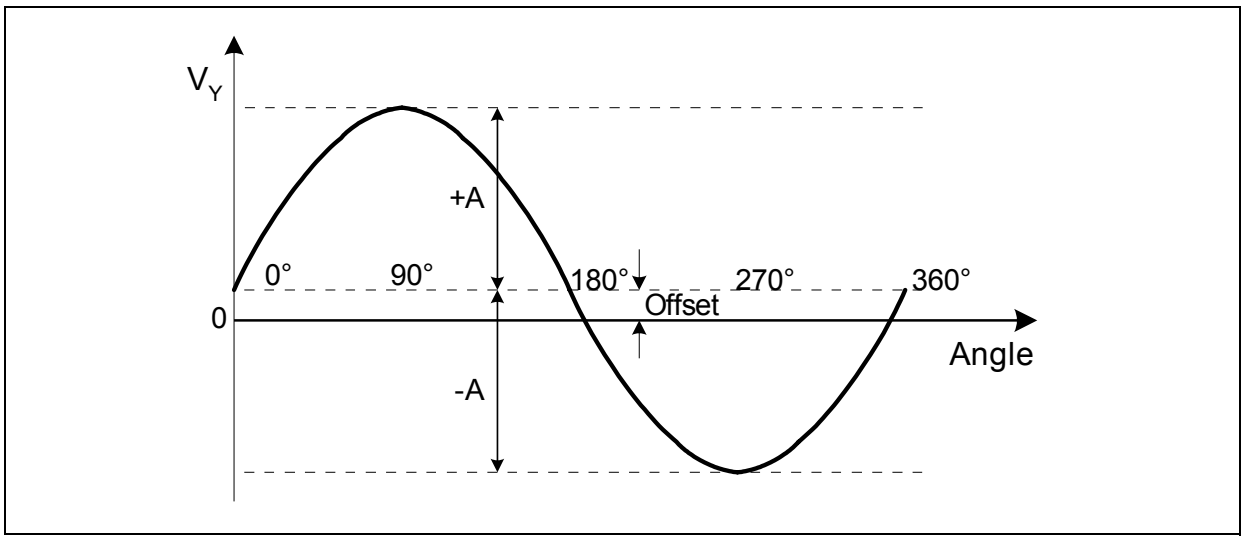


Figure 5 Offset and Amplitude

Offset Definition

The offset of the X and Y signals is defined as the mean value between the signed maximum and minimum values of the idealized sine or cosine wave.

$$O_{\mathrm{X}} = \frac{X_{\mathrm{MAX}} + X_{\mathrm{MIN}}}{2}$$

$$O_{\mathrm{Y}} = \frac{Y_{\mathrm{MAX}} + Y_{\mathrm{MIN}}}{2}$$

Amplitude Definition

The amplitude is defined as half the difference between the signed maximum and minimum values of the idealized sine or cosine wave.

$$A_{\mathrm{X}} = \frac{X_{\mathrm{MAX}} - X_{\mathrm{MIN}}}{2}$$

$$A_{\mathrm{Y}} = \frac{Y_{\mathrm{MAX}} - Y_{\mathrm{MIN}}}{2}$$

5.3.2 Temperature-Dependent Behavior

The temperature offset gradients for both channels depend on the value at 25°C. The gradients can be calculated using the following linear equations:

$$KT_{\mathrm{OX}} = tco\_d\_x + (tco\_k\_x \times O_{\mathrm{X25}})$$

$$KT_{\mathrm{OY}} = tco\_d\_y + (tco\_k\_y \times O_{\mathrm{Y25}})$$

O_{X25}, O_{Y25}: Offset values at 25°C in digits.

Table 8 GMR Temperature Coefficients

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Offset Temperature Coefficient Base	*tco_d_x*	-	+0.116296	-	digits_/_K	
	tco_d_y	-	-0.079401	-		
Offset Temperature Coefficient Gain	*tco_k_x*	-	-0.0010147	-	1_/_K	
	tco_k_y	-	-0.0010121	-		

5.3.3 Orthogonality Definition

The corresponding maximum and zero crossing points of the SIN and COS signals do not occur at the precise distance of 90°. The difference between X and Y phase is called the **Orthogonality Error**.

$$\varphi = \varphi_X - \varphi_Y$$

jideal = 0°

jX : Phase error of X (= cos) Signal

jY : Phase error of Y (= sin) Signal

5.4 Calibration

GMR Values

The end-of-the-line calibration can be accomplished using the following sequence.

- Turn magnetic field **left** and measure X and Y values
- Calculation of Amplitude, Offset, Phase correction values of left turn
- Turn further 90° left and 90° back right without measurement
- Turn magnetic field **right** and measure X and Y values
- Calculation of Amplitude, Offset, Phase correction values of right turn
- Calculation of **mean** values of Amplitude, Offset, Phase correction values

The conditions are specified in **Table 9**.

The above gained values must be stored in non-volatile memory. They are used for the correction of the read-out X and Y values before the angular calculation.

The resulting angular deviation is calculated using the above determined parameters.

Temperature Measurement

The signal amplitude T_{25} of the temperature measurement path at the calibration conditions must be measured and stored.

Calibration Conditions

All errors are related to calibration performed using the following conditions:

Table 9 GMR Calibration Conditions

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Flux density	B_{CAL}	-	30	-	mT	B_Z = 0 mT
Temperature	T_{CAL}	-	25	-	°C	

5.5 Angle Calculation

5.5.1 Components of the Output Signals

The X and Y signals at the output can be described by the following equations:

$$X = A_X \times \cos(\alpha + \varphi_X) + O_X$$

$$Y = A_Y \times \sin(\alpha + \varphi_Y) + O_Y$$

A_X : Amplitude of X (= cos) Signal
A_Y : Amplitude of Y (= sin) Signal
O_X : Offset of X (= cos) Signal
O_Y : Offset of Y (= sin) Signal
φ_X : Phase error of X (= cos) Signal
φ_Y : Phase error of Y (= sin) Signal

5.5.2 GMR Error Compensation

Temperature-Dependent Offset Value

To increase accuracy, the temperature-dependent offset drift can be compensated. The temperature of the chip must be read out. The Offset values O_X and O_Y can be described by the following equations.

$$O_X = O_{X25} + \frac{KT_{OX}}{S_T} \times (T - T_{25})$$

$$O_Y = O_{Y25} + \frac{KT_{OY}}{S_T} \times (T - T_{25})$$

O_{X25} , O_{Y25} : Offset value at 25°C in digits
T_{25} : Temperature value at 25°C in digits
T : Temperature value in digits
S_T : Sensitivity of the temperature measurement path, (see **“Temperature Measurement” on Page 46**).

Offset Correction

After the X and Y values are read out, the temperature corrected offset value must be subtracted.

$$X_1 = X - O_X$$

$$Y_1 = Y - O_Y$$

Amplitude Normalization

Next, the X and Y values are normalized using the peak values determined in the calibration.

$$X_2 = \frac{X_1}{A_X}$$

$$Y_2 = \frac{Y_1}{A_Y}$$

Non-Orthogonality Correction

The influence of the non-orthogonality can be compensated using the following equation, in which only the Y channel must be corrected.

$$Y_3 = \frac{Y_2 - X_2 \times \sin(-\varphi)}{\cos(-\varphi)}$$

Resulting Angle

After correction of all errors, the resulting angle can be calculated using the arctan function[1)].

$$\alpha = \arctan\left(\frac{Y_3}{X_2}\right) - \varphi_X$$

1) Microcontroller function “arctan2(Y_3,X_2)” to resolve 360°

5.6 GMR Parameters after Calibration

After calibration under the conditions specified in **Table 9 "GMR Calibration Conditions" on Page 19**, the sensor has a remaining error, as shown in **Table 10**. The error value refers to B_Z = 0 mT and the operating conditions given in **Table 3 "Operating Range" on Page 14**.

Table 10 GMR Parameter with Temperature-Dependent Offset Compensation

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ. [1]	max.		
Overall Error	α_{err}	-	0.7	2,0	°	2) 3)

1) At 25°C, B=30mT

2) Including hysteresis error

3) At 0h

6 Signal Processing

Table 11 Signal Processing

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.[1]	max.		
Internal Cutoff Frequency (-3dB) of sin or cos Value	$f_{Cut\text{-}Off}$	-	4.9	-	kHz	FIR_BYP=0
			19.6			FIR_BYP=1
Update Time of SIN or COS Value[2]	t_{upd}	-	81,9	-	µs	FIR_BYP=0
		-	20,5	-		FIR_BYP=1
Settle Time [3]	t_{settle}	-	163,8	-		FIR_BYP=0
		-	41,0	-		FIR_BYP=1
Peak ADC Output value	ADC_{Pk}	-	-	23230	digits	signed 16-bit integer (2s complement) [4] [5] [6]

1) For 4 Mhz input frequency

2) t_{upd} = 8192 / (25 x f_{CLK}) for FIR_BYP = 0
t_{upd} = 8192 / (100 x f_{CLK}) for FIR_BYP = 1

3) t_{settle} = 2 x t_{upd} , after change of ADC input source

4) Output values are valid up to this limit. Above it, corrupted results may occur due to non-linearity of the ADC.

5) One digit represent typically 5.166 µV.

6) Correspond to max. GMR output value.

7 Clock Supply (CLK Timing Definition)

The clock signal input “CLK” must fulfill certain requirements, as identified in this section:

- The high or low pulse width must not exceed the specified values, because the PLL needs a minimum pulse width and must be spike filtered.
- The duty cycle factor should be 0.5 but can deviate to the values limited by $t_{CLKh(f\_min)}$ and $t_{CLKl(f\_min)}$.
- The PLL is triggered at the positive edge of the clock. If more than two edges are missing, a chip reset is generated automatically.

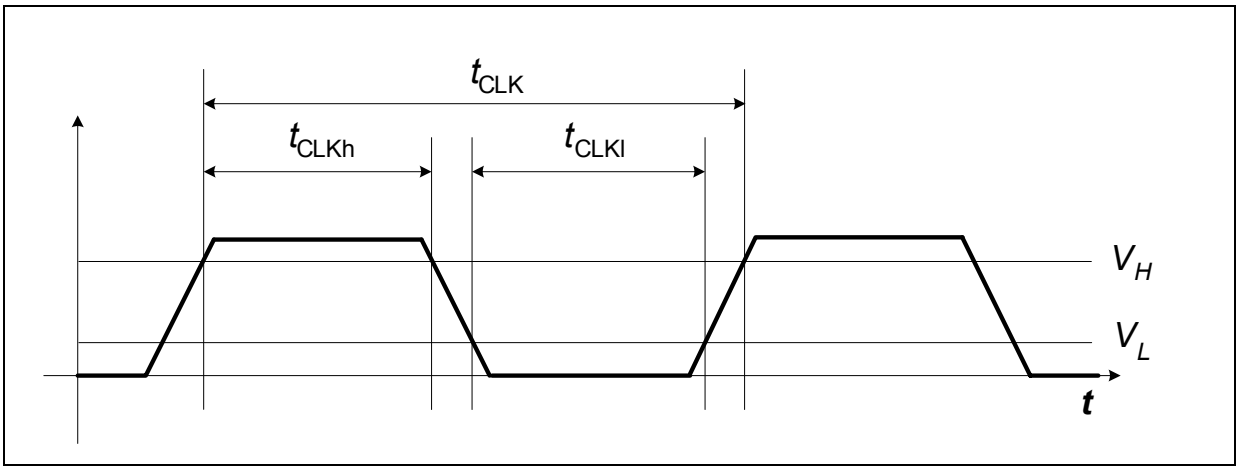


Figure 6 CLK Timing Definition

Table 12 CLK Timing Specification

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Input Frequency	f_{CLK}	3.9	4.00	4.2	MHz	
CLK Duty Cycle [1]	CLK_{DUTY}	30	50	70	%	
CLK Rise Time	t_{CLKr}	-	-	20	ns	from V_L to V_H
CLK Fall Time	t_{CLKf}	-	-	20	ns	from V_H to V_L
PLL Frequency	f_{PLL}	-	100	-	MHz	f_{CLK} * 25
Digital Clock	f_{DIG}	-	25	-	MHz	(25 / 4) * f_{CLK}
Digital Clock Period	t_{DIG}	-	40	-	ns	4 / (25 * f_{CLK})

[1] Minimum duty cycle factor: $t_{CLKh(f\_min)}$ / $t_{CLK(f\_min)}$ with $t_{CLK(f\_min)}$ = 1 / $f_{CLK(f\_min)}$
Maximum duty cycle factor: $t_{CLKh(f\_max)}$ / $t_{CLK(f\_min)}$ with $t_{CLKh(f\_max)}$ = $t_{CLK(f\_min)}$ - $t_{CLKl(min)}$

8 Synchronous Serial Communication Interface

The 3-pin Synchronous Serial Communication Interface (SSC) has a bi-directional data line (open drain), a serial clock signal and chip select.

The SSC Interface is designed to communicate with a microcontroller with a bi-directional SSC interface supporting Open Drain. Other microcontrollers may require an external NPN transistor. This allows communication with SPI-compatible devices.

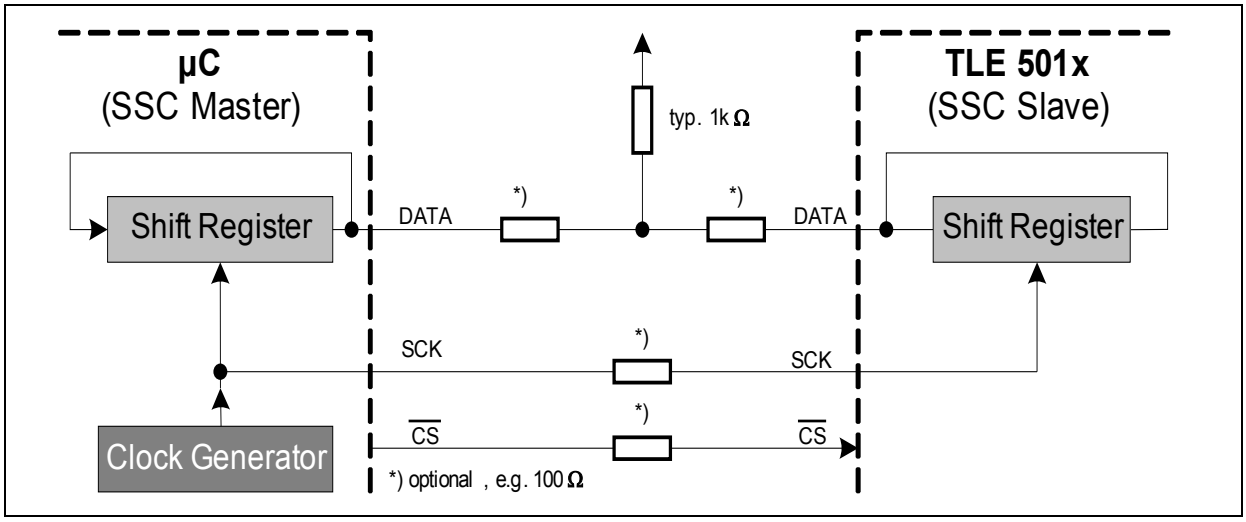


Figure 7 SSC Half-Duplex Configuration—Microcontroller with Open Drain

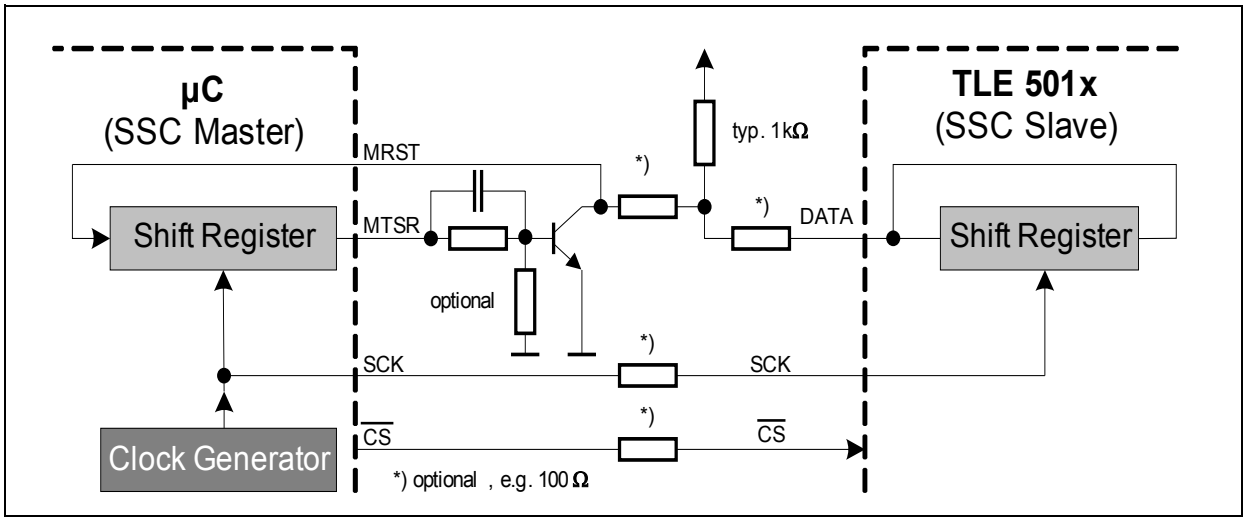


Figure 8 SSC Half-Duplex Configuration—Microcontroller without Open Drain

8.1 SSC Timing Definition

SSC Timing Diagram

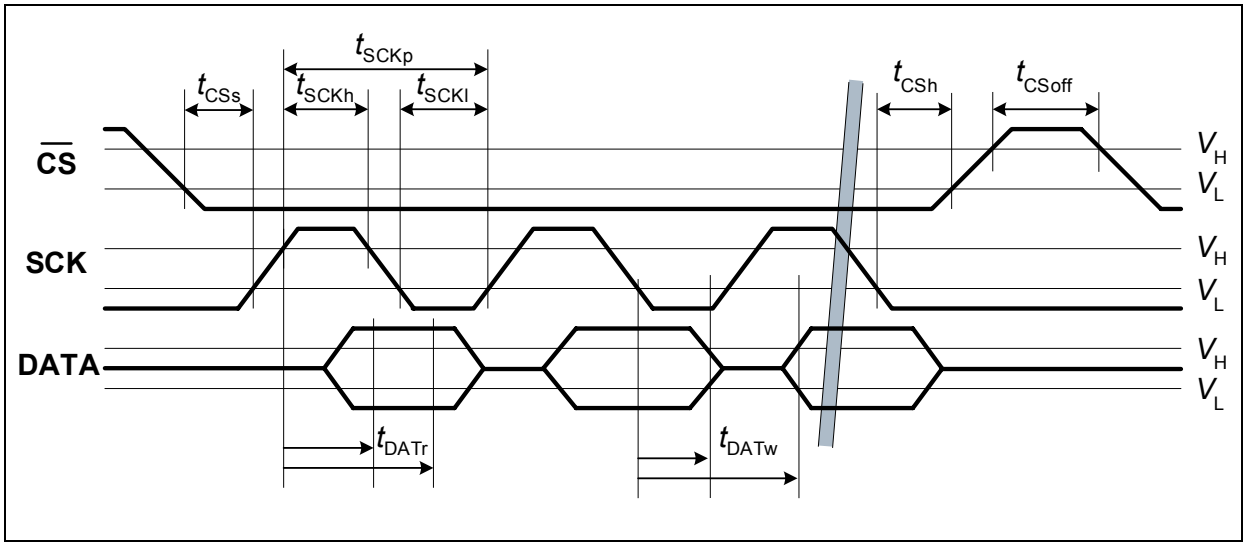


Figure 9 SSC Timing

SSC Inactive Time ($\overline{CS}_{off}$)

The SSC inactive time defines the delay time after a transfer before the TLE5010 can be selected again. The TLE5010 reacts to only one command after SSC inactive time. Then, the SSC Interface of the TLE5010 is disabled until the next SSC Inactive Time is present.

DATA Write Time (t_{DATW})

During this interval, the TLE5010 changes the data line, thus the data are invalid. The DATA Write Time values are defined without a pull-up resistor.

Pull-up Time Value (t_{PU})

The value in **Table 13 "SSC Timing Specification" on Page 27** is estimated at 60 ns.

Table 13 SSC Timing Specification

Note: Timings must be calculated according to **Table 12 "CLK Timing Specification" on Page 24**

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
SSC Baud Rate	f_{SSC}	-	2.0	2.1 [1)]	MBit / s	
$\overline{CS}$ Setup Time	t_{CSs}	$3*t_{DIG}+10$	-	-	ns	
$\overline{CS}$ Hold Time	t_{CSh}	$5*t_{DIG}+10$	-	-	ns	
$\overline{CS}_{off}$	t_{CSoff}	$10*t_{DIG}$	-	-	ns	SSC inactive time
SCK High	t_{SCKh}	$5*t_{DIG}$	-	-	ns	
SCK Low	t_{SCKl}	$5*t_{DIG}$	-	-	ns	
DATA Read Time (Data Valid Time)	t_{DATr}	$6*t_{DIG}-10$	-	$7*t_{DIG}+10$	ns	SSC_FILT = 0
		$5*t_{DIG}-10$	-	$7*t_{DIG}+10$		SSC_FILT = 1
DATA Write Time (Data Valid Time) [2)]	t_{DATw}	$6*t_{DIG}+25$	-	$7*t_{DIG}+50 + t_{PU}$	ns	
DATA Slope	t_{DATs}	-	20	30 [3)]	ns	Falling edge [4)]

1) $f_{CLK}/2$, synchronized to f_{CLK} if fCLK = f_{CLK}(max)

2) t_{PU} is the time generated by the pull-up resistor

3) Not tested.

4) Internal slope control of falling edge for data bit transition from V_H to V_L.

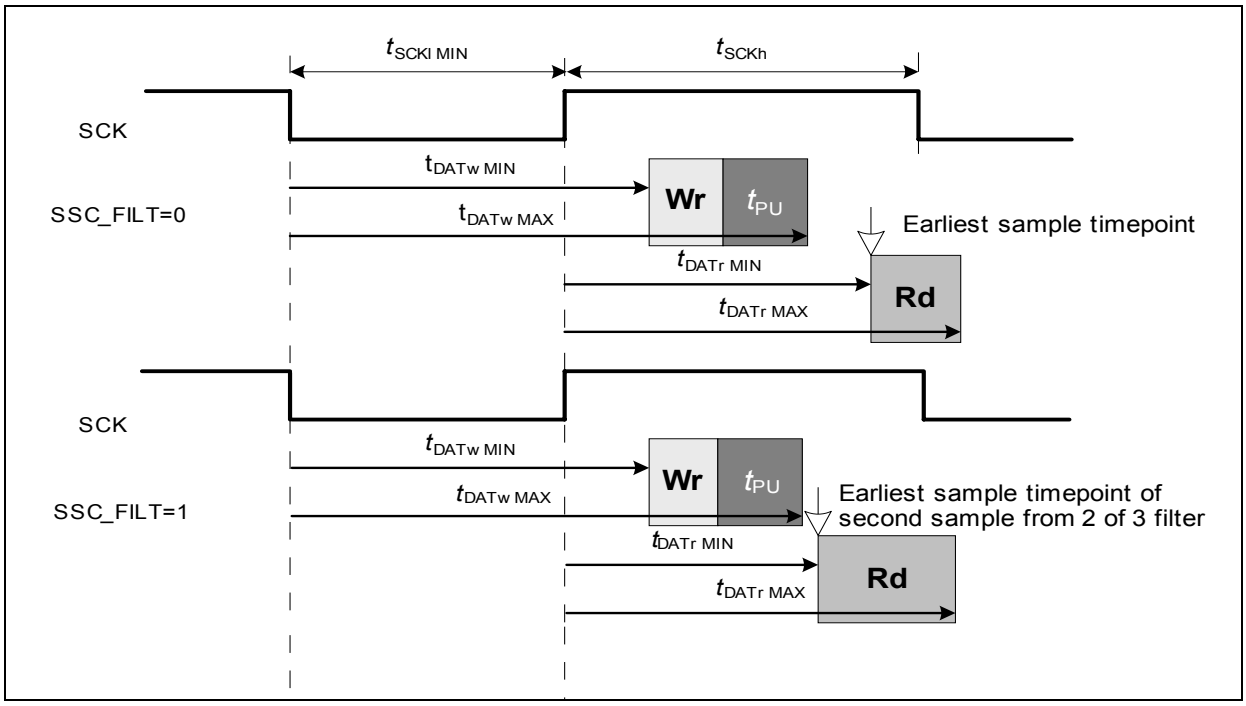


Figure 10 SSC Interface Timing Details—Worst-Case Specified Timing

Note: The read window includes the sampling of the data bit.
For SSC_FILT = 1, the 2-of-3 selection is already considered.
Only the two last data values need to be equal.
For SSC_FILT = 0, only one sample point is selected.

The margin time shown in **Table 14** is the time between write access to the SSC Data Line and the earliest possible sample read of the TLE5010 itself for read back.

It is useful to have a maximum distance between the WRITE and subsequent READ. This ensures a reliable read back of the written data for the Slave-Active Byte generation.

Table 14 Maximum Pull-up Time Margin with Worst-Case Specified Timing

SSC_FILT	SSC_TIMING	Min. t_{PU} Margin [1)]	Unit	Comment
0	don't care	90	ns	
1		50		

1) Calculation: Margin $=t_{SCKl(min)}+t_{DATwMAX}-(t_{PU})-t_{DATrMIN}$. For Margin<50 ns no problems can occur.

8.2 SSC Baud Rate

The SSC Baud rate depends on the internal clock frequency.

12 internal digital clock cycles are necessary to ensure reliable operation. Therefore, the maximum SSC baud rate depends on the external CLK.

$$f_{SSC} = \frac{f_{CLK}}{2}$$

8.3 SSC Spike Filter

A SSC Spike Filter for all SSC lines can be selected via the **SSC_FILT** bit.

8.3.1 SSC Spike Filter Off

When the spike filter is disabled, each slope of a rising voltage is used to define a bit. This is independent of the length of the sampled pulse. For example, a positive spike generates a rising and a falling edge.

8.3.2 SSC Spike Filter On

A sliding window with four consecutive sample bits is analyzed.

The sample frequency is:

$$f_S = \frac{1}{f_{DIGIT}}$$

Rising Edge Detect for SCK

The following conditions apply:

- After a rising edge (LH combination), at least one of the two following samples must be high. *Valid bit combinations: 01**11**, 01**10**, 01**01**.*
- A falling condition must be detected before.

Falling Edge Detect for SCK

The following conditions apply:

- After a falling edge (HL combination), at least one of the two following samples must be low. *Valid bit combinations: 10**00**, 10**01**, 10**10**.*
- A rising condition must be detected before.

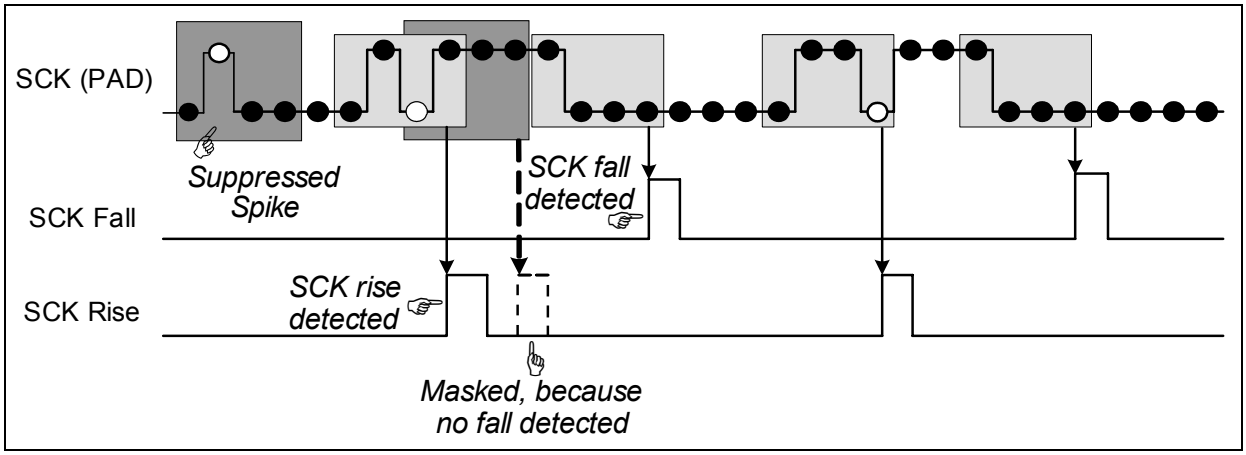


Figure 11 SSC Spike Filter

Filter for DATA and $\overline{CS}$

The following conditions apply:

- The DATA pin has a ’2-of-3’ filter.
- The $\overline{CS}$ input has a ’2-of-3’ filter, which suppresses only positive spikes.

8.4 SSC Data Transfer

The following transfer bytes are possible:

- Command byte (to access and change operating modes of the TLE5010)
- Data bytes (any data transferred in any direction)
- CRC byte (cyclic redundancy check)
- Slave Active byte (response of all selected slaves)

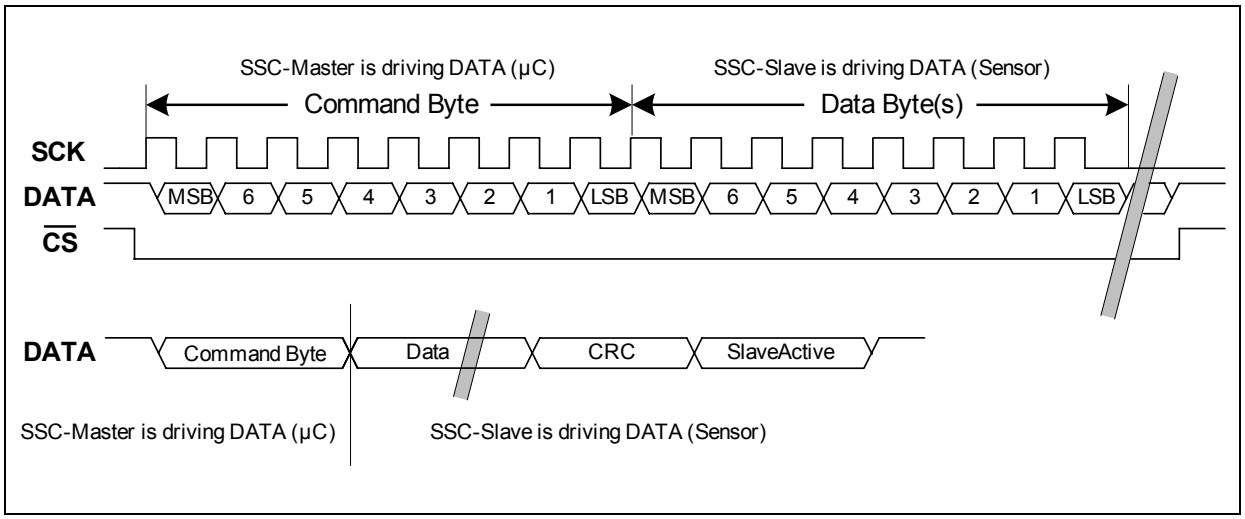


Figure 12 SSC Data Transfer (Data Read Example)

8.5 SSC Command Byte

The TLE5010 is controlled by a command byte. It is sent first at every data transmission.

Table 15 Structure of the Command Byte

Name	Bits	Description
RW	[7]	Read - Write 0 = write, 1 = read
ADDR	[6..3]	Address to be read / written 0..15 = register start address (address auto increment)
ND	[2..0]	Number of data bytes 0..7 = number of data bytes to be transferred

9 Register Table

This chapter defines the complete address range as well as all registers of the TLE5010. It also defines the read/write access rights of the specific registers. **Table 16** identifies the values with symbols. Access to the registers is accomplished via the SSC Interface.

Table 16 Address Map

Addr.	Name	Bits							
		7	6	5	4	3	2	1	0
00_H	CTRL1	-	-	-	-	SSC_ FILT	-	AUTO	UR
01_H	XL	X_{Low}							
02_H	XH	X_{High}							
03_H	YL	Y_{Low}							
04_H	YH	Y_{High}							
05_H	FCNT_ STAT	-	STAT_ VR	GMR_ OFF	UPDATE	FCNT			
06_H	FSYNC_ INV	FILT_ INV	FSYNC						
07_H	ANGT	-	ANGT_ EN	ANGT_Y			ANGT_X		
08_H	-	reserved							
09_H	-	reserved							
$0A_H$	-	reserved							
$0B_H$	-	reserved							
$0C_H$	TST	TEMP_ EN	ADCPY	FILT_ PAR	FILT_ CRS	FILT_ BYP	TST_ ADC	TST_ GMR	TST_ CHAN
$0D_H$	ID	DEV_ID				REV_ID			
$0E_H$	LOCK	LOCK							
$0F_H$	CRTL2	VDD_ OV	VDD_ OFF	GND_ OFF	VRG_ OV	VRA_ OV	VRD_ OV	S_NO	

Bit Types

The types of bits used in the registers are listed here:

Abbreviation	Function	Description
L	Locked	Locked register. Locked registers can be written only when the unlock-value is written in the lock register (**$0E_H$**). This ensures that these bits cannot be modified unintentionally during normal operation.
U	Update	Update-Buffer for this bit is present. In the case of an Update Command and the Update-Mode bit (UR in CTRL1) is set, the immediate values are stored in this Update-Buffer simultaneously. This enables a snapshot of all necessary system parameters at the same time.
S	Status	Reset only after readout
R	Read	Read-only registers
W	Write	Read and write registers

CTRL1
Addr: 00_H **Reset Value: 01_H**

7	6	5	4	3	2	1	0
reserved	**reserved**	**reserved**	**reserved**	**SSC_FILT**	**reserved**	**AUTO**	**UR**
-	-	-	-	W L	-	W L	W L

Field	Bits	Type	Description
reserved	7	-	Reserved, must be set to 0
reserved	6	-	Reserved, must be set to 0
reserved	5	-	Reserved, must be set to 0
reserved	4	-	Reserved, must be set to 0
SSC_FILT	3	W L	SSC Digital Spike Filter enable for all SSC lines ($\overline{CS}$, CLK and DATA) 0: Digital SSC Spike filters off 1: Digital SSC Spike filters on (modified timing)
reserved	2	-	Reserved, must be set to 0
AUTO	1	W L	Automatic update at angle tests 0: no automatic update in Angle Test Mode 1: automatic update-command after t_{settle}, counters FSYNC and FCNT are reset to 0. Then, the Angle-Test (ANGT_EN) is automatically disabled and switches back to normal operation. Also, the UPDATE bit is toggled
UR	0	W L	Update/Run Mode 0: Run Mode (Buffer1 values are immediate values) 1: Update Mode (Buffer2 values are stored values)

The values in Register 01H to 04H represent one byte of two's complement signed 16-bit integer values.

X_L
Addr: 01_H **Reset Value: 00_H**

7	6	5	4	3	2	1	0
X Low Byte							
R	U						

X_H
Addr: 02_H **Reset Value: 00_H**

7	6	5	4	3	2	1	0
X High Byte							
R	U						

Y_L
Addr: 03_H **Reset Value: 00_H**

7	6	5	4	3	2	1	0
Y Low Byte							
R	U						

Y_H
Addr: 04_H **Reset Value: 00_H**

7	6	5	4	3	2	1	0
Y High Byte							
R	U						

FCNT_STAT
Addr: 05_H **Reset Value: 80_H**

7	6	5	4	3	2	1	0
reserved	STAT_VR	GMR_OFF	UPDATE	FCNT			
-	R S	R U	R S	R U			

Field	Bits	Type	Description
reserved	7	-	
STAT_VR	6	RS	Voltage Regulator Status This bit is a logical OR combination of Digital, Analog, GMR and VDD_{OV} Comparator and GND_{OFF}, and VDD_{OFF} Comparator outputs. 0: Voltage Supply is OK 1: Voltage Supply is not OK
GMR_OFF	5	RU	ADC Values are not GMR values (e.g.: Temperature measurement is active) This bit indicates whether GMR values or any other values are connected to the ADCs. This value is read back from the multiplexer control signals. 0: X,Y Values are GMR values 1: X,Y Values normally represent temperature measurement or angle test values. In the case of non-functional MUX, this bit is set to 1
UPDATE	4	RU	Update Toggle bit. This bit toggles after every update (update command or automatic update at angle test) The bit is independent of the UR bit in CTRL1
FCNT	3-0	RU	Frame Counter (4- bit unsigned integer value) This counter counts every new X,Y value pair coming out of the data path. (approx. 80 µs) This counter is reset to 0_H after any write to FSYNC and after every change of the ANGT_EN bit. As t_{settle} time has to be waited for valid X,Y data, this counter must be $\geq 2_H$ to indicate valid X,Y values. If it overflows, it resets to 3_H to show, that values are still valid. *Note: If FIR_BYP is activated, this counter counts four times faster!*

FSYNC_INV

Addr: 06_H **Reset Value: 00_H**

7	6	5	4	3	2	1	0
FILT_INV	**FSYNC**						
WU	WU						

Field	Bits	Type	Description
FILT_INV	7	WU	Filter Input Inversion (to check the digital data path during operation) 0: Filter Inputs are not inverted 1: Filter Inputs are inverted
FSYNC	6-0	WU	Frame Synchronization (7bit unsigned integer value) The Filter Update time of approx. 80 µs results from the filter decimation. The phase of this decimation can be set and checked by this counter. If FIR_BYP is activated, this counter overflows at the value 31_D.

ANGT

Addr: 07_H **Reset Value: 00_H**

7	6	5	4	3	2	1	0
reserved	**ANGT_EN**	**ANGT_Y**			**ANGT_X**		
-	W	W			W		

Field	Bits	Type	Description
reserved	7	-	reserved, has to be set to 0
ANGT_EN	6	W	Angle Test Enable 0: Angle Test disable command 1: Angle Test enable command in this case X and Y values represent resistive test values, which can be used to simulate angle values
ANGT_Y	5-3	W	Angle Test X and Y value See: **Table 17 "Functional Angle Test" on Page 45**
ANGT_X	2-0	W	

Reserved Registers (08_H to $0B_H$)

The values in these registers are 8-bit unsigned integer values.

The values in addr.8 and addr.9 must be in reset status.

Reserved
Addr: 08_H **Reset Value: FF_H**

7	6	5	4	3	2	1	0
Reserved							

Reserved
Addr: 09_H - $0B_H$ **Reset Value: 00_H**

7	6	5	4	3	2	1	0
Reserved							

TST
Addr: $0C_H$ **Reset Value: 00_H**

7	6	5	4	3	2	1	0
TEMP_EN	**ADCPY**	**FILT_PAR**	**FILT_CRS**	**FIR_BYP**	**TST_ADC**	**TST_GMR**	**TST_CHAN**
W L	W L	W L	W L	W L	W L	W L	W L

Field	Bits	Type	Description
TEMP_EN	7	W L	Temperature Device Enable 0: Temperature Measurement disabled 1: Temperature Measurement enabled The X value represents the temperature. Automatic update mode enabled, if AUTO='1'
ADCPY	6	W L	Y Polarity 0: No inversion of Y bit stream 1: Inversion of Y bit stream (rotating direct. changed)
FILT_PAR	5	W L	Filter switched parallel 0: Filters in normal mode 1: Filters parallel, input selected by TST_CHAN
FILT_CRS	4	W L	Filter switched across 0: Filters in normal mode 1: Filters crossed, X and Y outputs are exchanged
FIR_BYP	3	W L	FIR Filter Bypass 0: No FIR Bypass 1: FIR Bypass
TST_ADC [1)]	2	W L	ADC input switch to TST1and TST2 0: No ADC input switch, normal operation 1: ADC input switched to TST1,2, ADC selected by TST_CHAN [2)]
TST_GMR [1)]	1	W L	GMR switch to TST1and TST2 0: No GMR switch, normal operation 1: GMR switched to TST1,2 [2)]
TST_CHAN	0	W L	Test Channel select 0: X channel linked to TST1and TST2 1: Y channel linked to TST1and TST2

1) Only for test purposes

2) if TST_ADC and TST_GMR are set to 1 at the same time, TST_GMR is forced to 0. TST_ADC has the higher priority.

ID

Addr: $0D_H$ **Reset Value: 12_H**

7	6	5	4	3	2	1	0
DEV_ID				DEV_REV			
R				R			

Field	Bits	Type	Description
DEV_ID	7-4	R	Device Identifier 001_H: TLE5010 productive chip
DEV_REV	3-0	R	Device Revision (current number) 00_H: TLE5010 productive chip, 1st revision (B11) 01_H: TLE5010 productive chip, 2nd revision (B21) 02_H: TLE5010 productive chip, 3rd revision (B31) 03_H: TLE5010 productive chip, 4th revision (B41) (Refer to Errata Sheets for later versions)

LOCK

Addr: $0E_H$ **Reset Value: 00_H**

7	6	5	4	3	2	1	0
LOCK							
W							

Field	Bits	Type	Description
LOCK	7-0	W	Lock Byte $\neq 5A_H$: Lock registers locked $= 5A_H$: Lock registers unlocked

CTRL2

Addr: $0F_H$ **Reset Value: 00_H**

7	6	5	4	3	2	1	0
VDD_OV	VDD_OFF	GND_OFF	VRG_OV	VRA_OV	VRD_OV	S_NO	
R S	R S	R S	R S	R S	R S	W L	

Field	Bits	Type	Description
VDD_OV	7	R S	V_{DD} Overvoltage Comparator 0: No V_{DD} Overvoltage occurred 1: V_{DD} Overvoltage occurred
VDD_OFF	6	R S	V_{DD} - Off Comparator 0: No V_{DD} - Off occurred 1: V_{DD} - Off occurred
GND_OFF	5	R S	GND - Off Comparator 0: No GND - Off occurred 1: GND - Off occurred
VRG_OV	4	R S	GMR Voltage Regulator Overvoltage Comparator 0: Voltage ok 1: VRG Overvoltage occurred
VRA_OV	3	R S	Analog Voltage Regulator Overvoltage Comparator 0: Voltage ok 1: VRA Overvoltage occurred
VRD_OV	2	R S	Digital Voltage Regulator Overvoltage Comparator 0: Voltage ok 1: VRD Overvoltage occurred
S_NO	1-0	W L	Slave Number Used in the SSC protocol

10 Data Communication via SSC

Data communication via the SSC Interface has the following characteristics:

- The data transmission order is “Most Significant Bit (MSB) first”.
- Data is put on the data line with the rising edge on SCK and read with the falling edge on SCK.
- The SSC Interface is byte-aligned. All functions are activated after each transmitted byte.
- A “high” condition on the negated Chip Select pin ($\overline{CS}$) of the selected TLE5010 interrupts the transfer immediately. The CRC calculator is automatically reset.
- Every access to the TLE5010 with the number of data (ND) ≥ 1 is performed with address auto-increment.
- After an auto-increment overflow, the addresses begin again from 00_H.
- For every data transfer with ND ≥ 1, an 8-bit CRC byte will be appended by the selected TLE5010. No CRC byte is sent in a data transfer with ND = 0 (e.g. Update Command).
- After the CRC byte is sent, the bit represented by S_NO is pulled low by the selected slave in the Slave-Active-Byte (bits [3..0], low nibble). In this way, broadcast-messages also produce individual feedback of every selected slave. This is necessary to differentiate the individual TLE5010 slave responses, because the CRC byte is written by both TLE5010 devices in parallel.
- If the CRC byte on the bus is the same as the internally generated CRC of each TLE5010, each slave pulls the dedicated bit in the Slave-Active-Byte (bits [7..4], high nibble) low. If not, the bit in the high nibble remains 1.
- A write command to address 00_H with ND = 0 will update all values inside the TLE5010, and only in this case can the transfer proceed. Furthermore, this command is added to the CRC-calculation of the following SSC Transfer.
- A command of 0000_0000 is called the **Update Command**.
  This command transfers the present immediate values of each register to the update register. After an Update Command, the $\overline{CS}$ line does not need to set and reset again.
- The transfer ends after the CRC and Slave-Active byte have been sent.
  The TLE5010 always sends logical 1 and all the following bits sent from the SSC Master are ignored (TLE5010 is in Idle Mode). To enable data transfers again, the Chip Select pin ($\overline{CS}$) of the TLE5010 must be deselected for $\overline{CS}_{off}$ (see **Table 13**) once.
- If Update Mode is selected (CTRL register, UR = 1), all accesses are performed to update registers where update registers are present. Other registers are accessed directly.

10.1 CRC Generation

This section identifies the requirements for CRC generation:

- This CRC is defined according to the *J1850* Bus-Specification of 15.Feb.1994 for Class B Data Communication.
- Every new transfer resets the CRC generation.
- Every byte of a transfer will be taken into account to generate the CRC (also the sent command(s)).
- Generator Polynomial: X8+X4+X3+X2+1, the fast CRC generation circuit is used for CRC generation. (See **Figure 13**)
- The remainder of the fast CRC circuit is initially set to 11111111_B.
- The remainder is bit inverted before transmission.

Figure 13 shows the fast CRC Polynomial.

The zero extension for initial CRC calculation is included!

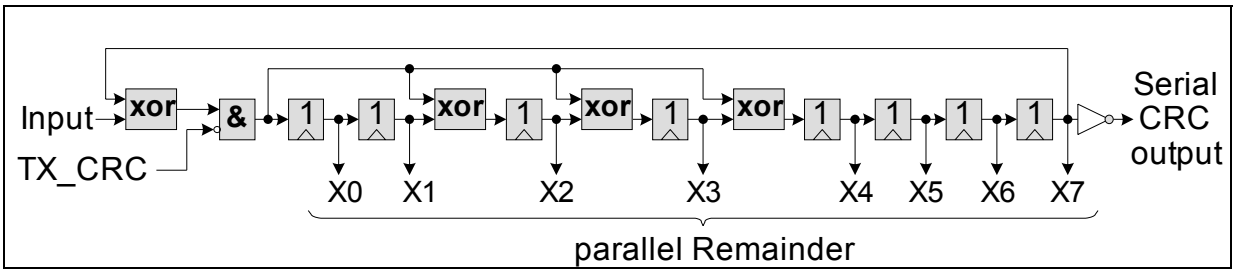


Figure 13 Fast CRC Polynomial Division Circuit

10.2 Slave Active Byte Generation

The position of the 0 in a nibble corresponds to the given slave number.

The slave active byte (cccc_nnnn) consists of:

- **low nibble** (nnnn). One 0 is generated always according to the slave number.
- **high nibble** (cccc). The 0 is only generated, if the readback CRC is correct.

Slave1: S_NO = 0 ⇨ bit 0 is pulled low Slave Active Byte: 1110_1110

Slave2: S_NO = 1 ⇨ bit 1 is pulled low Slave Active Byte: 1101_1101

Slave3: S_NO = 2 ⇨ bit 2 is pulled low Slave Active Byte: 1011_1011

Slace4: S_NO = 3 ⇨ bit 3 is pulled low Slave Active Byte: 0111_0111

Example for a communication disturbed by other bus participants:

Slave1: S_NO = 0 ⇨ bit 0 is pulled low, but the high nibble remains as 1111.
> Slave Active Byte: 111**1**_1110

Example: Update X and Y and set ADC-Test Mode

```
    Command     Data      CRC (init all '0')
    00000001    00000101  00000000
    ---------------------------------
xor 11111111
    --------
   =11111110.0        .         .A
xor 10001110.1        .         .
    --------.-        .         .
  = 01110000.10       .         .B
 xor 1000111.01       .         .
     -------.--       .         .
   = 0110111.110      .         .C
  xor 100011.101      .         .
      ------.---      .         .
     = 10100.0110     .         .D
   xor 10001.1101     .         .
       -----.----     .         .
     = 00101.101101   .         .E
     xor 100.011101   .         .
         ---.------   .         .
       = 001.11000001.         .F
       xor 1.00011101.         .
         ---.------   .         .
           =.11011100.0        .G
         xor.10001110.1        .
            .--------.-        .
           = 1010010.10        .H
          xor 1000111.01       .
              -------.-        .
            = 10101.1100       .I
           xor 10001.1101      .
               ----.-----      .
             = 100.000100      .J
           xor 100.011101      .
               ---.------      .
                  =01100100. Remainder
                   10011011  inverted Remainder
Transmitted Sequence:
Command  Data     CRC
00000001 00000101 10011011
```

11 Test Structures

Two different test signal structures are implemented in the TLE5010. These are:

- Functional Angle Test. In this case, well-known signals feed the ADCs.
- Temperature Measurement. This is useful to read out the chip temperature for compensation purposes.

11.1 Functional Angle Tests

It is possible to feed the ADCs with appropriate values to simulate a certain magnet-position and other GMR effects.

The values are generated with resistors on the chip.

The following X / Y ADC values can be programmed:

- 4 points, circle amplitude = 70.7%
  (0°, 90°, 180°, 270°)
- 8 points, circle amplitude = 100.0%
  (0°, 45°, 90°, 135°,180°, 225°, 270°, 315°)
- 8 points, circle amplitude = 122.1%
  (35.3°, 54.7°, 125.3°, 144.7°, 215.3°, 234.7°, 305.3°, 324.7°)
- 4 points, circle amplitude = 141.4%
  (45°, 135°, 225°, 315°)

Note: The 100% values typically correspond to 21700 digits and a voltage of ~ 110 mV.

Table 17 Functional Angle Test

Register Bits	X / Y Values (decimal)		
	min.	**typ.**	**max.**
000	-400	0	400
001	14800	15500	16200
010	20700	21700	22700
011	32767		
100 [1)]	-400	0	400
101	-14800	-15500	-16200
110	-20700	-21700	-22700
111	-32768		

1) Not allowed to use.

ADC Test Vectors

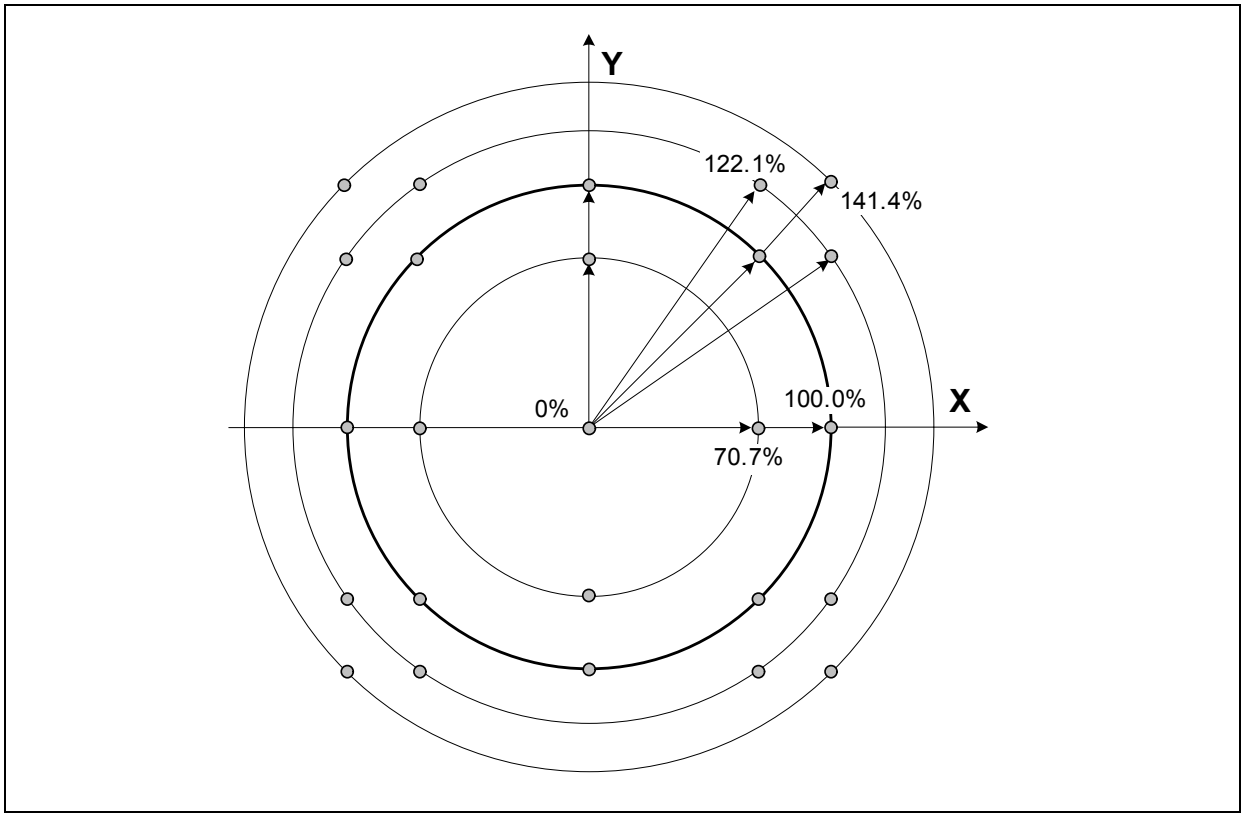


Figure 14 ADC Test Vectors

11.2 Temperature Measurement

An internal bandgap voltage can be used to measure the temperature on the chip. This may be used to compensate for temperature-dependent errors.

The temperature value is sent out instead of the X value.

Table 18 Temperature Measurement

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Value at -40°C	T_{-40}	-	-	+22000	digits	
Value at 25°C	T_{25}	+2550	+5775	+9000	digits	
Value at 150°C	T_{150}	-22000	-	-	digits	
Temperature Sensitivity	S_T	-	-188.75	-	dig / K	1)

1) Should be used for temperature compensation of offset errors

11.3 Angle Test and Temperature Measurement Timing

The angle test and the temperature readout is based on the same mechanism.

In Normal Mode, the output path is linked to the angle test or to the temperature measurement unit until the mode is terminated.

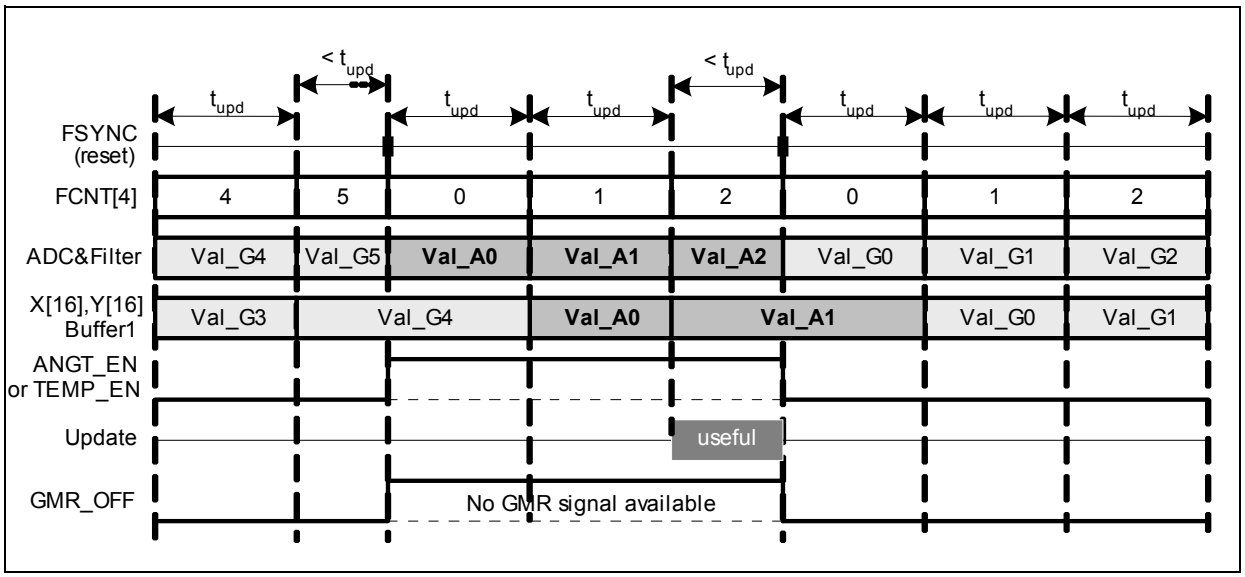


Figure 15 Measurement in Normal Mode

In Automatic Mode, the signal is automatically switched back to GMR measurement after the read-out of one value.

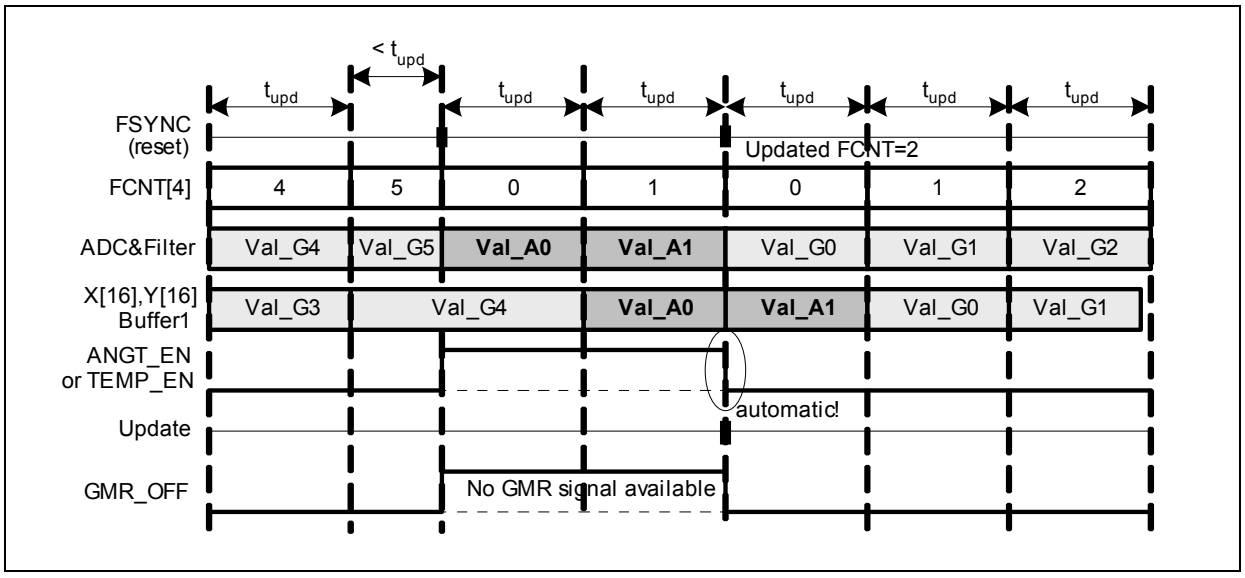


Figure 16 Measurement in Automatic Mode

12 Overvoltage Comparators

Various comparators monitor the voltage in order to ensure error free operation.
The overvoltages must be active for at least t_{DEL} to set the test comparator bits in the SSC Interface registers. This works as digital spike suppression.

Table 19 Test Comparators

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Overvoltage Detection	V_{OVG}	-	2.80	-	V	
	V_{OVA}	-	2.80	-	V	
	V_{OVD}	-	2.80	-	V	
V_{DD} Overvoltage	V_{DDOV}	-	6.5	-	V	
GND - Off Voltage	V_{GNDoff}	-	0.54	-	V	$V_{GND\_OFF} = V_{GND} - V_{TST1}$
V_{DD} - Off Voltage	V_{VDDoff}	-	0.48	-	V	$V_{VDD\_off} = V_{CLK} - V_{DD}$ or $V_{SCK} - V_{DD}$
Spike Filter Delay	t_{DEL}	-	10	-	µs	The error condition must be longer than this value (min. 256 clocks of f_{DIG})

12.1 Internal Supply Voltage Comparators

Every voltage regulator has an overvoltage comparator to detect a malfunction.
If the nominal output voltage of 2.5 V is larger than V_{OVG}, V_{OVA} and V_{OVD}, then this overvoltage comparator is activated. It sets the VRx_OV bit.

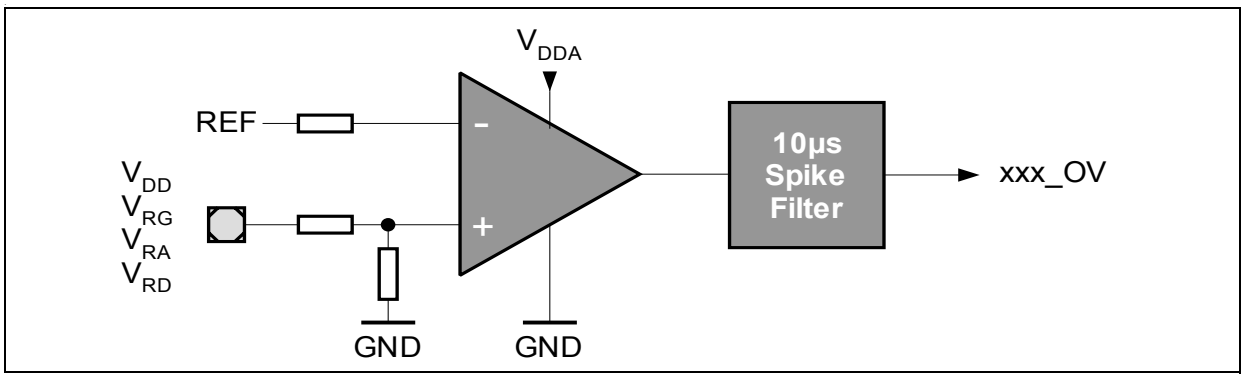


Figure 17 OV Comparator

12.2 V_{DD} Overvoltage Detection

The Overvoltage Detection Comparator monitors the external supply voltage at the V_{DD} pin. It activates the $STAT\_VR$ bit. (See **Figure 17**)

12.3 GND–Off Comparator

The GND–Off Comparator is used to detect a voltage difference between the GND pin and TST1 (which must be soldered to GND in the application). It activates the *STAT_VR* bit. This circuit can detect a disconnection of the Supply GND Pin.

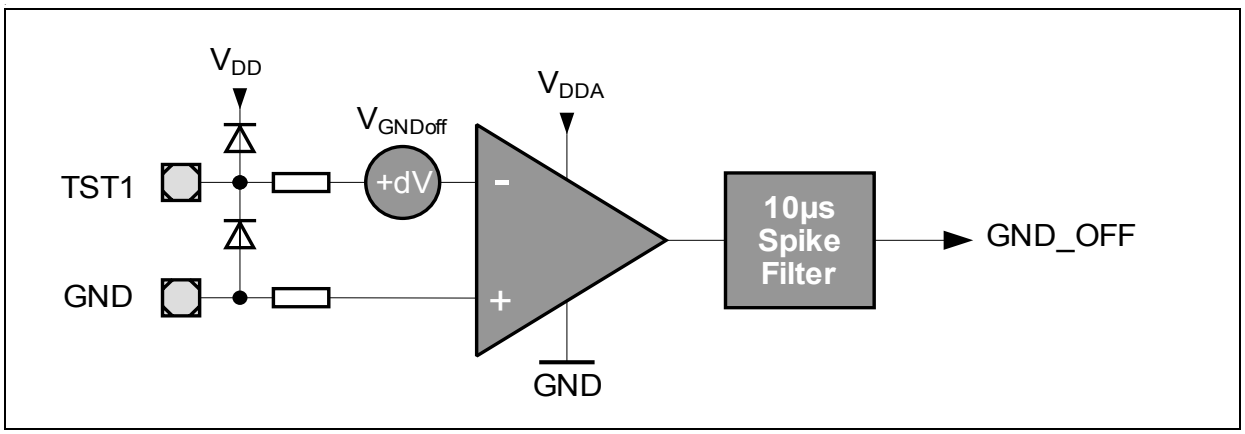


Figure 18 GND–Off Comparator

12.4 V_{DD}–Off Comparator

The V_{DD}– Off Comparator detects a disconnection of the V_{DD} pin supply voltage. In this case, the TLE5010 is supplied by the SCK, CLK and $\overline{CS}$ input pins via the ESD structures. It activates the *STAT_VR* bit.

The retriggerable analog monoflop is necessary because of the non-static signal of the CLK and SCK signals.

This comparator is also activated if spikes on CLK or SCK achieve the condition:

$(V_{CLK} - V_{DD}) > V_{VDDoff}$ or $(V_{SCK} - V_{DD}) > V_{VDDoff}$

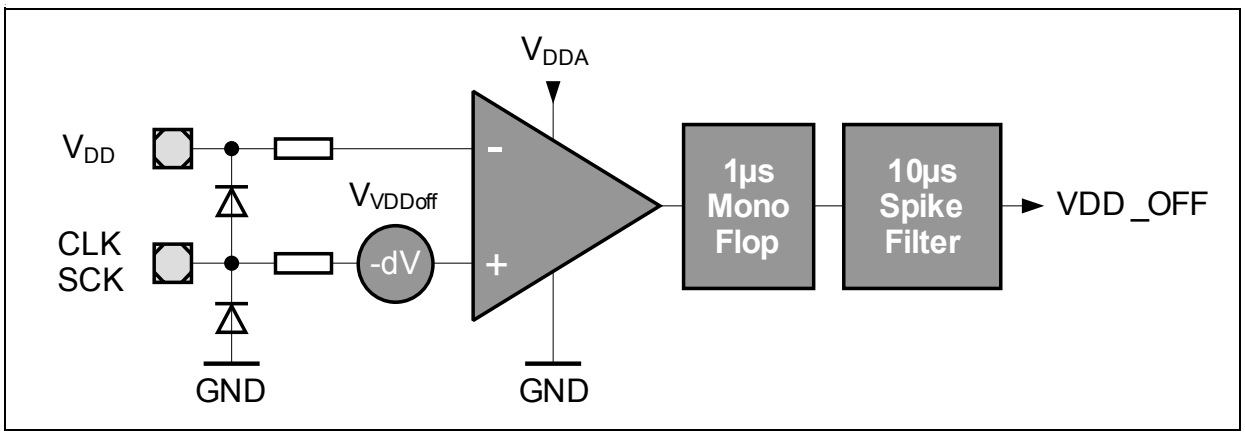


Figure 19 V_{DD}–Off Comparator

13 Typical Application Circuit

The application circuit shows the microcontroller version with Open Drain capabilities.

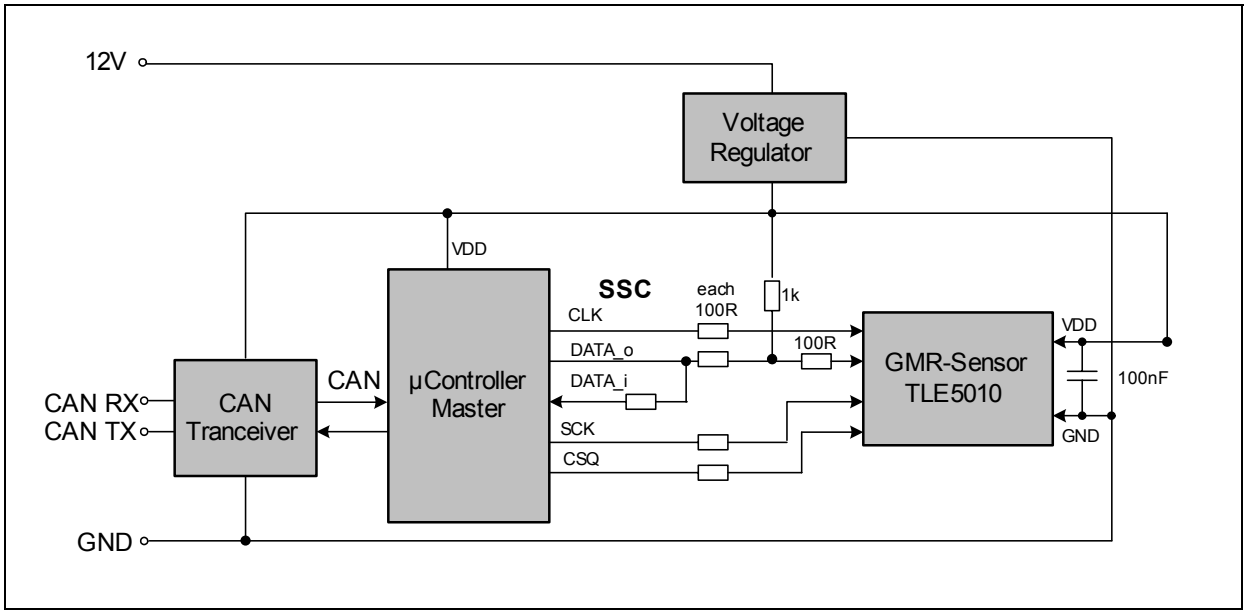


Figure 20 Application Circuit

13.1 Angle Sensor System

A complete system may consist of one TLE5010 and a microcontroller. A second TLE5010 may be used for redundancy to increase system reliability. The microcontroller should contain a CORDIC coprocessor for fast angle calculations and flash memory for the calibration data storage.

14 Package Information

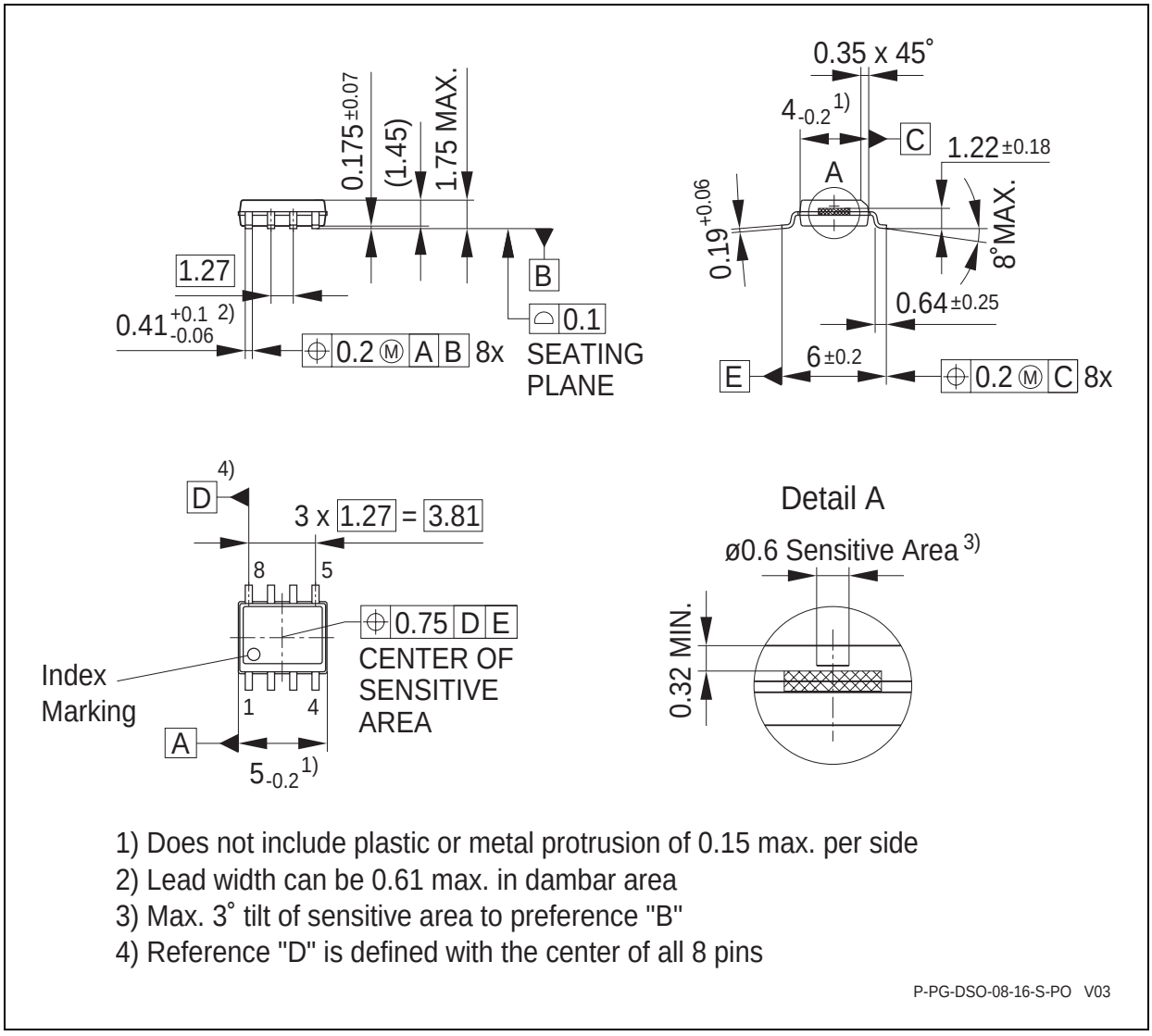
14.1 Package Parameters

Table 20 Package Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Thermal Resistance	R_{thJA}	-	150	200	K/W	Junction to Air [1]
	R_{thJC}	-	-	75	K/W	Junction to Case
	R_{thJL}	-	-	85	K/W	Junction to Lead
Soldering Moisture Level	MSL 3					260°C
Lead frame	Cu194 / OLIN					
Plating	Sn 100%					> 7 µm

[1] According to Jedec JESD51-7

Package Outline PG-DSO-8



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area
3) Max. 3° tilt of sensitive area to preference "B"
4) Reference "D" is defined with the center of all 8 pins

P-PG-DSO-08-16-S-PO V03

Figure 21 Package Outline PG-DSO-8

Footprint PG-DSO-8

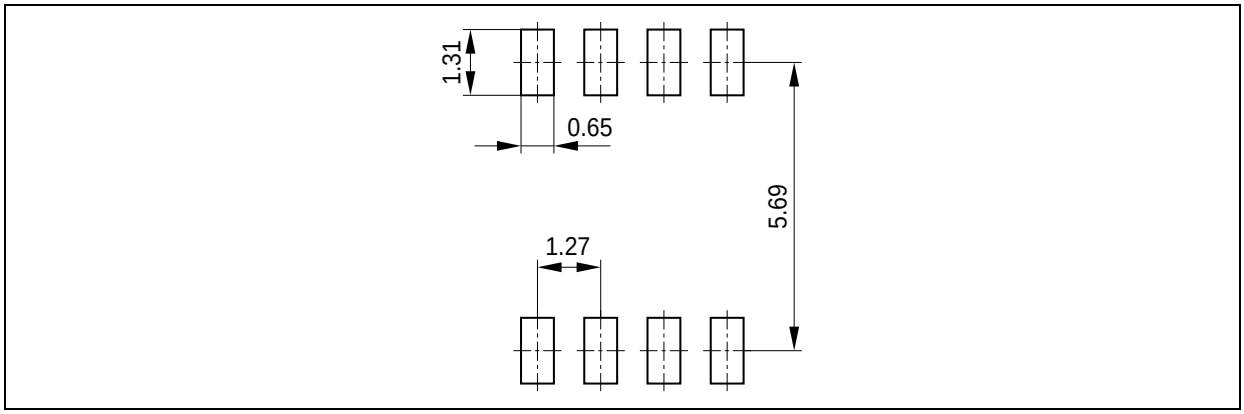


Figure 22 Footprint PG-DSO-8

Packing

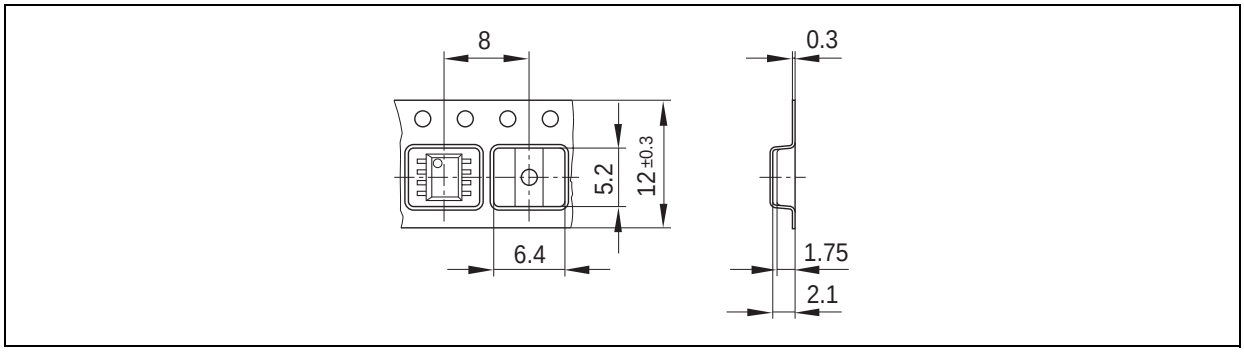


Figure 23 Tape and Reel

Marking

Position	Marking	Description
1st Line	*5010xx*	See ordering table on page 6
2nd Line	*xxx*	Lot code
3rnd Line	*Gxxxx*	G .. green, 4-digit .. date code

Processing

Note: For processing recommendations, please refer Infineon's Notes on Processing

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