Carlos Lemus
11/27/2016
Buck Converter Report

The goal of this project was to produce a buck converter that would regulate an output with various loads and temperature. In this case, the output should regulate at 2.5V.

1. To Simulate

a. To simulate buck converter
    i. Access the sim_buck_converter spectre_state 1
        1. This is only one simulate with one temperature and one power supply
b. To simulate comparator alone
    i. Access the sim_comparator spectre_state1
c. To simulate comparator with buffer
    i. Access the sim_converter_buffer1
d. To simulate SR latch
    i. Access the sim_sr_latch spectre_state1

2. Efficiency

The tables below show the best demonstration of how well the system works. Efficiency can be calculated using

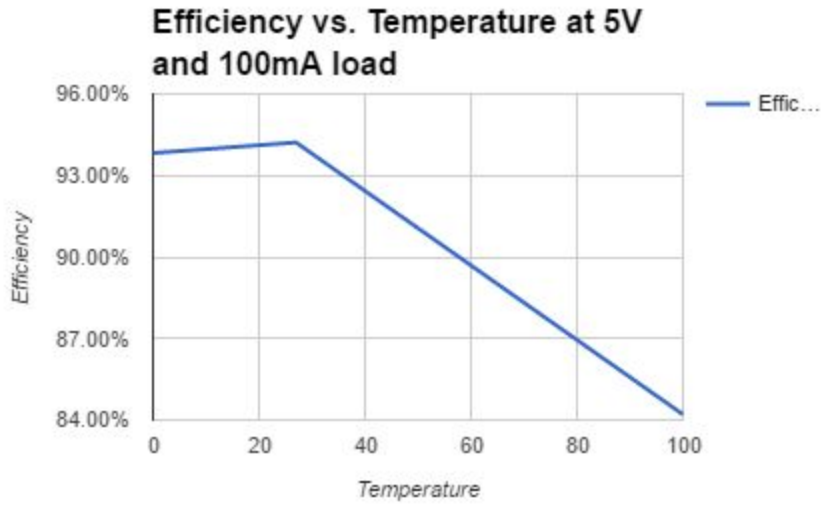
$$\varepsilon = \frac{Vout * I_{load}}{Vdd * Average(I(VDD))}$$

But the efficiency was also calculated using RMS. Some confusion among this part, because according to the formula as the power supply goes down the efficiency should go up. However, it shows reverse of that. This could be because the average of the current goes higher as the power supply drops. A 100mA load was tested to show that the device works best when supplying the max load.

At a Power supply of 4V			
Temperature (Celcius)	Current Load(Amps DC)	Efficiency using Average	Efficiency using RMS
0	100m	78.98%	55.36%
27	100m	75.22%	53.28%
100	100m	68.16%	51.02%

A 1m load was thrown on the end of this table to show that a small load will cause a very low efficiency because there is nothing to drive.

At a Power supply of 5V			
Temperature (Celcius)	Current Load(DC)	Efficiency using Average	Efficiency using RMS
0	100m	93.83%	65.30%
27	**100m**	**94.22%**	**65.66%**
100	100m	84.03%	56.98%
100	1m	38.64%	0.01%

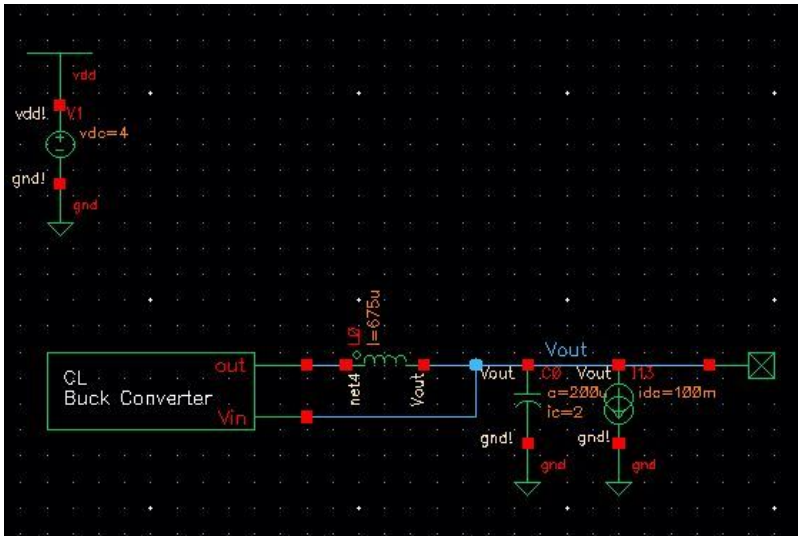


At a Power supply of 5.5V			
Temperature (Celcius)	Current Load(DC)	Efficiency using Average	Efficiency using RMS
0	100m	93.05%	61.68%
27	100m	93.18%	61.91%
100	100m	94.46%	62.77%

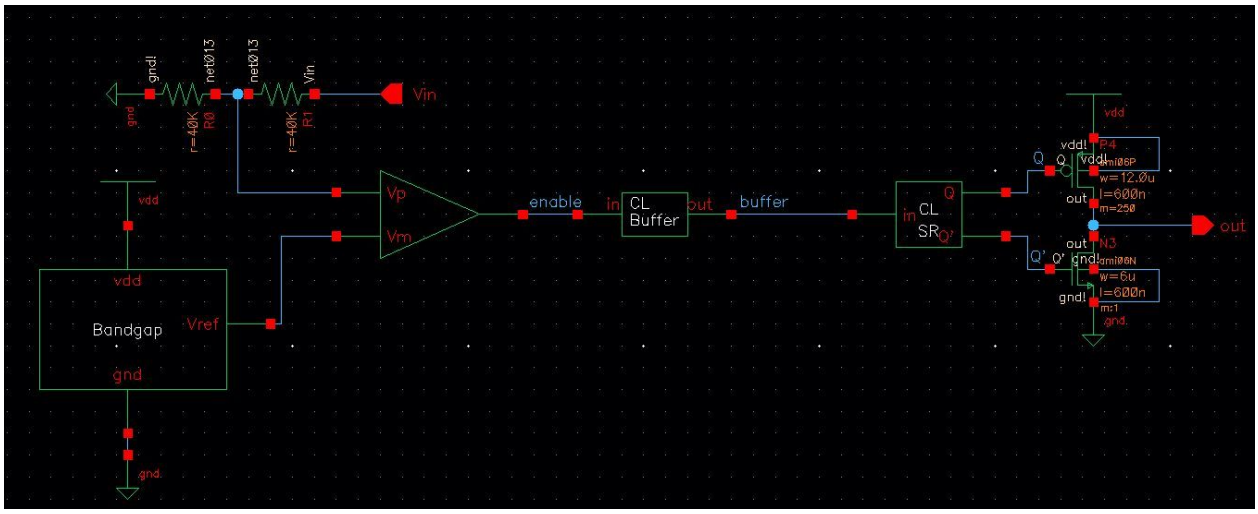
3. Overview

Simulations were ran using this schematic.

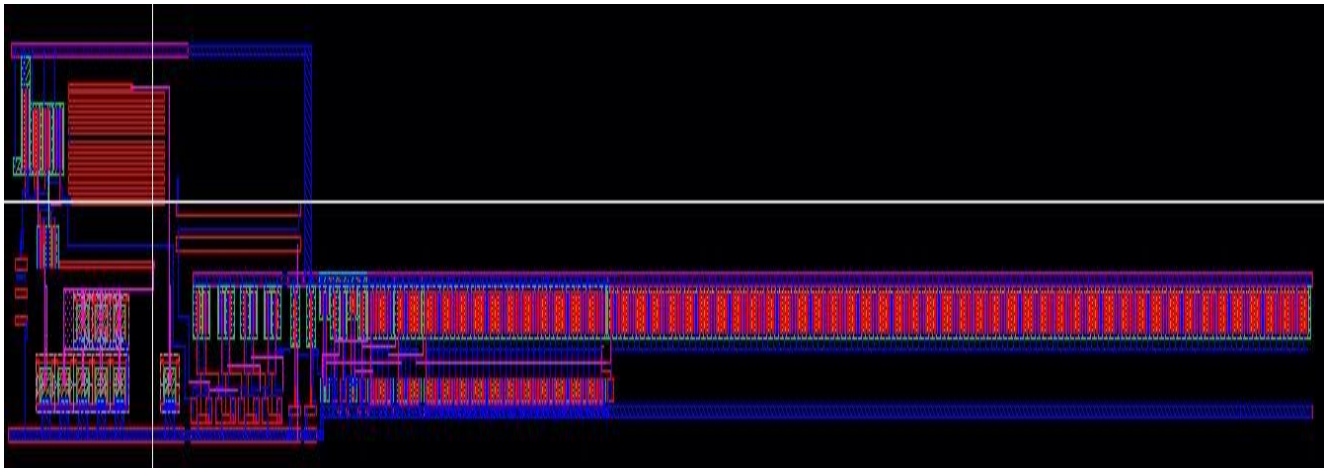
Carlos Lemus
11/27/2016
Buck Converter Report



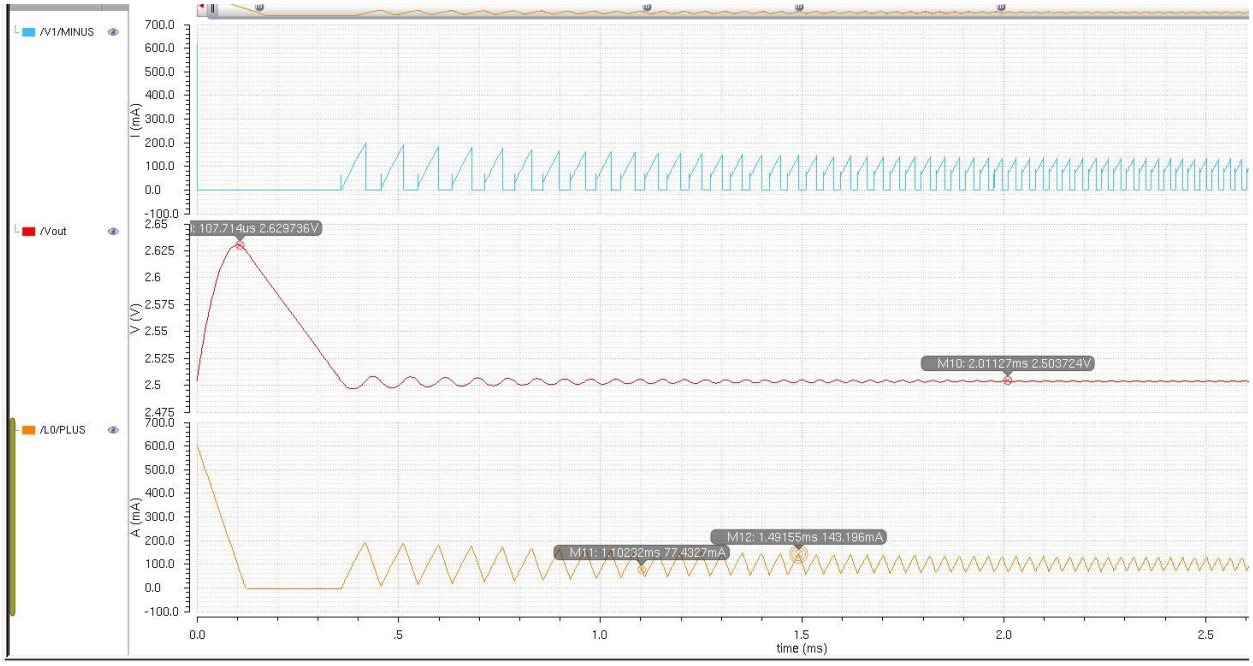
The schematic is examined from left to right, each which are explained individually. Components shown are the bandgap, the comparator, buffers, a clock control SR latch, a PMOS and NMOS switches, and a inductor, capacitor, and different loads (off chip) which lead back through a divider to the operator.



A layout shows all of the components of the chip together. Components will be shown separately.

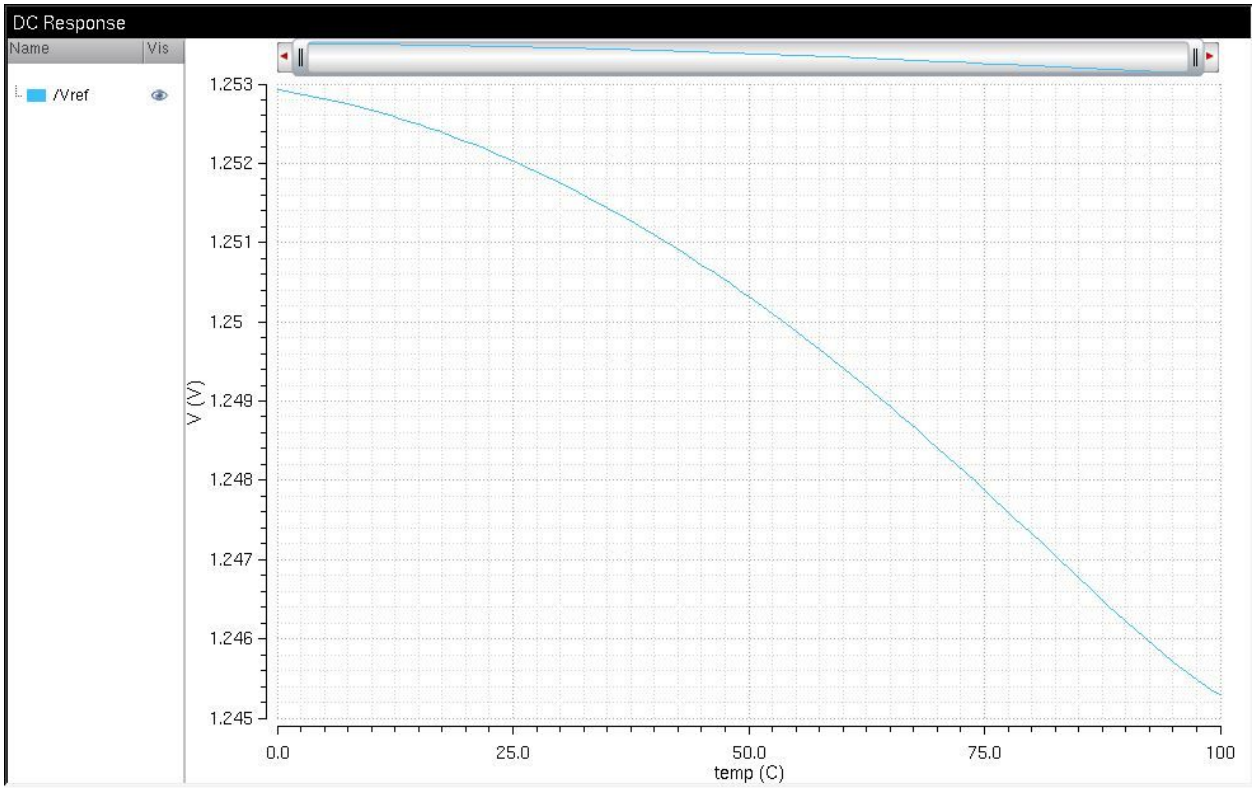


Simulations at 5V and 27C show low ringing, and a steady state of 2.5 Vout. The current through the inductor also shows <100mA

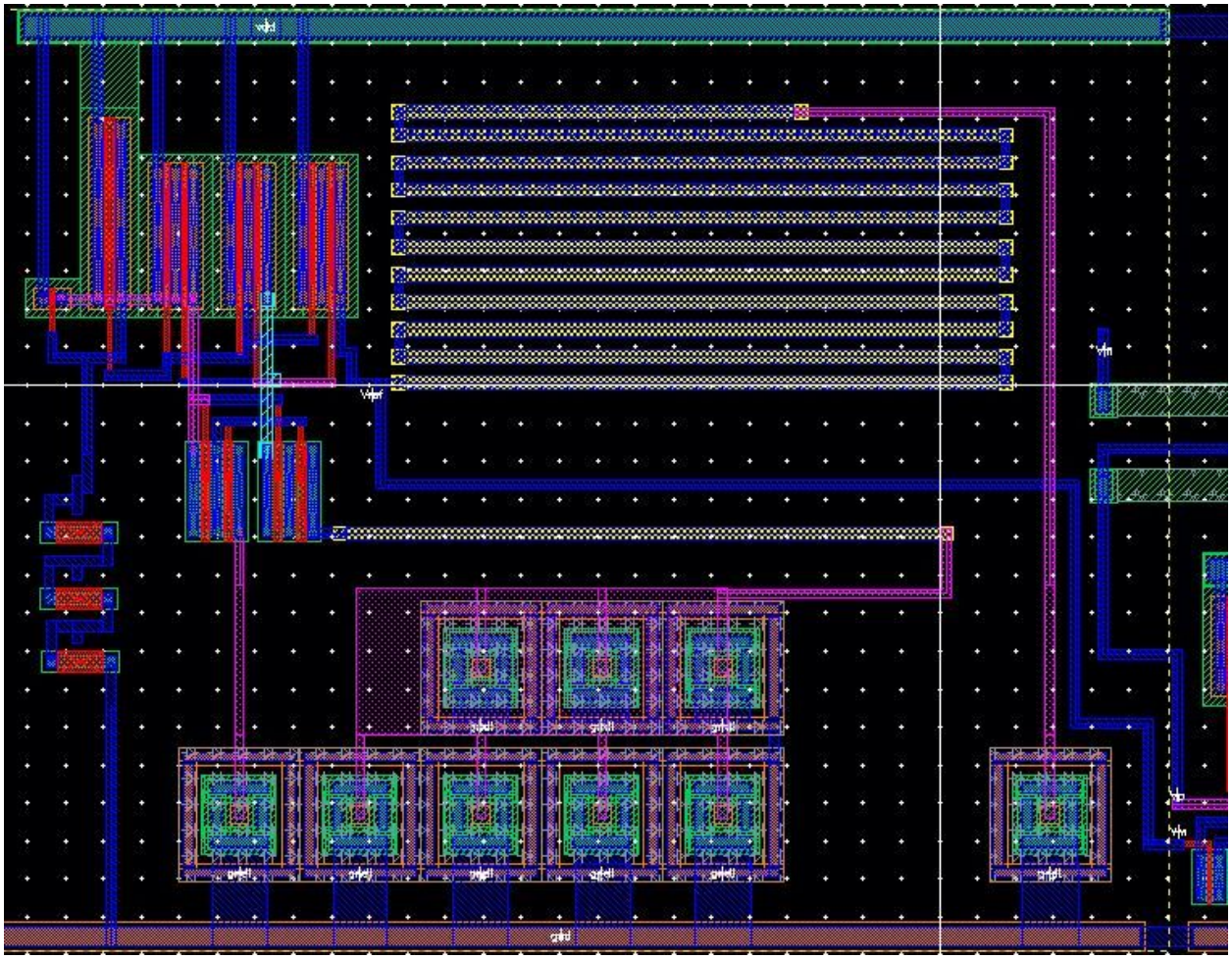


4. Bandgap

The bandgap is a device that outputs a set voltage (in this case 1.25V) and very little with changes in temperature and power supplies. The plot below shows the small changes in the bandgap output with changes in temperature.



Though the band gap was provided, the layout was put together and shows the first part of the buck converter. Vref (which outputs the 1.25) is connected to Vp of the Comparator.



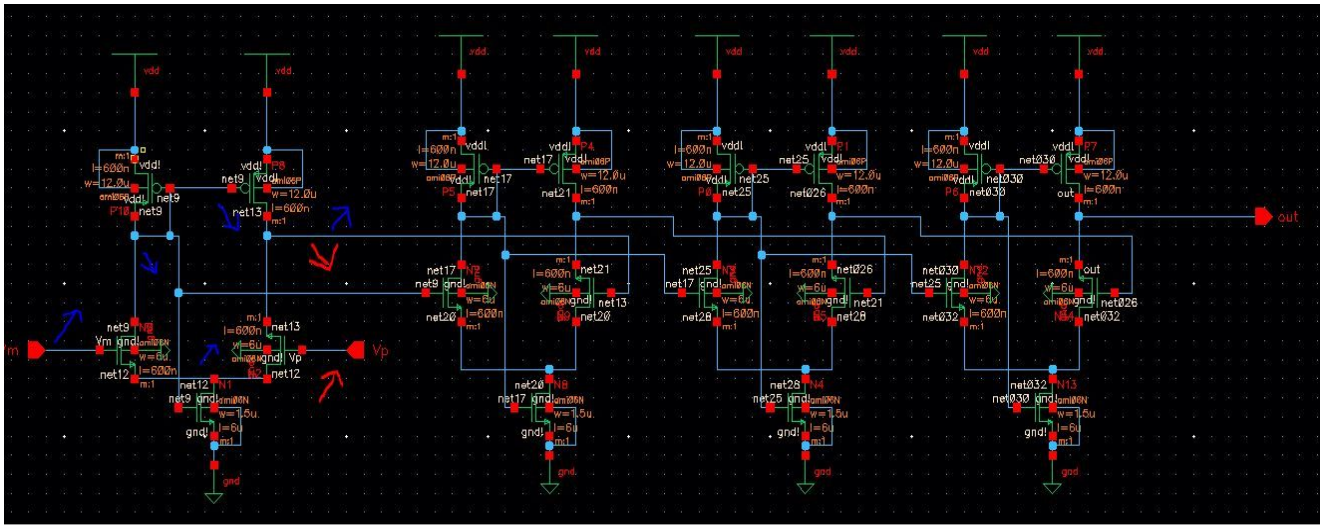
5. Comparator

The comparator is the next step in the buck converter. **This takes the value that is fed back through a divider to the Vm (negative terminal) and compares it to Vp (positive terminal, bandgap voltage reference).** It needs to go through a divider, in this case a 40k/40k divider, to half the output voltage of 2.5 to 1.25 and be able to compare it to the bandgap voltage reference 1.25.

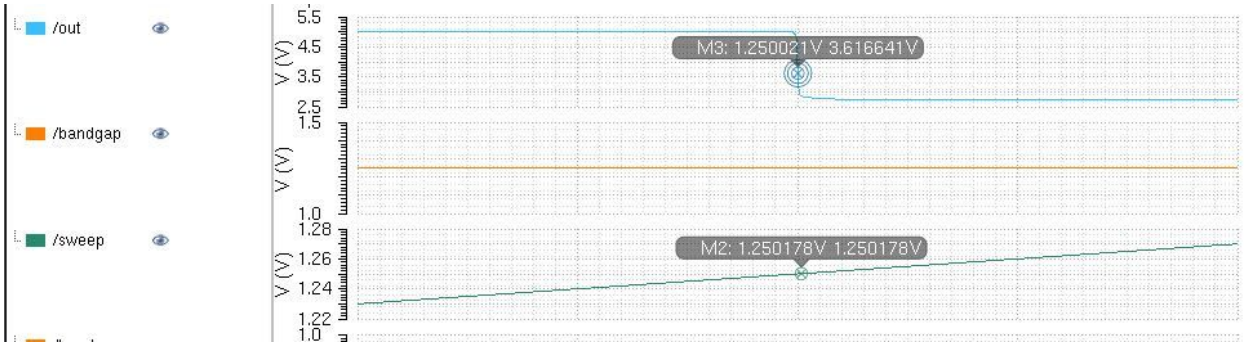
The schematic below shows the comparator. It uses 4 non-biasing diff amps to compare the positive to the negative terminal. The blue arrows show that if the Vm terminal goes high(higher than Vp) then it pulls the adjacent PMOS down and therefore bringing the final PMOS up. The red arrows show that if the Vp goes high (meaning reference is higher than the incoming voltage) then pull the PMOS down. This may seem reverse, but after 4 diff amps it turns out that the if Vm goes high then the final switching PMOS will shut off to regulate the Vout and vise versa. **It's important to note that the bottom NMOS helps pull down the power supply**

when the PMOS is on. Therefore, a weaker NMOS(longer L, small W) decreases current and speed, but gives more gain, sharpening the switching point of the comparator.

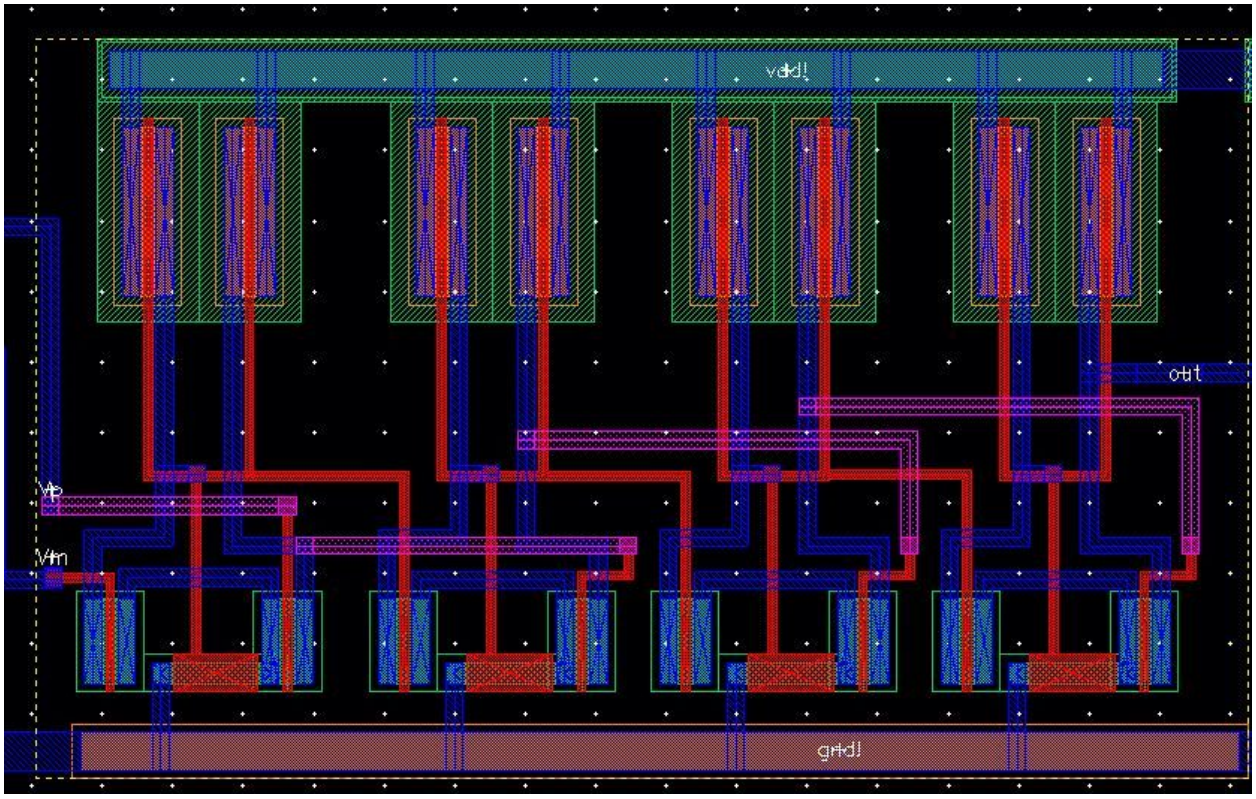
.



The schematic shows the switching point at 1.25 using a sweeping DC simulation and that at 1.25 the output from the comparator switches, but is **still not very sharp around the edges**



Compare the layout below to the buck converter. The bandgap is connected to Vp and the divider is connected to Vm.

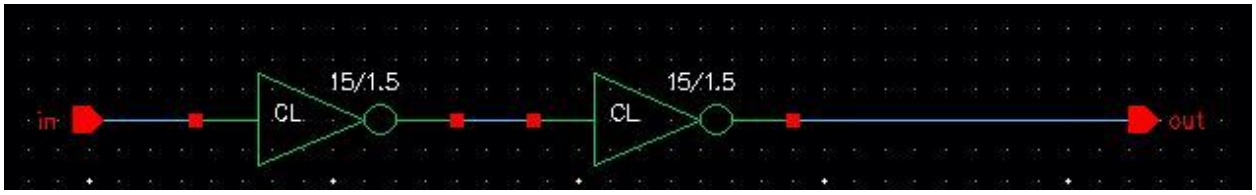


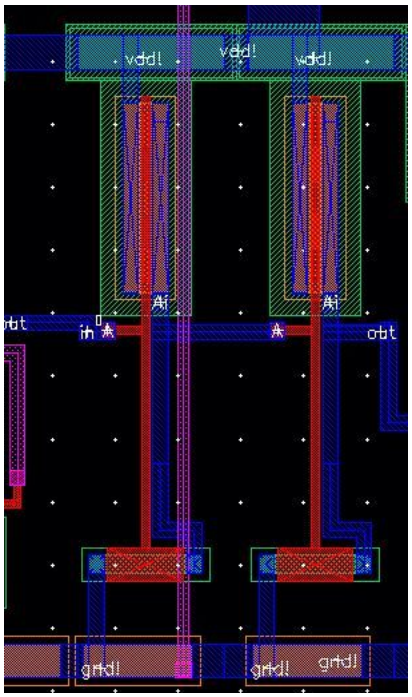
6. Buffers

Buffers provide the cleanup of the plot and amp up the gain from the comparator. **Two inverters are placed in series of the same size giving the output full logic levels.** A longer L was chosen in the bottom NMOS for efficiency.

The gain of the resulting switching voltage can be calculated by taking the derivative output voltage. **It shows, 2.9 M gain.**

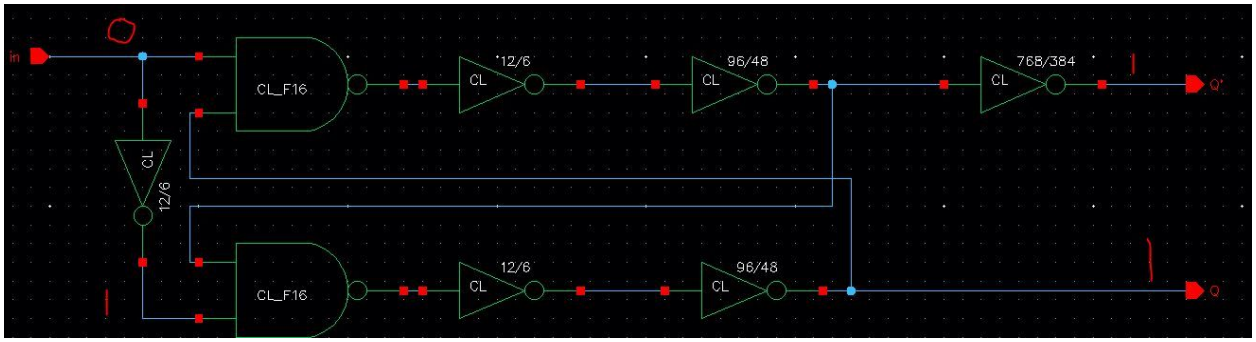
The layout shows the output from the comparator to the buffer size (15/1.5) to the input of the SR Latch

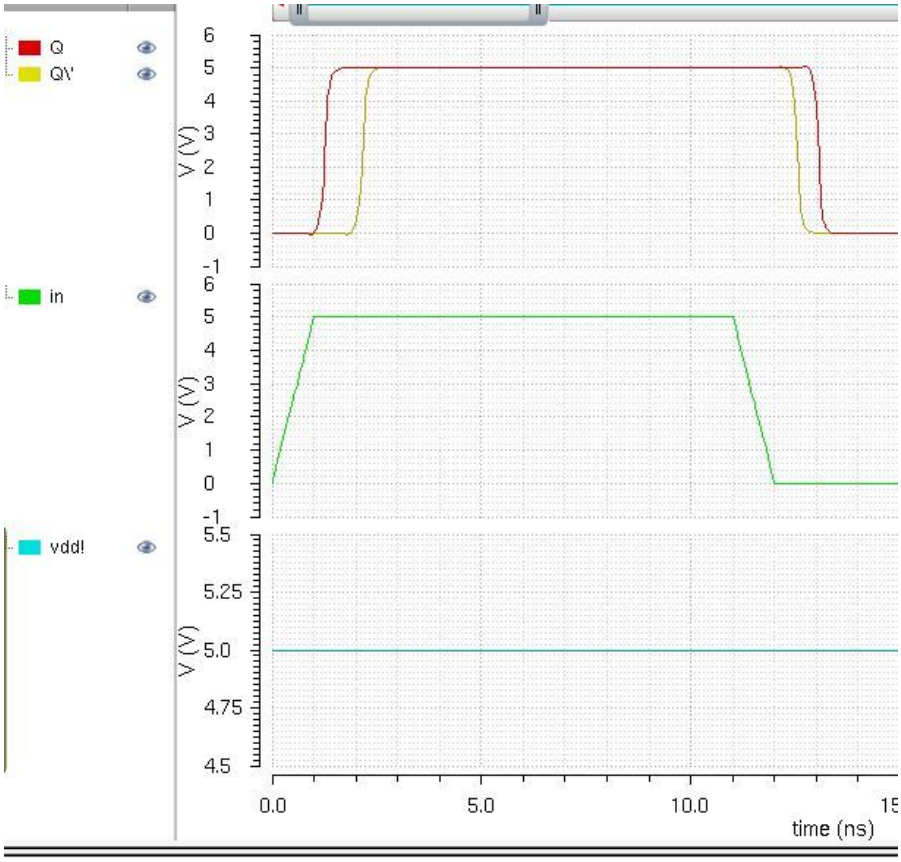




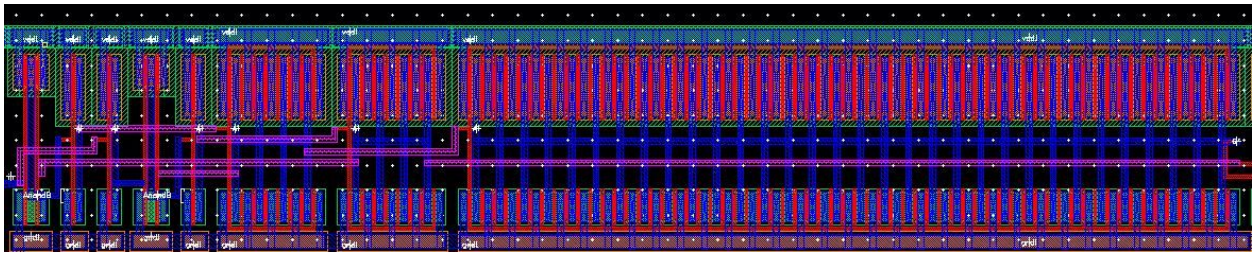
7. SR Latch

The SR Latch allows for clocking input to ensure that the PMOS and NMOS are never on at the same time causing a short circuit and huge drop in efficiency. The schematic below shows that incrementing buffers with multipliers of 8 are used to create a small delay between the PMOS and NMOS turning on; an extra inverter on the PMOS **allows both to be high or both to be low** since the PMOS and NMOS function inversely of each other.





The layout shows big multipliers so it may not be easy to see from the image below. Essentially, the Q and Q' will be fed to the switching PMOS and NMOS discussed in the next session.

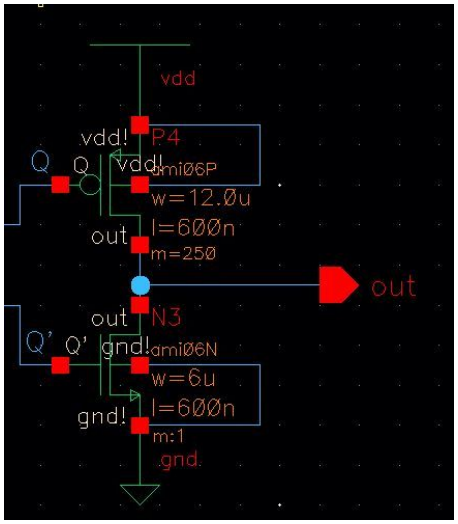


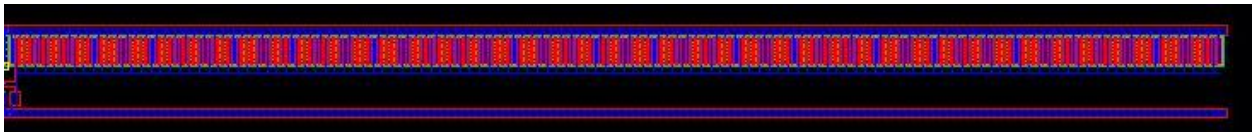
8. Switch PMOS and NMOS

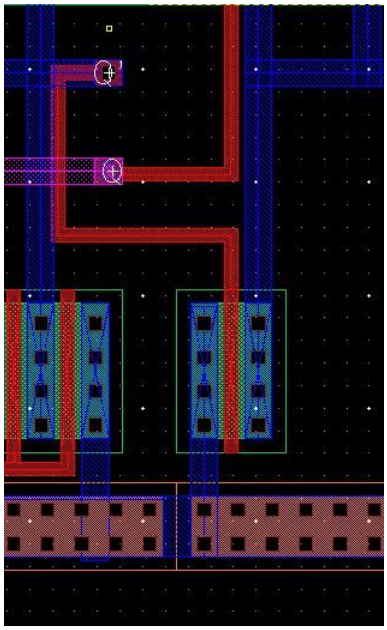
The last PMOS and NMOS may appear as inverter, but are not at the gates. A very small multiplier was chosen for the NMOS because the NMOS is dealing very little with power since most of the current will flow through the PMOS when it has to pull down from VDD. **Because of this a large multiplier (250) was chosen for the PMOS creating a small resistor, thus**

drawing less current and increasing our efficiency. In the C5 process, Rn' of PMOS is 30k. We can calculate the resistance using

$$Rn_p = Rn_p' \frac{L}{W} = 30k \frac{12*250}{.6*250} = 6\Omega$$

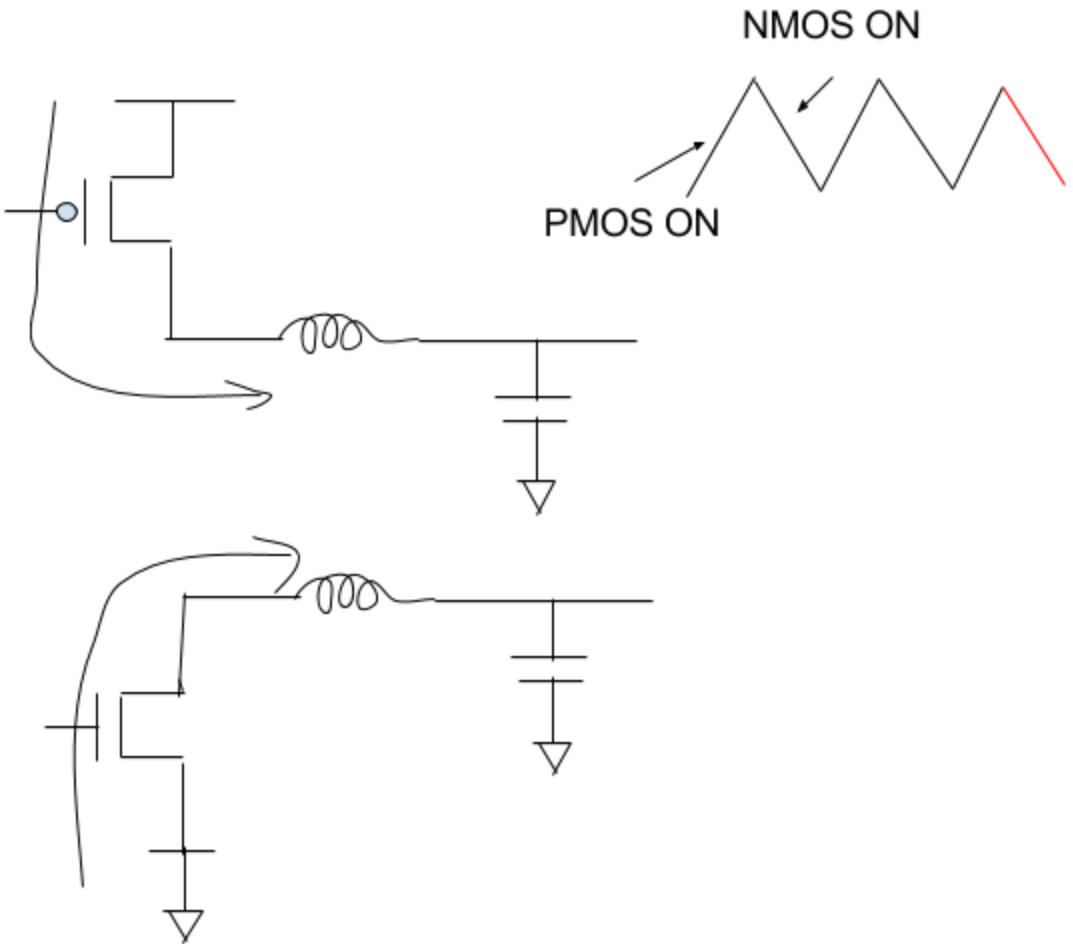






9. LC circuit (OFF CHIP)

Finally, we must account for the LC circuit that will lay off chip to prevent large ringing and a frequency of change in the circuit. The drawing below shows that the when the PMOS is on the current will be drawn from the PMOS to the inductor and capacitor, and vise versa.



These equations let us derive that

$$(1)\frac{Vdd-Vout}{L} = \frac{I_{max} - I_{min}}{(D * T)} \quad (2) Vout = D * Vdd$$

Equation (1) above can help us derive that

$$(3) L = \frac{D * T\ (VDD-Vout)}{(I_{max} - I_{min})}$$

We want to design for the worst case scenario of using a higher power supply (5.5V) and a high load (100mA). We can design Imax and Imin to be 10% of load and calculate D using equation (2). The project was designed with a T of 10us which is a frequency of 10MHZ

$$L = \frac{.45 * 10us\ (\ 5.5-2.5)}{(1.1m - .9m)} = 675uH$$

The capacitor was designed in a similar way. Assuming that we want the ringing to vary very small, 5mV was chosen

(1) $Q = CV$ (2) $I = C\frac{dV}{dT}$
(3) $Q = I_L T_L$

With equations, (1), (2), and (3) we can derive
(4) $C = \frac{I_l T_L}{dV}$

We can solve
$$C = \frac{100m * 10u}{5m} = 200uF$$

10. PIN connection

The chip only has one output pin. It would go to into an arbitrary pad(15 for example). Then ground would go to PIN 20 and VDD to PIN 1.