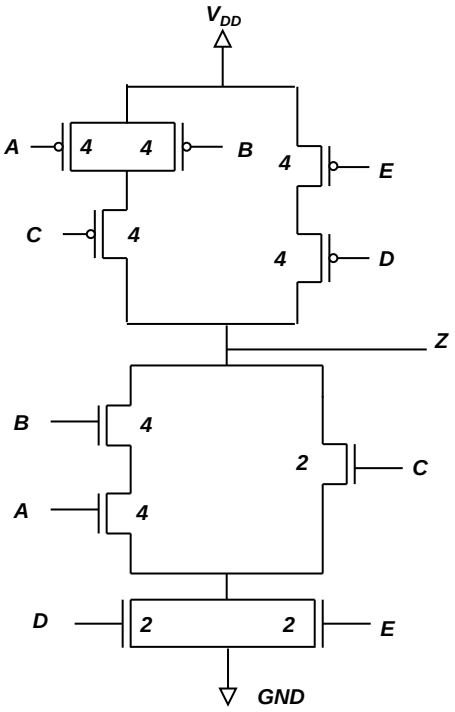
UNIVERSITY OF WARWICK School of Engineering		Year Summer 2012
ES3900	Title of Examination:– FUNDAMENTALS OF MODERN VLSI DESIGN	Sections A & B Pages 1-14
Questions 1-4		Mark Allocation

1.



Boolean function :

$$Z = \overline{((A \bullet B) + C) \bullet (D + E)}$$

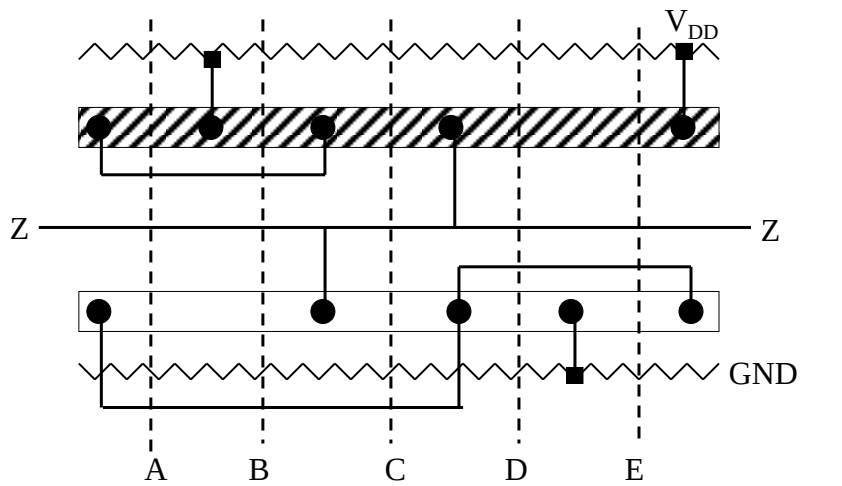
1 mark

For gate size S = 1 :
The resistances offered by the pull-up and pull-down paths under worst-case conditions should be identical to those of the unit size inverter assuming the sheet resistance of p-diff is twice that of n-diff i.e. equivalent to a pFET of width 2 and a nFET of width 1. Combined with the series/parallel rules, the widths shown on the schematic are obtained.

4 marks

Logical Efforts :
These give the input capacitance in units of that of the unit inverter -
A = B = 8/3 units
C = D = E = 6/3 units
Euler paths : identical paths can be found for each network e.g. ABCDE

4 marks



poly
p-diff
metal 1
contact cut
n-diff
metal 2
via

6 marks

Comparison of Layout Strategies

Strategy	*Advantages*	*Disadvantages*
Place and Route	*Ease of design* *Ease of modification*	*Random wiring* *Bad external I/O*
Standard Cell	*Easy V_{DD} and GND routing* *Encourages orthogonal design methodology*	*May need wide inter-cell routing channels* *Discourages mirrored layouts*
Partitioned	*No external wiring* *Optimised I/O for next level*	*Casting design into this form at late stage is difficult* *Generally different layout for each instance of logic function*
Tiled Cells	*Compact highly structured layout* *Reduces parasitics associated with wire length and area*	*Considerably increases design effort* *May force increase in size for some cells*

A place-and-route approach using library cells for the basic logic functions would save on design effort and time but result in a much less compact layout. Rarely would the P&R approach be desirable for such a logic block as combining the functionality of 4 - 5 basic gates in a single complex gate is generally more efficient in terms of chip area, power consumption and speed of operation.

A partitioned layout would reduce the area compared with P&R, but at the expense of greater design effort as, in general, there would be a separate instance of each gate in the logic block. Unless optimising the I/O interface to other functional blocks were a priority, there would be little benefit in adopting a partitioned approach.

A tiled cell layout could be considered if the logic block formed part of a 'bit-sliced' design. If it formed part of 'random' (i.e. unstructured) logic, then implementing as a PLA could be considered, which intrinsically lends itself to a tiled cell layout strategy.

From the information given, it is likely that the approach of choice would be to combine the logic block with other blocks in the design and specify a standard cell layout optimised at around 50 basic gates per cell.

6 marks

Comparison of Design Styles

Style	*Advantages*	*Disadvantages*
Static CMOS	*No power dissipation except when switching* *Ease of interface to next stage logic*	*2N transistors required for N-input gate* *Series transistor stack limits speed and gate fan-in*
Pseudo-nMOS	*Input capacitance less than for static CMOS* *Only N+1 transistors required for an n-input gate*	*Static power dissipation in pull-down state* *Design effort required to calculate transistor sizes for correct functionality*
Precharge-Evaluate	*Input capacitance less than for static CMOS* *Only N+2 transistors needed for an N-input gate* *No static power dissipation*	*Cannot cascade stages together directly due to problem of spurious evaluation* *Charge sharing at internal nodes resulting in degradation of logic levels*

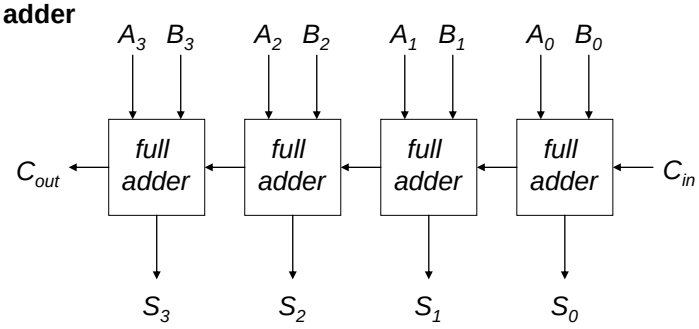
4 marks

Total

25 marks

2.

(a) 4-bit full adder



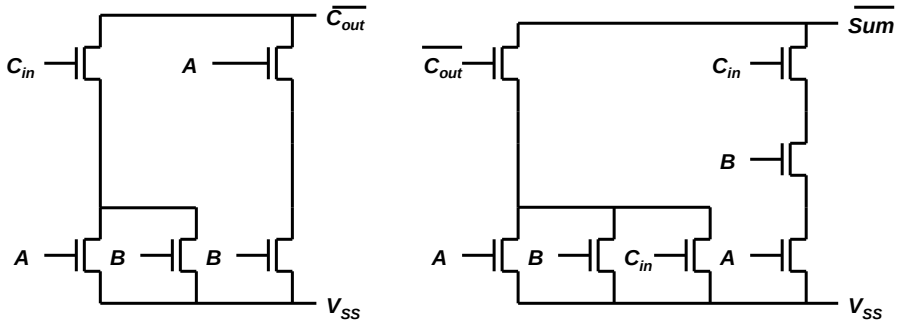
A	B	C_{in}	Sum	C_{out}	$\overline{C_{out}}$
0	0	0	0	0	1
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	0

One possible way of deriving the Sum and Carry signals is :

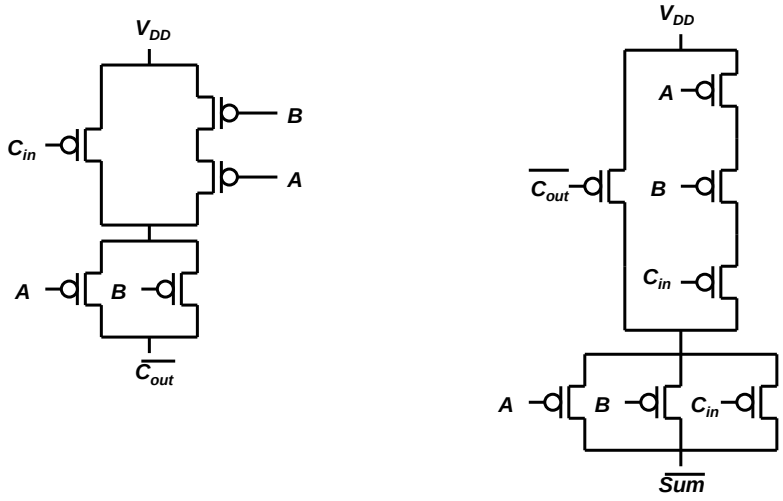
$C_{out} = A.B + B.C_{in} + A.C_{in} = A.B + C_{in}(A + B)$

$Sum = \overline{C_{out}}.(A + B + C_{in}) + A.B.C_{in}$

The corresponding nFET networks are shown below which provide the complement of the Sum and Carry signals, thus requiring two extra inverters per stage.

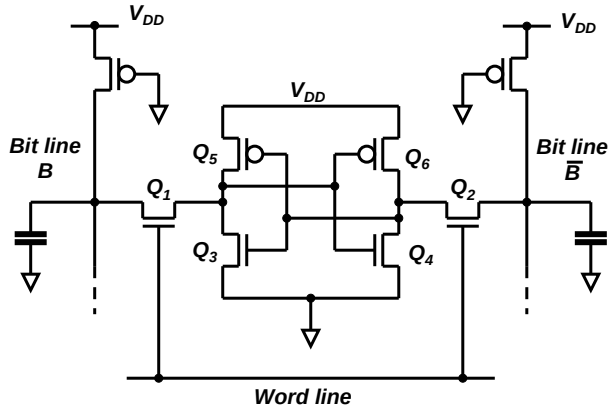


The pFET networks for the complement of Sum and Carry are shown below :



9 marks

(b) 6-T static RAM cell



The 6-T static RAM cell comprises pass transistors Q_1 and Q_2 which steer data to the cross-coupled inverters formed by (Q_3, Q_5) and (Q_4, Q_6) when the corresponding word line is asserted via the row address decoder.

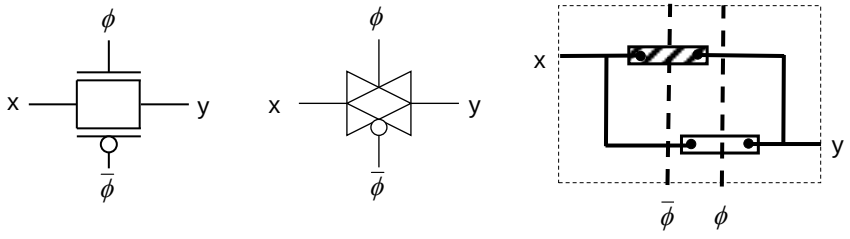
In a write operation, data is placed on the bit line and the complement of the data on the bit-bar line. If a '1' is to be written, this is steered through Q_1 and appears at the input of inverter (Q_4, Q_6). The output ('0') is coupled back to the input of inverter (Q_3, Q_5) whose output ('1') is in turn coupled back to the input of (Q_4, Q_6) to ensure stability. This is reinforced by the value of '0' steered through Q_2 to the input of (Q_3, Q_5). The converse occurs if a '0' is to be written.

During a read operation, both the bit and bit-bar lines are pre-charged to logic '1' through the corresponding pFETs. On asserting the word line via the row decoder, either bit or bit-bar will be pulled to a lower potential through Q_1 or Q_2 depending on whether a '0' or '1' is stored in the memory cell, thus making the data stored available on the bit lines. Additional circuitry to that shown is required for both write and read operations. For writing a memory cell, the data is gated with write-enable and bit-line select signals, the latter via the column address decoder. The bit and bit-bar lines are then driven to the required logic levels. For a read operation, the small voltage difference between the bit and bit-bar lines is amplified by a bistable sense amplifier before restoring valid logic levels using a differential amplifier.

8 marks

(c) CMOS transmission gate

A CMOS transmission gate is realised from a parallel connection of a pFET and an nFET, with sources and drains connected together. When control signal ϕ connected to the gate of the nFET is high and $\overline{\phi}$, connected to the gate of the pFET is low, then both FETs are on and a bidirectional link is made between input x and output y. This allows both undegraded logic "1's" and logic "0's" to pass bidirectionally through the gate. For the reverse control signal polarity both FETs are off, no connection is made and the gate is in a high impedance state.



The stick diagram shows a possible layout with source-source and drain-drain connections in metal1 allowing I/O's to be routed horizontally through the cell. Diffusion is run horizontally, and control signals routed vertically through the cell allowing multiple instances of the gate to be stacked by vertical abutment.

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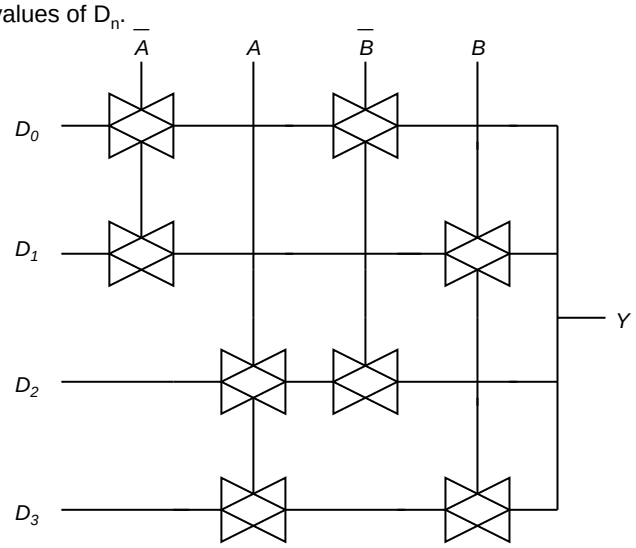
The arrangement of transmission gates shown below provides an implementation of a universal logic module of two input variables A and B. The variables and their complements are the control signals to the transmission gates which select data bits $D_0 – D_3$ to be steered to output Y. This allows the synthesis of any 2-input gate with appropriate values of D_n.



For example, the truth table below shows the values of $D_0 – D_3$ for the logic module to function as an equivalence gate. Advantages are that it vastly reduces overall transistor count (compared with providing specific gates for each possible logic function) and also clearly allows re-use of design effort. The concept can be extended to logic functions of 3 or more variables but with caution necessary in respect of timing delays and signal degradation introduced by cascading transmission gates. The technique is widely used for ALU design in microprocessors where $D_0 – D_n$ are now op-codes fetched from program memory which determine the functionality of the logic block.

		A	$\overline{A}$	B	$\overline{B}$	Y=A eq B
D_0	**1**	0	1	0	1	**1**
D_1	**0**	0	1	1	0	**0**
D_2	**0**	1	0	0	1	**0**
D_3	**1**	1	0	1	0	**1**

8 marks

Total

25 marks

3.

(a) Sketch out a block diagram illustrating the operating principles of a CMOS based operational amplifier. The block diagram should show the different stages in an op-amp and associated circuitry at a functional level. Briefly explain the purpose of each component diagram for the operational amplifier.

A sketch of the basic functional components in a two stage op-amp is show below:

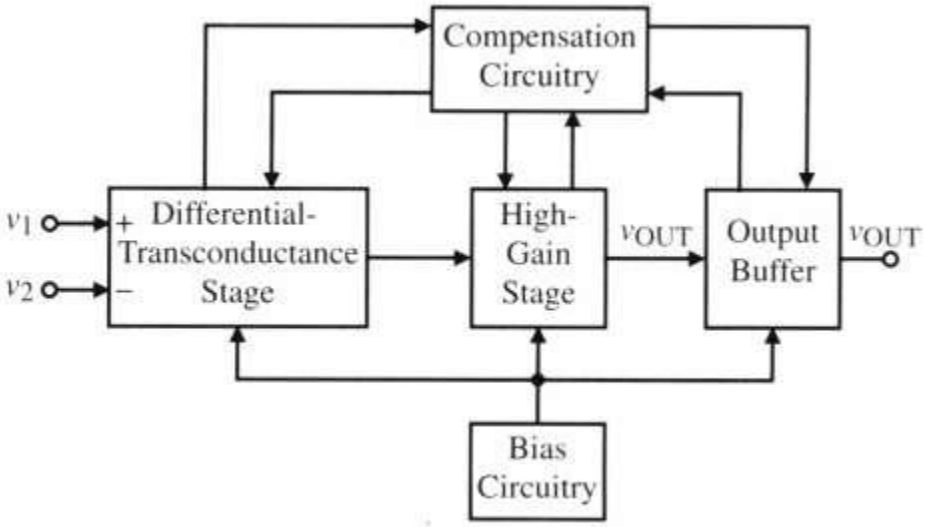


Figure 3.1: Schematic of two-stage operational amplifier

The basic component parts of the op-amp are:

- A differential trans-conductance front-end that converts the difference between the input signals v1 and v2 to a current.
- A high gain stage that amplifies the input signal
- An output buffer stage that is capable of driving a load resistor without reducing the gain
- Compensation circuitry to improve the frequency characteristics of the amplifier
- Bias circuitry to set the DC operating point of the different stages

6 marks

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The basic design comprises seven MOSFETs showing differential stage, current mirror and bias circuitry. The Miller capacitor is labelled as Cc.

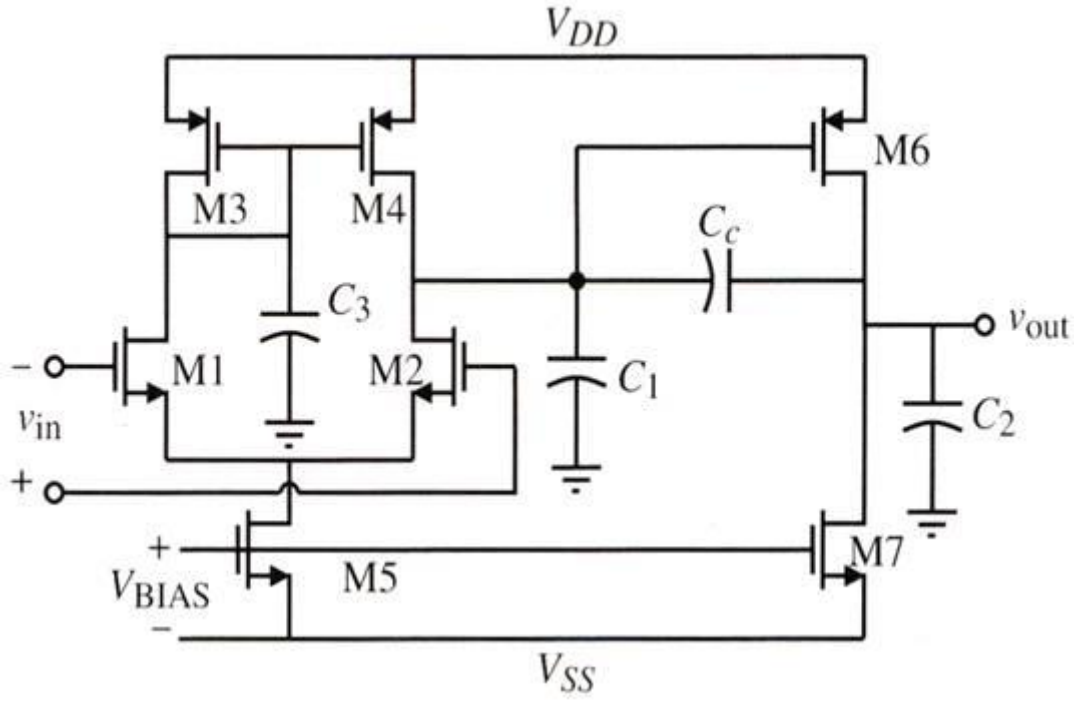


Figure 3.2: Design of basic operation amplifier with compensation

A capacitor is need to make sure that the amplifier does not ring or oscillate when transient signals are considered. The Miller capaciance is a large capacitor that improves the stability of the amplifier and stops unwanted ringing. It is an issue in a cost-effective circuit because it is a very large capacitor and takes up perhaps 40% of the floorplan. This means it increases the cost of the die and if it can be mininized in size then it will save considerable cost.

6 marks

3(b) *Describe two of the five possible analogue capacitors that can be made in a standard 3 metal 2 poly epi silicon CMOS process and sketch in each case a cross-section of the component. Comment on the nature of the capacitance per unit area and matching accuracy of your choices.*

There are 5 possible CMOS capacitors that have been given in the course and these are illustrated in the table shown below.

Table of 5 different CMOS capacitors and their properties

Component Type	Range of values	Accuracy	Matching accuracy	Temp. coefficient
MOS capacitor	2.2-2.7 fF/μm²	7 – 14 %	0.05 %	20 – 50 PPM/°C
Poly1 / Poly2 capacitor	0.8-1.0 fF/μm²	6 – 12 %	0.05 %	20 – 50 PPM/°C
Poly / M1 capacitor	0.021-0.025 fF/μm²	6 – 12 %	1.5 %	50 – 100 PPM/°C
M1 / M2 capacitor	0.021-0.025 fF/μm²	6 – 12 %	1.5 %	50 – 100 PPM/°C
M2 / M3 capacitor	0.021-0.025 fF/μm²	6 – 12 %	1.5 %	50 – 100 PPM/°C

From this table, the students can choose any two of the five. However the most common choice of integrated analogue capacitors are made from either a poly layer and p+/n+ diffusion region (see below left) or between the two poly layers (see below right):

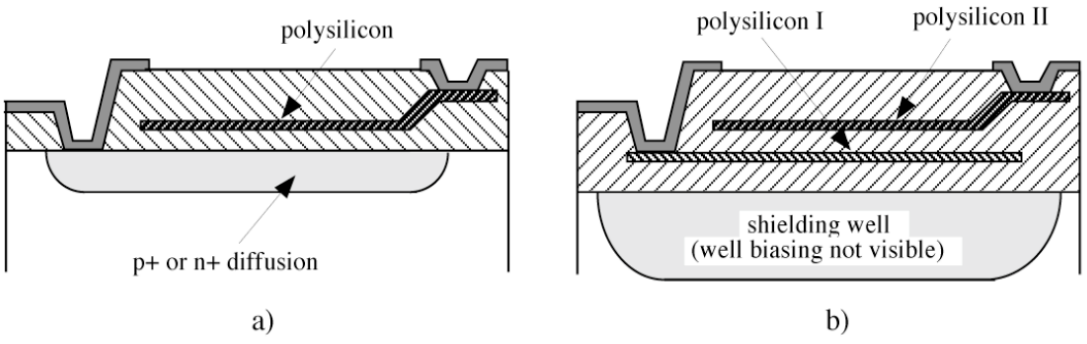


Figure 3.3: Cross-sections of two common CMOS capacitors

The advantages of these two capacitors are that the capacitance per unit area is almost 10 x higher than the other ones and also the matching accuracy is better than using metal layers. See table for values.

It is also possible to create capacitors between the metal layers, e.g. M1 to M2, M2 to M3. However this design is less popular because the thicker oxide layers produce smaller capacitances per unit area.

10

8 marks

3(c) *An analogue CMOS circuit requires a low pass filter with a corner frequency of 10 kHz. It is desirable to minimise the size of the chip die. Describe the design of a filter that will satisfy this constraint and explain your reasoning. Estimate the size required of the filter components.*

The main goal here is to reduce the physical size of the CMOS components that are used to obtain the desired corner frequency or time constant. Because there is no mention of the roll off rate or order of the filter, it can be a simple first order one to reduce complexity and hence size. So a basic RC filter should suffice.

The best choice of capacitor in terms of capacitance per unit area is the MOS capacitor based upon the poly to n+/p+ layer (see Table above). It has a capacitance of 2-3 fF per micron squared. Thus a capacitor of 100 microns by 50 microns would produce a 10 pF capacitor.

For a filter with a corner frequency of 10 kHz and capacitance of 10 pF then the resistance of the filter is given by:

4 marks

$$R = \frac{1}{f_c 2\pi C} .$$

Hence the resistor R needs to take a value of about 2 Mohms

The choice of resistor is also limited and the table shows the various layers:

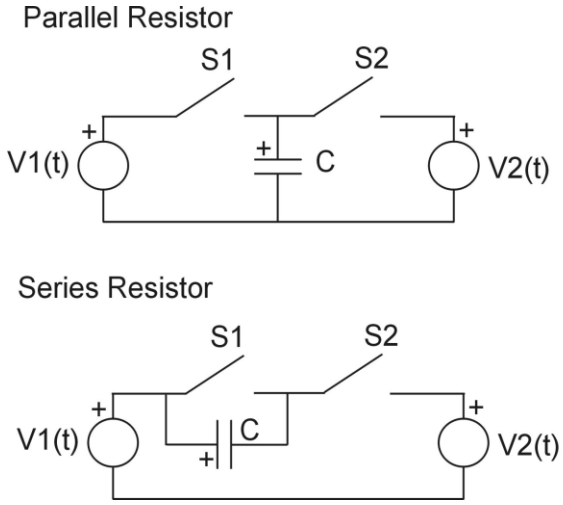
Table of different CMOS resistors and their properties

Type of Layer	Sheet Resistance	Accuracy	Matching Accuracy	Temperature coefficient
N+ diff	30 – 50 Ω/□	20 – 40 %	0.4 %	200-1K PPM/ºC
P+ diff	50 – 150 Ω/□	20 – 40 %	0.4 %	200-1K PPM/ºC
N-well	2K – 4K Ω/□	15 – 30 %	-	5K PPM/ºC
P-well	3K – 6K Ω/□	15 – 30 %	-	5K PPM/ºC
Poly 1	20 – 40 Ω/□	25 – 40 %	0.4 %	500-1500 PPM/ºC
Poly 2	15 – 40 Ω/□	25 – 40 %	0.4 %	500-1500 PPM/ºC

The best choice of layer is the P-well or N-well for a sheet resistance of typically 2-6k ohms per square.

This is a large resistor and in some case it may be possible to use a switched capacitor design and so generate a large resistance with a much smaller area. Both parallel and series resistors can be created by switched capacitors and they have an equivalent resistance of T/C where T is the time period of the clock. The circuits are shown below

4 marks



2 marks

Figure 3.4 Possible CMOS resistors for students to consider with sheet values and errors

4(a) *Give at least three advantages and three disadvantages of SOI CMOS over CMOS technology for low power low voltage devices.*

There are many advantages and disadvantages of SOI over standard CMOS technology. Some of the possible example answers are:

Advantages:

- Better electrical isolation through oxide,
- faster (when body floated),
- higher packing densities (with trench isolation),
- improved temperature performance (i.e. higher operating temperatures with reduced currents),
- reduced short channel effects,
- and lower track capacitance.

Disadvantages:

- More expensive to fabricate,
- kink effects,
- floating body effects,
- self-heating,
- more complex to design (more processes and masks),
- less robust.

4(b) *Explain the differences, in terms of structure and fabrication, between a partially depleted SOI MOSFET and a fully depleted SOI MOSFET.* 6 marks

The students may sketch out the two structures to illustrate the difference or state it in words:

- Partially depleted SOI
  - Here the depletion region does not reach through the entire source/drain region
- Fully depleted SOI
  - Here the depletion reach consumes the entire silicon area
- In terms of fabrication FD devices have no floating body, have high source/drain resistances, very thin silicon layer (<0.1 μm) and are hard to manufacture.
- PD devices have a floating body, have thicker active silicon (> 0.15 μm) is easier to manufacture than PD devices.

4(c) *Briefly discuss what a body contact is and why it is important for the performance of an SOI CMOS MOSFET. Sketch two examples of how body contacts are made for a partially depleted SOI MOSFET.* 4 marks

Body contacts are difficult to fabricate in SOI technology as only the area underneath the gate is not covered with silicon isolation (normally silicon dioxide) and either side of the gate is the source and drain. So how do you make a contact?

- Can only create non-diffused area under the gate
- Hence extend the gate beyond the source and drain to create a contact to the substrate. Then make a contact next to this extended gate.
- For example make T shape gate structures
- Design (a) below has issue of resistance along channel, hence reduces speed of the devices (affects performance)
- Design (b) below can only use source potential

Example body contacts are given below.

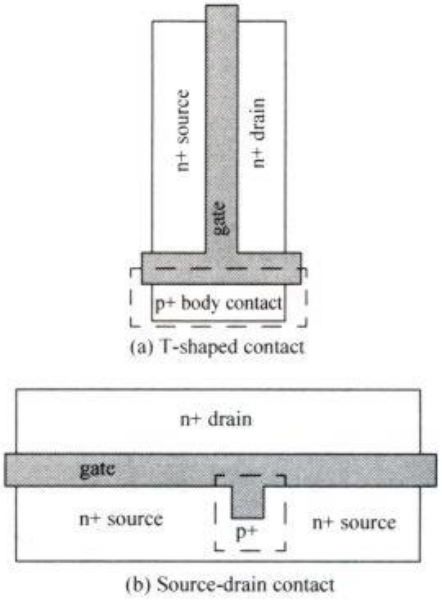


Figure 4.1 Two examples of body ties for PD SOI MOSFET structures

6 marks

4(d) *Sketch the cross-section of a double gated SOI MOSFET device. What is the advantage of this device over a normal SOI MOSFET.*

The cross-section of a double gated MOSFET is as shown here:

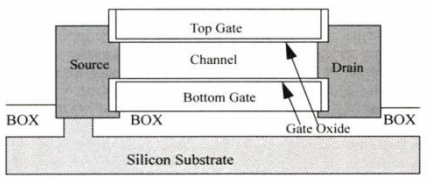


Figure 4.2 Schematic structure of a double gated MOSFET

This device gives significant improvement to the maximum current that can flow through the transistor as the channel has effectively been doubled thus reducing the on-state channel resistance.

4 marks

Total 20 marks