ES3B20

THE UNIVERSITY OF WARWICK

Third Year Examinations: Summer 2011

DIGITAL SYSTEMS DESIGN

Candidates should answer ALL FOUR QUESTIONS.

Time Allowed : 3 hours.

Only calculators that conform to the list of models approved by the School of Engineering may be used in this examination. The Engineering Databook will be provided.

Note: PIC16F84A for Q1 is provided with this paper.

Read carefully the instructions on the answer book and make sure that the particulars required are entered on each answer book.

---

1. A microcontroller based digital door lock system is to be designed using a telephone style keypad for entering the code, a solenoid for releasing the lock mechanism, a proximity switch and three LED's for displaying system status.

With the door assumed initially to be in the locked state a green LED is illuminated. A two digit number is input on the keypad and compared with the correct code stored in EEPROM. If they match, the solenoid is activated to open the door. If they do not match, an amber LED is illuminated, indicating that one further attempt is permitted to enter the correct code. If correct, the solenoid is activated to open the door. If incorrect, a red LED is illuminated and any further keypad input ignored until the system is reset manually. If successfully opened, a spring pulls the door shut whereupon the lock mechanism automatically engages and the proximity switch signals that the door is closed and locked.

It may be assumed that the keypad outputs 3 column and 4 row signals, that the proximity switch produces a logic output signal and that switching the solenoid is controlled by a standard logic signal.

With reference to the information on the PIC16F84A appended, provide the following :

(a) a software flowchart (10 marks)

(b) a block diagram of the system (5 marks)

(c) a summary of how and which microcontroller registers are used by the application (5 marks)

(d) an assembly language routine for validating the keypad input (5 marks)

(Total 25 marks)

Continued ….

2. (a) In the context of digital system specification using VHDL, briefly describe the following concepts :

(i) Port mode and type

(ii) Entity/architecture pairs

(iii) Processes

(iv) Sensitivity list (8 marks)

(b) A hardware module is specified as follows :

- Port A and B are 4-bit input only buses
- Port C is a 4-bit tri-state output only bus
- Port CLK and S are input bits
- Ports LT, EQ and GT are output bits

Sketch a block diagram of the system and write the Entity declaration in VHDL. (4 marks)

The functionality of the module is defined as follows :

- On CLK if S = 0 multiplex Port A data to output Port C
- On CLK if S = 1 multiplex Port B data to output Port C
- On CLK if A < B then LT = 1
- On CLK if A = B then EQ = 1
- On CLK if A > B then GT = 1

Write the Architecture for the module in VHDL. (6 marks)

(c) Provide the truth table for a 2 to 4 address decoder and, assuming a clocked version is required, write the Entity and Architecture in VHDL. (7 marks)

(Total 25 marks)

Continued ….

3.

a) Give the definition of Finite State Machine (FSM) and explain the difference between the Mealy and Moore type machine.

(*5 marks*)

b) There is a requirement for the design of a digital controller to control a traffic light at the intersection of a main street and a side street with the following specification. A green light on the main street should be on for a minimum of 30 s or as long as there is no vehicle on the side street. The side street should have a green light on until there is no vehicle on the side street or for a maximum of 30 s. There is to be a 5 s caution light (yellow) between changes from green to red on both traffic lights on the main street and on the side street. Derive a state diagram, state transition table and logic equations for the next states in order to implement a correct sequence of operation.

(*20 marks*)

(Total 25 marks)

Continued ….

4.

a) Describe a fault-oriented test pattern generation strategy in general followed by the detailed description of:

(*4 marks*)

i) the sensitive path algorithm and (*5 marks*)

ii) the D-algorithm. (*4 marks*)

b) Demonstrate the application of the D-algorithm by testing for A/0 in the circuit shown in Figure 2.1.

(*12 marks*)

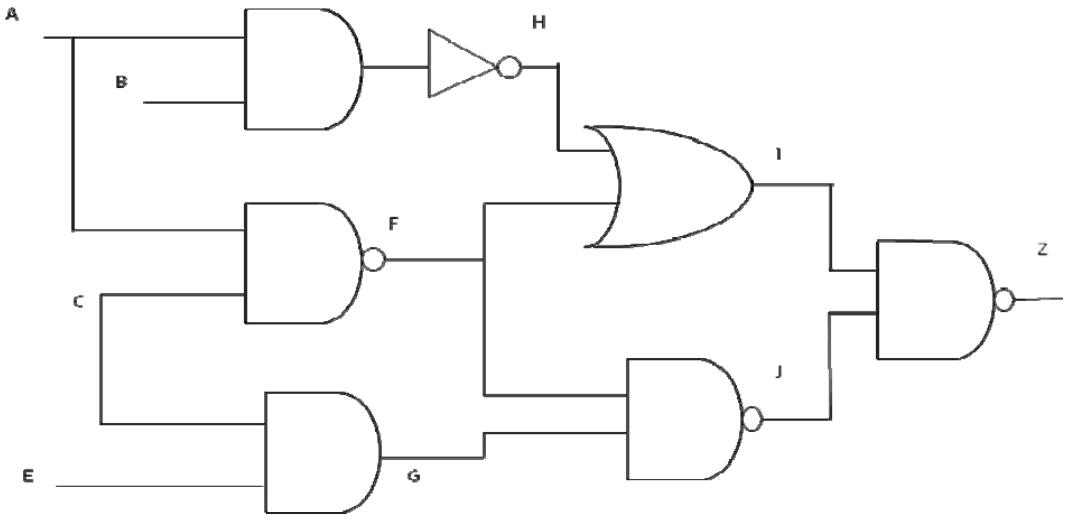

Figure 2.1

(Total 25 marks)

END