THE UNIVERSITY OF WARWICK

Third Year Examinations : Summer 2012

ANALOGUE SYSTEMS DESIGN

Candidates should answer ALL 4 QUESTIONS.

Time Allowed : 3 hours.

Only calculators that conform to the list of models approved by the School of Engineering may be used in this examination.

Read carefully the instructions on the answer book and make sure that the particulars required are entered on each answer book.

ES3A3

1. Identify the type of oscillator shown in the schematic of Figure 1. Give one reason why this type of oscillator is used in preference to RC-based oscillators over a specified frequency interval, stating typically what this frequency interval is. (3 marks)

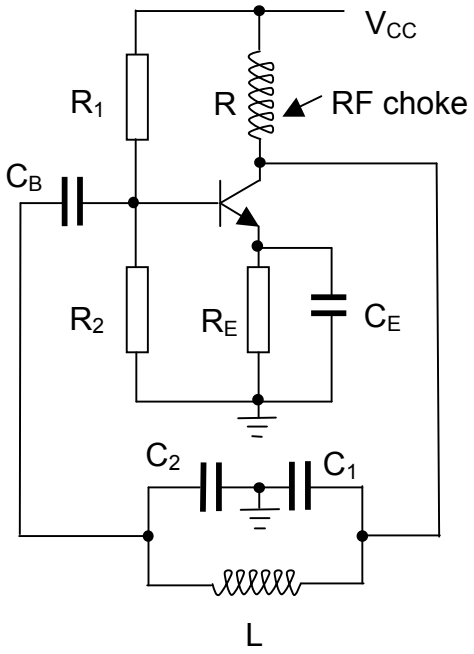

Figure 1

Describe the operation of the circuit by referring to the components shown on the schematic, where R represents the dc resistance of the RF choke and C_B is a blocking capacitor. In particular, explain the action of the RF choke, the LC circuit and the blocking capacitor. (3 marks)

Derive a simplified equivalent circuit for the oscillator. The equivalent circuit should not include any of the biasing components and also parasitic capacitances may be neglected. (4 marks)

Use Kirchhoff's Current Law to obtain from the equivalent circuit an expression for the resonant frequency of the oscillator in terms of circuit component values. State clearly the condition for the circuit to start oscillating and explain how stable oscillations are maintained. (10 marks)

If R = 10 Ω, L = 50 μH, the transconductance g_m of the transistor is 150 mS and C_1 and C_2 both have value 0.47 nF, does the circuit oscillate and if so at what nominal frequency ? (5 marks)

(Total 25 marks)

2. Derive a high frequency equivalent circuit for the amplifier of Figure 2 below, showing clearly how use of the Miller theorem allows the parasitic capacitances associated with the FET to be included in the model. It may be assumed that the reactances of C_1, C_2 and C_s are negligible at the signal frequency.

(6 marks)

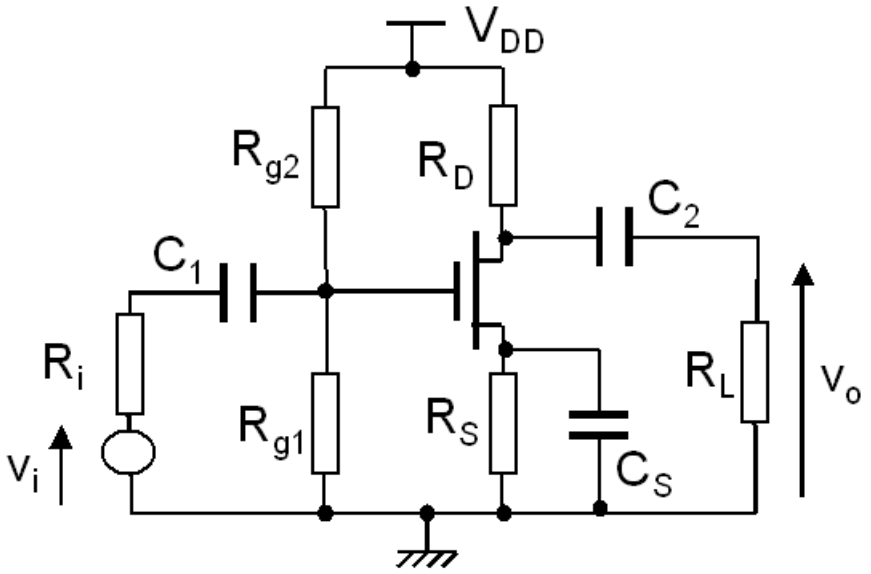

Figure 2

With reference to the equivalent circuit, deduce an expression for the high frequency gain of the stage in terms of the transconductance, drain-source resistance and parasitic capacitances of the FET and of the resistor values in the circuit, where R_i represents the internal resistance of the voltage source.

(12 marks)

Identify the number of poles in the high frequency response of the amplifier, calculate the pole frequencies and state the amplifier bandwidth given that $C_{gs} = 20$ pF, $C_{gd} = C_{ds} = 1$ pF, $g_m = 2 \times 10^{-3}$ S, $r_d = 15$ kΩ, $R_L = R_D = 5$ kΩ, $R_{g1} // R_{g2} = 2$ MΩ and $R_i = 1$ kΩ.

(7 marks)

(Total 25 marks)

3. The design of an IC operational amplifier calls for an extremely high gain stage using a single npn transistor. Describe how such a stage could be configured by use of an active load, illustrating your answer with a simple circuit schematic. (5 marks)

Carefully explaining your reasoning, derive an expression for the stage gain in terms of transistor Early voltages and the thermal voltage. Calculate the stage gain if the Early voltage for the active load transistors is 100 V, for the npn transistor is 150 V and the thermal voltage at room temperature is 26 mV. (4 marks)

Sketch the h-parameter equivalent circuit for the differential amplifier shown in Figure 3, assuming that the current mirror is equivalent to resistance R_{EE} in the emitter circuit of Q_1 and Q_2. Use the equivalent circuit to deduce the differential mode and common mode gain for the amplifier. (8 marks)

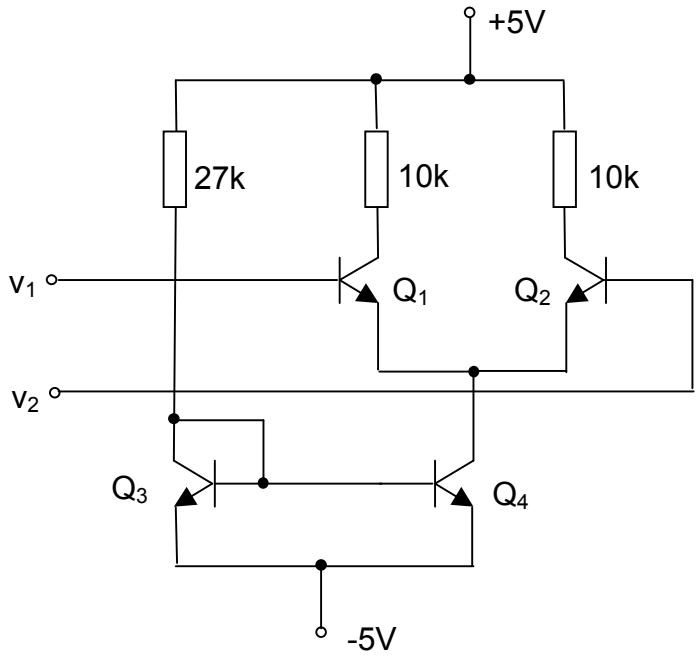

Figure 3

Given that transistors Q_1 and Q_2 are a matched pair, the Early voltages for Q_3 and Q_4 are 100V and that the emitter area of Q_4 is three times that of Q_3, calculate the following :

(i) the bias current being supplied to the differential amplifier

(ii) the differential mode gain of the amplifier

(iii) the common mode gain of the amplifier

(iv) the common mode rejection ratio.

(8 marks)

(Total 25 marks)

4. Sketch a block diagram of a Phase Locked Loop (PLL), clearly labelling the phase detector, loop filter, voltage controlled oscillator (VCO) and frequency divider. Indicate where the input is applied and where the output is extracted from the system. (3 marks)

State the transfer function for each functional block in the system, explain how the PLL can be modelled as a negative feedback system and state an expression for the overall loop gain. (5 marks)

Assuming that the PLL exhibits linear behaviour when in, or close to, the locked state, obtain from the loop gain the phase transfer function $\Phi(s)$ of the system. (3 marks)

Given the loop filter shown in Figure 4 below, deduce that the PLL response when in, or close to, lock is that of a damped second order system. (7 marks)

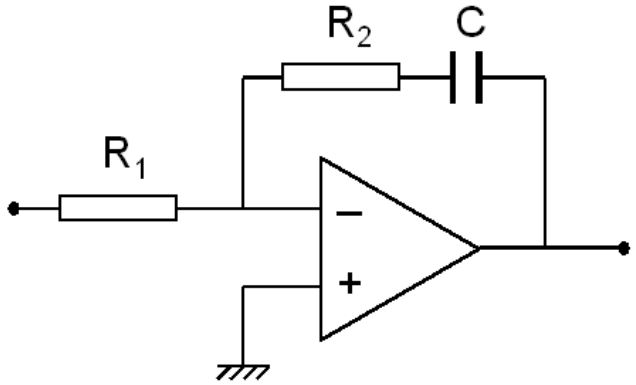

Figure 4

State the natural frequency and the damping factor of the PLL in terms of the parameters associated with the functional blocks and the filter component values. (5 marks)

Explain why the damping factor would often be selected to give either a critically damped or a Butterworth response. (2 marks)

(Total 25 marks)

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