**THE UNIVERSITY OF WARWICK**

**Third Year Examinations : Summer 2010**

**ANALOGUE SYSTEMS DESIGN**

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Candidates should answer 4 QUESTIONS.

**Time Allowed : 3 hours.**

**Only calculators that conform to the list of models approved by the School of Engineering may be used in this examination. The Engineering Databook and standard graph paper will be provided.**

*Read carefully the instructions on the answer book and make sure that the particulars required are entered on each answer book.*

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**ES3A3**

1. Sketch a simple schematic diagram to show the configuration of a generic tuned oscillator and use it to define the difference between Colpitts-type and Hartley-type oscillators. (3 marks)

Derive the condition for resonance of a parallel tuned circuit, taking into account the resistance of the inductor. (5 marks)

Obtain an expression for the maximum impedance of the arrangement and sketch plots showing qualitatively how the impedance changes with frequency for differing quality factors Q. If the resistance of the inductor is neglected, what is the resonant frequency ? (5 marks)

Identify the function of the circuit of Figure 1 and name one possible application for the arrangement. Give a description of the operation of the circuit. (7 marks)

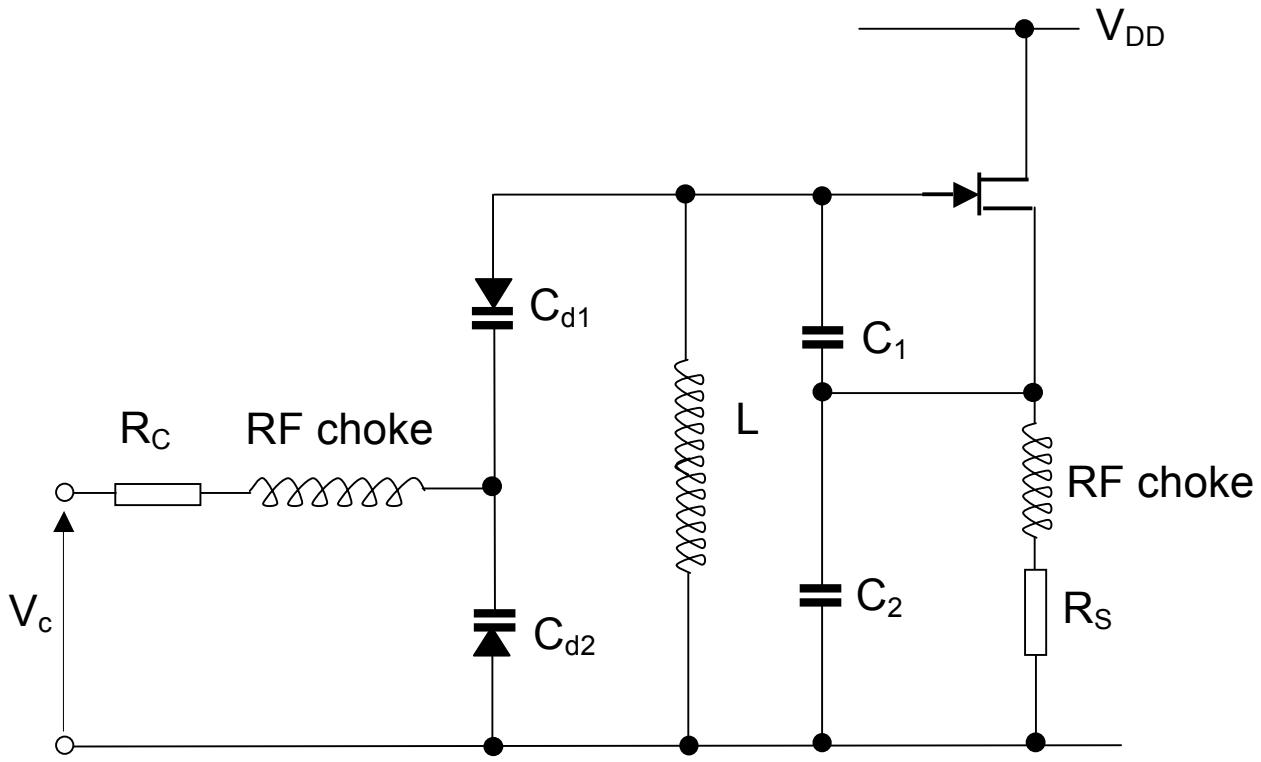


Figure 1

Explain, but without carrying out any detailed circuit analysis, how an approximate value for the resonant frequency of the circuit could be obtained. Given the following component values estimate the resonant frequency : $C_1$ = 22 pF; $C_2$ = 47 pF; $C_{d1} = C_{d2}$ = 10 pF; L = 150 nH. (5 marks)

(Total 25 marks)

2. Draw a low frequency equivalent circuit suitable for modelling the behaviour of a field effect transistor (FET) in common source configuration. (2 marks)

The FET in the common-source amplifier circuit shown in Figure 2 has $g_m = 3.5 \times 10^{-3}$ S and $r_{ds} = 50$ kΩ. List any advantages or disadvantages of using a FET as opposed to a bipolar junction transistor to implement the amplifier. (3 marks)

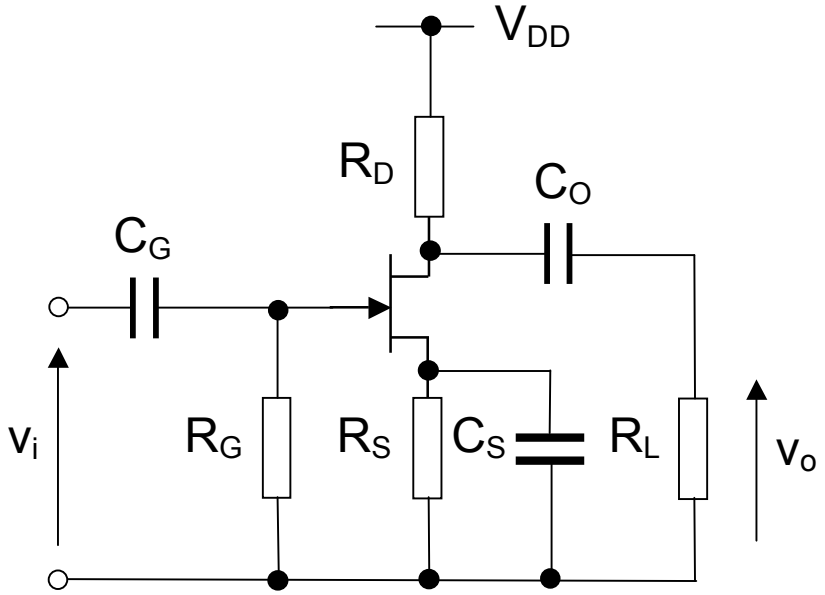


Figure 2

Draw a low-frequency equivalent circuit for the amplifier suitable for modelling the behaviour in the mid-band, where the reactances of all capacitors can be assumed to be negligible. (5 marks)

By using the equivalent circuit calculate :

(i) the mid-band voltage gain $A_v$;

(ii) the input resistance $R_{in}$;

(iii) the output resistance $R_{out}$.

given component values : $R_G = 1$ MΩ; $R_D = 2$ kΩ; $R_S = 1$ kΩ; $R_L = 5$ kΩ. (6 marks)

Given $C_G = 0.1$ μF; $C_O = 1$ μF; and $C_S = 22$ μF; determine the lower cut-off frequency for the amplifier. (6 marks)

An upper cut-off frequency of 150 kHz is desired. Calculate the value of an additional component necessary to achieve this and show on a circuit schematic where this component would be connected. (3 marks)

(Total 25marks)

3. Show how the parasitic capacitances associated with the bipolar junction transistor (BJT) in Figure 3 are influenced by the Miller Effect and hence derive an equivalent circuit suitable for modelling the behaviour of the amplifier at high frequencies. (8 marks)

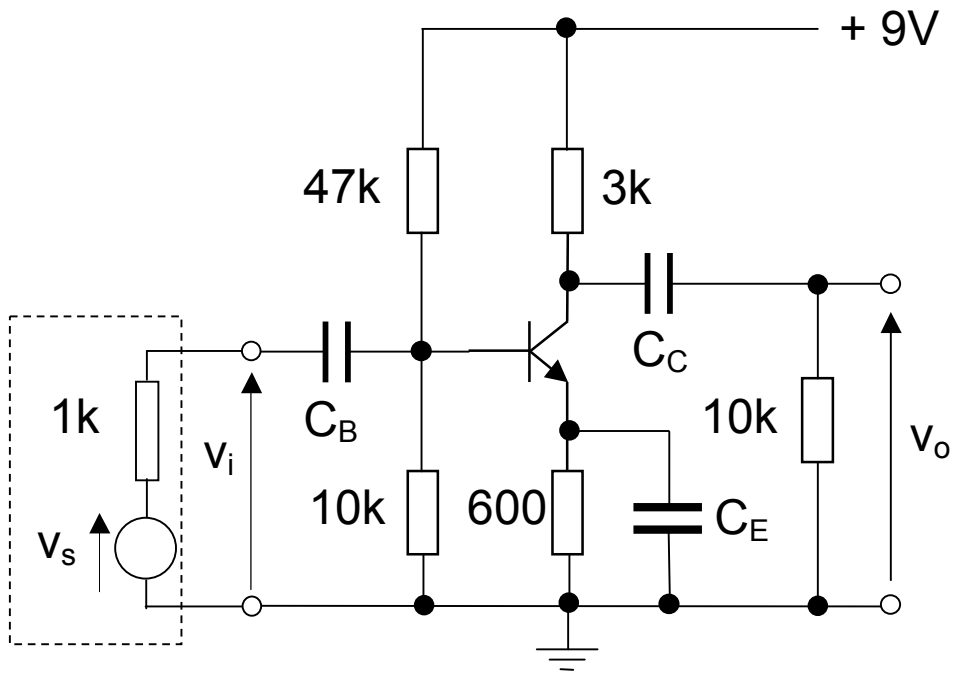


Figure 3

Given BJT parameters $\beta = 250$; $C_{be} = 8$ pF; $C_{bc} = 4$ pF; calculate the following :

(i) The mid-band voltage gain $A_V$ for the amplifier;

(ii) The corner frequency due to the input CR network;

(iii) The corner frequency due to the output CR network.

(10 marks)

With the same circuit configuration and BJT, suggest one method by which the high-frequency cut-off could be increased and describe the effect this would have on other aspects of circuit performance. (3 marks)

Propose an alternative circuit configuration which could provide an improved high frequency response. Give a brief account of the operation of the circuit but do not attempt to carry out any detailed analysis. (4 marks)

(Total 25 marks)

4. In the context of analogue integrated circuit design, discuss how each of the following functional blocks could be implemented in either bipolar or MOS technology :

(i) Current mirror (5 marks)

(ii) Level shifting circuit (5 marks)

(iii) Active load (5 marks)

(iv) Difference amplifier (5 marks)

(v) Complementary follower stage (5 marks)

Provide in each case a concise statement of the purpose of the block, a brief account of the mode of operation (including simple circuit schematics and design methodology where appropriate), and one distinct advantage of the method described.

(Total 25 marks)

5. Describe the operation of each of the following, illustrating your answers as appropriate with basic circuit schematics, annotated block diagrams or simple sketches :

(i) R-2R digital to analogue converter (9 marks)

(ii) Quantised feedback analogue-to-digital converter (8 marks)

(iii) Charge-balance frequency to voltage converter (8 marks)

(Total 25 marks)

6. With the aid of a labelled block diagram describe the basic functionality of a Phase Locked Loop (PLL) and explain how (a) the phase detector and (b) the loop filter could be implemented.

(7 marks)

Explain how a PLL could be configured for :

(i) Division of a reference frequency by an arbitrary ratio;
(ii) Phase modulation;
(iii) Frequency modulation.

(6 marks)

Briefly outline what aspects of dynamic PLL behaviour are of practical relevance to the designer in implementing PLL-based systems and explain what simplifying assumptions are usually made in the mathematical analysis of PLL behaviour. (4 marks)

A PLL is locked to the frequency of an incoming signal when that frequency changes by $\Delta\omega$ to a new frequency still within the capture range. It can be shown that the consequent fractional phase error is given by :

$$\frac{\phi_e}{\Delta\omega/\omega_n} = \omega_n t\, e^{-\omega_n t}$$

where $\omega_n$ is the system natural frequency.

Determine at what time the phase error has a maximum value.
Deduce the maximum relative phase error that occurs before the system regains lock.
Obtain an expression for the fractional frequency error and determine at what time the frequency error is instantaneously zero.

(6 marks)

What practical steps should be taken to ensure that time taken to regain lock is minimised ? (2 marks)

(Total 25 marks)

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**END**