ES3900

THE UNIVERSITY OF WARWICK

Third Year Examination: June 2012

FUNDAMENTALS OF MODERN VLSI DESIGN

Candidates should answer <u>all</u> the questions given in each of the two sections.

Time Allowed: 3 hours.

Only calculators that conform to the list of models approved by the School of Engineering may be used in this examination. The Engineering Data-book and standard graph paper will be provided.

Read carefully the instructions on the answer book and make sure that the particulars required are entered on each answer book.

USE A SEPARATE ANSWER BOOK FOR EACH SECTION

SECTION A

1. State the Boolean expression describing the functionality of the logic block shown in Figure 1 below. (1 mark)

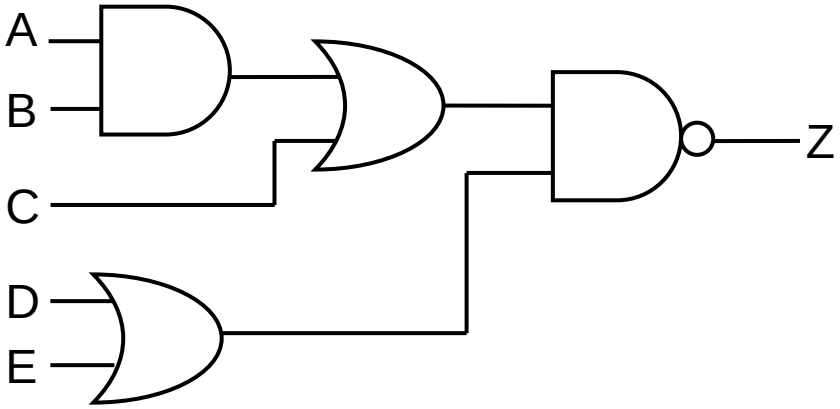

Figure 1.

Draw circuit schematics for the pull-up and pull-down FET networks required to implement the circuit as a complex static CMOS gate. (4 marks)

Together with a brief justification of your reasoning, give the widths of each of the FETs (assumed to be of minimum length) if the complex gate is to have size S = 1, and state the Logical Effort for each of the inputs. (4 marks)

Identify identical Euler paths (if they exist) around the pFET and nFET networks and draw a stick diagram representation, including a key to the symbols used, of a compact layout for the gate that would be suitable for fabrication in standard cell layout style. (6 marks)

Compare and contrast the relative advantages and disadvantages of alternative layout strategies under the headings of Place and Route, Standard Cell, Partitioned Layout and Tiled Cell methodologies. Discuss whether any alternative to a standard cell layout would be desirable in this case. (6 marks)

Briefly compare and contrast the relative advantages and disadvantages of alternative design styles under the headings of Static CMOS, Pseudo-nMOS and Precharge-Evaluate methodologies.(4 marks)

(Total 25 marks)

Continued …

2. (a) Draw a block diagram of a 4-bit ripple-carry full adder. Provide the truth table for the adder, and from it derive Boolean expressions for the Sum and Carry signals for each bit.

Sketch circuit schematics showing the nFET and pFET transistors necessary to implement each stage of such an adder, assuming the design is based on static CMOS complex gates.

(9 marks)

(b) Describe the operation of the 6-transistor (6-T) static RAM cell shown in Figure 2 below. Your answer should specify the means of writing and reading either a '0' or '1' into and out of the cell. Briefly explain, but without attempting to provide detailed schematics, the need for additional circuitry to implement the write and read operations. (8 marks)

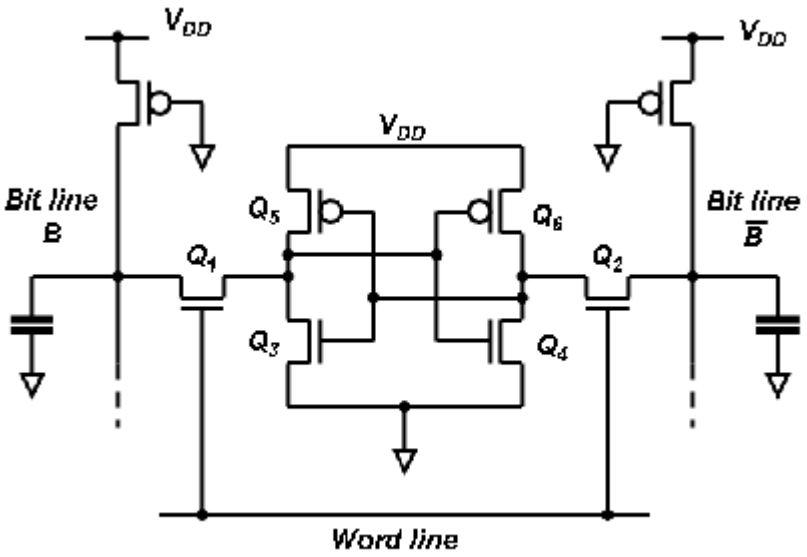

Figure 2.

(c) With the aid of appropriate circuit schematics, outline the principle of a CMOS transmission gate and sketch a suitable layout for such a gate using conventional stick diagram symbols. Explain how transmission gates can be used to implement a universal logic module of two input variables, illustrated with a truth table showing the evaluation of a specific logic function.

(8 marks)

(Total 25 marks)

Continued …

SECTION B

3. (a) Sketch out a block diagram illustrating the operating principles of a CMOS based operational amplifier. The block diagram should show the different stages in an op-amp and associated circuitry at a functional level. Briefly explain the purpose of each component diagram for the operational amplifier.

(6 marks)

Now sketch out a circuit diagram for a CMOS operational-amplifier. Your circuit should include key capacitors including the Miller capacitance. What is the purpose of the Miller capacitor and why is it an issue when designing cost-effective CMOS circuitry?

(6 marks)

(b) Describe two of the five possible analogue capacitors that can be made in a standard epi silicon CMOS process and sketch in each case a cross-section of the component. Comment on the nature of the capacitance per unit area and matching accuracy of your choices.

(8 marks)

(c) An analogue CMOS circuit requires a low pass filter with a corner frequency of 10 kHz. It is desirable to minimise the size of the chip die. Describe the design of a filter that will satisfy this constraint and explain your reasoning. Estimate the size required of the filter components.

(10 marks)

(Total 30 marks)

Continued …

4. (a) Give at least three advantages and three disadvantages of SOI CMOS over CMOS technology for low power low voltage devices.

(6 marks)

(b) Explain the differences, in terms of structure and fabrication, between a partially depleted SOI MOSFET and a fully depleted SOI MOSFET.

(4 marks)

(c) Briefly discuss what a body contact is and why it is important for the performance of an SOI CMOS MOSFET. Sketch two examples of how body contacts are made for a partially depleted SOI MOSFET.

(6 marks)

(d) Sketch the cross-section of a double gated SOI MOSFET device. What is the advantage of this device over a normal SOI MOSFET.

(4 marks)

(Total 20 marks)

END