**ES3900**

**THE UNIVERSITY OF WARWICK**

**Third Year Examination: June 2010**

**FUNDAMENTALS OF MODERN VLSI DESIGN**

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**Candidates should answer FOUR QUESTIONS, TWO from SECTION A and TWO from SECTION B.**

**Time Allowed: 3 hours.**

**Only calculators that conform to the list of models approved by the School of Engineering may be used in this examination. The Engineering Data-book and standard graph paper will be provided.**

*Read carefully the instructions on the answer book and make sure that the particulars required are entered on each answer book.*

**USE A SEPARATE ANSWER BOOK FOR EACH SECTION**

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## SECTION A

1. Derive, giving an explanation of your reasoning, circuit level schematics for the nFET and pFET networks required to design a static CMOS complex gate implementing the Boolean function:

$$f = \overline{A(B+C)+D+EF}$$ (4 marks)

Explain the concept of an Euler path around a network of transistors and determine whether identical Euler paths exist for both the nFET and pFET networks. If so, give an example of such paths and give two implications for devising a compact layout for the circuit topology.

(3 marks)

Sketch an appropriate layout using stick-diagram symbols for the complex gate. Include with your sketch a key to the various mask layers and contacts. (8 marks)

List other features, not conventionally shown in a stick diagram, which would also need to be specified in the layout. (3 marks)

For what reasons would additional types of contact be required? Suggest how many should be included in the layout and where they should be placed. (3 marks)

Identify any features of the layout you have devised that would make it suitable for standard-cell type composition and outline advantages and disadvantages of a standard-cell layout approach in hierarchical design methodology. (4 marks)

(Total 25 marks)

2. Explain how the following design styles differ from static CMOS:

(a) pseudo-NMOS

(b) precharge-evaluate logic

For (a) illustrate your answer with reference to the design, at the transistor level, of a 2-input NAND gate and a 2-input NOR gate and, for (b) the design of an inverter and an OR-AND-INVERT (OAI) gate. (6 marks)

For the case of an inverter implemented in pseudo-NMOS derive a criterion, in terms of transistor dimensions, required to give acceptable performance. (5 marks)

In pseudo-nMOS design show how this criterion would be applied to:

(i) 2-input NAND and NOR gates

(ii) AND-OR-INVERT (AOI) gates

(2 marks)

Describe how the problems of charge sharing and spurious (false) evaluation can occur in precharge-evaluate logic design. In each case propose one possible solution to the problem.

(6 marks)

Compare and contrast the relative advantages and disadvantages of the static CMOS, pseudo-nMOS and precharge-evaluate design styles. (6 marks)

(Total 25 marks)

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3. Describe the operation of a CMOS transmission gate at the transistor level and sketch a possible physical layout for a single gate using a stick diagram representation. Assume that to satisfy the design requirements control signals must be routed vertically through the cell and inputs and outputs must be routed horizontally. (5 marks)

   Explain how transmission gates can be used for implementing:

   (a) level-sensitive latches; (5 marks)

   (b) master-slave latches; (5 marks)

   (c) multiplexers; (5 marks)

   (d) logic gates; (5 marks)

(Total 25 marks)

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## SECTION B

4. a) How does a BiCMOS process differ from either Bipolar or CMOS processes? Sketch the circuit schematic diagram for an inverter fabricated in BiCMOS technology.

(6 marks)

b) Give two advantages and two disadvantages of Bipolar over CMOS technology.

(4 marks)

c) Sketch a transistor diagram of a CMOS two stage operational amplifier and give a detailed description of the operation of both the input and output stages.

(12 marks)

Discuss the function of the compensation capacitor in a CMOS two stage operational amplifier.

(3 marks)

(Total 25 marks)

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5. Write a brief essay on low-voltage low-power (LVLP) SOI CMOS devices and circuits. Your answer should both discuss the advantages and disadvantages of SOI CMOS technology over bulk and epi CMOS for:

a. LVLP SOI CMOS devices in general (10 marks)

b. LVLP circuits (10 marks)

c. Provide some typical applications. (5 marks)

(Total 25 marks)

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6. a) Explain the differences, in terms of structure, fabrication and performance, between a partially depleted SOI MOSFET and a fully depleted SOI MOSFET.

(8 marks)

b) Sketch the cross-section of a double gated SOI MOSFET device. What are the advantages of this device over a normal SOI MOSFET.

(5 marks)

c) Briefly discuss why body contacts are difficult to make in a SOI CMOS MOSFET. Sketch two examples of how body contacts are made for a partially depleted SOI MOSFET. Explain how adding this body contact affects the performance of a NAND gate.

(12 marks)

(Total 25 marks)

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**END**