ES3900

THE UNIVERSITY OF WARWICK

Third Year Examination: June 2011

FUNDAMENTALS OF MODERN VLSI DESIGN

Candidates should answer <u>all four</u> questions given in two sections.

Time Allowed: 3 hours.

Only calculators that conform to the list of models approved by the School of Engineering may be used in this examination. The Engineering Data-book and standard graph paper will be provided.

Read carefully the instructions on the answer book and make sure that the particulars required are entered on each answer book.

USE A SEPARATE ANSWER BOOK FOR EACH SECTION

SECTION A

1. Briefly describe the function of the p-block and n-block transistor networks when realising complex gates in the static CMOS style of design. (2 marks)

   Explain the concept of gate size and the design procedure whereby complex CMOS gates can be assigned a unique size. (4 marks)

   Draw a transistor-level schematic of the circuit required to implement the Boolean function given below as a complex static CMOS gate:

   $$f = \overline{(A+B)\bullet(C+D)}$$

   Mark on your schematic the transistor widths necessary for the gate to be of unit size, giving an explanation of your reasoning. (4 marks)

   Define the meaning of "Euler path" in the context of circuit layout topology. What are the implications of identical Euler paths existing for both nFET and pFET networks in a CMOS gate ? (3 marks)

   Identify appropriate Euler paths around each of the n-FET and p-FET networks in the logic function above and, using conventional stick diagram symbols, sketch the gate layout. Clearly label the gate inputs and output and provide a key identifying the mask layers shown in the stick diagram. (5 marks)

   What additional layers, not traditionally shown in the stick diagram representation, would be required for actual fabrication and why? (2 marks)

   If the complex gate above were to be designed using the precharge-evaluate design style, draw the corresponding transistor-level circuit schematic, give a brief explanation of the design methodology and describe any advantages or disadvantages in choosing this implementation. (5 marks)

(Total 25 marks)

Continued …

2. (a) The circuit schematic in Figure 1 shows a possible implementation of a memory array row or column address decoder. Explain the principle of operation and provide a truth table describing the functionality. (8 marks)

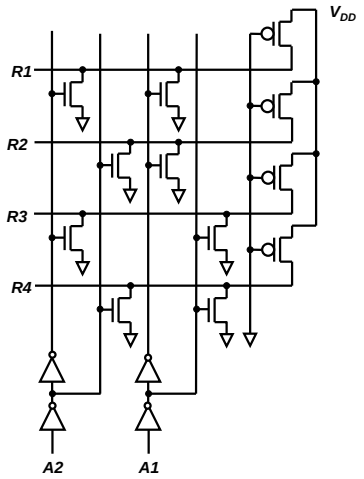

Figure 1

(b) The truth table in Figure 2 describes the functionality of a NOR-based ROM array. Devise a transistor-level circuit schematic showing one possible implementation and explain the principle of operation. (8 marks)

R_1	R_2	R_3	R_4	C_1	C_2	C_3	C_4
1	0	0	0	0	0	1	1
0	1	0	0	1	1	0	0
0	0	1	0	0	1	0	1
0	0	0	1	1	0	1	0

Figure 2

(c) Describe how a Programmable Logic Array (PLA) configured in NOR-NOR form using the pseudo-nMOS design style could be used to implement a set of logic functions expressed as sum-of-products Boolean equations. Outline a design *strategy* for the layout of such an array (a full detailed layout is not required) and explain what advantages such an implementation may have over alternative methodologies. (9 marks)

(Total 25 marks)

Continued …

SECTION B

3. (a) VLSI technology is mainly based upon silicon as the active material; however it is also possible to use gallium arsenide. What are the advantages and disadvantages of using gallium arsenide compared with silicon for a VLSI circuit?

(6 marks)

(b) Sketch the cross-section of a GaAs MESFET and briefly explain how it works.

(9 marks)

(c) Describe how GaAs transistors can be used to make digital logic devices. Illustrate your answer by showing the circuit for a GaAs inverter and explain the various components and how they work.

(10 marks)

(Total 25 marks)

Continued ….

4. a) Give at least three examples of physical factors that can affect the absolute resolution of a passive CMOS resistor. (3 marks)

b) Using the process parameters given in Table B1 (see below) calculate the dimensions necessary to produce a 2 kΩ resistor in

i) Poly 1

ii) N-Well

Sketch the layouts for the above resistors clearly labelling all the dimensions. Note that good layout practices should be followed. (8 marks)

c) Describe how a switched capacitor circuit can be used to emulate a passive resistor placed in series with other circuitry. Give two advantages of using switched capacitor circuits over passive resistors. (8 marks)

d) Design a switched capacitor circuit using the CMOS layers given in Table B1 in order to produce an equivalent resistance of 500 kΩ at a clock frequency of 200 kHz. Choose the appropriate layer for a capacitor design to achieve the most efficient design in terms of area. (6 marks)

Table B1.

Material	**Sheet resistance (Ω/□)**	**Minimum width (μm)**	**Minimum spacing (μm)**	**Capacitor layers**	**Capacitor value ($fF/\mu m^2$)**
Metal 1	0.1	4	4	MOS capacitor	2.2
Poly 1	20	2	3	Poly1 to Poly 2	0.8
Poly 2	30	2	3	Metal 1 to Poly 1	0.021
N-Well	1000	10	5	-	-
P-diffusion	100	5	4	-	-
N-diffusion	40	5	4	-	-

(Total 25 marks)

END