ES3B20

THE UNIVERSITY OF WARWICK

Third Year Examinations: Summer 2012

DIGITAL SYSTEMS DESIGN

Candidates should answer ALL FOUR QUESTIONS.

Time Allowed : 3 hours.

Only calculators that conform to the list of models approved by the School of Engineering may be used in this examination. The Engineering Databook will be provided.

Note: PIC16F84A for Q1 is provided with this paper.

Read carefully the instructions on the answer book and make sure that the particulars required are entered on each answer book.

USE A SEPARATE ANSWER BOOK FOR EACH SECTION

SECTION A

1. A digital temperature control system is to be designed for an industrial furnace. Once loaded and the door closed and locked, the furnace must be heated to a preset temperature and then allowed to cool, assisted by a steady flow of inert argon gas. When at ambient room temperature, the door lock mechanism must be released to allow operator access. An emergency stop capability is to be provided, whereupon the heating source is immediately switched off and rapid cooling achieved with a high flow rate of gas.

The system is to be microcontroller based, with input from push-button PB0 used to start the heating cycle and from PB1 for emergency stop. A contact switch produces a logic HIGH output signal when the furnace door is closed. The solenoid door lock mechanism and the electrical heating element are both activated by logic HIGH signals. Two digital temperature sensors, DTS0 and DTS1, indicate ambient room temperature and the final preset temperature respectively by outputting a logic HIGH signal. The gas flow valve has digital control signals corresponding to OFF, and LOW and HIGH flow rates.

A future system upgrade will incorporate a single character common-anode seven-segment display (SSD) to indicate diagnostic information.

Referring to the attached information on the PIC16F84A, provide the following :

(a) a software flowchart, excluding the SSD functionality (7 marks)
(b) a block diagram of the system, including the SSD interface (5 marks)
(c) initialisation code for the control program (3 marks)
(d) annotated code for the main program loop (10 marks)

(Total 25 marks)

Continued ….

2. (a) Briefly describe the following terms with reference to their usage in VHDL :

(i) Entity and Architecture;

(ii) Concurrent and sequential statements;

(iii) Structural descriptions;

(iv) Behavioural descriptions. (8 marks)

(b) The I/O specification of a system is given as follows :

- Ports CLK and PRST are input bits
- Ports ENBL and LOAD are input bits
- Port DATA is a 8-bit input only bus
- Port COUNT is a 8-bit bidirectional bus

Sketch a block diagram of the system and write the Entity declaration in VHDL. (4 marks)

The functionality of the system is defined as follows :

- On PRST then COUNT = 00001111
- On CLK if ENBL = 1 then COUNT = COUNT + 1
- On CLK if LOAD = 1 then COUNT = DATA

Write the Architecture for the module in VHDL. (4 marks)

(c) An eight-bit circular barrel-shifter is to be designed, capable of shifting data left or right in pre-settable increments of 0 to 7 places. Provide the following :

(i) A block diagram of the module;

(ii) The Entity declaration in VHDL;

(iii) The Architecture in VHDL, carefully noting any assumptions. (9 marks)

(Total 25 marks)

Continued ….

SECTION B

3. (a) Give the definition of Finite State Machine (FSM) and explain the difference between the Mealy and Moore type machine.

(5 marks)

(b) State the basic steps that should be followed in designing an FSM.

(5 marks)

(c) Design a digital circuit with serial data input (D) to generate logic 1 at the output (Z) only when three successive bits from the serial data input are: 001, 010, 100 or 111. Derive a state diagram, state transition table and logic equations for the next states and the output in order to implement the circuit.

(15 marks)

(Total 25 marks)

Continued ….

4. a) Describe a generic Field-Programmable Gate Array (FPGA) architecture.

(5 marks)

b) Briefly explain:

i) floating gate (3 marks)

ii) SRAM (3 marks)

and

iii) antifuse (3 marks)

FPGA programming technologies stating their advantages and disadvantages.

(c) Design a Look-up Table (LUT) to store values of a simple mathematical function $Y = X^3 + X + 2$ using ROM architecture, where $X \leq 7_{10}$.

(5 marks)

(d) Explain how combinatorial logic given by the function F below can be stored in 16×1 SRAM Look-up Table?

$F = \overline{B}\,\overline{C}D + \overline{A}C + A\overline{C}\,\overline{D}$

(6 marks)

(Total 25 marks)

END