UNIVERSITY OF WARWICK School of Engineering		Year 2011 Summer
ES3900	Title of Examination:– FUNDAMENTALS OF MODERN VLSI DESIGN	Section A & B Pages 1-11
Questions 1-4		Mark Allocation

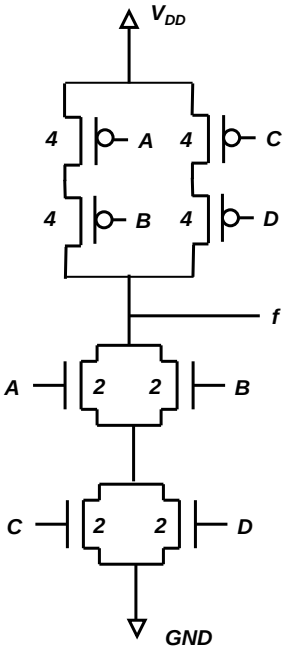
1.

- The p-block transistor network provides a transmission path from the output node to the supply rail (logic HIGH) for all input combinations where the output is logic “1”. The n-block transistor network provides a transmission path from the output node to ground (logic LOW) for all input combinations where the output is logic “0”.

2 marks

- The concept of gate size relates to the definition of an inverter of unit size, implemented in static CMOS, such that there is equal, minimum, signal propagation delay through the inverter regardless of whether the output transitions $0 \rightarrow 1$ or $1 \rightarrow 0$. The nFET is assumed to be fabricated with the minimum length and width allowed by the specific process and the sheet resistance of p-type diffusion is assumed to be twice that of n-type diffusion. Thus, for minimum length transistors, the pFET should be fabricated with twice the width of the nFET to offer the same resistance and hence the same CR time constant when driving a given capacitive load. Doubling the widths of both nFET and pFET results in an inverter of size 2 etc. The idea is extended to complex gates by ensuring that identical resistances, under worst-case conditions, exist in both pull-up and pull-down paths to that of an inverter of identical size and that those resistances are (approximately) equal. The worst-case scenario assumes that for transistors in parallel, only one need be switched on to complete the transmission path i.e. offering the higher resistance.

4 marks



UNIVERSITY OF WARWICK School of Engineering		Year 2011 Summer
ES3900	Title of Examination:– FUNDAMENTALS OF MODERN VLSI DESIGN	Section A & B Pages 1-11
Questions 1-4		Mark Allocation

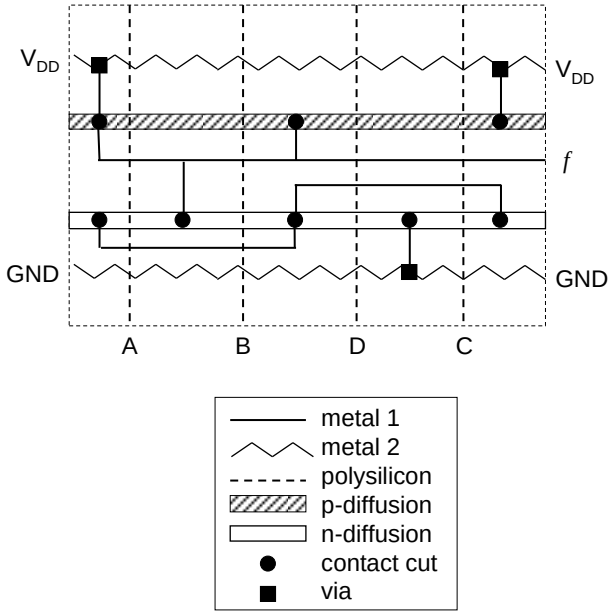
- For the n-block transistors, all should be width 2 units
  - equivalent to nFET width 2 in worst-case scenario for inputs A and B
  - same for inputs C and D
  - overall equivalent to single nFET width 1
- For the p-block transistors, all should be width 4 units
  - equivalent to pFET width 2 for inputs A and B
  - same for inputs C and D
  - overall equivalent, worst case, to single pFET width 2 i.e unit size gate

4 marks

- If a network can be traversed completely without retracing any part of the path, the route is termed an Euler path around the network.
  If identical Euler paths can be found for both n-FET and p-FET networks then :
  (i) each can be fabricated using a single, unbroken, line of diffusion
  (ii) identical ordering of gate signals to each block can be used, with each line of diffusion sharing common polysilicon interconnects, thus leading to a highly compact layout.

3 marks

- One possible identical Euler path for both n-FET and p-FET networks above would be ABDC



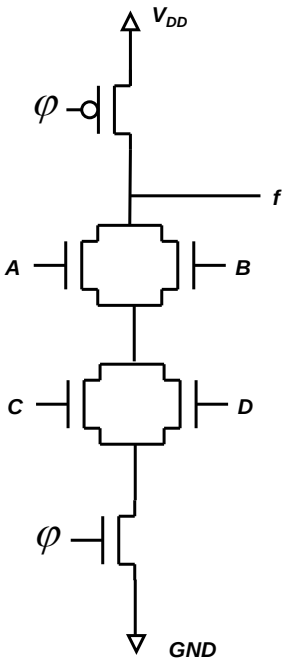
5 marks

UNIVERSITY OF WARWICK School of Engineering		Year 2011 Summer
ES3900	Title of Examination:– FUNDAMENTALS OF MODERN VLSI DESIGN	Section A & B Pages 1-11
Questions 1-4		Mark Allocation

- For a p-type substrate, an n-well would be required to isolate the p-diffusion forming the p-FET transistors. Vice-versa for a n-type substrate.
- Well and substrate taps (contacts) would be required for the n-well or p-well and for the substrate to ensure that locally the diodes formed between diffusion and well or substrate were reverse biased to prevent the possibility of excessive current flow (latch-up).

2 marks

- The precharge-evaluate design methodology replaces the p-block transistors with a single pFET and introduces an extra nFET between the n-block transistors and ground. A single-phase clock signal φ is required to be connected to the gates of those transistors. The output of the gate is precharged to logic '1' through the pFET on φ and the output evaluates and is conditionally discharged through the n-block transistors and series nFET on φ.
- Advantages of precharge-evaluate logic
  - Input capacitance less than for static CMOS
  - Only N+2 transistors needed for an N-input gate
  - No static power dissipation
- Disadvantages of precharge evaluate logic
  - Cannot cascade stages together directly due to problem of spurious evaluation
  - Charge sharing at internal nodes can result in degradation of logic levels



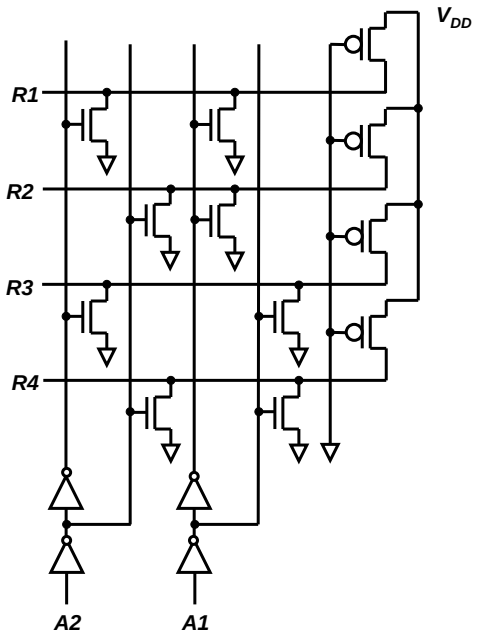
5 marks

Total

25 marks

2.

(a) Memory array row or column address decoder



- The circuit schematic shows a 2-bit decoder which would enable one (and only one) of row (or column) lines R1 – R4 to be selectively held logic HIGH depending on the status of address lines A1 and A2
- Lines R1 – R4 are pulled HIGH by the corresponding pFET, each with gate grounded and drain connected to V_{DD}
- R1 – R4 are conditionally pulled LOW by one or both of the corresponding nFETs according to the status of the address lines
- The array is populated with nFETs such that only one row line can remain HIGH for each input address
- For example, if A1 = A2 = '0' then R2, R3, and R4 are discharged to ground through one or both nFETs connected to these lines and only R1 remains HIGH as both nFETs connected to R1 are OFF
- Other combinations are shown in the truth table

A1	*A2*	*R1*	*R2*	*R3*	*R4*
0	*0*	*1*	*0*	*0*	*0*
0	*1*	*0*	*1*	*0*	*0*
1	*0*	*0*	*0*	*1*	*0*
1	*1*	*0*	*0*	*0*	*1*

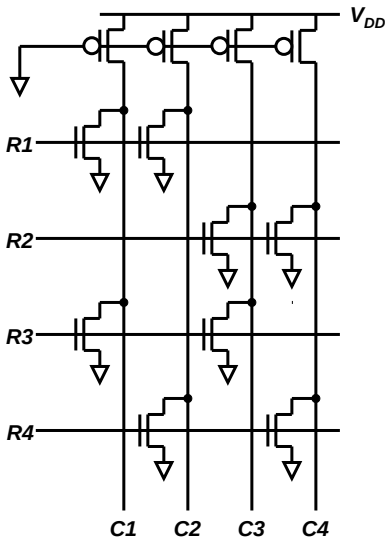
7 marks

7 marks

(b) NOR-based ROM array

R1	*R2*	*R3*	*R4*	*C1*	*C2*	*C3*	*C4*
1	*0*	*0*	*0*	*0*	*0*	*1*	*1*
0	*1*	*0*	*0*	*1*	*1*	*0*	*0*
0	*0*	*1*	*0*	*0*	*1*	*0*	*1*
0	*0*	*0*	*1*	*1*	*0*	*1*	*0*

- The data stored in ROM is shown in the truth table
- The functionality implies that an address decoder places a logic HIGH on one of lines R1 – R4 enabling the contents stored at that row to be read out
- One possibility to implement this is to pull column lines C1 – C4 to logic HIGH by ON pFETs and populate the memory array with nFETs such that C1 – C4 are selectively pulled LOW as required by the truth table when the corresponding row address is asserted
- For example if R1 = '1' then C1 = C2 = '0' and C3 = C4 = '1' for the nFET configuration shown in the circuit schematic
- Outputs dictated by the truth table are obtained when R2 – R4 are asserted



7 marks

7 marks

(c) Programmable Logic Array

- Any logic function expressable as a sum-of-products Boolean equation can be rewritten in NOR-NOR form by the recalling the De Morgan theorem :

i.e. If $X = A.B + C.D$

$X = \overline{(\overline{A} + \overline{B})} + \overline{(\overline{C} + \overline{D})}$ (by De Morgan's theorem)

$\overline{X} = NOR\,(NOR(\overline{A}, \overline{B}), NOR(\overline{C}, \overline{D}))$

- Hence any such logic function can be implemented in a PLA by replacing the AND and OR planes implied by the sum-of-products form with two NOR planes manipulating the complements of the input variables and producing the complement of the required logic function as the output
- The design strategy would firstly from an inspection of the system Boolean equations identify the number of inputs, outputs and distinct product terms required
- For generality the PLA design would allow for the generation of the complement of each input and for each input and complement to be fed into the first NOR plane
- The number of distinct product terms would dictate the number of outputs from the first NOR plane and hence inputs to the second NOR plane
- The second NOR plane generates the required number of outputs which are inverted to produce the logic functions called for
- NOR gates manipulating the inputs to both planes are pseudo-nMOS gates with the p-block transistors replaced with a single ON pFET
- The layout considerations should ideally employ principles of orthogonality of orientation of metal, diffusion and polysilicon layers
- An approach leading to a compact layout would route inputs and complements vertically in polysilion into the first NOR plane
- Metal could be routed horizontally in interdigitated form for output and ground, vertically for power to the pFETs
- Diffusion would be routed horizontally for both pFETs and nFETs with metal routed as appropriate
- Orientation of layers would be switched in the second NOR plane thus producing a compact rectangular layout
- Advantages of using a NOR-NOR pseudo-NMOS design are mainly a reduction in area and increase in speed compared with, say, static CMOS

11 marks

Total 25 marks

UNIVERSITY OF WARWICK School of Engineering		Year 2011 Summer
ES3900	Title of Examination:– FUNDAMENTALS OF MODERN VLSI DESIGN	Section A & B Pages 1-11
Questions 1-4		Mark Allocation

3(a) There are both advantages and disadvantages of using GaAs technology to make VLSI devices which have been discussed in the lecture course. The table below lists some of them:

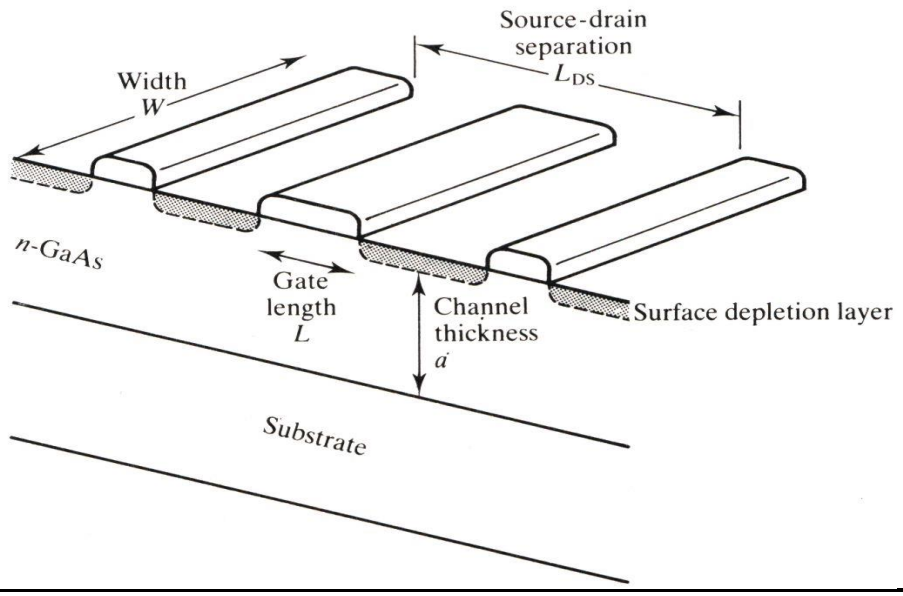
Table: Some advantages and disadvantages of GaAs technology

Advantages GaAs vs Si	**Disadvantages GaAs vs Si**
Higher electron mobility	**Lower hole mobility**
Lower noise at high frequencies	**Higher noise at low frequencies**
Semi-insulating substrate	**Higher cost**
Higher radiation hardness	**Great fragility**
Opto-electronic integration	**Lower thermal conductivity**

For example, when considering the difference in electron mobility, namely, silicon is 800 $cm^2V^{-1}s^{-1}$ whereas GaAs is much higher at 8000 $cm^2V^{-1}s^{-1}$. This means GaAs devices with the same doping will have **much** lower resistivity when compared to silicon. If you compare the speed of devices then consider the RC time constant for two devices with the same power dissipation then the GaAs channel dimensions will be longer and thinner. This will reduce the switching capacitance and so the device is significantly quicker

6 marks

3(b) The figure below shows the cross-section of a metal field effect transistor or MESFET as opposed to the silicon MOSFET structure.



The hole mobility is lower than the electron mobility in GaAs devices and so nearly all devices are n-type rather than p-type. Because there is no oxide layer, GaAs devices are MESFET devices and there is no inversion layer as in MOSFET devices. Instead the thickness of the channel is modulated by varying the thickness of the depletion region. In essence the metal semiconductor interface forms a Schottky diode that is modified by the gate voltage.

9 marks

3(c) Logic devices can be made from GaAs technology using a combination of depleted (D) and enhanced (E) MESFETs. These are both n-channel devices (and so have exploit higher carrier mobility) with the D type doped so they are normally in the ON state and the E type doped so they are normally in the OFF state. By normally, it means when the gate to source voltage is set to zero. In this way a logic inverter can be made simply from one E-MESFET and one D-MESFET as show below:

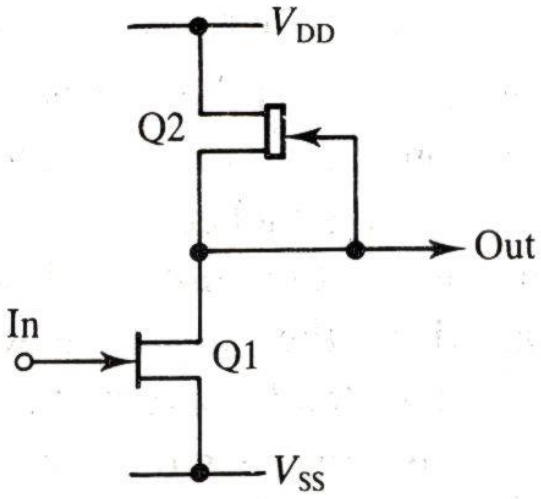


Figure: GaAs based logic inverter

The input signal drives the gate of the E-MESFET Q1 which is an n-channel device and so commoned to Vss and acts as a switch. The D-MESFET Q2 effectively acts as a resistive and because of its high source-drain resistance can also be used to match the load resistance on the output side.

12 marks

Note: Better circuits can use depletion mode only devices as easier to fabricate, higher voltage swings and better noise margins. Students could provide this as alternative solution to that provided in lectures.

(Total 25)

4(a) There are many factors that can affect the absolute resistance of a CMOS layer, these include: the level of doping (i.e. implantation process), the intrinsic stress, the absolute temperature, the level of crystal defects/impurities, the side diffusivity, the etching process, the geometric errors etc.

3 marks

4(b) The resistance of a CMOS component is given by:

$$R = 2R_{cont} + \frac{L}{W}R_{\square}$$

Where Rcont is the contact resistance, L the length and W width of the structure, and Rsq is the sheet resistance or resistance per square.

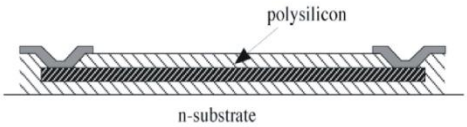
For a polysilicon CMOS layer, the sheet resistance is given as 20 Ω/square. If we require a 2 kΩ resistor then for W = 2 µm (minimum value) then L = 200 µm.

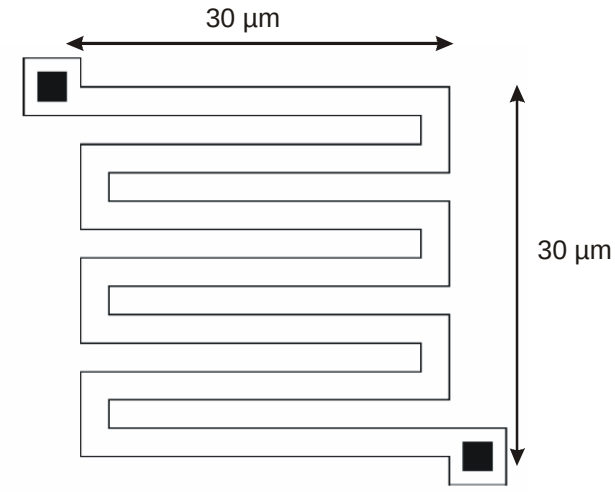
For an N-well component to give a resistance value of 2 kΩ then with a sheet resistance of 1kΩ per square (from Table) we need say W = 10 µm (minimum value) and L = 20 µm.

(Note: These values must always equal or exceed the minimum values shown in Table).

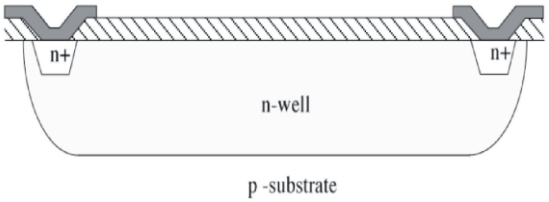
In both cases we assume that the contact resistance is milliohms and so has a negligible effect and can be ignored.

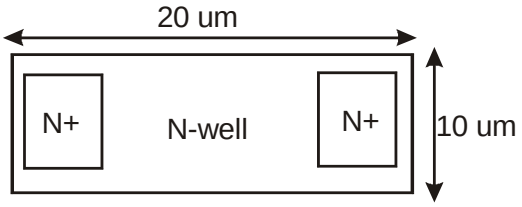
Example layout of Polysilicon resistor. The students can layout any reasonable layout based on the "serpentine" design. An example is below:





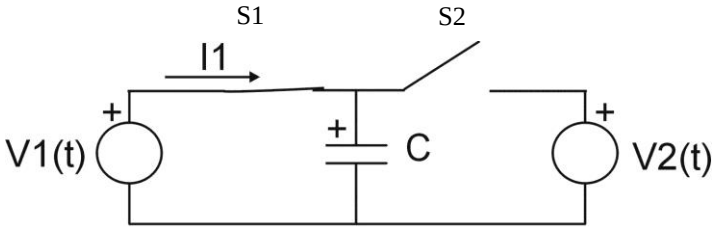
Example layout for N-Well with track width of 2 Ωm (not to scale)

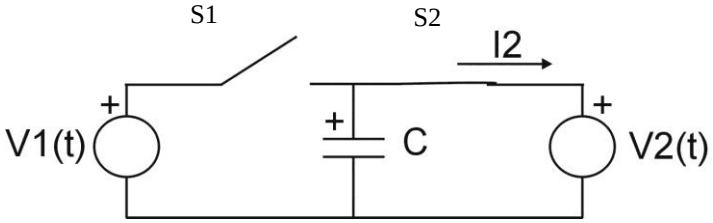




8 marks

4(c) Switched capacitor circuits are a simple way of producing a high value resistance, and are achieved with a capacitor and a switch. Such a circuit does require a two phase non-overlapping clock. They operate as shown below:





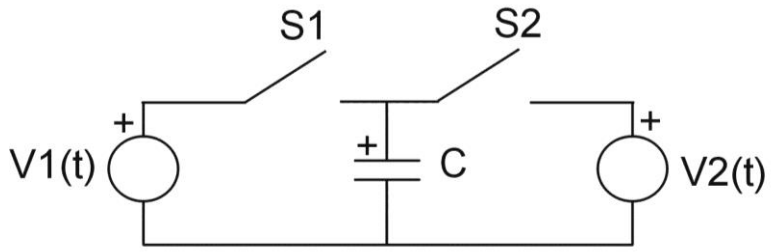
- S1 closed current moves from V1 to capacitor C (charge movement)
- S1 opens, charge remains on capacitor
- S2 closed current moves from capacitor to V2

Hence carriers have moved from V1 to V2 over a certain length of time. If you consider the average movement of charge then the circuit has a current flowing from V1 to V2

The two main advantages are that the device is much smaller as it only requires one capacitor and two switches. Secondly, the absolute resistance of the resistor is higher as capacitors have a higher accuracy than resistors.

8 marks

4(d) The equivalent resistance circuit involving a capacitor C and two switches S1 and S2 is shown below.



For 200 kHz the time period is 5 µs, thus using C = T/R then C = 10 pF. Using the data provided in Table B1 and use a MOS capacitor at 2.2 fF/µm2. Hence for square capacitor required 4,545 μm^2 making the capacitor 67 µm × 67 µm.

6 marks

Total 25