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Barrier reduction and current transport mechanism in Pt/n-InP Schottky diodes using atomic layer deposited ZnO interlayer

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ABSTRACT

Modification of interface properties in Pt/n-InP Schottky contacts with atomic layer deposited ZnO interlayer (IL) (5 and 10 nm) has been carried out and the electrical properties were investigated using current–voltage (*I*–*V*) and capacitance–voltage (*C*–*V*) techniques. The insertion of ZnO IL in the Pt/n-InP interface reduced the effective barrier height. The barrier heights from *C*–*V* method were higher with respect to those from *I*–*V* method. The interface state density for 5 nm thick ZnO was higher than that for 10 nm thick ZnO. The barrier heights according to thermionic field emission model showed much closer to those from *C*–*V* method. Surface passivation and interfacial dipole were suggested to modulate the Schottky barrier at the Pt/ZnO/n-InP interface.

1 Introduction

Recently, atomic layer deposition (ALD) growth of ZnO has gained significant interest due to its unique advantage [1–10]. ALD is a promising deposition method, based on self-limiting and saturated surface reactions, affording highly conformal and uniform films with accurate thickness control over large area [11]. ZnO layer by ALD can be grown at low temperatures, applicable to flexible substrates [4]. Because of these reasons, ALD grown ZnO has been used for various devices such as transparent electrode [6, 8], active medium for fiber-optic Fabry–Perot interferometer [9], photocatalysis [12], electron transporting layers in organic solar cells [13], and thin film transistor circuits [14]. Most of all, ALD grown ZnO has been employed to modify the interface characteristics in metal/semiconductor (MS) contacts [15, 16].

The Fermi levels (FLs) of metals are pinned near the charge neutrality levels (CNLs) of the semiconductors when the MS contacts are formed [17, 18]. This FL pinning limits to attain the metal work function dependent Schottky barrier. As presented in ref. 17, the CNLs of the most semiconductors are quite far from the valence band edge (e.g., GaN: 2.3 eV, ZnO: 3.27 eV, 4H-SiC: 1.55 eV, GaAs; 0.55 eV, InP: 0.6 eV, and Si: 0.2 eV). This in turn hinders to

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obtain good ohmic contact with a low contact resistance and good Schottky contact with a low leakage current. In this respect, alleviation of strong FL pinning using an interlayer (IL) grown by ALD has been demonstrated for many semiconductors. For example, Agrawal et al. achieved a barrier height of 0.15 eV in Ti/n-Si contacts with a 1 nm thick TiO_2 IL [19]. Kim et al. reported a significant reduction in contact resistivity for metal/n-GaAs using a ZnO IL [20]. AlN IL has been studied as a passivation layer for GaN-based power devices [21]. Akazawa and Hasezaki utilized a 1 nm thick Al_2O_3 IL in metal/GaN Schottky diodes and observed the increased barrier height with a Al_2O_3 IL [22]. However, they also observed that it became almost independent of the metal work function, although FL depinning by blocking metal wave function was expected. Hence more comprehensive and systematic approach is required for each IL/semiconductor structure.

It was shown in high-k HfO_2 on GaAs that about 2 nm thick ZnO IL could passivate the interface states, especially in the bottom half of the GaAs band gap [23]. About 1.5 nm thick ZnO was also found to act as an effective passivation layer for HfO_2 films on InP substrate [24]. Due to the high electron affinity of ZnO [15], ZnO/semiconductor can provide negative conduction band offset. Recently, Algadi et al. employed a 10 nm thick ZnO IL in indium tin oxide (ITO)/InP Schottky photodetectors and they attributed the improved efficiency to the hole barrier by the valence band offset at the ZnO/InP interface [25]. About 14 nm thick ZnO encapsulation layer for InP quantum dots was found to improve the solar cell performance [26]. Zhu et al. deposited ZnO/AlN (220 nm/1.9–11.4 nm) stacks on Ti substrate and found the improved piezo-electric performance [27]. Using ZnO as an IL in Pt/GaN Schottky contacts, we observed the average barrier height (ideality factor) of 0.64 eV (2.33) and 1.01 eV (1.16) for 5 and 20 nm thick ZnO, respectively [16]. All these works suggest the importance of relatively thick ZnO IL (> 5 nm). Furthermore, increasing the thickness above 2 nm can provide better surface coverage and reduction in the density of dangling bonds. In this work, we prepared two different thick ZnO ILs to modulate the electrical properties of Pt/n-InP Schottky diodes.

2 Experimental

Pt/ZnO/InP Schottky junctions were fabricated using a single-side polished and undoped InP (100) substrate (thickness: 350 μm, carrier concentration: $\sim 1 \times 10^{16}$ cm^{-3}). After cutting the wafer into small pieces (about 5 × 10 mm), native oxide was removed by dipping into an HCl:H_2O (1:1) solution. Two different thick ZnO layers grown by thermal ALD at 100 °C were obtained by varying the number of ALD cycles. Diethyl-zinc (DEZn: $Zn(C_2H_5)_2$) and H_2O were used as the Zn precursor and the oxidant, respectively. About 100 nm thick Al metal was deposited over the entire back surface of the samples to serve as an Al back contact. For Schottky contacts, 50 nm thick Pt metal (diameter: 500 μm) was deposited on the front surface through a shadow mask. The inset in Fig. 1a shows a schematic diagram of Pt/ZnO/InP/Al structure. During the thermal annealing process for ohmic contact, phosphorous can out-diffuse from the InP front surface. Hence, InP substrate was employed as a proximity cap to cover the front surface [28]. Recently, it was shown in Al/n-InP Schottky diode that the rectifying characteristics was improved after annealing at 400 °C for 3 min [29]. These works indicate that the annealing process for Al/n-InP structure can change the surface condition for InP and degrade the ohmic contact property. Due to these reasons, we did not perform the thermal annealing for Al/n-InP before forming the ZnO layer on InP. Capacitance–voltage (C–V) and current–voltage (I–V) characteristics were measured using a HP 4284A LCR meter and a Keithley 238 current source, respectively.

3 Results and discussion

First, we analyzed the C–V characteristics under reverse bias to obtain the flat-band barrier height. The capacitance in the Schottky diode is varied with the applied voltage through the following relation [30]

$$\frac{A^2}{C^2} = 2\left(\frac{V_{bi} - V - kT/q}{qN_D\varepsilon_S\varepsilon_0}\right) \quad (1)$$

where A is the contact area, V_{bi} is the built-in potential, N_D is the carrier concentration ε_0 is the permittivity of free space, and ε_S is the dielectric constant of the semiconductor (ε_S = 12.4 for InP). From the plot of A^2/C^2 vs. V, the Schottky barrier

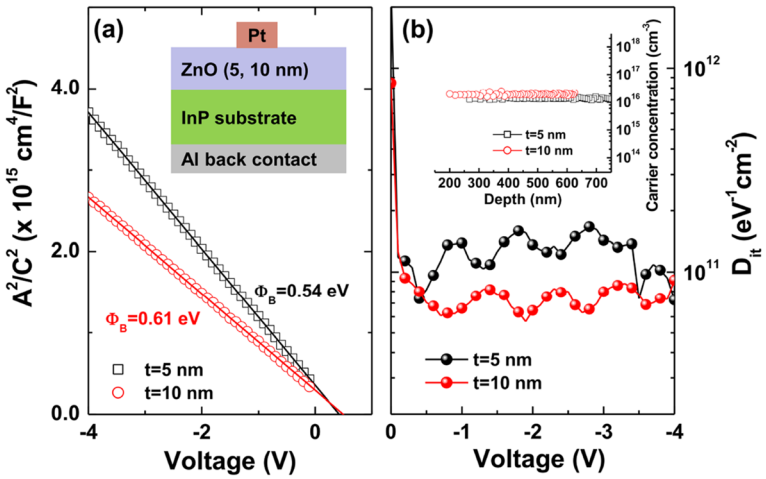

Fig. 1 **a** Plots of A^2/C^2 versus V measured at 1 MHz and **b** interface state density calculated from high-low frequency method. The insets in **a** and **b** show a schematic diagram of Pt/ZnO/InP/Al structure and plots of carrier concentration versus depth, respectively

height can be obtained by $q\phi_B^{C-V} = qV_0 + qV_n + kT$, where V_0 is the intercept with the voltage axis and $qV_n = E_C - E_F$. From the slopes of A^2/C^2 vs. V plots as shown in Fig. 1a, the N_D values were calculated to be 1.36 × 10^{16} and 1.92 × 10^{16} cm^{-3} for 5 and 10 nm thick ZnO, respectively. Noe that the inset in Fig. 1b shows the plots of carrier concentration versus depth. The barrier heights were calculated to be 0.54 and.0.61 eV for 5 and 10 nm thick ZnO, respectively.

The interface state density (D_{it}) was calculated using the high-low frequency method, in which D_{it} is given by [31]

$$D_{it} = \frac{1}{qA}\left[\left(\frac{1}{C_{LF}} - \frac{1}{C_i}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_i}\right)^{-1}\right] \quad (2)$$

where C_{HF} and C_{LF} are high and low frequency capacitances, respectively (1 MHz and 1 kHz, in order), and C_i is the interfacial capacitance. The attained D_{it} versus V plots are shown in Fig. 1b, revealing the lower interface state density for 10 nm thick ZnO.

Figure 2a shows the current density–voltage (J–V) data at room temperature. The Schottky contacts without ZnO IL (i.e., t = 0 nm) were also included as a reference. With ZnO ILs, the current values increased for both forward and reverse bias conditions. Barrier height and ideality factor for each sample were extracted assuming the thermionic emission (TE) to be dominant for the forward J–V characteristics [30]. In TE model, the current density is given by

$$J = A^{**}T^2 \exp(-q\phi_B/kT)[\exp\{q(V - IR_S)/nkT\} - 1] \quad (3)$$

where A^{**} is the effective Richardson constant (9.4 $A/cm^2\ K^2$ for n-InP), ϕ_B is the effective barrier height, R_S is the series resistance, and n is the ideality factor. Figure 2b shows plots of barrier height versus ideality factor obtained from several contacts for each sample. Compared to the reference sample, the barrier height decreased and the ideality factor increased with a ZnO IL. For the samples with a ZnO IL, the barrier height from I–V is lower than those from C–V, associated with the nonuniform interfacial layer and the interfacial charges at MS interface [32]. Figure 2b also shows that the ideality factor became higher than 2 with a ZnO IL. Normally the ideality factor is found to be in the range of 1 and 2 in InP Schottky diodes. Such high ideality factor can be due to the potential drop in the ZnO IL [33, 34], nonuniform interface [35] and the involvement of tunneling current.

As suggested by Card and Rhoderik [36], the interface state density is related to the voltage-dependent ideality factor $n(V)$ as follows

$$D_{it}(V,T) = \frac{1}{q}\left[\frac{\varepsilon_i\varepsilon_0}{\delta}(n(V,T) - 1) - \frac{\varepsilon_S\varepsilon_0}{W_D}\right] \quad (4)$$

where W_D is the deletion width at zero voltage, ε_i and δ are the dielectric constant and the thickness of the interfacial layer, respectively. Figure 2c shows the interface state density obtained using the method by Card and Rhoderik [36]. Like high-low method shown in Fig. 1b, lower interface state density is observed for 10 nm thick ZnO. Kang et al. reported that an interfacial layer observed from the HfO_2 (2 nm)/InP interface was not observed from the HfO_2 (> 6 nm)/InP interface, attributed to the in-situ self-cleaning effect [37]. Chang et al. deposited ~ 7.4 nm

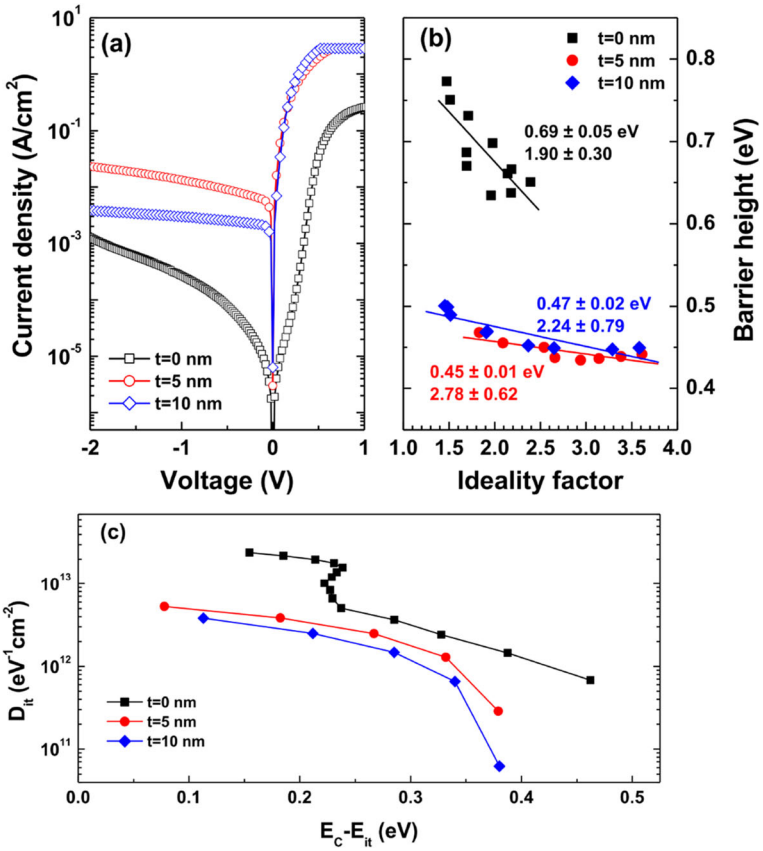

Fig. 2 **a** Current density–voltage (J–V) curves for each sample, **b** plots of barrier height versus ideality factor, and **c** interface state density obtained from forward current–voltage (I–V) characteristics

thick HfO_2 film by ALD on native oxide covered InGaAs and observed the removal of oxide layer [38]. Hou et al. deposited ~ 9 nm thick Al_2O_3 by ALD on native oxide (~ 2.8 nm) covered InSb and observed a similar in-situ cleaning of native oxide [39]. Based on these works, we speculate that the in-situ self-cleaning becomes more effective for thicker IL. For this reason, lower interface state density might be obtained for 10 nm thick ZnO. In addition, the lower interface state density is observed for the samples with a ZnO IL compared to the sample without ZnO IL. This indicates that surface passivation due to ZnO IL occurred at ZnO/InP interface.

Figures 3a and b show the typical J–V curves measured at various temperatures. The linear portion in the forward J–V curves becomes narrower with increasing the temperature. As the linear range of the forward J–V plots is reduced, the accuracy of the obtained barrier height and ideality factor is poorer. Hence, we did not use the TE model expressed by Eq. (3). Instead, Cheung and Cheung model was employed to calculate both the barrier height and the ideality factor. In this model [40], the barrier height and the ideality factor can be obtained using the following equations

$$dV/d(\ln I) = nkT/q + IR_S \tag{5}$$

$$H(I) = V - (nkT/q)\ln(I/AA^*T^2) \tag{6}$$

where $H(I) = n\phi_B + IR_S$. Figure 4a shows $dV/d(\ln I)$ and H(I) plots as a function of current (I) at 300 K and the similar procedure was applied to other temperatures. The obtained barrier heights and the ideality factors are shown in Fig. 4b. Note that the ideality factor lower than unity was obtained above 375 K and thus, the data above 375 K were not included. Lower ideality factor and higher barrier height were observed for 10 nm thick ZnO. Here, we applied Eqs. (5) and (6) to the room temperature I–V data whose electrical parameters from Eq. (3) are shown in Fig. 2b. The barrier heights were calculated to be 0.45 (± 0.02) and 0.48 (± 0.03) eV for 5 and 10 nm thick ZnO, respectively. The ideality factors were found to be 2.10 (± 0.84) and 1.64 (± 0.76), respectively, for 5 and 10 nm thick ZnO. The obtained ideality factors are a little lower than those values in Fig. 2b. But still the values are higher than unity.

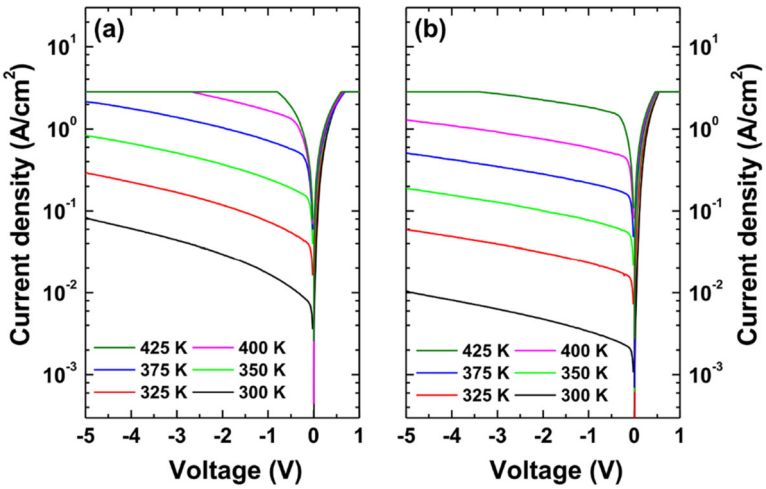

Fig. 3 Temperature dependent current density–voltage (*J*–*V*) characteristics for **a** 5 nm and **b** 10 nm thick ZnO

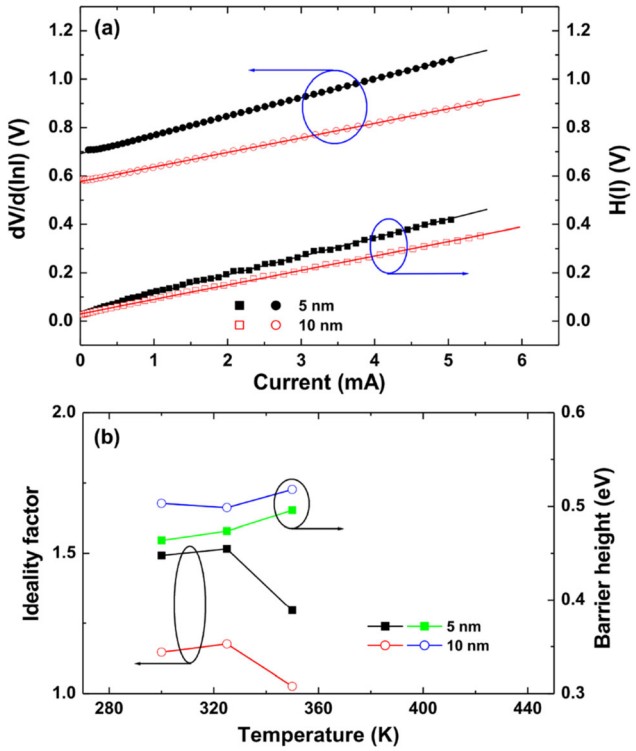

Fig. 4 **a** d*V*/d(ln*I*) and H(*I*) as a function of current (*I*) at 300 K and **b** the extracted ideality factors and barrier heights using Cheung and Cheung method

Such high ideality factor implies again the involvement of other current transport mechanisms such as thermionic field emission (TFE) or field emission (FE) than pure TE model.

Instead of TE model, we applied TFE model to analyze the reverse *J*–*V* characteristics, which is given by [41]

$$J_{\mathrm{R}}^{\mathrm{TFE}} = \frac{A^{**}T}{k}\sqrt{\pi E_{00} q\left[V + \frac{\phi_{\mathrm{B}}}{\cosh^2(E_{00}/kT)}\right]} \times \exp\left(-\frac{q\phi_{\mathrm{B}}}{E_0}\right)\exp\left(-\frac{qV}{\varepsilon'}\right) \quad (7)$$

$$\varepsilon' = \frac{E_{00}}{E_{00}/kT - \tanh(E_{00}/kT)}, \quad E_0 = E_{00}\coth(E_{00}/kT) \quad (8)$$

where $E_{00} = q\hbar/2(N_{\mathrm{D}}/m_{\mathrm{e}}\varepsilon_{\mathrm{S}})^{1/2}$ is the energy parameter. Here, E_{00} and ϕ_{B} were used as fitting parameters. Figures 5a and b show the comparison between experimental and fitting data. The obtained barrier heights shown in Fig. 6a exhibit almost constant values. These values are closer to the barrier heights from *C*–*V* method than those from *I*–*V* method. Using the E_{00} values obtained, the N_{D} values were calculated to be 4.15×10^{16} and 2.17×10^{16} cm^{-3} for 5 and 10 nm thick ZnO, respectively. For 10 nm thick ZnO, the N_{D} value is similar to that from *C*–*V* method. In contrast, the N_{D} value for 5 nm thick ZnO is higher than that from *C*–*V* method. Such discrepancy for 5 nm thick ZnO indicates that interface states might contribute to the current conduction by TFE model. This result is also consistent with the higher interface state density for 5 nm thick ZnO shown in Figs. 1b and 2c.

Using the E_{00} values obtained, we applied TFE model to the forward *J*–*V* characteristics, using the following equation [41, 42]

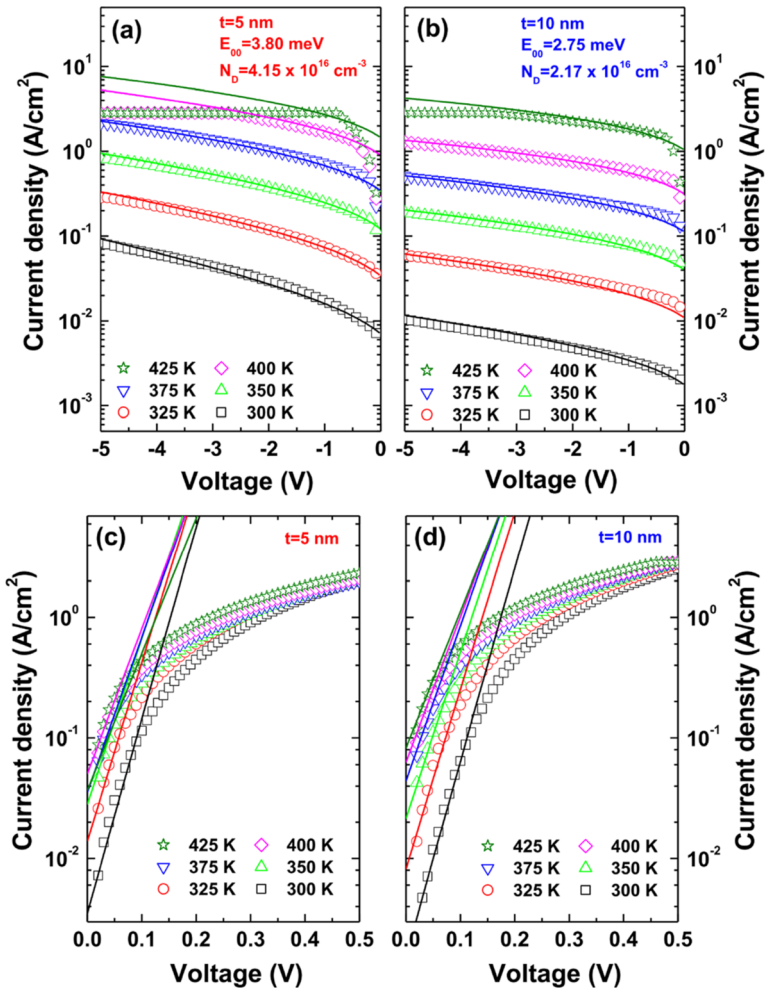

Fig. 5 Fitting results of the reverse bias current–voltage (I–V) data (**a** and **b**) and forward bias I–V data (**c** and **d**) according to thermionic field emission (TFE) model. The lines represent theoretical current components for each temperature

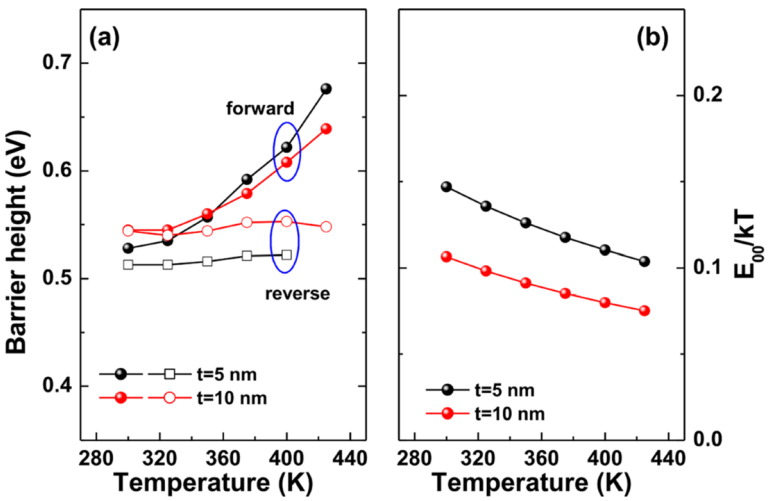

Fig. 6 **a** Barrier heights extracted from thermionic field emission (TFE) model and **b** plots of E_{00}/kT versus temperature

$$J_{\mathrm{F}}^{\mathrm{TFE}} = \frac{A^{**}T\sqrt{\pi E_{00}q(\phi_{\mathrm{B}} - V - V_n)}}{k\cosh(E_{00}/kT)} \exp\left[-\frac{qV_n}{kT} - \frac{q(\phi_{\mathrm{B}} - V_n)}{E_{00}\coth(E_{00}/kT)}\right] \quad (9)$$

Figures 5c and d show the experimental and fitting data and the barrier heights obtained are shown in Fig. 6a. Below 350 K, these values are similar to those from reverse *J*–*V* characteristics by TFE. Above 350 K, the barrier height increased with the temperature. Based on the TFE theory, Hudait and Krupanidhi found in n-GaAs Schottky diodes that the increase of barrier height with the temperature is higher when the carrier concentration is higher [43]. More rapid increase for 5 nm thick ZnO, thus, indicates again higher N_{D} value due to the involvement of interface states in the current conduction. Figure 6b also shows that E_{00}/kT is not much lower than unity, implying that the TFE model is more appropriate to explain the current transport [44]. Considering the barrier lowering in TFE model, given by [43, 45]

$$\Delta\phi^{\mathrm{TFE}} = \left(\frac{3}{2}\right)^{2/3} E_{00}^{2/3} V_{\mathrm{bi}}^{1/3} \quad (10)$$

The barrier heights at 300 K were determined to be 0.55 and 0.57 eV, respectively, for 5 and 10 nm thick ZnO. These values are quite similar to the barrier heights from *C*–*V* method. Lin et al. found in Ni/n-GaN Schottky diodes with a thin native oxide layer that the barrier height from TFE model is similar to that from *C*–*V* method [46]. Reddy et al. also observed the similar behavior in Au/Ni/n-GaN Schottky diodes [47]. These works indicate that the tunneling current contributed to the total current conduction and the reduced barrier height and the increased ideality factor were obtained by TE model. The barrier height from *C*–*V* method is measured under zero electric field (i.e., flat-band condition), approaching to the real barrier height. The similar values for barrier heights from TFE and *C*–*V* methods, thus, implies that the current conduction in the Pt/ZnO/InP Schottky contacts is governed by TFE model.

Hu et al. demonstrated that bulk and interface fixed oxide charges contribute to the barrier height reduction in Al/Al_2O_3/n-GaAs heterojunctions [48]. To explore any effect of fixed oxide charges on the barrier reduction in Pt/ZnO/n-InP structure, we performed *C*–*V* hysteresis measurements and the relevant plots are shown in Fig. 7. For both thicknesses, flat-band voltage (V_{FB}) shift is hardly observed and V_{FB} values are very similar. This indicates that the density of fixed oxide charges is very low and the contribution to the barrier reduction is insignificant. According to the oxygen areal density (σ) model [49], oxygen atoms move from higher σ side (σ_{H}) to lower σ side (σ_{L}) at the interface and thus, forming interfacial dipole ($\sigma_{\mathrm{L}} \rightarrow \sigma_{\mathrm{H}}$). Kim et al. compared the σ values of ZnO (0.168 cm^{-2}) and TiO_2 (0.208 cm^{-2}) to the σ value at GaAs side due to native oxide (0.1775 cm^{-2}) by averaging the σ values of Ga_2O_3 and As_2O_3 (0.207 and 0.148 cm^{-2}, respectively) [50]. Further, they argued in ZnO/TiO_2/GaAs interface that the interfacial dipole at TiO_2/GaAs interface (σ [TiO_2] > σ [GaAs]) directing to TiO_2 would increase the barrier and the interfacial dipole at ZnO/TiO_2 interface (σ [ZnO] < σ [TiO_2]) directing to TiO_2 would reduce the barrier. Assuming that the native oxides of InP are In_2O_3 and $InPO_4$ (σ values: 0.182 and 0.206 cm^{-2}, respectively), the average σ value at InP side becomes 0.194 cm^{-2}. Then, the relation of σ [ZnO] < σ [In_2O_3] holds at ZnO/InP interface, leading to the formation of interfacial dipole directing to InP side. This would reduce the barrier of Pt/n-InP contact.

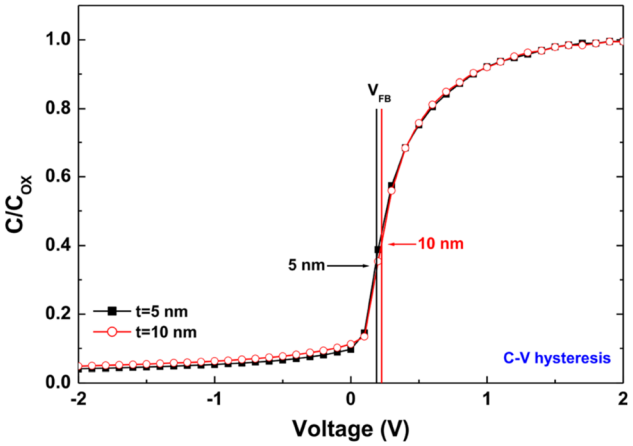

Fig. 7 Plots of capacitance–voltage (*C*–*V*) hysteresis measured at 1 MHz

In metal/IL/semiconductor structure, interfacial dipole can be present at metal/IL and IL/semiconductor interfaces [51]. According to the σ value difference as stated before, energy barrier can be reduced or enhanced according to the direction of interfacial dipole at the MS interface. Jang et al. could achieve low contact resistance MoS_2 transistor using a ZnO IL [52]. They attributed this to the following

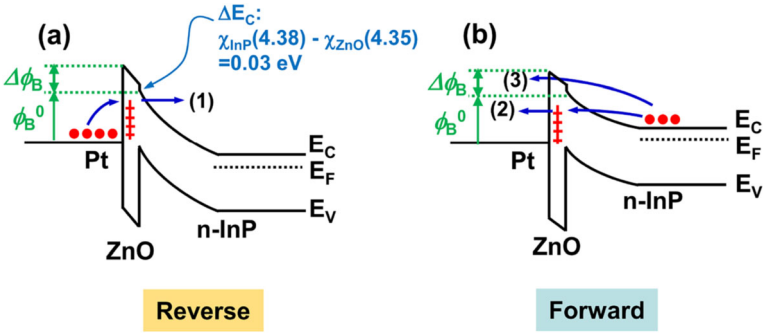

Fig. 8 Schematic band diagrams under **a** reverse bias and **b** forward bias conditions

mechanisms: (i) FL depinning at ZnO/MoS_2 interface due to the surface passivation and (ii) FL shifting of the contact metal due to the interfacial dipole at metal/ZnO interface, leading to additional barrier modulation. As shown in Fig. 2c, we observed lower interface state density with a ZnO IL. Hence, FL depinning might occur at ZnO/InP interface due to surface passivation. In any case (surface passivation or σ value difference), the barrier reduction would be possible at ZnO/n-InP interface.

Based on the results so far, we drew schematic band diagrams for Pt/ZnO/InP Schottky contacts as shown in Fig. 8. Using the electron affinities of InP (4.38 eV [53] and ZnO (4.35 eV) [54]), the conduction band offset (ΔE_C) was calculated as 0.03 eV. The barrier height ($\phi_B{}^0$) may correspond to the $\phi_B{}^{C-V}$ or $\phi_B{}^{TFE}$. $\Delta\phi_B$ is the sum of the energy barrier across the ZnO layer and ΔE_C. Under reverse bias condition, the current may flow mainly (1) across the depletion region. Under forward bias condition, electrons may travel (2) across the depletion region below 350 K. At high temperatures (above 350 K), more electrons gain sufficient energy to surmount higher barrier. Hence, $\phi_B{}^{TFE}$ in this region increases with the temperature. Most of all, the interface states for 5 nm thick ZnO might contribute to the total current more significantly.

It has been reported that the carrier concentration of ALD grown ZnO film can increase from $\sim 10^{17}$ up to 10^{20} cm^{-3} by increasing the ALD growth temperature [1, 10, 55, 56]. To explain the abnormally large reverse leakage current in GaN Schottky diodes, Hashizume et al. suggested that a thin surface barrier (TSB) formed by surface defects in the surface layer can induce significant tunneling leakage current [57]. Lingaparthi et al. also employed such TSB model to explain the reverse leakage current in Ga_2O_3-based Schottky diode [58]. By varying the ALD growth conditions, we can modify the carrier concentration of ZnO layer and the thin ZnO layer can act as a TSB. In that case, the TFE model combined with a TSB would be useful to analyze the current conduction. In this respect, this work will provide some guidance to understand the current transport mechanism in the Schottky diode with a ZnO IL.

4 Conclusion

As a modification method for interface characteristics in Pt/n-InP Schottky contacts, we employed atomic layer deposited ZnO interlayer (IL) (5 and 10 nm) and investigated its electrical properties. It was shown that the barrier heights from *C–V* method were higher than those from *I–V* method. The interface state density for 5 nm thick ZnO was calculated to be higher than those for 10 nm thick ZnO. High ideality factor than unity was obtained with a ZnO IL, indicating other current transport mechanism than pure TE model. The barrier heights using TFE theory became closer to those from *C–V* method, implying that TFE is a dominant current transport mechanism in the Pt/ZnO/n-InP contact. The analysis by TFE model showed that the interface states for 5 nm thick ZnO contributed to the total current with a higher level.

Acknowledgements

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