Extraction of Si-SiO_2 Interface Trap Densities in MOS Structures With Ultrathin Oxides

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***Abstract*—Si-SiO_2 interface trap densities can be measured in MOS structures with ultrathin oxides using charge pumping (CP) and small gate pulses. This presents three decisive advantages with respect to the conventional large gate voltage swing approach. First, the extraction is simple as carrier emission does not contribute to the CP signal so that the CP current magnitude directly reflects the interface trap density. Second, the tunneling current is strongly reduced allowing a more easy extraction of the CP signal and third, such a reduction prevents the insulator and the insulator–silicon interface from any degradation. By doing so, Si-SiO_2 interface trap densities are measured in MOSFETs with oxides which are 1.8 and 1.3 nm thick.**

***Index Terms*—Charge pumping (CP), MOS devices, tunneling current, ultrathin gate oxides.**

I. Introduction

In very large-scale integration (VLSI) MOS devices, conventional interface trap characterization techniques become unusable as soon as parasitic Fowler-Nordheim (FN) or direct tunneling currents become significant. This is an important problem as interface trap density $D_{\rm it}$ measurements have always been a standard characterization tool for technological processes. The use of charge pumping (CP) at high frequencies has been proposed, but the ratio CP over leakage currents remains small [1]. Considered unreliable or unfeasible [2], this extraction has been attempted from stress induced leakage current (SILC) [2], [3]. In this letter, $D_{\rm it}$ is measured simply with CP using small voltage pulses. This strongly increases the frequency range in which the CP signal can be measured allowing reliable $D_{\rm it}$ values to be obtained.

II. Principle of the Method

In CP and assuming an n-channel device, the transistor is switched between biases V_h in inversion and V_l in accumulation [$V_{\rm sw} = (V_h - V_l)$]. This allows the filling of the traps between the two Fermi level positions E_h and E_l at the interface, successively by electrons and holes. In the conventional large gate voltage swing approach, when returning from one level to the other, i.e., during the transition time, t_r or t_f of the gate signal, a part of the captured carriers is emitted toward the nearest band [4]. The other carriers, those trapped in defects located closer to the intrinsic level E_i, recombine with the other carrier type giving rise to a substrate current which is measured.

The use of small gate pulses has been proposed by Wachnik and Lowney [5]. Assuming rectangular gate pulses, they note that at Elliot curve maxima (curves for which V_l is scanned while keeping $V_{\rm sw}$ constant) [6], the traps situated at E_h and E_l are such that the capture rates $c_n(E_h) = n(E_h)\sigma_n v_{\rm th}$ and $c_p(E_l) = p(E_l)\sigma_p v_{\rm th}$ are equal. n and p are the electron and hole concentrations, respectively, at the Si-SiO_2 interface during the time at E_h and E_l. σ_n and σ_p are the trap cross sections for electrons and holes, respectively, and $v_{\rm th}$ is the average carrier thermal velocity.

As E_h and E_l correspond to Fermi level positions, one also has $e_n(E_h) = c_n(E_h)$ and $e_p(E_l) = c_p(E_l)$, where e_n and e_p are the emission rates for electrons and holes, respectively. As a result, when switching the device between V_h and V_l, the traps between E_h and E_l fill by capture before having emitted their carriers toward the nearest carrier band and emission does not contribute to the CP current. Then, $Q_{\rm cp}$, the charge recombining during one period of the gate bias, reads

$$Q_{\rm cp} = \frac{I_{\rm cp}}{f} = qA\int_0^K \int_{E_l}^{E_h} N_t(E,K)\Delta F(E,K)dEdK \quad (1)$$

where

$I_{\rm cp}$ CP current;
f gate signal frequency;
q absolute electron charge;
A device area.

$\Delta F(E,K)$ is the filling function variation derived by Wachnik and Lowney but extended to the case of a distribution of trap time constants [7], as unambiguously evidenced experimentally [8], [9]. K, the characteristic parameter of the trap distribution, is the distance of a trap to the Si-SiO_2 interface in the case of a pure tunneling mechanism [8]. K is the barrier height if the capture is thermally activated [9]. $N_t(E,K)$ is therefore the trap concentration at E and K.

With abrupt transition times, as assumed by Wachnik and Lowney [5], emission does not contribute to $Q_{\rm cp}$, regardless of the experimental conditions. In practical situations, emission is negligible if the trap at $E_{{\rm em},e}$ and $E_{{\rm em},h}$ that could emit their carrier are outside the $(E_h - E_l)$ interval after t_r or t_f, that is [10], [11]

$$(E_i - E_{{\rm em},h}) = -kT\ln(n_i\sigma_p v_{\rm th}t_r) > (E_i - E_l)$$

and

$$(E_{{\rm em},e} - E_i) = -kT\ln(n_i\sigma_n v_{\rm th}t_f) > (E_h - E_i). \quad (2)$$

Fig. 1(a) shows E_h and E_l between which emission can be neglected as function of $t_{r,f} = t_r = t_f$, for three values of σ_n

Manuscript received August 5, 2002. This work was supported by Ultimox/RMNT and RA-Nanodiel projects. The review of this letter was arranged by Editor B. Yu.

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Digital Object Identifier 10.1109/LED.2002.805008

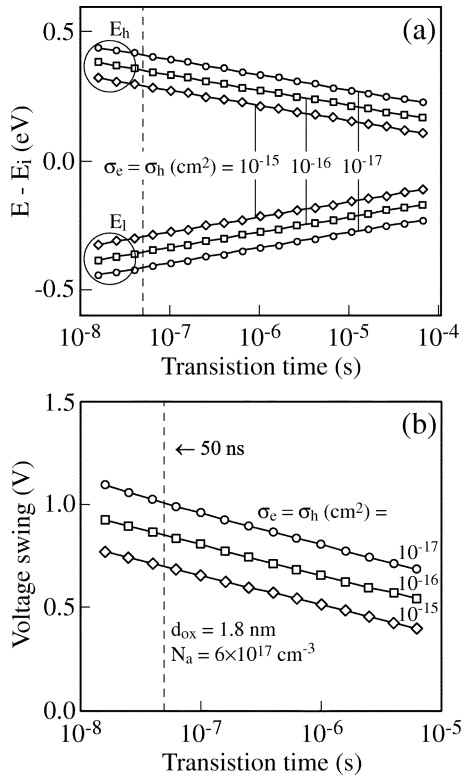

Fig. 1. (a) E_h and E_l positions at the interface between which emission can be neglected, as a function of the transition time of the gate signal for three values of the trap capture cross sections. (b) Corresponding $V_{\rm sw}$ values when $d_{\rm ox} = 1.8$ nm and $N_a = 6 \cdot 10^{17}$ cm^{-3}.

and σ_p. Fig. 1(b) gives the corresponding values of $V_{\rm sw}$ when $d_{\rm ox}$, the oxide thickness and N_a, the doping concentration, are equal to 1.8 nm and $6 \cdot 10^{17}$ cm^{-3}. The transition time, 50 ns, used for the measurements is shown Fig. 1. Depending on the cross sections, emission is negligible up to $V_{\rm sw} = 0.7$ to 1 V. As a result, if emission does not contribute to $Q_{\rm cp}$ and if the traps, from fast to slow traps, are filled in accumulation and in inversion, i.e., $\Delta F(E, K) = 1$ up to the largest possible values of K, $D_{\rm it}$, the areal trap concentration, can be obtained at Elliot curve maxima from

$$D_{\rm it} = \frac{Q_{\rm cp}}{qA\Delta E}. \tag{3}$$

Note that contrary to the large voltage pulse approach [4], $D_{\rm it}$ is independent of the trap cross sections and that if the biases corresponding to E_h and E_l are between the device threshold and flatband voltages, no quantization of the inversion and accumulation layers occurs so that ΔE can be obtained in a conventional manner. In the conventional large voltage swing approach, saturation of the traps with carriers is achieved by the large capture rates. In the small voltage swing mode, it is completed by increasing the time for capture, i.e., by decreasing the gate signal frequency. Therefore, increasing $V_{\rm sw}$ and reducing f, the interface trap density is obtained when $D_{\rm it}$ given by (3) becomes independent of $V_{\rm sw}$ and f (all the traps contribute to $Q_{\rm cp}$) in the $V_{\rm sw}$ region given in Fig. 1 (no emission).

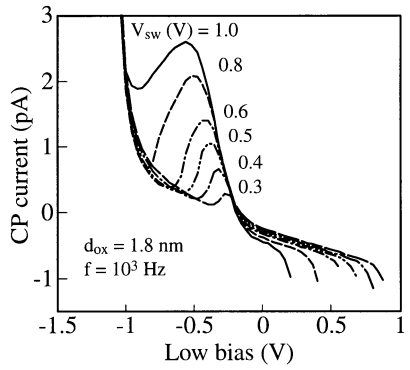

Fig. 2. Elliot curves recorded at 10^3 Hz from a device with $d_{\rm ox} = 1.8$ nm for different $V_{\rm sw}$ values.

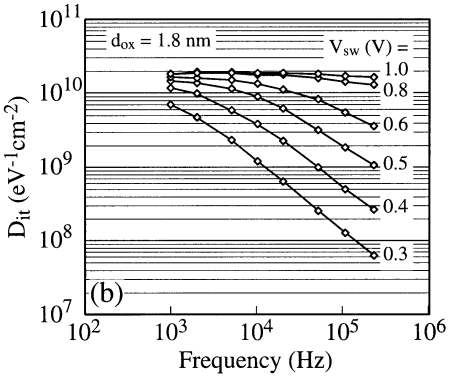

Fig. 3. Evolution of $D_{\rm it}$ given by (3) for the device of Fig. 2 as a function of the gate signal frequency for different $V_{\rm sw}$ values.

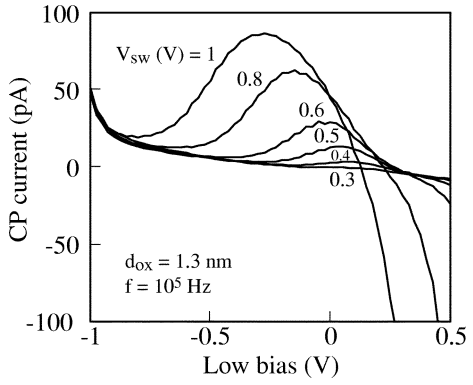

Fig. 4. Elliot curves recorded at 10^5 Hz from a device with $d_{\rm ox} = 1.3$ nm for different $V_{\rm sw}$ values.

III. Results

Fig. 2 shows Elliot curves recorded at 10^3 Hz from a MOS device with an oxide 1.8 nm thick, for $V_{\rm sw}$ values between 0.3 and 1 V. Under such small $V_{\rm sw}$ conditions, the CP current clearly emerges from the leakage current at such a low frequency [1]. However, removal of the leakage current by subtracting a curve recorded at lower frequency, where the CP current is negligible [1], is required.

The trap densities obtained are shown in Fig. 3. As expected, $D_{\rm it}$ calculated using (3), saturates when both increasing $V_{\rm sw}$

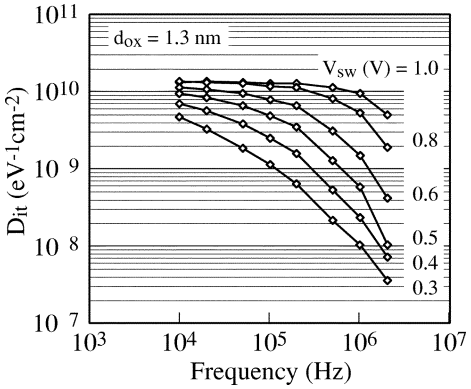

Fig. 5. Same curves as in Fig. 3 when $d_{\rm ox} = 1.3$ nm.

and reducing the signal frequency. Saturation of $D_{\rm it}$ occurs at low frequencies when $V_{\rm sw}$ equals 0.8 to 1 V, in agreement with Fig. 1 and with no quantization of the inversion or accumulation layers, so that $D_{\rm it} = 1.8\text{–}2 \cdot 10^{10}$ eV^{-1} cm^{-2}.

The results for a technology with $d_{\rm ox} = 1.3$ nm are shown in Figs. 4 and 5. In Fig. 4, as in Fig. 2, one can clearly see evidence of the advantage of using small gate pulses with regard to the leakage current: the CP current is easily measurable at $V_{\rm sw} = 0.3$ to 0.4 V; at $V_{\rm sw} = 1$ V CP curve edges begin to be swamped in the leakage current. In Fig. 5, the same behavior as in the previous device is obtained, except that frequencies higher than 10^4 Hz are now required to extract $Q_{\rm cp}$. $D_{\rm it}$ is around $1.3 \cdot 10^{10}$ eV^{-1} cm^{-2}.

IV. Conclusion

Interface trap densities can be measured in MOS transistors with ultrathin oxides using CP in the small voltage pulses mode. This strongly reduces the leakage current, prevents the devices from any degradation and allows $D_{\rm it}$ to be directly obtained from the CP current magnitude. Interface trap densities have been easily extracted from transistors with oxides 1.8 and 1.3 nm thick.

Acknowledgment

The author wishes to thank M. Gri from IMEP for technical assistance.

References

[1] P. Masson, J. L. Autran, and J. Brini, "On the tunneling component of the charge pumping current in ultrathin gate oxide MOSFETs," *IEEE Electron Device Lett.*, vol. 20, pp. 92–94, Feb. 1999.

[2] A. Ghetti, E. Sangiorgi, J. Bude, T. W. Sorsch, and G. Weber, "Tunneling into interface states as reliability monitor for ultrathin oxides," *IEEE Trans. Electron Devices*, vol. 47, pp. 2358–2365, Dec. 2000.

[3] D. Ielmini, A. S. Spinelli, M. A. Rigamonti, and A. L. Lacaita, "Modeling of SILC based on electron and hole tunneling—Part II: Steady-state," *IEEE Trans. Electron Devices*, vol. 47, pp. 1266–1272, June 2000.

[4] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. de Keersmaecker, "A reliable approach to charge-pumping measurements in MOS transistors," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 42–53, Jan. 1984.

[5] R. A. Wachnik and J. R. Lowney, "A model for the charge-pumping current based on small rectangular voltage pulses," *Solid State Electron.*, vol. 29, pp. 447–460, Apr. 1986.

[6] A. B. M. Elliot, "The use of charge pumping currents to measure surface state densities in MOS transistors," *Solid State Electron.*, vol. 19, pp. 241–247, 1976.

[7] D. Bauza and G. Ghibaudo, "Analytical study of the contribution of fast and slow oxide traps to the charge pumping current in MOS structures," *Solid State Electron.*, vol. 39, pp. 563–570, Apr. 1996.

[8] D. Bauza and Y. Maneglia, "In-depth exploration of Si-SiO_2 interface traps in MOS transistors using the charge pumping technique," *IEEE Trans. Electron Devices*, vol. 44, pp. 2262–2266, Nov. 1997.

[9] F. Rahmoune and D. Bauza, "Si-SiO_2 interface trap capture properties," *Microelectron. Eng.*, vol. 59, pp. 115–118, Nov. 2001.

[10] W. Shockley and W. T. Read, "Statistics of the recombination of holes and electrons," *Phys. Rev.*, vol. 87, pp. 835–842, 1952.

[11] R. N. Hall, "Electron-hole recombination in germanium," *Phys. Rev.*, vol. 87, p. 387, 1952.