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Low thermal conductivity porous Si at cryogenic temperatures for cooling applications

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Abstract

Porous Si thermal conductivity was determined in a wide temperature range from 20 to 350 K using the steady-state direct current method and a subsequent finite element method. The method was applied to a 40 μm thick porous Si layer of ~60% porosity, formed on p-type Si of resistivity 1–10 Ω cm. It was found that in the temperature range 20–80 K the thermal conductivity of the studied porous Si layer was more than four orders of magnitude lower than that of bulk crystalline Si, due to phonon confinement in the nanostructured skeleton composing porous Si. The temperature distribution as a function of distance from a heater on the porous Si layer and as a function of depth from the porous Si/metal interface was also calculated for different values of the applied electric power and for two different temperatures, 20 and 290 K, using a combination of experimental results and simulations. The effectiveness of local thermal isolation from the Si substrate by a thick highly porous Si layer in a wide temperature range was demonstrated, showing that this material is challenging for use in Si micro-cooling devices.

(Some figures may appear in colour only in the online journal)

1. Introduction

For the fabrication of efficient Si-based micro-cooling devices it is essential to develop a local low thermal conductivity substrate to thermally isolate the device from the highly thermally conductive bulk crystalline Si substrate. Free standing microstructures (membranes, cantilevers) are generally used to provide a platform for the integration of the above devices. As an alternative to the above fragile microstructures, a thick highly porous Si (PSi) layer locally formed on the Si substrate by electrochemical etching of Si can be used (Lysenko and Volz 2000, Nassiopoulou and Kaltsas 2000), which provides an excellent platform for the thermal isolation from the Si substrate due to its very low thermal conductivity compared with that of Si and its mechanical stability and compatibility with Si processing (Nassiopoulou 2013). At room temperature porous Si shows a thermal conductivity that is more than two orders of magnitude lower than that of bulk crystalline Si. The other advantage of porous Si is that layers of several tens of μm can be fabricated on the Si wafer, having a surface that is planar to that of the Si wafer. In addition, the different properties of porous Si, including its thermal conductivity, are tunable by tuning material porosity, morphology and structure by the electrochemical conditions used and the choice of type and resistivity of the Si substrate (Canham 1997, Lust and Lévy-Clément 2002). Due to the versatility of porous Si material depending on the above, there is a significant scattering of the values of its thermal conductivity that are found in the literature. The values found for porous Si fabricated from p-type Si range from 0.03 W m^{-1} K^{-1} to 7.33 W m^{-1} K^{-1} at room temperature for porosities of 89% to 45%, respectively (Gesele *et al* 1997, Srinivasan *et al* 2007). On the other hand, for PSi from (1 0 0) p$^+$-type wafers with resistivity in the range 10–20 mΩ cm the reported thermal conductivity values range from 0.3 to 80 W m^{-1} K^{-1} for the as-grown samples (Drost *et al* 1995, Benedetto *et al* 1997, Lysenko *et al* 1999, Maccagnani *et al* 1999) at room temperature, while this is limited to the range 0.3–2.7 W m^{-1} K^{-1} for the slightly oxidized material (Drost *et al* 1995, Lysenko *et al* 1999, Maccagnani *et al* 1999).

The above values were measured using different techniques, including micro-Raman scattering (Drost *et al* 1995, Ould-Abbas *et al* 2012), the optical pump probe method (Bernini and Lettieri 2001), scanning thermal probe microscopy (Lysenko and Volz 2000), the 3-omega method (Gesele *et al* 1997), the photoacoustic technique (Benedetto *et al* 1997), the direct current (dc) method (Kaltsas and Nassiopoulou 1999, Tsamis *et al* 2003, Yang *et al* 2010) and the lock-in thermography method (Wolf and Brendel 2006).

The thermal conductivity of porous Si was also calculated theoretically using different models. Since nanostructured porous Si is a complex material, composed of a Si skeleton of interconnected nanowires and nanocrystals, separated by voids, the low thermal conductivity of the material is attributed to the reduction of phonon transport due to phonon confinement in nanostructures and an increased phonon scattering at surfaces. The models used in the literature to determine the dependence of thermal conductivity on temperature and nanocrystal size are based either on the grey media approximation, or on Boltzmann transport equation. Monte Carlo simulations (Randrianalisoa and Baillis 2008), molecular dynamics (Lee *et al* 2007, Fang and Pilon 2011), and a combination of effective medium theory and radiative heat transfer (De Boor *et al* 2011) were used. The phonon hydrodynamic approach (Alvarez *et al* 2010) was also used, which considers the heat carriers as a fluid whose hydrodynamic-like equations describe the heat transport.

Although there is a lot of work in the literature on the room temperature thermal conductivity of porous Si, very little work has been devoted to the low-temperature thermal conductivity of this material (Gesele *et al* 1997). Low-temperature measurements exist on other silicon-based aerogel and xerogel films (Bauer *et al* 2011, Hopkins *et al* 2012), as well as on other porous elemental films (Bullen *et al* 2000).

In this paper, we performed a systematic work on the determination of porous Si thermal conductivity in the temperature range from 20 to 350 K using the dc method in combination with the finite element method (FEM) analysis. A thick porous Si (PSi) layer (thickness 40 μm) formed on p-type Si was used. We also investigated the temperature distribution around a Pt heater integrated on the porous Si layer at different values of the applied electric power. The influence of porous Si layer thickness on the effectiveness of thermal isolation provided by porous Si was also investigated. Our results show that a thick highly porous Si layer provides an excellent platform for thermal isolation on the Si wafer and opens important perspectives in cooltronics for the fabrication of efficient Si-based micro-cooling devices.

2. Sample fabrication

Porous Si (PSi) samples were fabricated by electrochemical etching of (1 0 0) p-type Si with resistivity in the range 1–10 Ω cm, using a constant current density of 20 mA cm^{-2} and an HF: ethanol solution with 3 : 2 volume ratio. The thickness of the porous Si layer, accurately measured from scanning electron microscopy (SEM) images, was 40 μm. The porosity was 63% and it was determined using the three-weight

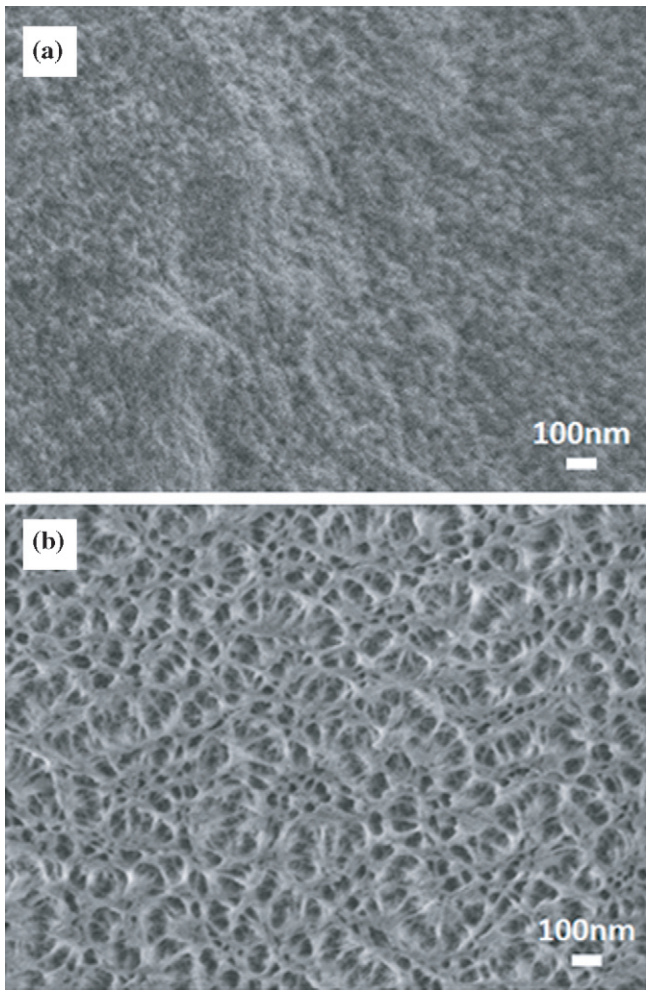

Figure 1. SEM images of the studied porous Si layer. In (*a*) the sample was imaged directly after its formation. In (*b*) the sample was subjected to a mild reactive ion etching process with SF_6 for 30 s and the porous Si skeleton was clearly revealed.

measurement method by which the porosity P is calculated from (Canham 1997):

$$P = \frac{m_1 - m_2}{m_1 - m_3}, \tag{1}$$

where m_1 is the initial mass of the sample, m_2 is the mass after anodization and m_3 is the mass of the sample after removing the formed PSi layer.

Porous Si from a p-type wafer material is composed of randomly distributed pores in a sponge-like morphology. The structure and morphology of the layer are illustrated in figure 1. In figure 1(*a*) the sample was imaged directly after its formation without any further processing. In figure 1(*b*) the sample was subjected to a mild reactive ion etching process with SF_6 for 30 s and the porous Si skeleton was clearly revealed.

The mean crystallite size of our PSi layer was 3 nm. For the present application, the material was slightly oxidized for porous Si internal surface passivation.

The test device for resistivity measurements was a four-point probe structure illustrated in figure 2 composed of two similar Pt resistors, one on the porous Si layer and one on bulk crystalline Si, which were deposited by sputtering and

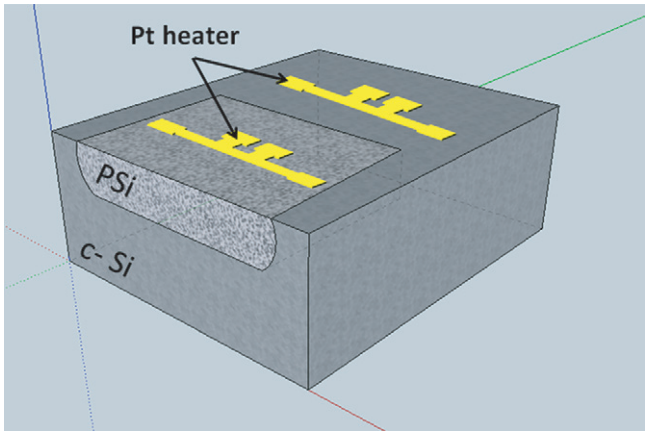

Figure 2. 3D schematic representation of the Pt resistor test structure (the four-point probe structure) on porous Si and on bulk crystalline Si (reference resistor).

patterned using optical lithography and the lift-off technique. The thickness of the Pt resistor was 200 nm, while its length and width were 640 μm and 20 μm, respectively. This second resistor served as reference resistor for calibrating the reference temperature. It was also used to extract the thermal conductivity of bulk Si and validate the method used in this work by comparing the obtained results with well-known results for Si from the literature. A 20 nm thick SiO_2 layer was deposited on the Si wafer before Pt deposition. In order to improve adhesion of the Pt layer and the SiO_2 layer, a thin Ti layer was deposited between SiO_2 and Pt. Both the reference resistor and the resistor on porous Si lie on the SiO_2 layer. This layer was also considered in the simulations.

3. Method used for the determination of thermal conductivity

The steady-state dc method was used for the determination of porous Si thermal conductivity (Stojanovic *et al* 2007, Siegert *et al* 2012). This method is based on the measurement of the temperature difference across a Pt resistor lying on the porous Si layer (substrate under investigation) in response to an applied heating power. For the extraction of the substrate thermal conductivity, a combination of experimental results and FEM analysis is used. The reference temperature was measured on bulk Si using as thermometer a second resistor on bulk crystalline Si, identical to the one on porous Si. Since with the applied heating power on the Pt resistor the temperature of porous Si is slightly different than that of the bulk, we calculated for each temperature the mean temperature of porous Si through its whole volume under the heater and corrected the measured temperature on bulk Si with the obtained value. However, in all cases this correction did not exceed the 2 K.

Measurements were obtained using the four-point probe method and accurate Keithley equipment.

The resistivity as a function of temperature of each resistor was determined from current–voltage (I–V) measurements. The resistor and pad geometry are shown schematically in figure 2. Current was passed through the two external pads and the voltage was measured on the internal pads (the four-point probe method). Measurements were performed in a He cryostat in the temperature range 20–350 K.

Two different current regimes were considered.

(a) Low-current regime.
In this case, the applied current was low, in order to stay within the linear regime of the I–V curves (negligible Joule heating). From these curves, the temperature coefficient of resistance (TCR) of the Pt resistor on Si was calculated using the following formula:

$$\mathrm{TCR} = \frac{(R_T - R_{\mathrm{ref}})/R_{\mathrm{ref}}}{T - T_{\mathrm{ref}}}, \qquad (2)$$

where R_T is the measured resistance of the Pt heater at temperature T, R_{ref} is the resistance at a reference temperature T_{ref} and TCR is the temperature coefficient of resistance.

(b) High current regime.
In this case, the applied current was high enough to induce a temperature increase on the heater, due to the Joule heating. With the TCR of the Pt resistor known from the low-current measurements, the temperature difference as a function of the applied electric power on the resistor is determined and the thermal resistance as a function of temperature is calculated. The thermal conductivity as a function of temperature is determined by comparing the measured and simulated results.

4. Results and discussion

The thermal resistance and the thermal conductivity of porous Si were determined as a function of temperature in the temperature range 20–350 K and compared with those of bulk crystalline Si.

4.1. Thermal resistance of porous Si

At low current, the I–V curves of the Pt resistor are linear, while they deviate from linearity at higher currents due to the Joule heating. From the low-current I–V curves we can calculate the TCR of the Pt resistor as a function of temperature. A reference temperature T_{ref} was used, measured on bulk crystalline Si, and $(R_{\mathrm{ref}} - R_T)/R_{\mathrm{ref}}$ was plotted as a function of $(T_{\mathrm{ref}} - T)$ for the Pt resistor. As an example, the results of the TCR of the Pt resistor for a reference temperature of 300 K are plotted in figure 3, from the slope of which the value of TCR is obtained (0.0018 K^{-1}). This value is characteristic of the 200 nm thick Pt resistor used. It is lower than that of bulk Pt (TCR = 0.0039 K^{-1}), in agreement with results in the literature (Puente *et al* 2006).

Knowing the TCR of the Pt resistor, we calculate the temperature difference on the resistor as a function of the applied electric power and plot the corresponding curves $\Delta T = f(Q)$. The results obtained for the Pt resistor on PSi for different temperatures are given in figure 4 for the electric power range 0–15 mW. At low Q the corresponding curves are linear. The observed curvature at higher Q is a

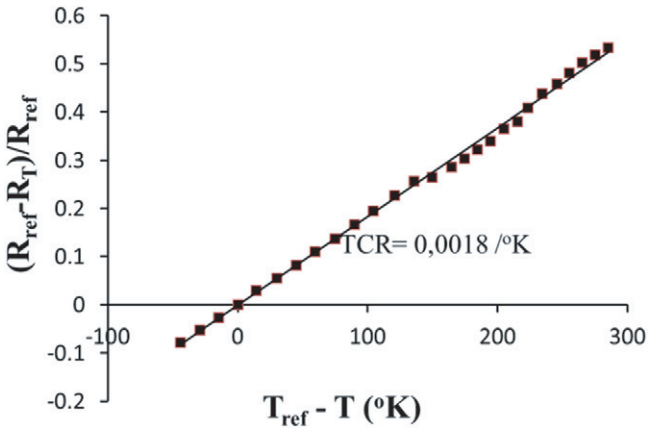

Figure 3. Resistance variation as a function of temperature of the Pt resistor on bulk crystalline Si. The temperature of 300 K was used as a reference temperature. From the slope of the curve the TCR of the Pt resistor was obtained (TCR $= 0.0018\,\mathrm{K}^{-1}$).

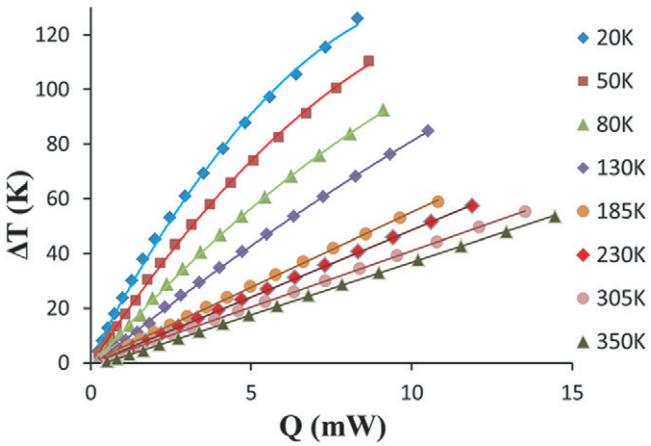

Figure 4. Increase in the temperature difference (ΔT) on the Pt resistor on PSi as a function of the applied electric power in the range 0–15 mW for different temperatures of the Si substrate.

result of the temperature-dependent thermal conductivity of the sample. The thermal conductivity increases with increasing temperature (increasing Q) and therefore the ΔT versus Q slope becomes increasingly shallower at higher temperatures, resulting in the observed negative curvature. This curvature is more prominent (on a linear scale) in the low-temperature curves, as these curves correspond to the temperature region in which the thermal conductivity changes more rapidly with temperature. In our experiments we used the linear part of the curves. For temperatures in the range 20–80 K we limited the applied electric power to values below $\cong$2 mW and the corresponding linear curves $\Delta T = f(Q)$ were plotted (see figure 5) and used to extract the thermal resistance of PSi.

From the slope of the linear part of the curves, the thermal resistance of the porous Si substrate was calculated. The exact equivalent circuit in our experiments is that of the thermal resistance of porous Si (40 μm thick layer) in series with that of the remaining 340 μm thick Si substrate (see figure 6). However, the thermal resistance of bulk Si being much lower than that of PSi, the total thermal resistance is dominated by that of PSi and the equivalent thermal circuit is simplified as in figure 6.

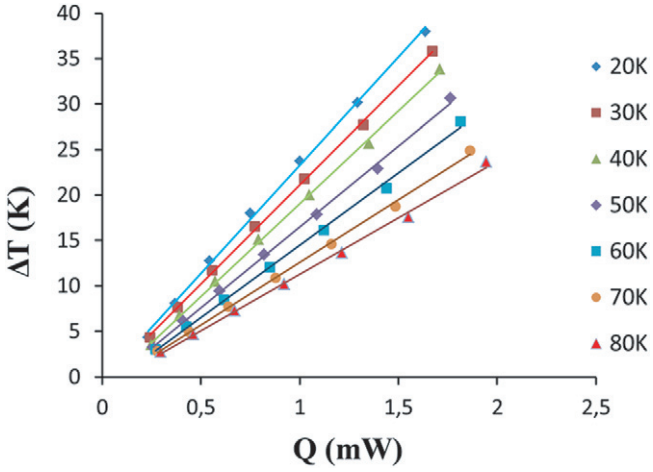

Figure 5. Increase in the temperature difference ΔT on the heater on PSi as a function of an applied electric power limited to values below 2 mW for different temperatures in the range 20–80 K.

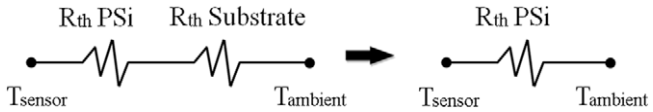

Figure 6. Equivalent thermal circuit of the structure under investigation (PSi (40 μm thick)/bulk crystalline Si (340 μm thick)).

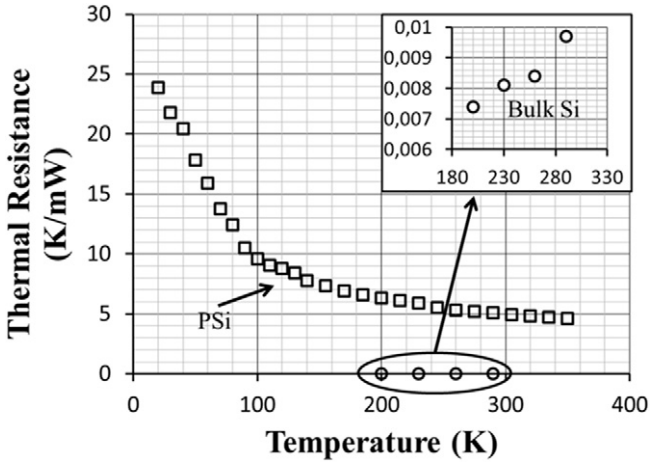

Figure 7. Temperature dependence of thermal resistance of PSi (open squares) and bulk Si (open circles, inset).

The calculated thermal resistances of porous Si and bulk Si as a function of temperature are illustrated in figure 7.

A change in slope of the corresponding characteristic, and a much faster increase with decreasing temperature are obtained for temperatures below $\cong$100 K. The measured thermal resistance of bulk crystalline Si is also illustrated in figure 7 and in the inset. In this case the measurements were limited to temperatures above $\cong$200 K, since the electric power needed for lower temperatures was extremely high.

4.2. Thermal conductivity of porous Si compared with bulk crystalline Si

The thermal conductivity of PSi was determined by combining the experimental results with simulations using

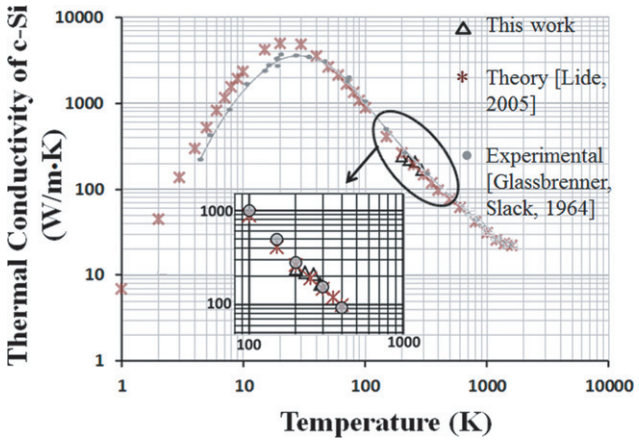

Figure 8. Thermal conductivity of bulk crystalline Si as a function of temperature. Results obtained in this work are represented by open triangles, while experimental (Glassbrenner and Slack 1964) and theoretical (Lide 2005) results from the literature with full circles and stars respectively.

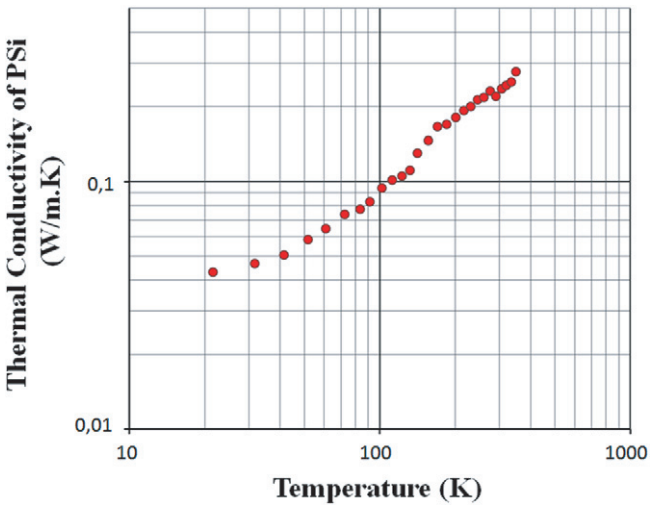

Figure 9. Temperature dependence of thermal conductivity of porous Si from 20 to 350 K.

three-dimensional (3D) FEM analysis based on the Comsol Multiphysics software. The 3D model used for the analysis was designed using the exact dimensions of the fabricated experimental device. In order to reduce the computational complexity, we used as length of the Pt resistor the length between the inner voltage pads. We tested this approximation by considering few examples with the full 3D Pt pattern and found that the error stayed always below 0.7%, it is thus acceptable. The differential steady-state heat conduction equation,

$$\nabla(-k \cdot \nabla T) = q, \tag{3}$$

where q is the volumetric heat generation (heat source) in $\mathrm{W\,m^{-3}}$, was solved using boundary conditions determined from the experiment. Negligible radiation losses and self-heating phenomena were assumed, and care was taken in all cases to limit the current to values that do not introduce any self-heating phenomena. The model was first applied to bulk crystalline Si, using as input parameters the data obtained from the experiment (temperature at the backside of the Si wafer and temperature on the Pt resistor). The thermal conductivity of p-type bulk crystalline Si was thus obtained in the temperature range 200–290 K and compared with experimental and theoretical results from the literature (Glassbrenner and Slack 1964, Lide 2005). The results are illustrated in figure 8. The results of this work are represented by open triangles in the main figure and in the inset, while experimental results from Glassbrenner and Slack (1964) and theoretical results from Lide (2005) are represented by full circles and stars, respectively. From figure 8 it is depicted that the results of this work are in good agreement with those of the literature. This is a validation of the method used, which was then applied to the porous Si layer.

For the determination of the thermal conductivity of PSi, the boundary conditions were also determined experimentally. Sample architecture was composed of a 40 μm thick porous Si layer on 340 μm thick bulk crystalline Si and the Pt resistor on top. The width of the Pt resistor was 20 μm and its length was 640 μm in the case of PSi (four-point probe measurements) and 3 mm (two-point probe measurements) in the case of bulk Si substrate. We also considered porous Si as an isotropic and homogeneous material, which is macroscopically a realistic approximation, since the PSi material from p-type Si is sponge-like, with homogeneous structure in the micrometre range. The values of thermal conductivity and heat capacity of bulk crystalline Si and Pt used in the simulation were taken from the literature (Flubacher *et al* 1959, Glassbrenner and Slack 1964).

The dissipated power per unit volume on the Pt resistor was calculated from the applied current, the measured voltage drop and the dimensions of the Pt resistor, using as boundary condition the temperature measured at the backside of the Si substrate.

The equation of continuity was solved at boundaries in thermal contact:

$$-n_1 \cdot (-k_1 \cdot \nabla T_1) - n_2(-k_2 \cdot \nabla T_2) = 0, \tag{4}$$

while the formula of continuity/symmetry

$$-n \cdot (-k \cdot \nabla T) = 0 \tag{5}$$

was applied at every other boundary. We assumed no heat transfer between the sample and the environment, as the measurements were carried out in vacuum. The thermal conductivity of the porous Si layer was the unknown parameter in the simulation, and it was calculated performing successive iterations until the average temperature over the entire volume of the heater reached the measured temperature of the heater.

The obtained results of the thermal conductivity of PSi as a function of temperature are illustrated in figure 9.

A comparison of the obtained thermal conductivity of porous Si with that of bulk crystalline Si, α-Si, a-Si:H and some other C-MOS compatible dielectrics is shown in figure 10. It is clearly seen that the obtained values of thermal conductivity of PSi are much lower than those of bulk crystalline Si, this difference exceeding four orders of magnitude at temperatures below 50 K. It is also comparable to/or lower than other materials usually used for thermal insulation.

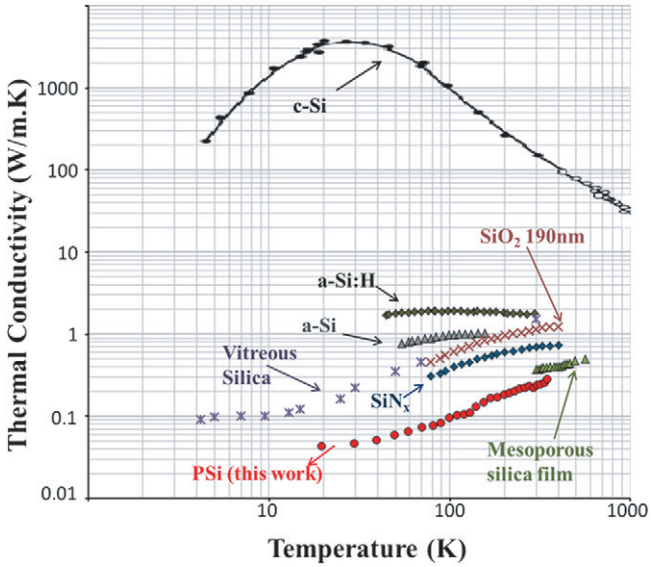

Figure 10. Comparison of the thermal conductivity of porous Si (this work) with that of bulk crystalline silicon (Glassbrenner and Slack 1964), a-Si (Lee *et al* 1991), a-Si : H (Cahill *et al* 1989) and different other C-MOS compatible films (mesoporous silica (Shin *et al* 2008), vitreous silica (Smith *et al* 1978) and silicon nitride (Lee and Cahill 1997)).

4.3. Discussion

The temperature dependence of pure bulk crystalline Si follows that of single crystal dielectric materials. It goes through a maximum at a temperature of about 20 K. Below this maximum the thermal conductivity follows temperature dependence close to that of the specific heat of the lattice ($k = f(T^3)$). Above the maximum, the thermal conductivity decreases with increasing temperature, following the phonon mean free path decrease due to increased phonon–phonon scattering. In figure 8 the ideal k versus T curve for pure Si from Glassbrenner and Slack (1964) is depicted. The full curve represents theoretical results obtained by assuming that phonons are the only carriers of heat and they are scattered by other phonons, the Si isotopes and the crystal boundaries, while the circles are experimental results from the same reference.

In porous Si, the thermal conductivity decreases significantly with increasing porosity due to the increasing air/nanostructured Si ratio and phonon confinement in the Si nanostructures. Theoretical models often treat the problem using kinetic theory for phonons, molecular dynamic simulations (Fang and Pilon 2011) or using the so-called phonon hydrodynamics model (Alvarez *et al* 2010), which is a generalization of Fourier's law, incorporating non-local effects and thermal slip along the nanostructure walls. Based on this last method, an analytical expression of the effective thermal conductivity of porous Si was obtained by Alvarez *et al* (2010) as a function of porosity, pore radius and phonon bulk mean free path. We used the analytical expression of Alvarez *et al* (2010) to calculate the thermal conductivity of our samples as a function of temperature and compare the corresponding theoretical results with our experimental results obtained in this work. The parameters used in the calculation were the following: material porosity 63%, mean diameter of pores

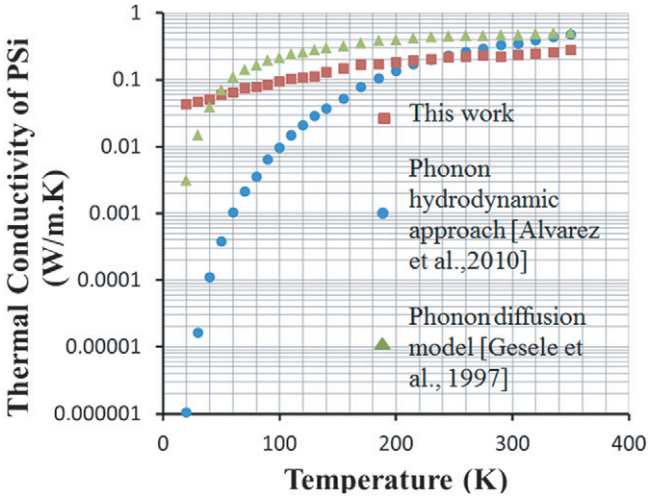

Figure 11. Comparison of the experimental data of thermal conductivity of PSi obtained in this work with theoretical ones obtained using our experimental parameters and analytical expression for two different models from the literature.

6 nm and a phonon bulk mean free path that was calculated from the classical analytical expression of thermal conductivity due to phonons:

$$k = \tfrac{1}{3} \cdot C \cdot v \cdot l, \tag{6}$$

where k: thermal conductivity, C: specific heat capacity, v: mean phonon velocity and l: phonon mean free path of Si.

The obtained theoretical results using the above approach are depicted in figure 11 (represented by full circles). In the same figure we represented the results obtained using a simplified model that takes into account only the porosity of the PSi layer and the mean crystallite size of Si (Gesele *et al* 1997). For this model we used the value of 3 nm for the mean crystallite size of our PSi layer and the corresponding results are represented in figure 11 with full triangles. For comparison, the experimental results obtained in this work are represented by full red squares.

From figure 11 we deduce that the simplified phonon diffusion model is in relatively good agreement with our experimental results, while the phonon hydrodynamic model gives much lower values than the experimental ones, at temperatures below ∼180 K. Both theoretical models predict a sharp decrease with decreasing temperature (at temperatures below 50 K for the phonon diffusion model and below ∼120 K for the phonon hydrodynamic approach). This is not the case for our experimental results that show a smooth decrease in k with decreasing temperature. This can be attributed to an inaccuracy of the models at these low temperatures

5. Effectiveness of thermal isolation by a thick porous Si layer

The obtained 3D temperature distribution within the PSi layer by applying a heat power of 3 mW on the Pt heater is illustrated in figure 12(*a*) for a reference temperature of 290.5 K, while in (*b*) the one-dimensional (1D) representation of the temperature distribution on the PSi surface on the left and right side of the

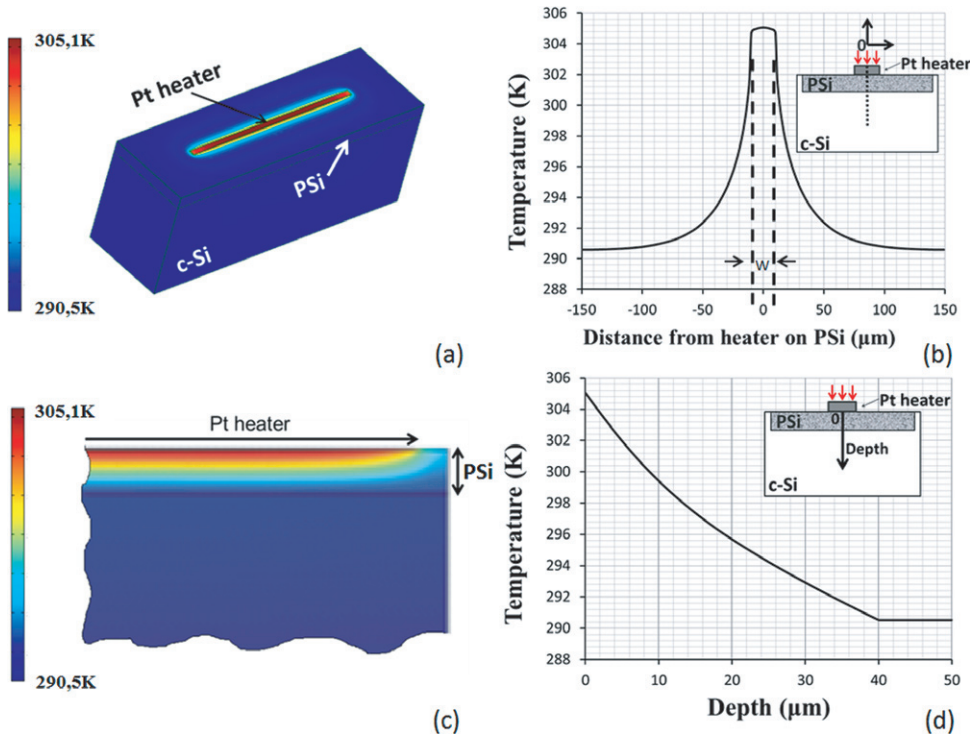

Figure 12. 3D schematic representation of the temperature distribution on the PSi surface around the heater (*a*), and in a cross sectional view of the structure underneath the heater (*c*) for an applied heat power of 3 mW. The graphs in (*b*) and (*d*) show the temperature distribution as a function of the distance from the heater (*b*) and as a function of depth from the metal/PSi interface (*d*) for the given heat power on the heater.

Pt resistor for the above applied heat power is depicted. A cross sectional view of the temperature distribution in porous Si under the above conditions is given in figure 12(*c*), while in (*d*) the 1D representation of the temperature variation as a function of depth with the zero taken at the Pt/PSi interface is shown. It is depicted that for the given reference temperature (290.5 K) the temperature on the heater is ∼304 K for an applied heat power of only 3 mW, while the temperature on the PSi surface at ∼100 μm from the heater is equal to the reference temperature. The high-temperature difference around the heater on PSi is due to the effective thermal isolation from the Si substrate by the thick PSi layer.

Due to the much lower thermal conductivity of porous Si at low temperatures, the above temperature difference on the PSi surface under an applied heat power on the heater is much higher at lower temperatures.

We used simulations to obtain the temperature distribution around the surface of the PSi layer for two reference temperatures, 20 and 290 K and for different values of the heat power. The results are given in figure 13. For a heat power of 2 mW, the temperature difference on the heater is ∼9 K at a reference temperature of 290 K, while it is more than 45 K at a reference temperature of 20 K.

We also investigated the effect of the PSi layer thickness on the temperature distribution as a function of depth from the PSi surface for the same applied heat power (3 mW) for a reference temperature of 290 K, as well as the maximum temperature difference on the heater as a function of PSi layer thickness for the same heat power on the heater and for two reference temperatures, 290 and 20 K. PSi layer thickness was taken between 10 and 100 μm. The results are given in figures 14(*a*) and (*b*), respectively. The obtained maximum temperature difference on the heater under an applied heat power increases significantly with increasing PSi layer thickness for thicknesses below ∼40 μm, while it tends to saturate for higher thicknesses. This explains the choice of 40 μm PSi layer thickness in our experiments. This thickness is sufficient to provide almost maximum thermal isolation from the Si substrate, while it is small enough to guarantee a mechanically stable PSi layer.

From the above results it is clearly demonstrated that thick porous Si layer technology provides an efficient local thermal isolation technology on the Si wafer that is much more efficient at cryogenic temperatures. This makes the above technology very promising for application as a local substrate on the Si wafer for the integration of high performance cooling devices, as for example Si bolometers.

6. Conclusion

We used the steady-state dc method in combination with 3D FEM analysis to determine the thermal conductivity of PSi with a porosity of ∼63%, formed on p-type Si, in the temperature range from 20 to 350 K and compared with that of other low-thermal-conductivity materials and that of bulk crystalline Si. Experimental results were tested on several samples and are reproducible. Our results on PSi were also compared with theoretical results using a simplified phonon diffusion model and a phonon hydrodynamic approach. Better agreement was obtained with the first above method. The main conclusions of

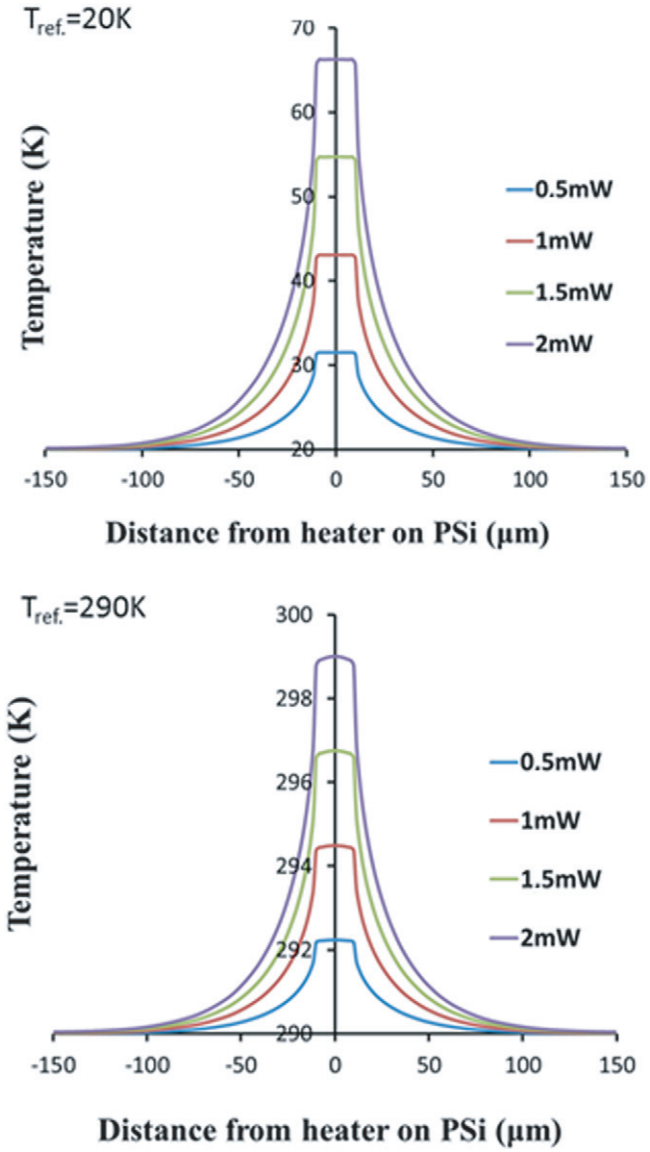

Figure 13. Temperature distribution on the PSi surface around the heater for different values of the applied heat power for two different reference temperatures, 20 and 290 K.

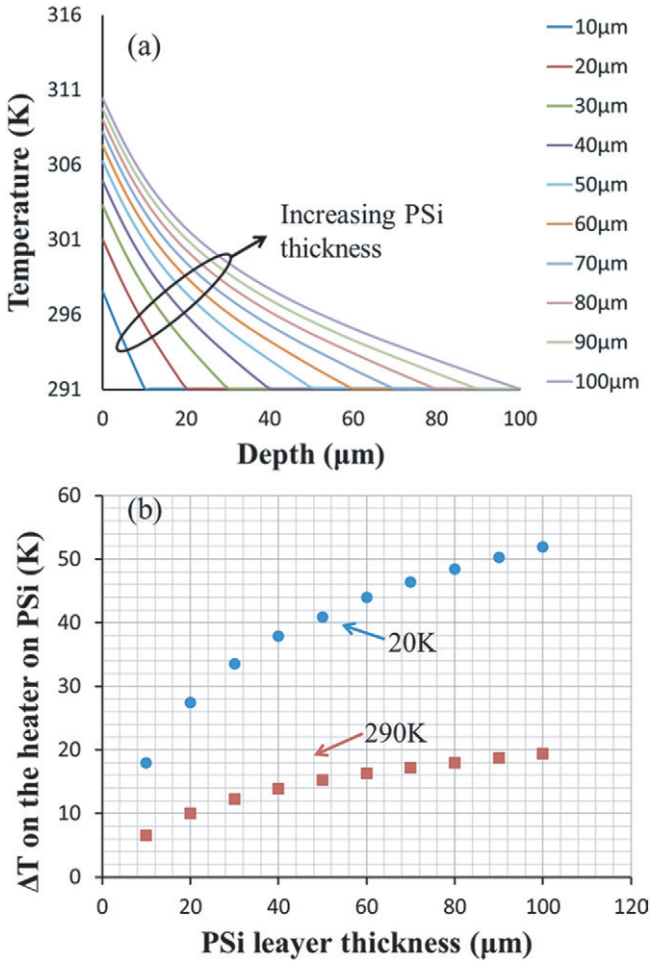

Figure 14. Simulation results of the temperature distribution as a function of depth for different values of PSi layer thickness (*a*) and the temperature difference on the heater for an applied heat power of 3 mW for two different values of the reference temperature (20 and 290 K) (*b*). At 20 K the obtained temperature difference is much higher than at 290 K due to the lower thermal conductivity of PSi.

this work are as follows: porous Si shows a much lower thermal conductivity than bulk crystalline Si, this difference exceeding four orders of magnitude at temperatures below 50 K. The variation of PSi with temperature is monotonic and does not show any maximum for the measured temperature range, as in the case of bulk crystalline Si and other dielectric materials. Phonon confinement in Si nanostructures composing porous Si as well as phonon-wall scattering is expected to be at the origin of the above temperature dependence. We also calculated the temperature distribution around the heater on PSi and the temperature difference under different values of heat power on the resistor and different thicknesses of the PSi layer at two reference temperatures, 20 and 290 K. We thus illustrated the effectiveness of PSi layers as an isolation material on the Si wafer, which is better at 20 K than at room temperature, showing that PSi isolation technology is very appropriate for use in Si cooling devices at cryogenic temperatures.

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