Interface state energy distribution and P_b defects at Si(110)/SiO_2 interfaces: Comparison to (111) and (100) silicon orientations

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Traps at the (110)Si/SiO_2 interface are investigated by combining electrical methods with electron spin resonance (ESR) measurements, and the results are compared to the well studied (100) and (111)Si/SiO_2 interfaces. At all three Si crystal faces, the interface trap density D_{it} as function of energy E in the Si band gap exhibits two peaks at about 0.25 and 0.85 eV above the Si valence band, found to be well correlated with $P_{b(0)}$ centers ($Si_3 \equiv Si\bullet$ defects). By comparing capacitance-voltage (CV) curves at 300 and 77 K of both n- and p-type samples, the $P_{b(0)}$ defects are confirmed to be amphoteric. Effective passivation of interface traps by H_2 annealing suggests that P_{b0} defects are responsible for most of interface traps observed in (110)Si/SiO_2. The truly amphoteric behavior, implying that one P_{b0} defect delivers two interface trap levels, was observed for the (100) and (111)Si faces but not for the (110) face. The estimated interface trap density N_{it} at the (110)Si/SiO_2 interface oxidized at 930 °C is $(6.7 \pm 0.5) \times 10^{12}$, while the P_{b0} density as determined by ESR is about $(6 \pm 1) \times 10^{12}$ cm^{-2}. Lowering of the oxidation temperature leads to further reduction in the electrically active P_{b0} centers fraction at the (110)Si/SiO_2 interface. © *2011 American Institute of Physics*. [doi:10.1063/1.3527909]

I. INTRODUCTION

Compared to the workhorse (100) face, transport along the (110) silicon plane offers improvement in hole mobility and more compact architecture of metal-oxide-semiconductor (MOS) field-effect transistor (MOSFET) structures (e.g., vertical MOSFET, multigate FINFET devices[1,2]) while remaining within the framework of the highly successful Si MOS fabrication process. It is known that the hole mobility is more than doubled at the (110) silicon face compared with the conventional (100) one, while the electron mobility is still the highest on the (100) face.[3,4] The enhanced hole mobility reflects the fact that the effective mass of holes is lower at the (110) surface than at the (100) one.[3,4]

The performance and reliability of a MOS device is significantly influenced by the quality of the grown Si/SiO_2 interface. Studies of Si/SiO_2 interface traps using MOS capacitors were first introduced by Terman,[5] and then extended in other works.[6–11] So far only the (100)Si/SiO_2 and (111)Si/SiO_2 interfaces have been extensively investigated, for more than 50 years, less so the (110)Si/SiO_2 one. In the 1960s, using the temperature-dependent capacitance-voltage (CV) technique, Gray and Brown[6] evaluated the density of interface states D_{it} versus energy, E, at SiO_2/Si interfaces for three silicon interface orientations. However, as the SiO_2 layers were grown at $T_{ox}=1000$ °C by wet oxidation (O_2 +80 ppm H_2O), it is difficult to evaluate to what extend the hydrogen passivation factor may have come in, which precludes from quantitative comparison. In addition, the $D_{it}(E)$ profiles reported by Gray and Brown disagree with later experimental results. The D_{it} reported for the (100) face is far higher than observed by other groups,[12–14] while the two peaks on all $D_{it}(E)$ profiles are much closer to the Si band gap edges than reported by other researchers for the (100) and (111)Si face orientations.[12–20]

The goal of this work is to provide dependable information regarding the electrical behavior of (110)Si/SiO_2 interface traps as analyzed by current state-of-the art electrical techniques using three methods. To this end, D_{it} and the total density of interface traps are evaluated in a comparative way on thermal Si/SiO_2 structures for the three low-index Si faces and, in aiming to link with structural/physicochemical insight, are compared to the density of interfacial Si dangling bonds (DBs, P_b-type centers) determined by electron spin resonance (ESR) on identical samples. This quantitative comparison of the (110)Si/SiO_2, (111)Si/SiO_2, and (100)Si/SiO_2 interfaces in terms of P_b-type defect density and D_{it} is carried out under well controlled H-passivation conditions, which is a prerequisite to meaningful comparative assessment.

II. EXPERIMENTAL

Three batches of samples were independently prepared by oxidation at 930 °C in dry O_2 (nominal hydrogen content <0.1 ppm) for times t=180–209 min of n- and p-type Si wafers with (110), (100), and (111) crystallographic surface orientations and doping levels in the range of 1×10^{15}–2×10^{16} cm^{-3}. After oxidation, the samples were allowed to cool down in unaltered ambient with semiexponential temperature decay (cooling time constant of ≈200 s). To avoid passivation of the interface defects by traces of moisture in the room ambient, the samples were unloaded at room tem-

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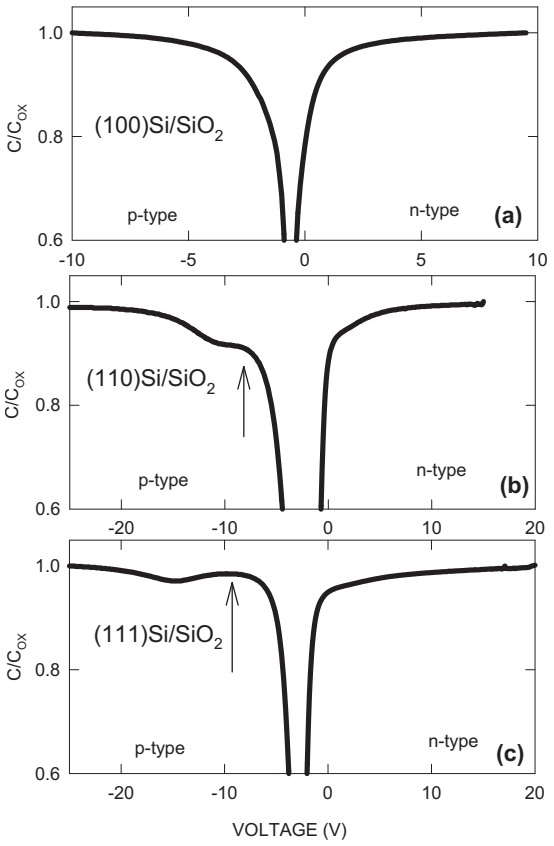

FIG. 1. Magnified plots of normalized 100 kHz CV curves measured at 300 K on (100)Si/SiO_2 (a), (110)Si/SiO_2 (b), and (111)Si/SiO_2 (c) n- and p-type samples. Vertical arrows in panels (b) and (c) mark the capacitance peak associated with interface trap response.

perature. Control depassivation of some samples by annealing in vacuum (30 min at 630 °C) affirms the absence of any detectable defect passivation. The oxide thickness determined using spectroscopic ellipsometry was in the range of 25–30 nm for (100)Si/SiO_2, 35–42 nm for (110)Si/SiO_2, and 45–50 nm for (111)Si/SiO_2 samples. The oxidized Si samples were split in two sets: The first one was left in the as-oxidized state to exclude passivation of interface defects by hydrogen, i.e., to ensure their maximal manifestation. The second set of samples was passivated by 30 min annealing in H_2 (1.1 atm) at 400 °C. Finally, MOS capacitors were prepared by evaporation of Au electrodes of $(0.8-1.5)\times10^{-4}$ cm^2 area.

Electrical measurements were performed at liquid nitrogen and room temperatures in the frequency range f=20 Hz–1 MHz using a HP4284A precision LCR meter. The energy distribution of interface traps $D_{it}(E)$ was extracted using either the ac conductance (GV) method according to Nicollian and Brews,[21] or the low frequency CV technique described by Berglund.[22] The total density of interface traps per unit area (N_{it}) was then calculated by integrating $D_{it}(E)$ over the silicon band gap. In addition, the total interface trap density N_{it} (integrated across the Si band gap) was independently determined from the absolute difference between the flatband voltages (V_{FB}) inferred from 100 kHz CV curves taken on p- and n-type Si MOS-capacitors at 77 K.[15] The latter method offers much better accuracy by eliminating uncertainties related to the surface potential calculations.

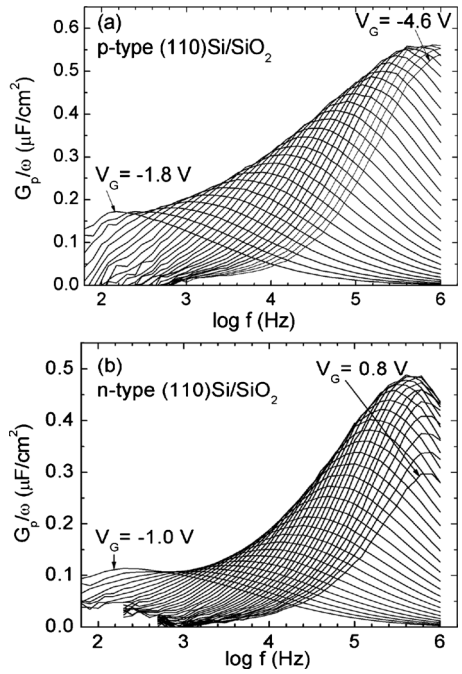

FIG. 2. The parallel conductance (G_p) to angular frequency ($\omega=2\pi f$) ratio as a function of frequency with the metal bias (V_G) as parameter of as-oxidized p- and n-Si(110)/SiO_2 samples measured at 300 K.

Results of electrical measurements were compared to the density of Si DBs (P_b-centers) measured using ESR spectroscopy.[15] The ESR experiments were conducted on the same samples (p-Si) as those used for electrical measurements. The ESR spectra were taken at 4.2 K using a K-band (≈20.5 GHz) spectrometer operated in the adiabatic slow passage mode. Absolute densities of P_b-type centers were determined by double numerical integration of the recorded absorption-derivative ESR spectra using the signal of a calibrated comounted Si:P marker (g=1.99869) as reference. The attained absolute accuracy is estimated at better than 20 %.

III. RESULTS AND DISCUSSION

Initial characterization of the samples was done using 100 kHz CV measurements at 300 K. Typical results obtained for (100), (110), and (111) orientations of the Si substrate crystal are shown in Fig. 1 for both n- and p-type samples. As indicated by arrows in panels (b) and (c), p-type (110)Si/SiO_2 and (111)Si/SiO_2 samples exhibit a peak in the capacitance associated with the response of interface traps.[16–19] Remarkably, this response is observed even at 100 kHz frequency thanks to fast supply of the minority carriers (electrons) from the unmetallized periphery of the MOS capacitors inverted by the positive fixed charge present at the interface.[17]

More detailed information was obtained from the analysis of the parallel conductance (G_p) to angular frequency ($\omega=2\pi f$) ratio measured at 300 K as a function of frequency with the applied metal bias (V_G) as parameter for as-oxidized (no passivation) p- and n-Si(110)/SiO_2 samples (Fig. 2). The interface trap density D_{it}, the hole and electron trapping time constants τ_p and τ_n, and the capture cross sections of holes

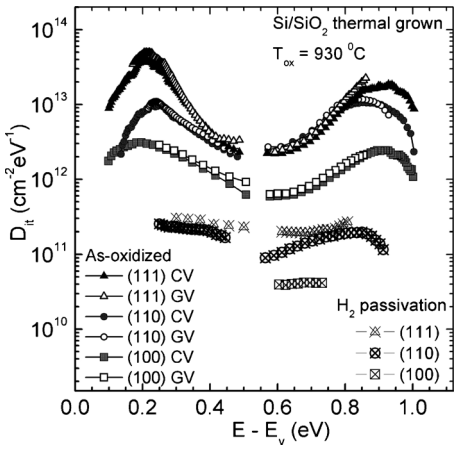

FIG. 3. $D_{it}(E)$ profiles of Si/SiO_2 interfaces derived from the CV (solid symbols) and GV (open symbols) methods in Si/SiO_2 samples fabricated on (100), (110), and (111) faces of Si. Results are shown for both the as-oxidized samples (no H-passivation) and those subjected to H_2 passivation (30 min anneal in 1.1 atm H_2 at 400 °C).

(σ_p) and electrons (σ_n) can be determined from the (G_p/ω)-f curves by fitting the experimental data with the statistical model of Nicollian and Brews[21] which accounts for the surface potential fluctuations. Then, the $D_{it}(E)$ profile can be determined after calculation of the surface potential as a function of gate voltage. The latter was achieved from the low frequency (20 Hz) CV measurements through numerical integration (the Berglund integral[22]) in combination with a determination of V_{FB} from the high-frequency (1 MHz) CV curve. The $D_{it}(E)$ profiles obtained by both CV and GV methods are compared in Fig. 3. The $D_{it}(E)$ distributions of as-oxidized samples clearly show two peaks, located at about 0.25 eV and about 0.85 eV above the silicon valence band (VB) top.

Figure 4 compares the inferred (τ_p, τ_n) and (σ_p, σ_n) at (110), (111), and (100)Si/SiO_2 interfaces of the unpassivated samples as a function of energy in the Si gap. While both τ and σ are strong functions of energy,[23] it appears that near the band gap edges they are of the same order of magnitude.

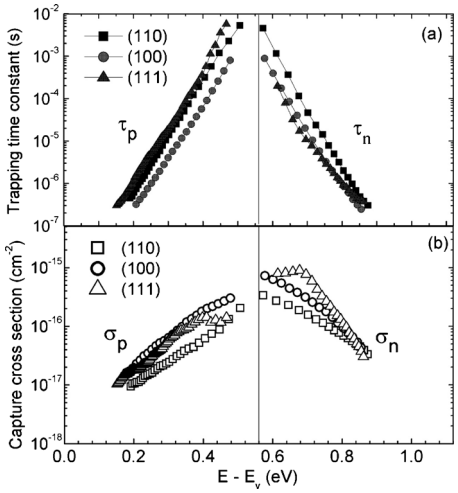

FIG. 4. Hole and electron trapping time constants (a) and capture cross sections (b) in the as-oxidized (110) (111) and (100)Si/SiO_2 entities as a function of energy in the Si band gap.

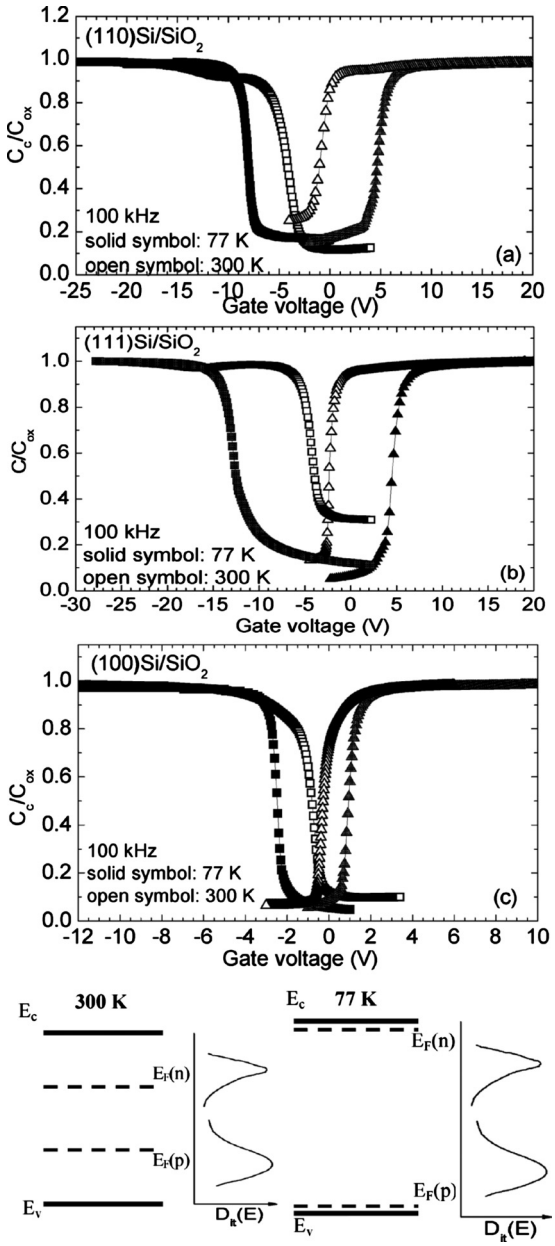

FIG. 5. Normalized 100 kHz CV curves measured at 300 K (open symbols) and 77 K (solid symbols) of n- and p-type (110), (111), and (100)Si/SiO_2 samples [(a), (b), and (c)], where C_{ox} is the oxide capacitance per unit area. The bottom panel illustrates the shift of the Fermi level in n- and p-type Si relative to the interface trap energy distribution caused by sample cooling from 300 to 77 K.

This suggests the same kind of traps present at all three interfaces, which is corroborated by the nearly identical shapes of the $D_{it}(E)$ profiles. Nevertheless, it is worth mentioning here that we also found a slight difference (~0.05 eV) in the interface trap distribution peak position between (100)Si/SiO_2 and the two other interface orientations of silicon, a finding also recently suggested on the basics of transient spectroscopy results.[14]

Figure 5(a) compares 100 kHz C-V curves of both p- and n-type (110)Si/SiO_2 samples measured at 300 and 77 K. Upon cooling to 77 K, the CV curve of the p-type sample shifts to a larger negative gate voltage indicating the presence of donor-type traps in the lower half of the band gap,

TABLE I. Density of P_{b0} centers, D_{it} peak values, and $(N_{it})_{1/2}$, the integral of D_{it} obtained from GV measurements over the upper (n-type) and lower (p-type) half of Si bandgap at Si/SiO_2 interfaces studied in the present work.

Si orientation	Type	$[P_{b0}]$ (10^{12} cm^{-2})	$(D_{it})_{peak}$ (10^{12} cm^{-2} eV^{-1})	$(N_{it})_{1/2}$ (10^{12} cm^{-2})
(100)	p	1.0 ± 0.2	3.1 ± 0.3	0.7 ± 0.2
(100)	n		2.5 ± 0.3	0.8 ± 0.2
(110)	p	6 ± 1	10 ± 2	1.8 ± 0.5
(110)	n		11 ± 2	2.2 ± 0.8
(111)	p	5 ± 1	48 ± 10	4 ± 1
(111)	n		20 ± 5	3.0 ± 0.8

while the CV curve of n-type sample shifts to a more positive gate voltage indicating that acceptor-type traps ate present above Si midgap. The same behavior is seen in (111) and (100) samples, as illustrated in Figs. 5(b) and 5(c). At 77 K, the Fermi level is positioned at about 30 meV above the VB in the p-type silicon and at about 30 meV below the conduction band in the n-type silicon. For the doping levels of the used Si wafers (1×10^{15}–2×10^{16} cm^{-3}), the difference in V_{FB} between 77-K CV curves of n- and p-type samples corresponds to a shift in Fermi level over 1.1 eV in the Si band gap at 77 K (1.16 eV), i.e., nearly over the entire Si band gap at 300 K (1.12 eV) as illustrated in Fig. 5(d). Then, assuming the same oxide fixed charge densities in n- and p-type samples, the total density of interface traps, N_{it}, across Si band gap can be evaluated from the difference between the V_{FB} values inferred from 100 kHz CV curves taken on p- and n-type Si MOS-capacitors at 77 K (Fig. 5) according to following equation:

$$V_{FB}(n) - V_{FB}(p) \approx E_g(Si) + \frac{qN_{it}}{C_{ox}}, \quad (1)$$

where $E_g(Si)=1.16$ eV at 77 K, q is the elemental charge, and C_{ox} is the oxide capacitance per unit area. The N_{it} evaluation using Eq. (1) does not require additional surface potential calculations thus helping to attain better accuracy. Moreover, at low temperature, the thermal emission of carriers from most of the traps is negligible, making it easy to attain high-frequency CV curves, thus adding to accuracy enhancement of the measurements.

The inferred N_{it} using Eq. (1) for the $(110)Si/SiO_2$ interface is $(6.7\pm0.5)\times10^{12}$ cm^{-2}. As outlined, N_{it} was also estimated by integrating $D_{it}(E)$ profiles extracted from CV and GV methods over the Si band gap, yielding N_{it} values of $(5\pm1)\times10^{12}$ cm^{-2} and $(4\pm1)\times10^{12}$ cm^{-2} (cf. Table I), respectively. The latter values obtained from the CV and GV methods are clearly lower than the result obtained from the difference between V_{FB} values (n- and p-type) at 77 K, which arises because of the wider energy range covered by the latter technique. We also found that the density of the donor traps below Si midgap and of acceptor traps above Si midgap are equal within the accuracy of our measurements.

Next, the electrical results are compared to ESR data. The latter reveal the occurrence of one major type of defect at the $(110)Si/SiO_2$ interface as can be seen from the ESR spectrum taken at 4.2 K on $(110)Si/SiO_2$ (Fig. 6), exhibiting a prominent P_{b0} signal of axial symmetry with g matrix prin-

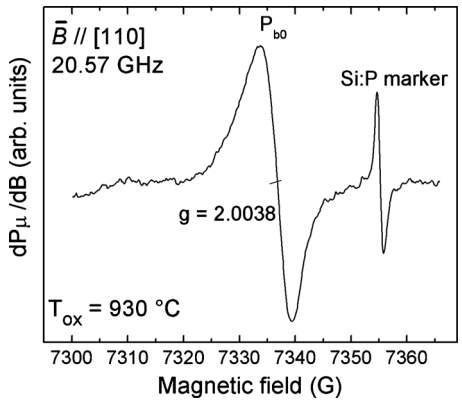

FIG. 6. K-band derivative-absorption ESR spectrum observed at T=4.2 K with the applied magnetic field $\bar{B}$ aligned with a normal to the $(110)Si/SiO_2$ interface, showing the signal with characteristic signature of P_{b0} defects. The spectrum was measured using an incident microware power ≈0.2 nW and field modulation amplitude ≈0.3 G. The label Si:P denotes the signal from a comounted Si:P marker sample.

cipal values $g_{\|}=2.0079$ and $g_{\perp}=2.0018$, corresponding to a density of unpaired spins (spin $S=1/2$ centers) $[P_{b0}]=(6\pm1)\times10^{12}$ cm^{-2}. Therefore, the two broad peaks observed in $D_{it}(E)$ are likely related the P_{b0} centers revealed by ESR analysis, as was inferred previously for (111) and (100)Si faces.[17–19,24] In previous research, the P_{b0} defect was identified as trivalent interfacial Si, denoted $Si_3\equiv Si\bullet$, where the dot symbolizes an unpaired electron in a dangling $sp^3\langle111\rangle$-like orbital.[20,25]

To assess the contribution of the P_{b0} centers to the interface trap density, we also investigated the electrical trap density in the hydrogen-passivated samples. It is known that Si DBs can be very efficiently passivated by H_2 as revealed by their elimination from the ESR spectrum, a fact which has also been affirmed here by ESR for the P_{b0} centers at the $(110)Si/SiO_2$ interface. The mechanism of P_b defect passivation in molecular hydrogen can be explained by the simple chemical reactions[26]

$$P_b + H_2 \rightarrow P_bH + H, \quad (2)$$

or

$$Si_3\equiv Si\bullet + H_2 \rightarrow Si_3\equiv SiH + H. \quad (3)$$

The passivation of interfacial Si DBs (P_b-type centers) by hydrogen is a well known and standard technological procedure, but for $(110)Si/SiO_2$ it has not been quantified before. Figure 3 compares $D_{it}(E)$ of all three Si/SiO_2 interfaces grown at 930 °C, before and after H_2 passivation. The results clearly show that the trap density is reduced more than an order of magnitude after passivation, so most of the interface traps at all three (110), (111), and (100) Si faces are removed after hydrogen annealing. For the (110) orientation, the value of N_{it} after passivation as determined from Eq. (1) was $(7\pm1)\times10^{10}$ cm^{-2}. As the vast majority of interface traps, like the P_{b0} centers, can be effectively passivated by H_2 annealing, it is highly likely that the P_b-type defects are responsible for most of the interface traps observed for the (110)Si face, in line with the $(100)Si/SiO_2$ and $(111)Si/SiO_2$ cases. Next, as the electrical results on the passivated

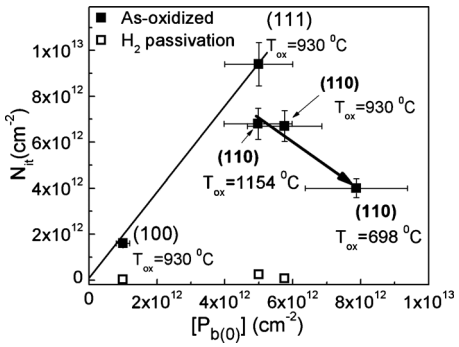

FIG. 7. Electrically active defect density N_{it} of (100), (110), and (111) Si/SiO_2 interfaces grown at $T_{ox}=930$ °C compared to $[P_{b(0)}]$ obtained from ESR. The data for the (110)Si/SiO_2 interfaces grown at $T_{ox}=698$ and 1154 °C are also shown for comparison. The solid line denotes the ratio $N_{it}/[P_{b(0)}]\approx 2$, expected from isolated amphoteric centers. The bold arrow indicates the trend found in (110)Si/SiO_2 when the oxidation temperature is decreased.

samples show that most of the interface traps in the as-oxidized samples are related to the amphoteric Si DB type defects ($P_{b(0)}$-centers), each of them should contribute two trap levels to the $D_{it}(E)$. Would all DBs contribute to $D_{it}(E)$, the total density of interface traps N_{it} integrated over Si band gap is then expected to be twice the P_b density.

To assess the validity of the above picture, Fig. 7 shows the total density of interface traps N_{it} determined from 77 K CV curves as a function of DB density $[P_b]$ in (100) Si/SiO_2, (110)Si/SiO_2, and (111)Si/SiO_2 samples all grown at $T_{ox}=930$ °C. In addition, also shown are N_{it} and $[P_b]$ results for (110)Si/SiO_2 samples grown at $T_{ox}=698$ and 1154 °C. For convenience, the numerical data of ESR and GV measurements are also listed in Table I. As already mentioned the sum of trap densities in the lower and upper halves of the Si gap is slightly lower than N_{it} obtained from 77 K CV measurements because the GV technique does not allow one to access the entire gap. As expected from the amphoteric behavior, the ratio $N_{it}:[P_{b(0)}]\approx 2:1$ is observed for the (100) and (111)Si faces but not for the (110) face. For (110)Si/SiO_2 oxidized at 930 °C, the ratio is less, perhaps approaching 1:1, meaning that less (only about half) of P_b defects operate as trapping centers. It is unlikely that the bias applied during electrical measurements causes partial passivation of interface traps as no such effect is seen in (111)Si/SiO_2 samples. Comparing (110)Si/SiO_2 interfaces grown at different T_{ox}, one may notice that with lowering T_{ox}, there is a trend that N_{it} decreases while $[P_{b0}]$ is increasing (cf. arrow in Fig. 7). Thus, at a lower oxidation temperature, a larger fraction of P_{b0} defects are not detected as interface traps. Yet, the total density of P_{b0} centers detected by ESR seen as to become higher as the oxidation temperature decreases (cf. Fig. 7) is consistent with trends reported for other faces of silicon.[15] Put in the context of the exposed similarity of the three low-index Si/SiO_2 interfaces in terms of occurring $P_{b(0)}$-type interface defects, and the gathered detailed understanding about their electrical behavior and atomic nature, the finding regarding the partially electrically-inactive P_{b0} centers at the (110)Si/SiO_2 interface may come as a surprise, indeed.

We hypothesize that electrical inactivation of a significant density of Si DBs as interface traps is caused by the Coulomb blockage when the electric field of one charged defect precludes capture of a charge carrier of the same sign by a neighboring trap. However, in a picture where the defects would be randomly distributed over a two dimensional interface plane, such effect, earlier observed for the oxide hole traps near the (100)Si/SiO_2 interface,[27] would require areal trap densities in excess of 10^{13} cm^{-2}, which is higher than the occurring density of P_{b0} centers in (110)Si/SiO_2. Therefore, we suggest that P_{b0} centers at (110)Si/SiO_2 interface are clustered, and this trend becomes more pronounced with lowering of the oxidation temperature.

IV. CONCLUSIONS

In summary, the interface trap density $D_{it}(E)$ of (110), (111), and (100)Si/SiO_2 systems has been analyzed by conductance and capacitance methods. It is found that D_{it} is highly sensitive to the Si interface orientation, highest for the (111) face, and lowest for the (100) face, with (110)Si/SiO_2 closely resembling the (111)Si/SiO_2 case. Two peaks in the $D_{it}(E)$ profile within Si band gap, at about 0.25 and 0.85 eV above the VB, are observed for all three orientations and appear to be strongly correlated with P_b interface defects, responsible for the majority of amphoteric interface traps. While the atomic nature and the energy distribution of the traps at the studied interfaces are much identical, comparison between the density of the Si DB defects (P_{b0}-centers) and the areal density of (110)Si/SiO_2 interface traps reveals that not all P_{b0}s are acting as charge traps. We suggest clustering of the interfacial Si-DB defects as the possible mechanism of electrical inactivation of part of the P_{b0}-centers in (110)Si/SiO_2.

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