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Leakage mechanism in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures with AlN interlayer

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Abstract

Leakage of $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures was investigated by admittance–voltage profiling. Nominally undoped structures were grown by low-pressure metal-organic vapor-phase epitaxy. The investigated structures had an Al-content of 30%. They are compared to structures with an additional 1 nm thick AlN interlayer placed before the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ layer growth, originally to improve device performance. Conductance of field effect transistor devices with AlN interlayer, measured from depletion of the two-dimensional electron gas (2DEG) to zero volt bias at frequencies ranging from 50 Hz to 10 kHz, could be described by free charge carriers using a Drude model. The voltage dependent conductance shows a behavior described by either Poole-Frenkel emission or Schottky emission (SE). From the size of the conductance, as well as simulation of the tunneling current injected from the gate under off-state conditions by universal Schottky tunneling, SE is obvious. Evaluating the data by SE, we can locate the leakage path, of tens of nm in the range between gate and drain/source with contact to the 2DEG, originating from the AlN interlayer. The static dielectric constant in growth direction, necessary for the evaluation, is determined from various $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures to $\epsilon_{\parallel}(0) = 10.7 \pm 0.1$.

Keywords: metal-organic vapor-phase epitaxy, condensed matter, electrical properties, III–V semiconductor heterojunctions, dielectric constant

1. Introduction

Leakage currents reduce device reliability and performance caused by defects and impurities especially in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures, since the III-Nitrides are known to contain a large density of defects and dislocations [1]. Ionized donor states, located on the surface of $\text{Al}_x\text{Ga}_{1-x}\text{N}$, also contribute to the device quality [2, 3]. Waller *et al* [4]

showed on $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ high electron mobility transistor (HEMT) structures a leakage behavior that manifests as a frequency-independent conductance (G); or G/ω rises toward low frequency ν ($\omega = 2\pi\nu$).

In a recent publication [5], admittance–voltage profiling of $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HEMT structures was used to also determine the frequency dependent G/ω of field effect transistor (FET) devices. A Drude model describes the low frequency data originating from a current between gate and drain. Although not explicitly named as leakage, this part of G influences the performance of the devices, showing the same behavior as the one published by Waller *et al* [4]. We essentially used admittance–voltage profiling of $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HEMT structures to determine the frequency dependent capacitance (C) and G/ω of FET devices, describe the results using Debye and Drude

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models and relate the corresponding equivalent circuit to the complex dielectric function. A conventional HEMT structure, used as reference, and a structure with an additional 1 nm thick AlN interlayer placed before the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ layer growth were compared. These samples showed an obvious difference with respect to leakage, which was higher by a factor of 30 for the sample with an AlN interlayer while other parameters of the two structures were comparable. A Drude model describes the difference [5]. An in-depth interpretation, with regard to trap states [6, 7] as well as Al incorporation after growth [8], however, was at that time beyond the scope of the article.

Thus, an additional similar pair of structures were investigated with thicker $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ layers and otherwise optimized processing procedure, which will be described in section 2, for a better understanding of the leakage behavior. In the appendix, we will make use of C for the determination of the dielectric constant, which will be needed for further interpretation of G and the parameters determined by the Drude model.

2. Growth, experimental details and theoretical model

Epitaxial structures were grown by low pressure metal-organic vapor-phase epitaxy (MOVPE) on semi-insulating SiC substrates. (Samples used for the evaluation in the appendix are grown by MOVPE and by plasma-assisted molecular beam epitaxy (MBE), see also details there.). Two typical HEMT structures were selected for the investigation in a first approach [5]. Details of growth temperature, buffer growth and quality are described in [5]. A two-dimensional electron gas (2DEG) is formed at the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{GaN}$ interface (schematic diagram of sample A, see figure 1, left side). An additional 1 nm thick AlN interlayer is placed in one structure before the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ layer growth (schematic diagram of sample B, see figure 1, right side). A 10 nm thick GaN layer caps both structures. Due to the difference in leakage, another pair of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{GaN}$ HEMT structures, grown recently, were added to the investigation. Based on experiences made, the structures were modified in barrier and cap thickness. Both samples C and D have an 18 nm thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ layer, sample D has an additional 1 nm thick AlN interlayer grown before the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$. Both structures are capped by a 3 nm thick GaN layer (schematic diagrams see figure 1).

Recessed gate transistors (samples A and B) were fabricated in one process run such that the ohmic contacts are on the GaN cap while the gate was placed on the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ barrier. The recess is 0.8 μm wider than the gate metal to avoid lateral leakage [5]. Samples C and D were grown and processed with considerable optimization and processed in two different runs. The process was especially optimized for sample D due to the AlN interlayer, which leads to enhanced incorporation of residual impurities [6–8]. The gate was placed for both samples on the GaN cap layer, i.e. the process was done without recess compared to samples A and B. Devices were fabricated according to standard processing including passivation, wafer thinning and backside

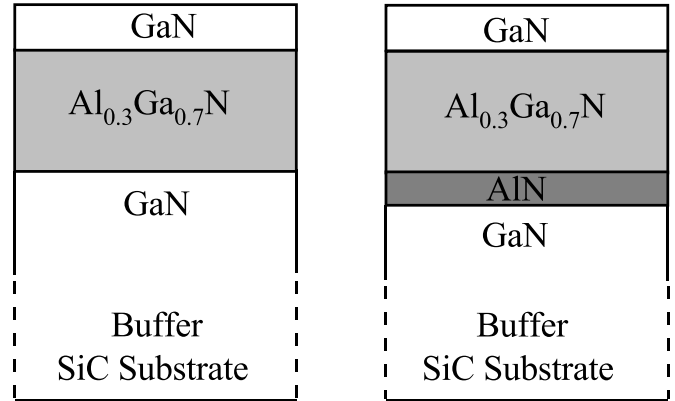


Figure 1. Schematic of the investigated HEMT structures. Conventional HEMT structure, used as reference, left side. Structure with an additional 1 nm thick AlN interlayer placed before the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ layer growth, right side. The respective thickness of the layers, see text.

vias. Small gate length devices show drain saturation currents around 1 A mm^{-1} and output powers at 10 GHz amount to 3.5 W mm^{-1} . Large area devices placed on the process monitor are investigated for the admittance measurements.

The Al-content and thickness of the heterostructure layers were determined by high-resolution x-ray diffraction (HRXRD). Details are described in [9]. However, the most accurate determination of the heterostructure dimensions with an uncertainty of ± 0.2 nm is only obtained for the sum of the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ barrier and the GaN cap layer. Besides the additional information on the AlN layer, a qualitative difference of samples with and without AlN interlayer is not seen with HRXRD.

As already seen for samples A and B the sheet resistance differs considerably that is due to the additional AlN layer. The AlN interlayer yields an increased electron concentration and a higher electron mobility of the 2DEG [5]. Hall effect measurements using Van der Pauw method of samples C and D confirm these results. Sample C has a sheet carrier density of $8.2 \times 10^{12} \text{ cm}^{-2}$ and a mobility of $1200 \text{ cm}^2 \text{ V s}^{-1}$, while sample D has a higher carrier density of $1.2 \times 10^{13} \text{ cm}^{-2}$ and a higher mobility of $1720 \text{ cm}^2 \text{ V s}^{-1}$. One expects improved device performance from the improved electrical properties.

Typical I – V characteristics of the transistors from sample C and D with gate length of 0.25 μm and gate width of 1200 μm are shown in figure 2. The graph depicts the leakage characteristics as well as the drain current at forward bias of the transistors with and without AlN interlayer, respectively. The sample with AlN interlayer shows a drain current in on-state being twice as much as for the sample without interlayer. However, the gate leakage current of the sample with interlayer raises strongly by two orders of magnitude as compared to the sample without interlayer. As expected, the drain current merges with the gate current at large reverse bias.

Admittance–voltage investigation was performed on processed FET devices in the frequency range from $\nu = 50$ Hz to

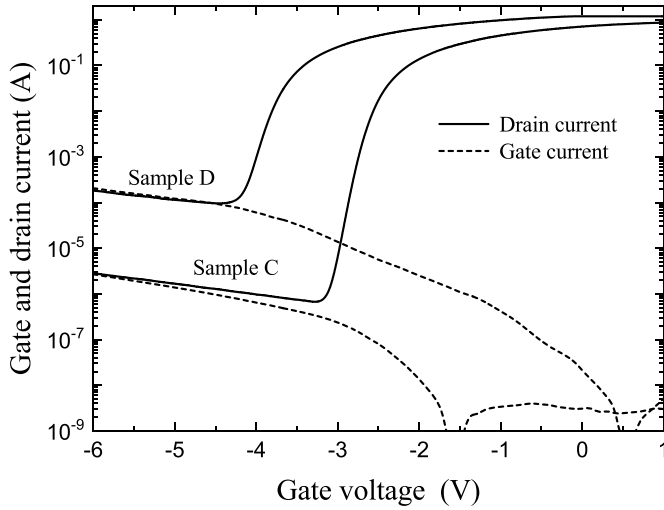


Figure 2. Gate and drain current as function of gate voltage of the samples with (D) and without (C) AlN interlayer. Gate length and width are $0.25 \mu\text{m}$ and $1200 \mu\text{m}$, respectively. The data are taken at a drain voltage of 10 V .

$\nu = 12 \text{ MHz}$. Measurements were done in steps of 0.1 V with a superimposed ac voltage of 50 mV using an HP 4192A Impedance Analyzer with a tungsten probe and automatic cable compensation. The procedure is identical to the one already applied in [5] where further details such as pad dimensions, contacting and measurement conditions are described. The measurement limit is $10^8 \Omega$. Frequency dependent admittance was obtained from the admittance–voltage measurements for defined voltages. The FET dimensions are $80 \mu\text{m} \times 200 \mu\text{m}$ (gate length \times gate width) with a gate-to-drain distance of $2 \mu\text{m}$. Smaller eight finger devices with dimensions of $0.3 \mu\text{m} \times 60 \mu\text{m}$ (gate length \times gate width) with a gate-to-drain distance of $3.5 \mu\text{m}$ showed similar results. However, due to the smaller capacity, reduced by a factor 100, only results above 100 kHz were measurable.

To simulate the tunneling current injected from the gate under the off-state conditions we use the universal Schottky tunneling (UST) model implemented in the ATLAS software from SILVACO. The tunneling current in this model is represented by localized tunneling rates at grid locations near the Schottky contact that is most relevant for the two-dimensional simulation of the HEMT device. Note that the thermal emission over the potential barrier due to the high-energy tail of the electron distribution in the gate metal is also taken into account. In the following, the combination of these two current components is referred as Schottky emission (SE).

3. Results and discussion

The contribution of free charge carriers in G/ω -profiles is seen preferably at frequencies below 10 kHz . The different behavior between samples with AlN interlayer and without interlayer is at these frequencies obvious. Examples

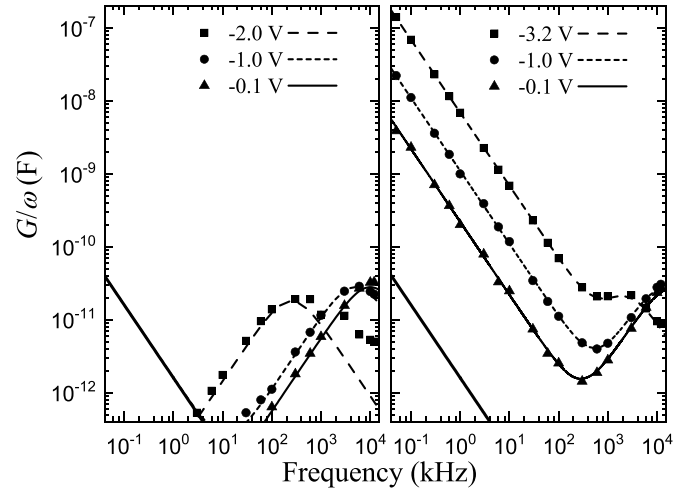


Figure 3. G/ω versus ν both on logarithmic scale of sample C (left side) and sample D (right side) in the frequency range 50 Hz to 12 MHz for three representative voltages. The lines are obtained by fitting the results by means of Debye and Drude model [5]. Assignment of data points and fitted curves see inset. The most negative voltage of sample C (-2.0 V) is close to threshold voltage; of sample D denotes the maximum of $G(V)$. Lower limit of measurement range is given by a bold line determined from $R_p = 10^8 \Omega$.

of G/ω -voltage profiles with frequency as parameter of sample B measured at frequencies of 50 Hz to 3 kHz are shown in figure 6 of [5]. The data show a behavior that is related to the dielectric function of free carriers with constant conductance [10]: G/ω increases with decreasing ν , the maximum stays at a fixed voltage and C remains unchanged.

Typical examples of G/ω versus ν are given in figure 3, both on logarithmic scales, of sample C (left side) and of sample D (right side) in the frequency range from 50 Hz to 12 MHz with bias as parameter, reaching from depletion onset of the 2DEG to near zero volt bias. In the frequency range above 10 kHz trap states are dominating, described by the Debye equations. Below 10 kHz essentially the free carriers are of importance, which is the part for the present analysis. The conductance is given by the following expression [5]:

$$\frac{G}{\omega} = \frac{C_s \omega \tau}{1 + \omega^2 \tau^2} + \frac{1}{\omega R_p}. \quad (1)$$

Here the series RC network having the capacitor C_s , the relaxation time τ of the interface states (Debye equation) is in parallel to the resistance R_p (Drude equation). Based on equation (1) the data are fitted. Though not necessary for the current evaluation, the Debye part is fitted for completeness. The results in figure 3 show clearly the influence of Drude-like behavior below 10 kHz of sample D with the AlN interlayer. In contrast, sample C exhibits only interface states. The contribution of free charge carriers is at least below the lower limit of the measurement range of the admittance–voltage setup of $10^8 \Omega$. Using $R_p = 10^8 \Omega$ in equation (1), yields the bold line.

Results of sample A and B, as reported earlier, revealed in both cases a contribution of free electrons [5]. However, sample B with the 1 nm AlN layer placed between barrier and 2DEG had a higher leakage by a factor of 30 or which is equivalent a lower R_p . Besides the contribution of enhanced incorporation of residual impurities, one may expect surface oxidation due to residual Al that induces surface traps and thus increases leakage. The values of R_p for sample A were at its minimum in the range of $10^7 \Omega$, which is quite close to the measurement limit of the admittance voltage profiling setup of $10^8 \Omega$.

Despite the slightly changed structure and the different processing, the leakage is found for both structures with AlN interlayer. Sample D with optimized process even yields a maximum G/ω , which is an order of magnitude greater as for sample B. One has to keep in mind that sample B is a recessed gate transistor. The recess range is $0.8 \mu\text{m}$ wider than the gate metal to avoid lateral leakage which may account for the lower values of G/ω .

Mitrofanov and Manfra [11] reported Poole-Frenkel emission (PFE) from traps in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ transistors. Consequently, it should follow that in admittance-voltage profiling PFE should also be observed. However, as described in detail by Simmons [12], a quite similar behavior is found for SE if the electronic mean free path in the investigated barrier is less than the thickness of the barrier. Hence, before applying SE, the critical parameter ‘mean free path’ is determined based on the considerations given by Sze and Ng [13]. The mean free path is estimated in the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{AlN}$ barrier, using the thermal velocity of electrons and electron mobility between 10 and $100 \text{ cm}^2 \text{ V s}^{-1}$, with the lower value assigned to layers of higher Al-content [14–18]. The resulting electronic mean free path ranges from 0.3 to 3.3 nm that is smaller than the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{AlN}$ barrier. The modified version of SE is therefore applied further on.

Thus, PFE and SE should show the same exponential behavior as well as a prefactor for the conductivity σ , which is in both cases independent from the electric field. This is seen by plotting the logarithm of conductance versus the square root of the electric field. The electrical field is given by the bias V over the respective width w , where w denotes the electron path. The conductivity σ , originating from PFE due to the residual defects in the semiconductor, is given by [12, 19]:

$$\sigma = en_c \mu \exp\left(-\frac{\varphi_T}{kT}\right) \exp\left(\frac{\sqrt{e^3 |V| / (w\pi\epsilon_{||}(0)\epsilon_0)}}{kT}\right), \quad (2)$$

with electron charge e , electron density in the conduction band n_c and mobility μ , trap energy level φ_T , Boltzmann constant k , temperature T , static dielectric constant parallel to the c -axis $\epsilon_{||}(0)$ (see appendix) and dielectric constant of vacuum ϵ_0 .

A very similar expression for σ originating from the modified SE yields [12]:

$$\sigma = eN_c \mu \exp\left(-\frac{\varphi_B}{kT}\right) \exp\left(\frac{\sqrt{e^3 |V| / (4w\pi\epsilon_{||}(0)\epsilon_0)}}{kT}\right), \quad (3)$$

with electron effective density of state $N_c = 2(2\pi mkT/h^2)^{3/2}$ (N_c , see for example Spenke [20]) in the conduction band with an effective mass $m = 0.25 m_0$, Planck constant h and conduction band offset φ_B , taken as Schottky barrier height. Other notations are as above.

Multiplying the appropriate device dimensions, length w and cross-sectional area Q with σ , the expression for $1/R_p$ is obtained:

$$\frac{1}{R_p} = \sigma \frac{Q}{w}. \quad (4)$$

Results of the fitted free carrier contribution $1/R_p$ are given in figure 4 for samples B and D. The same result is achieved by multiplying G/ω with ω : $G \approx 1/R_p$ for $\nu \leq 10 \text{ kHz}$. However, a reduced data scatter is the advantage of the fit. The slope of $1/R_p$ -voltage curve leads to a straight line in this plot. All fitted data are above threshold voltage. Besides natural constants, only two other parameters may influence this slope: $\epsilon_{||}(0) = 10.7$ (result see appendix) and w of the device. In the current analysis, only w is of relevance which yields $w = (11.4 \pm 1) \text{ nm}$ for sample B and $w = (29.8 \pm 1.2) \text{ nm}$ for sample D if SE is assumed. For PFE both values have to be multiplied by a factor of four. An illustration of the principal geometrical situation between a biased gate and drain is given in the inset of figure 5, left side (not to scale) with w (dashed line) obtained by SE and distance d (full line) between gate and 2DEG.

Apart from PFE and SE we also considered Fowler-Nordheim tunneling [19] within the framework of the evaluation of samples B and D. However, the data could not be fitted in the measured voltage range, since the functional behavior of σ is proportional to $V \exp(-b/V)$ [19]. The constant b summarizes natural constants, w and φ_B .

A possible chance to discriminate between the two mechanisms PFE and SE is the bias independent prefactor of equation (2) (PFE) and 3 (SE). However, material properties have to be presumed in both cases, for PFE (n_c , μ and φ_T) and for SE (μ and φ_B). The introduction of AlN leads to enhanced incorporation of impurities, especially the donor oxygen that might affect the electrical performance of a device [6, 7]. In a straightforward way, we use material properties of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ with the residual impurity oxygen for PFE, $n_c = 5 \times 10^{17} \text{ cm}^{-3}$, $\mu = 100 \text{ cm}^2 \text{ V s}^{-1}$ and the activation energy of $\varphi_T = 90 \text{ meV}$ [14, 21]. Due to the GaN cap, $\varphi_T = 29 \text{ meV}$ is also considered [22]. Besides $N_c = 3.14 \times 10^{18} \text{ cm}^{-3}$ and the same μ , merely $\varphi_B = 0.39 \text{ eV}$, determined by the conduction band offset for an Al-content of

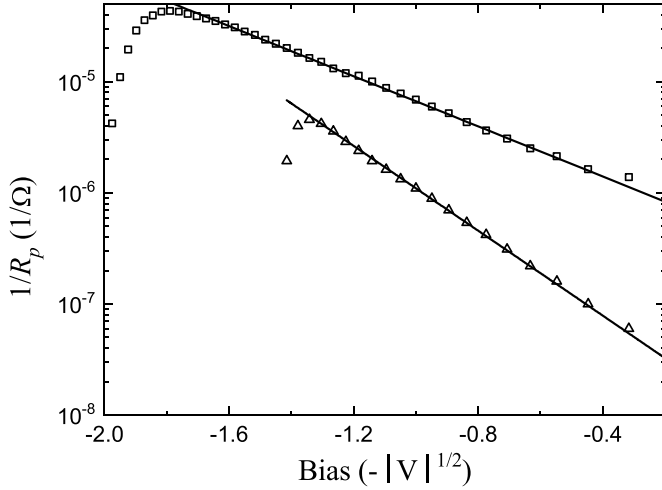


Figure 4. Free carrier contribution $1/R_p$ versus the square root of bias for frequencies below 100 kHz fitted by the Drude model of sample B (open triangles) as well as sample D (open squares). Both results are fitted by model based on SE (lines).

30% [23], is used for SE. The higher Al-content of the AlN barrier is ignored. For the dimensions of R_p , we take w and for the cross-sectional area Q , i.e. the gate width of 200 μm and a current carrying thickness of d , i.e. barrier and cap. Using the given numbers for sample D, the estimation yields $9 \times 10^{-4} \Omega^{-1}$ or considering the GaN cap $9 \times 10^{-3} \Omega^{-1}$ for PFE and $2 \times 10^{-7} \Omega^{-1}$ for SE. It has to be noted, that the contribution of φ_T (PFE) and φ_B (SE) is dominant. Similar results are achieved for sample B. The prefactor of the fitted results is $1.4 \times 10^{-8} \Omega^{-1}$ for sample B and $4.9 \times 10^{-7} \Omega^{-1}$ for sample D [24]. These values are close to the results obtained for SE. Thus, we may conclude that SE is the dominating process.

Further support of SE is obtained by UST. As observed in the simulation, the largest tunneling rate occurs at the drain-side gate edge (see the insert of figure 5 on the right side). It should be noted that the tunneling current depends strongly on the doping concentration of the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ barrier (assumed doped with acceptors) which, in turn, substantially affects the low-field mobility of electrons propagating through the barrier. However, geometrically the pathway of the leakage current towards the 2DEG remains essentially the same at different acceptor concentrations of the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ barrier, i.e. tilted at the same angle relative to the vertical direction. The results of the simulation (circles) are given in figure 5 where the length of current path w is plotted versus distance d of the 2DEG channel from gate. Data from samples B and D, assuming SE, are given by squares. The error bars indicate the accuracy of the fits.

For both samples B and D, w is slightly wider than the distance d between gate and 2DEG. The result seems to support the earlier assumption to place R_p of the equivalent circuit between gate and drain [5]. However, the resulting values of w are far too small compared to the distance of 2 μm between

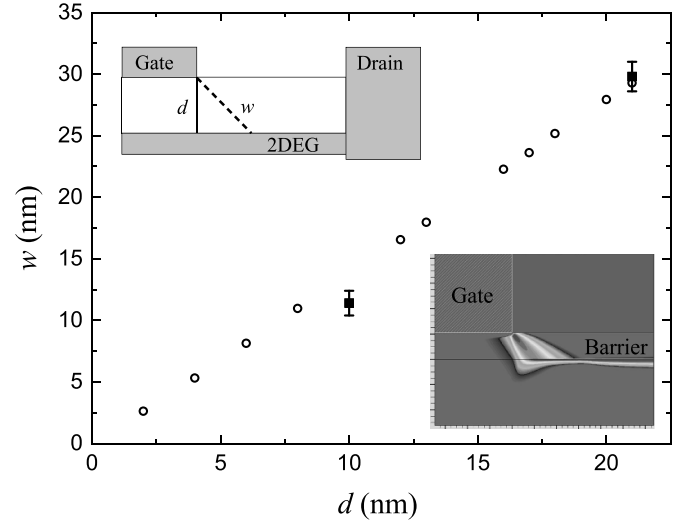


Figure 5. Length of current path w versus distance of 2DEG channel from gate d , results of simulation (circles) and data from samples B and D (squares). Error bars indicate the accuracy of the fits. An illustration of the principal geometrical situation between a biased gate and drain (not to scale) is given in the inset (left) with w (dashed line) obtained by SE and distance d (full line) between gate and 2DEG. The inset on the right shows the current distribution obtained by simulation.

gate and drain, i.e. w associated with the electric field does not match the geometrical dimensions of the devices. A detailed explanation of the behavior of samples B and D has to consider two points. First, enhanced incorporation of residual impurities after growth of the AlN layer yields higher n-type behavior of the following $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and GaN layers and therefore a lower of R_p . Second, one needs to consider that the electric field induced by the gate voltage stretches laterally out to the drain region. However, barrier and cap layer are depleted by the surface potential of the un-gated region. Further, the interface charge between SiN passivation layer and $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ barrier also contributes to the depletion. As discussed in literature [25–27] this charge is in most cases positive and the interface charge affects the 2DEG concentration in the access regions and only slightly the thickness of the depletion region under the gate as well. Thus, the leakage path must be connected to the drain contact by the well conducting 2DEG channel of the un-gated region between gate and drain. The simulation results at different values of the interface charge showed that the tilted angle of the leakage current pathway remains approximately the same. Hence, based on the simulation results, one may conclude that the distance w for the leakage current from the drain-side gate edge to the 2DEG depends only on the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ barrier thickness. Based on the results of SE, we conclude that the leakage path connects to the 2DEG, though not directly under the gate, but in a distance w for the respective samples. The conclusion is supported by the behavior of $1/R_p(V)$, which drops with the depletion of the 2DEG channel.

4. Conclusion

Leakage of $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures was investigated by admittance–voltage profiling. The nominally undoped structures, grown with an Al-content of 30%, were compared to structures with an additional 1 nm thick AlN interlayer placed before the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ layer growth. Conductance of FET devices with AlN interlayer, measured in the frequency range from 50 Hz to 10 kHz, could be described quantitatively by free charge carriers using a Drude model. We propose that the devices with AlN interlayer have leakages located in the range between gate and drain/source with direct contact to the 2DEG. The voltage dependent conductance shows a behavior described best by SE. Simulation of the tunneling current by UST model supports the experimental result. With the additional pair of structures C and D as well as optimized wafer processing, we obtained an improved quality of the sample C, i.e. the samples showed no leakage. With the samples containing an AlN interlayer, we could demonstrate the influence of defect incorporation during growth in the following $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ barrier. These defects prevent the improvements expected at the AlN/GaN interface that are increased electron concentration and mobility.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

Acknowledgments

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Appendix: The static dielectric constant of $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures

The dielectric constant was determined by measuring the capacitance of HEMT structures. The frequency independent $C(\nu)$ below 100 kHz, clearly above threshold voltage, is only dependent on the respective applied gate voltage [5]. A zero gate voltage is a prerequisite to avoid introducing a series capacitance of the analyzer setup. Then $C(\nu)$ allows an extrapolation to the static value of the capacitance, $C(0)$.

Since $\text{Al}_x\text{Ga}_{1-x}\text{N}$ is an anisotropic material, there are two components that describe the response of the crystal when an electric field is applied, either parallel or perpendicular to the c -axis of the crystal. Capacitance–voltage measurements are done on devices grown in c -direction. The probed material properties are those parallel to the c -direction and $C(0)$ is related to $\varepsilon_{\parallel}(0)$ and ε_0 , by the capacitor dimensions:

$$C(0) = \varepsilon_{\parallel}(0) \varepsilon_0 \frac{A}{d}, \quad (\text{A1})$$

which is the gate area A and distance d between gate and 2DEG. Both, A and d are known dimensions for a processed HEMT and it is possible to determine $\varepsilon_{\parallel}(0)$ from $C(0)$. While A is easy to obtain for processed devices, the gate-to-electron channel separation is critical, since d of HEMT structures is in the range of tens of nm.

It is not differentiated between a single $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer and an $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructure for the evaluation of $\varepsilon_{\parallel}(0)$, explained based on published experimental [28–33] and theoretical [34, 35] data of GaN and AlN. The experimental results for $\varepsilon_{\parallel}(0)$ of GaN range from 9.8 ± 0.3 [30], determined by spectroscopic method, to 10.6 ± 0.3 [31], determined by capacitance–voltage profiling. The experimental value for $\varepsilon_{\parallel}(0)$ of AlN is 10.7 [29], close to the results of GaN. A similar situation holds for the theoretical data for $\varepsilon_{\parallel}(0)$ of GaN with 10.28 [34] and 10.34 [35] as well as AlN with 10.31 [34]. Therefore, we conclude, due to the similarity of $\varepsilon_{\parallel}(0)$ of GaN and AlN it is sufficient to use $\varepsilon_{\parallel}(0)$ determined by HEMT structures.

Eight samples from four different HEMT structures with $d > 20$ nm were selected for the determination of $\varepsilon_{\parallel}(0)$, see table 1. Capacitance–voltage profiles of two representative FETs, with different d , are shown in figure 6, left side, measured at 10 kHz with a gate voltage ranging from 0.5 V to -3 V. As expected from equation (A1), C increases with decreasing d at zero bias. The 2DEG is depleted towards negative voltage and the capacitance drops accordingly. Capacitance–frequency profiles, taken at zero gate voltage, confirm the constant $C(\nu)$ below 100 kHz, see figure 6 right side, and $C(0)$ is obtained directly from the measured data.

The dielectric constant $\varepsilon_{\parallel}(0)$ is obtained from the capacitance measurements by means of equation (A1) using the averaged data of $C(V = 0)$ below 100 kHz. The finite width of the 2DEG as well as the penetration of the 2DEG into the graded $\text{Al}_x\text{Ga}_{1-x}\text{N}$ has to be taken into account, see Mkhoyan *et al* [36]. The distance $\Delta d_{2\text{DEG}}$ of the 2DEG maximum from the center of the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ interface for an Al-content of 30% is in the range of 0.8 nm (0.9 nm for the sample with an AlN interlayer) and 0.7 nm for the sample with an Al-content of 20%. Thus, $\Delta d_{2\text{DEG}}$ is added to d for the determination of $\varepsilon_{\parallel}(0)$ (see table 1).

The results of $\varepsilon_{\parallel}(0)$ are given in table 1. Averaging the results, we obtained $\varepsilon_{\parallel}(0) = 10.7 \pm 0.1$ that is rather close to the values of GaN and AlN. The accuracy of the data is now discussed and the selection of samples substantiated. A major contribution comes from the resolution limit of the HRXRD data for d with $\Delta d = \pm 0.2$ nm. The error is given by $\Delta \varepsilon \cong \pm \varepsilon_{\parallel}(0) \times 0.2 \text{ nm}/d$ and the deviation is below 0.1 only for $d > 20$ nm. Due to the increase in uncertainty for $d < 20$ nm, we excluded such samples. The error of A with $\pm 0.5 \mu\text{m}$ for both, gate length and width, contributes less than 0.7% and the error associated with the electrical measurement contributes below 0.3%. Both contributions are therefore not considered. The impedance of the channel is much smaller than that of the barriers; the series resistance of the channel is thus omitted.

Table 1. List of relevant structure data under the gate of samples for the determination of $\varepsilon_{||}(0)$. A detailed description of parameters see text.

structure epitaxy	Al-content x	AlN interlayer	C (pF)	d (nm)	$\Delta d_{2\text{DEG}}$ (nm)	$\varepsilon_{ }(0)$
C	0.3	no	69.0	21.2	0.8	10.72
MOVPE			69.1			10.73
D	0.3	yes	69.0	21.0	0.9	10.67
MOVPE			68.2	21.3		10.69
E	0.3	no	72.0	20.2	0.8	10.67
MOVPE			71.9			10.66
F	0.2	no	60.0	25.0	0.7	10.88
MBE			59.5			10.79

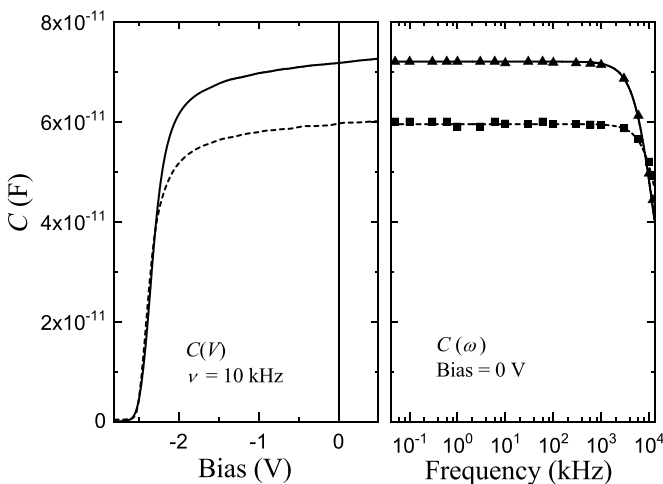


Figure 6. Capacitance–voltage profiles of two representative FET devices measured at $\nu = 10$ kHz (left side): sample E (full line, $d = 20.2$ nm) and sample F (short dashed line, $d = 25$ nm). The lines are viewing aids. Data points, measurements in steps of 0.1 V, are omitted since the data are well represented by the viewing aids. A line indicates zero gate voltage. Capacitance–frequency profiles taken at zero gate voltage (right side) of the same samples as on the left side, sample E (triangles) and sample F (squares). The lines are obtained by fitting the results of capacitance and conductance (not shown) by means of the Debye equations [5].

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