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Highly insulating, fully porous silicon substrates for high temperature micro-hotplates

Frieder Lucklum[a,*], Alexander Schwaiger[b], Bernhard Jakoby[a]

[a] Institute for Microelectronics and Microsensors, Johannes Kepler University Linz, Altenberger Str. 69, A-4040 Linz, Austria
[b] Research and Development, E+E Elektronik Ges.m.b.H., A-4209 Engerwitzdorf, Austria

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ABSTRACT

As alternative to established thermal substrates and thin membranes, we have investigated fully porous silicon substrates as highly insulating material for thermal devices. Exhibiting a thermal conductivity similar to silica glass and considerably lower than silicon nitride due to increased phonon scattering, thick mesoporous silicon also offers improved thermal and mechanical stability. Our work has focused on full wafer thickness porosification as a not extensively documented use of porous silicon and its application to thermal devices. Here we present measurement and finite element simulation results for our latest generation thin film microheaters on fully porous silicon substrates as proof of concept devices. Porosity, mass density, and specific heat capacity of porous silicon are deduced from fabrication parameters, thermal conductivity is determined by the so-called 3ω-measurement method, and all material properties are validated by fitting measurement data to our finite element models. For thick fully porous domains we estimated a thermal conductivity of ≈0.9 W/m/K, as well as a density of ≈1200 kg/m^3, a specific heat capacity of ≈780 J/kg/K and a corresponding volumetric porosity of ≈50%. Thin film fabrication of nitride passivation and molybdenum meander microheaters on fully porous domains allowed characterization of thermal performance and insulation. For 10 mm^2 microheaters we measured a power efficiency of 0.40 K/mW stable up to a maximum temperature of 475 °C, compared to 0.37 K/mW stable up to 440 °C on silica glass. Both static and dynamic heater measurements show superior performance of fully porous silicon substrates compared to reference samples on thin silica glass substrates.

1. Introduction

Thermal effects are used for a wide range of sensors and actuators in microsystems, with miniaturization offering, e.g., improved sensitivity, decreased reaction times, reduced energy consumption, and easier integration with other microsystem components. Highly localized temperature hotspots, large temperature gradients, precise spatial and temporal temperature and heat flow control can be achieved to realize temperature sensors, flow sensors, microheaters, or gas and humidity sensors. In order to facilitate such precise control, thermal insulation between regions of different temperatures to minimize thermal losses poses one of the biggest challenges in design and fabrication of such devices. One standard approach is to place the heated structures onto thin, often suspended membranes made of materials with low thermal conductivity, e.g. silicon nitride membranes, thin glass substrates, or more exotic material combinations [1–3]. A disadvantage to this approach is the increasing fragility and decreasing stability of thinner and thinner membranes or substrates of a few microns down to a few 10 nm.

In our work we have been investigating alternative technologies for improved performance of thermal devices. One such technology is the use of porous silicon as membrane or substrate material. Porous silicon (pSi) is a rather new material with unique physical properties and compatible to standard MEMS processing technologies [4–6] developed for use in a variety of applications, ranging from, e.g., optical and photonic devices [7,8], bulk sacrificial and structural material for MEMS [9–13], microfluidic devices [14,15], gas sensors [16,17], explosives [18], to thermal insulation layers [19]. Porous silicon can be electrochemically etched from bulk silicon wafers. The remaining silicon crystallites retain high mechanical stability, however at pore sizes below the mean free path of thermal phonons [20] and depending on porosity and pore morphology, the thermal conductivity is drastically reduced to the same order of magnitude as silica glass and below that of silicon nitride [21–23]. While a number of applications utilizing mesoporous silicon insulation layers and membranes of up to several 10 μm thickness have been demonstrated [24–26], to our

* Corresponding author. Tel.: +49 421 218 62645; fax: +49 421 218 62570.
E-mail address: flucklum@imsas.uni-bremen.de (F. Lucklum).

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knowledge fully porosified substrates have been attempted [27], but have not yet been extensively characterized and applied to thermal devices. As presented in this paper, moderately thick porous silicon substrates offer a promising alternative to fragile membranes or substrates.

To verify our approach of fully porous silicon substrates, we have extensively characterized our porous silicon fabrication process in terms of achievable volumetric porosity, etch rate, as well as pore size and morphology [28]. We utilized the 3ω-method for thermal conductivity measurements on thick porous silicon layers. We deposited thin film molybdenum microheaters on porous silicon, as well as on reference silicon and silica glass substrates for static and dynamic micro-hotplate characterization. Measurement results for first generation samples already showed a notable improvement, as published previously [29], however not achieving thermal insulation similar to the glass reference due to a thin residual non-porous silicon slice in the center of the porous region acting as thermal shortcut. In the following chapters, we will present the latest results of an improved fabrication process with backside thickness reduction for our second generation samples with confirmed full thickness porosification yielding device characteristics similar to or even better than microheaters on glass substrates or membranes. Additionally, we developed simulation models using the finite elements method (FEM) to validate the material properties of the fully porous silicon substrates by comparison with measurement data and thermal imaging.

2. Thick, fully porous silicon substrates

Porosification of silicon is an electrochemical wet etching process utilizing hydrofluoric acid (HF) to locally anodize the wafer surface and etch pores into single-crystalline silicon substrates. Anodization is achieved by the accumulation of positive charges (holes) at the semiconductor surface due to the presence of an electric field, which remove covalent bonds of surface atoms to the bulk material and thus increase the susceptibility to dissolution or oxidization of these atoms in the HF electrolyte. Operating in a high anodic potential regime with a surplus of holes arriving at the silicon–electrolyte interface results in etching on the whole wafer surface, a process termed electropolishing of silicon. Conversely, operating in a low anodic potential regime by limiting the applied current and thus the amount of positive charges leads to a statistically distributed etching effect. Here, these initial etch pits and other defect sites offer preferential break-through locations for further charges, yielding pore growth into the depth of the substrate. A general review of pSi formation, properties, and applications can be found in, e.g., [4–6,30–32]. Resulting porosity, etch rate, and pore morphology are dependent on a wide variety of process parameters. For the application as thermal insulation layers, small pore sizes, high porosities and sponge-like pore morphology are most desirable. The fabrication setup, electrochemical etching process, characterization of fabrication parameters, as well as process challenges of our work have been published previously [29].

2.1. Porosity and morphology

Volumetric porosity P as the ratio between pores/air and remaining silicon can be estimated gravimetrically by $P=(m_0-m_1)/(m_0-m_2)$ where m_0 is the initial mass of the wafer, m_1 the mass after porosification, and m_2 the mass after removal of the porous silicon in a weak potassium hydroxide (KOH) solution. The obtained volumetric porosity for (100) p^+-type silicon wafers ranged from 20% to 85% with a standard deviation of 2.6% for repeated etch steps. The layer thickness d_{pSi} can also be calculated from gravimetric measurements by $d_{pSi}=(m_0-m_2)/(\rho_{Si}\times A)$, where ρ_{Si} is the mass density of silicon and A the effective wafer surface area under etch. The average etch rate r is then calculated using the etching time, resulting in a range of a few micrometer per minute and up to 10 μm/min with a standard deviation of 3%. Aside from thickness verification we also used a surface profiler (*Dektak XT Stylus Profiler*, Bruker Nano) for etch profile determination. For most of the wafer surface the etch depth is uniform within ≈1%, however, there is a pronounced overetching of around +10% at electrically insulated edges of each etch region due to a converging electric field and therefore a local increase of the current density. When etching through a complete substrate this edge effect leads to a local "break through" spots with a large local current density increase resulting in large local mechanical stress. To reduce this stress effect we employ an alternated double-side etching scheme described in Section 2.3. The effective heat capacity of porous silicon as the product of mean mass density and specific heat capacity of the remaining silicon crystallites can be determined directly from the volumetric porosity.

Pore size and morphology, investigated via SEM imaging and documented in [29], show a mesoporous surface with pore sizes between 5 and 40 nm. For standard samples with 50–60% porosity we measured pore sizes of around 15 nm and the desired sponge-like morphology. Investigation of the breaking edge of a sample from the center region of a fully porosified wafer also indicated full wafer porosification with little to no remaining bulk silicon which could act as a thermal shortcut and reduce the insulation effect.

2.2. Thermal conductivity

To determine the thermal conductivity of these porous silicon substrates we employed the 3ω-measurement method [33]. Applying a sinusoidal heating current at frequency ω across a line source heater generates a thermal wave propagating into the substrate at 2ω, which results in a corresponding resistance modulation of the heater line. By virtue of Ohm's law, this dynamic resistance modulation together with the driving current yields additional spectral voltage components at frequencies ω and 3ω. The amplitude of the 3ω component is only related to the temperature amplitude ΔT, i.e., $U_{3\omega}=1/2\,\alpha R_0\Delta T I_0$, with temperature coefficient α, operating resistance R_0, and driving current amplitude I_0 as parameters. The penetration depth of the thermal wave is determined by the square root of thermal diffusivity D divided by 2ω. Here, $D=\lambda/(\rho c_p)$, with thermal conductivity λ and ρc_p the volumetric heat capacity. Within the constraints of penetration depth smaller than layer thickness but much larger than width of the heater to satisfy the line source condition and with the limitation to isotropic and homogeneous materials, an approximate solution for the temperature amplitude has been established [33]. In complex notation assuming a harmonic time dependence $\exp(j\omega t)$, the temperature amplitude ΔT can be written as $\Delta T=P/(\pi l\lambda)\,[1/2\ln(4D/r^2)-1/2\ln(2\omega)-\gamma+j\pi/4]$ with $\gamma\approx0.5772$ being the Euler–Mascheroni constant and j the imaginary unit. The real part of the temperature change is proportional to the logarithm of the frequency, with parameters being heating power P per unit length l and thermal conductivity λ of the penetrated material. Therefore the slope of a $\mathrm{Re}(\Delta T)-\ln(\omega)$ plot taken from the measurement of the 3ω component of the voltage across a line source heater allows direct determination of the thermal conductivity.

We utilize a custom tunable measurement circuit with a Wheatstone bridge layout driven by an arbitrary function generator (*Agilent 81150A*), bridge output amplified by an instrumentation amplifier (*INA 129U*, Texas Instruments) and the 3ω component extracted with a lock-in amplifier (*SR830*, Stanford Research Systems). An exemplary measurement result is given in Fig. 1 for a 175 μm thick pSi layer on silicon substrate (red dots) compared to

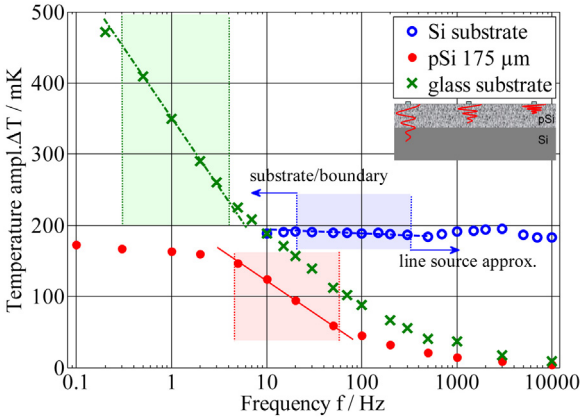

Fig. 1. Exemplary 3ω-measurement results for silicon (blue circles), porous silicon (red dots), and silica glass (green crosses), with shaded area indicating the linear region for determination of the thermal conductivity; with inset of a porous silicon layer on silicon substrate showcasing thermal wave penetration larger than layer thickness being dominated by the conductivity of silicon, corresponding to <5 Hz in the red graph (left), in the linear region (middle), and below the line source approximation limit, corresponding to >60 Hz in the red graph (right). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

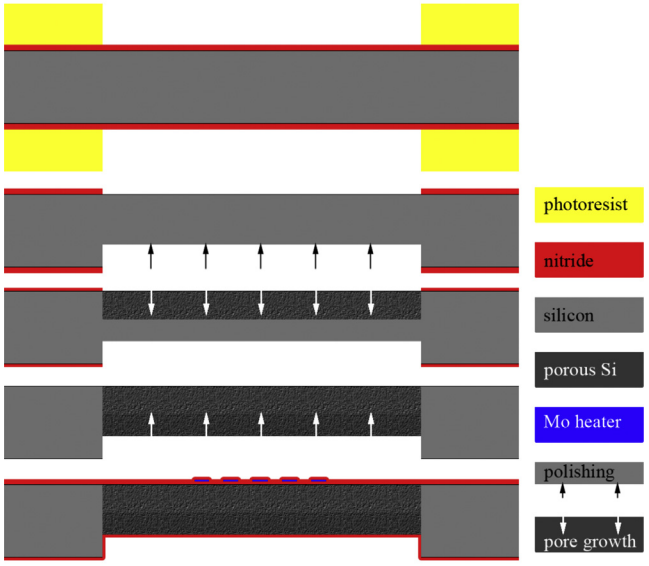

Fig. 2. Simplified process flow for thermal devices on fully porosified, reduced thickness silicon substrates with alternated etching scheme; microheater (blue) on the top surface above porous region and cavity defined by silicon nitride mask (red) surrounded by silicon frame. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

a pure silicon substrate (blue circles) and silica glass (green crosses) with the shaded areas indicating the linear regions. From the linear fit we calculate a conductivity of about 0.9–4.7 W/m/K for different pSi samples, with a mean value of ≈1.5 W/m/K for our 60% porosity fabrication samples, compared to 133 W/m/K for silicon and 0.5 W/m/K for thin silica glass substrates. The latter correspond to literature values and thus serve as validation for our measurement procedure. These results show that compared to non-porous silicon we have successfully reduced the thermal conductivity of thick porous silicon by two orders of magnitude into the same range as silica glass substrates and lower than silicon nitride thin films.

The conductivity values for our 3D porous structure are in line with measurements of other mesoporous layers with similar pore sizes [19,21], and show better insulation characteristics than 2D pores fabricated by lithographic methods as well as nanobeams and nanofilms of comparable size [20]. The three-dimensional sponge like structure is responsible for increased phonon scattering both in-plane and out-of-plane and thus increased thermal insulation even for full substrate thickness.

2.3. Device fabrication

First generation microheaters were deposited on full wafer thickness (≈500 µm) porous regions. While the etch rate for electrochemical porosification is high compared to other methods, it still required etch times of several hours, during which small changes in electrolyte concentration, applied current, or temperature can lead to large variations in etch depth. The variation in heater performance of first generation samples was quite large, with most devices suffering from a remaining non-porous silicon slice at the center of the wafer of up to 150 µm thickness acting as a thermal shortcut beneath the insulating thick porous silicon layer. For the second generation fabrication we therefore employed a wafer thickness reduction step prior to porosification to reduce the required etch times and uncertainties about full porosification (which can only be verified in a destructive process after complete wafer processing). Fig. 2 shows the complete second generation process flow, starting with a silicon nitride mask (red) on a silicon wafer to define the porous regions, the thickness reduction from the rough backside up to 200 µm depth using the same electrochemical etch operating in the electropolishing regime (black arrows), and the alternated porosification etch from the front and back (white arrows). For polishing and porosification we utilized an etch bath consisting of 25% HF, 40% ethanol as surfactant, and DI water in our double-cell electrochemical setup (MPSB100, AMMT GmbH, Germany). Standard process parameters for our 4″ p^+ doped (1 0 0) silicon wafers (0.01–0.05 Ω cm) included the constant current source set to an applied current density of around 150 mA/cm^2 for backside etching and 30–50 mA/cm^2 for porosification, with a resulting voltage drop across electrolyte and wafer of 8–10 V and 2–3 V, respectively. While illustrated only as a two-step process here, the porosification can also be done in the form of a pulsed, multi-step etch for improved uniformity and reduced stress. After porosification and thorough rinsing and drying, the wafer is stabilized at 300 °C in ambient atmosphere and passivated with a silicon nitride layer. The stabilization results in a uniform native oxide layer on the whole porous surface area and partially reduces the stress introduced during porosification. The thick nitride passivation layers seal the porous domains and prevent further oxidization, thus drastically reducing aging effects observed for as-prepared porous silicon. Finally, thin film deposition of thermal devices, in our case sputtering of molybdenum meander microheaters (blue) directly on the nitride passivation, is possible with only minor modifications to the thin film process parameters due to changed surface characteristics. The wafers are then separated into dies with the porous region surrounded by a 1 mm silicon frame for additional stability with an overall die size of 8.7 × 7.3 mm^2 (Fig. 3).

3. Measurements, simulation and discussion

The molybdenum meander microheaters have a footprint of around 10 mm^2 and a room temperature resistance on the order of 100 Ω. We investigated the maximum achievable heater temperature on porous silicon with a reduced thickness of 350 µm and an estimated porosity of ≈50% and compared the heater performance and power consumption to similar heaters on 300 µm borosilicate glass (*D 263 T*, Schott AG, Germany) substrates and 550 µm thick pure silicon wafers, as well as earlier pSi samples. Utilizing a climate control chamber (*WKL 100*, Weiss Klimatechnik GmbH, Germany)

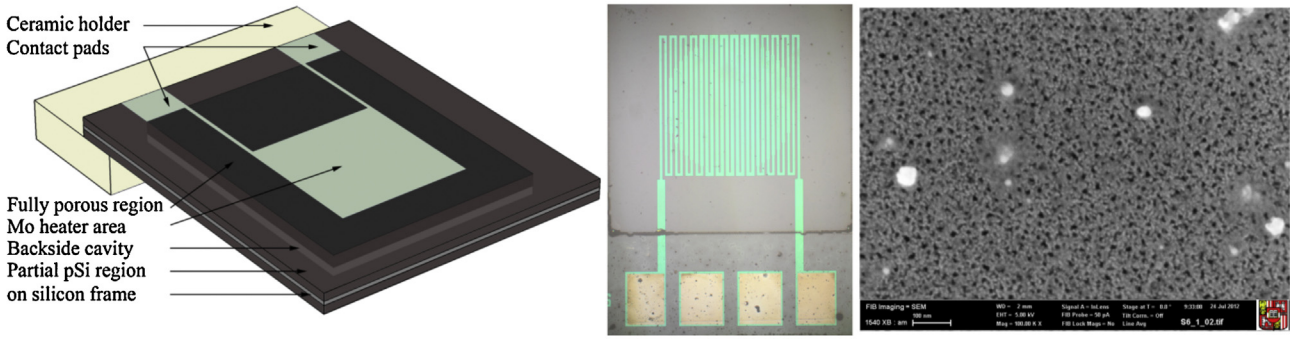

Fig. 3. Design of microheater measurement setup (left), micrograph of fabricated heater meander on fully porous region (middle), and SEM image of porous surface with around 15 nm pore sizes and sponge-like morphology (right).

we calculated the linear and quadratic temperature coefficient of the heater resistance between 0 and 150 °C, with the linear coefficient being on the order of 0.003 K^{-1}. The heater resistance was then simultaneously used to determine the mean heater temperature. All samples were placed in a custom spring-tip measurement setup designed for minimal heat conduction into the mechanical holder and electrical connections. The setup was placed in an airtight chamber to ensure only natural convection, the ambient room temperature was kept constant within ±2 K. The samples were connected to a current source (*EL302RT*, TTi, UK), applied current and resulting voltage were measured with precision meters and used to determine heater resistance, and thus mean heater temperature, as well as input power.

3.1. Static heater performance

A primary microheater characteristic is the power efficiency, mainly influenced by the insulation beneath the heater and thus the thermal conductivity of the substrate material. For this static measurement, the hotplates were suspended in air in a vertical rotation to ensure similar convection on front and back. The data points of the mean heater temperature (average temperature across heater area) were recorded when thermal equilibrium had been reached. Fig. 4 shows the static performance of the second generation porous silicon devices with a reduced substrate thickness of 350 μm beneath the heater, compared to the 300 μm thick reference silica glass samples, pure silicon wafers, and the first generation pSi with a remaining silicon slice of 150 μm in the middle of the substrate. Each data point corresponds to a stepwise increase,

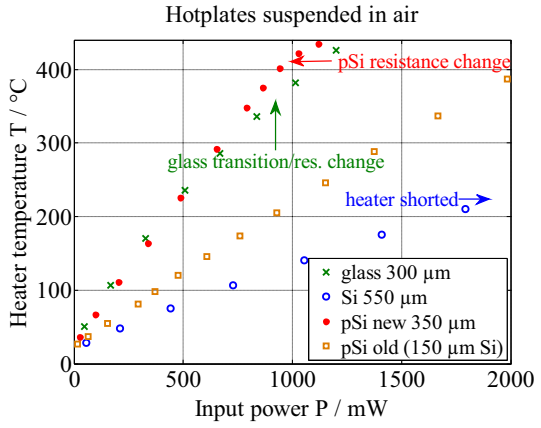

Fig. 4. Mean heater temperature calculated from heater resistance for different substrate types showing similar power efficiency for new porous silicon and glass, with pSi samples reversibly operating at 400 °C, transition effects for glass observed at temperatures above 350 °C.

applied current and resulting voltage are measured after waiting for thermal equilibrium, in general within 1 min. The data shows an improvement toward and above glass insulation behavior. The maximum mean heater temperature observed on pSi samples was consistently above 400 °C, where changes in the surface properties and metallization led to changes in the heater resistance usually followed by the formation of hotspots and heater burnout. A similar resistance change was repeatedly observed on glass samples at mean heater temperatures as low as 250 °C, and in general around 350 °C as marked in Fig. 4. While the transition temperature of the *D 263 T* borosilicate glass is listed at around 550 °C, most glass samples showed evidence of irreversible glass transition above this point, as well as changes in metallization and burnout at higher temperatures. These fault mechanisms currently limiting the maximum operating temperature do not affect the porous silicon substrate but only its metallization layer, while glass substrates are mechanically destroyed due to the transition stress effects. This result confirms a higher thermal stability of porous silicon than a standard silica glass.

The power efficiency of the 10 mm^2 molybdenum heaters can be calculated for the mean heater temperature from Fig. 4 to 0.40 K/mW, compared to 0.37 K/mW on silica glass, 0.18 K/mW on first generation porous silicon, and 0.10 K/mW on pure silicon substrates. Comparing these values to smaller devices from silicon nitride [34] and thin porous silicon membranes [26] already shows superior behavior of thick porous silicon substrates. Scaled to the heater area we calculate an effective power of 94.4 mW/mm^2 necessary to reach 400 °C on second generation pSi substrates, compared to 312.5 mW/mm^2 and 2000 mW/mm^2 for the referenced thin suspended membrane devices, respectively.

Handling during processing, pressing into experimental setups, and heating beyond maximum temperature also showcased the mechanical stability of porous silicon in a qualitative fashion. While thin membranes of smaller dimensions may break upon touch, the porous silicon samples are nearly as rigid as pure silicon dies. And while the similarly thick glass substrates broke apart beyond their maximum heater temperature, the porous silicon samples showed no sign of cracking, with the heater failure always restricted to the thin film layers.

As a different measurement, we also fixed the devices with thermal grease on a metal heat holder to act as a defined heat sink. Naturally, this is not the intended operating mode, but it allowed us to study the effect of heat conduction through the different substrates only, while losses due to convection, radiation, and conduction into holder and connectors can be neglected. The results are given in Fig. 5, where the new pSi heaters show an even better performance than glass samples. This effect can be partially attributed to the rough backside and reduced thickness cavity of the wafer, which therefore required a much thicker layer of thermal paste. Additionally, with heat flowing predominantly vertically from the

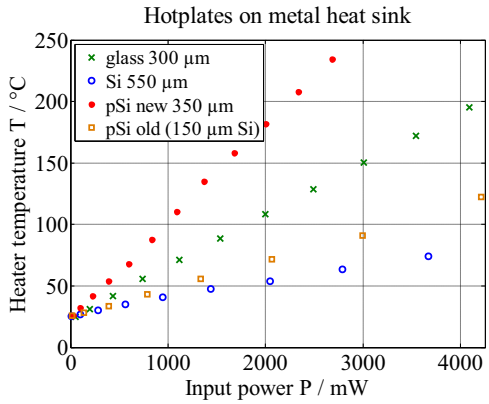

Fig. 5. Mean heater temperature for different substrate types with samples placed on metal holder as well defined heat sink, new pSi performance due to more limited thermal contact with heat sink as well as no thermal shortcut through thickness of wafer.

surface heater through the substrate into the metal heat sink, the silicon frame (see Fig. 3) around the porous area beneath the heater can be neglected in contrast to its influence on in-plane heat flow for operation as a suspended plate.

3.2. Thermal imaging of temperature distribution

We also used infrared imaging (*testo 890-2*, Testo AG, Germany) primarily to qualitatively visualize and compare spatial temperature distribution and insulation behavior across the hotplate devices. Additionally, for quantitative measurements the samples were coated with a thin high-emissivity, low conductivity black coating to verify mean heater temperature as well as to determine maximum heater temperatures. The known emissivity of the black coating was then entered into the camera software. We did not observe the coating to affect static heater performance, differences in temperature distribution for coated and uncoated samples and differences in required input power were negligible. Thus we could extract the mean temperature across the heater surface, showing good agreement with values from resistance measurements. Fig. 6 shows the thermographic images for glass, first generation pSi, and second generation pSi dies. While the remaining silicon slice in earlier pSi samples (middle) resulted in a considerable heat flux into substrate and measurement setup (blue and light blue regions), the heat is well concentrated and insulated at the heater region for glass substrates (left) and new porous silicon heaters (right). The temperature measurement also indicated that for good insulation the maximum temperature at the center of the heater is considerably higher than the mean temperature over the whole heater area, e.g., 415 °C maximum and 360 °C mean temperature for a new pSi heater.

3.3. Numerical simulation procedure

To qualify the thermal insulation behavior and quantify the previous measurements with thermal properties, we utilized numerical simulation tools (*COMSOL Multiphysics 4.3a*) to model the different samples. Micro-hotplate, electrical spring-tip contacts, and ceramic holder on which the hotplate was suspended were included in a 3D model (as shown in Fig. 3). Boundary conditions included a thin thermally conductive layer with the material properties of molybdenum as the metallization, a thin resistive layer between substrate and ceramic, and a boundary heat source on the heater area applying an input power similar to measurements. The heat loss mechanisms in the model comprised heat transfer coefficients for conduction through electrical connectors and ceramic substrate into holder, natural convection in air, as well as surface to ambient radiation. Material properties for glass and silicon, as well as molybdenum, copper contacts, and the ceramic, were taken from material datasheets in general for a range in excess of 0–500 °C.

The initial step was to fit the static and time-dependent simulations of glass and silicon substrates to measurement data for determination of the heat loss transfer coefficients. In this step the material properties are known and the heat transfer coefficients are entered as parameters into an optimization solver. The results of a static simulation for glass and silicon are shown in Fig. 7 with the heating power taken from the measurement parameters corresponding to the thermographic image for glass in Fig. 6 and similar for silicon, with the color scale adjusted appropriately. Maximum and mean temperature, heat flux, and temperature profile match very well with the same boundary conditions and model parameters for both materials.

The second step took the boundary conditions determined from the known material properties of glass and silicon and applied them to models for first and second generation porous silicon samples to determine those material properties and validate previous measurements and fabrication parameters. Here, the fit parameters of the optimization solver included mass density, thermal conductivity, and specific heat capacity of the porous silicon regions applied to lower temperature time-dependent heating curves as discussed in Section 3.4. We also used this simulation as a secondary means to determine the thickness of the remaining silicon slice in earlier pSi samples. Fig. 8 displays the static high temperature performance as validation of the model for first (left) and second generation porous silicon (right) again corresponding to the infrared images in Fig. 6 with a very good agreement of temperature and heat distribution. The result for earlier pSi proves the heat flowing primarily through the silicon slice (150 µm thick in this sample), while the reduced

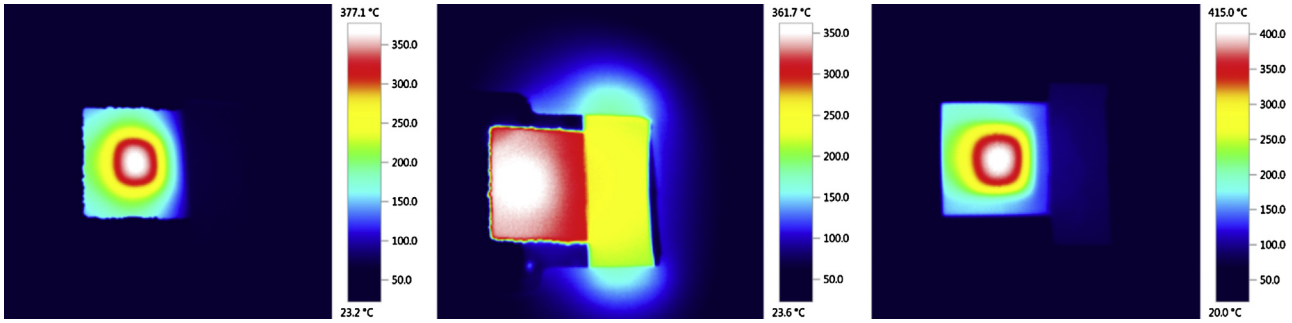

Fig. 6. Thermographic images of backside of suspended hotplate dies, with borosilicate glass substrate showing ideal insulation (left), first generation pSi samples limited by thermal shortcut through remaining silicon slice (center), and optimized second generation pSi sample with similar insulation to glass (right). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

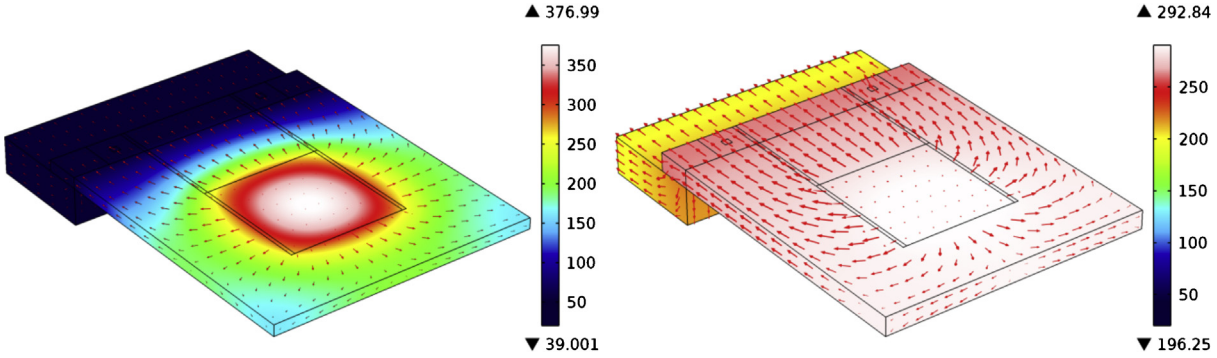

Fig. 7. FEM simulation results of temperature distribution (colors) and heat flow (arrows) corresponding to thermographic measurements in Fig. 6 using similar color table for good heater insulation on glass substrate (left) and no insulation on pure silicon sample (right). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

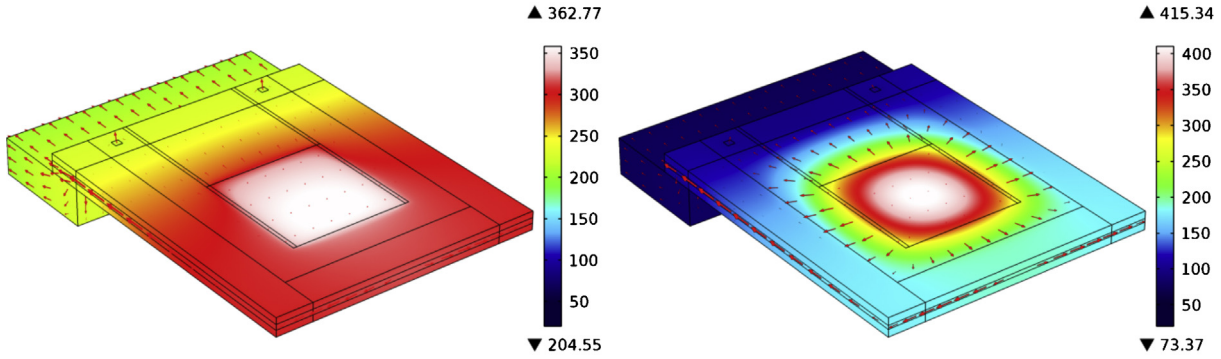

Fig. 8. FEM simulation results again corresponding to Fig. 6 for first generation pSi sample with mediocre insulation due to remaining silicon slice in middle of wafer (left) and good insulation similar to glass substrate for second generation pSi sample (right).

thickness porous region for the new dies insulates much better. The silicon frame around the porous region dominates the flow of the remaining heat into the substrate similarly to the silicon slice, but it is nearly negligible due to the strong insulation from the heater area.

3.4. Dynamic performance and thermal properties estimate

The second property of importance is the heat capacity of porous silicon, influencing the rise and fall times of heat steps. While the specific heat capacity will remain nearly unchanged as it is dominated by the silicon component of the silicon–air porous mixture, the effective, volumetric heat capacity of a pSi region is the product of specific heat capacity and mass density. The latter is directly proportional to the volumetric porosity. We applied power steps to porous silicon, silica glass, and silicon heaters and measured the temperature response, with a target of similar equilibrium temperatures for optimal comparison. These measurements were also used with the FEM simulation to determine the material properties for porous silicon.

In Fig. 9, we show dynamic measurement results both in ambient air and in a light vacuum. The porous silicon displays a faster response than glass samples due to a lower effective heat capacity even at a larger and thus more stable substrate thickness. We calculated the rise times between 10% and 90% of the temperature equilibrium of these curves to 10.0 s for new porous silicon devices, compared to 13.1 s for silica class and 27.3 s for silicon. The thin dotted line shows the very good fit of the FEM simulation. Additionally, the gray curves measured in a light vacuum (0.3 bar) and thus reduced natural convection validate a similar influence of convection on all samples.

As described in Section 3.3, the fit of the FEM simulation to these dynamic low temperature measurements, and then validated for static high temperature measurements, allowed us to extract material properties for porous silicon and compare them to the 3ω-measurements and electrochemical process parameter field. With the boundary conditions taken from the fits of the optimization solver for the glass and silicon heating curves, we can estimate a thermal conductivity of the porous silicon domains of ≈0.9 W/m/K, as well as a density of ≈1200 kg/m^3 and a specific heat capacity of ≈780 J/kg/K corresponding to a volumetric porosity of ≈50%. The 3ω-measurements and porosity estimate from the etch process parameters chosen for fabrication are in line with these values.

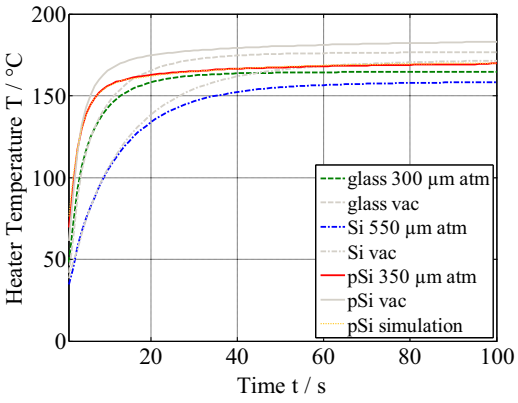

Fig. 9. Rise of mean heater temperature over time for glass, silicon and porous silicon substrates, including FEM results for pSi.

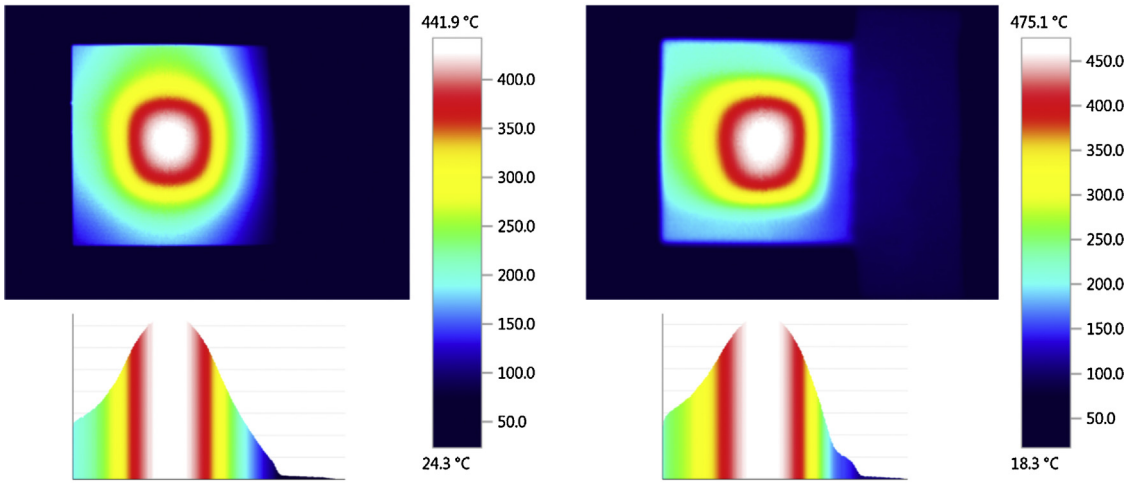

Fig. 10. Comparison of temperature distribution and line profile for silica glass substrate (left) and second generation pSi sample (right) showing nearly identical thermal insulation behavior.

Compared to the reference borosilicate glass substrate we fabricated a thicker and mechanically more stable porous silicon substrate with a similar low thermal conductivity and thus power efficiency, a higher reversible operating temperature maximum, and a considerably lower heat capacity and thus faster response times. Optimal performance samples are compared in Fig. 10, with glass (left) reaching a maximum reversible temperature of 440 °C and a mean heater temperature of 380 °C at 1 W input power, and porous silicon (right) reaching 475 °C maximum reversible temperature and a mean temperature of 415 °C at 1.2 W input power. Similar power efficiency, higher reversible temperature, faster rise time, and nearly identical temperature distribution and line profile as shown in Fig. 10 strongly support our proposal of using thick fully porous silicon substrates for thermal applications.

4. Summary and conclusions

We have investigated the use of porous silicon as substrate and membrane material for thermal devices. While thin mesoporous silicon layers up to several 10 μm have been established as MEMS material, used as thermal insulation layers and for thin membranes, we have proposed the use directly as moderately thick substrate material. Such substrates with thermal properties comparable to and better than these porous layers, thinner glass substrates, or silicon nitride membranes, also offer much better thermal and mechanical stability characteristics. The electrochemical etching process yields mesoporous sponge-like structures up to full wafer thickness with 20–85% volumetric porosity and pore sizes around 15 nm, which is below the mean free path of thermal phonons thus leading to a drastic reduction of thermal conductivity. Initial full porosification samples suffered from remaining non-porous silicon slices acting as thermal shortcuts, achieving only limited insulation but successfully validated the concept and material properties.

As presented in this paper, adjusting the fabrication process for reduced thickness full porosification yielded second generation porous silicon devices with optimal performance characteristics. Thin film molybdenum microheaters deposited on the fully porous regions achieved similar thermal insulation and power efficiency, faster response times, and higher operating temperatures than reference silica glass samples. Static and dynamic heater experiments were validated with thermographic measurements and finite element simulations. We also used the FEM results to investigate the different heat loss mechanisms and to determine the unknown material properties of the fully porous silicon domains. The results of this approach correspond very well to 3ω-measurements of thermal conductivity and to gravimetric porosity estimates for calculation of heat capacity and mass density. The various measurement results and the validation of these material properties strongly support the suitability of thick, fully porous silicon substrates for high-temperature thermal devices and applications.

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Biographies

Frieder Lucklum graduated from the Otto-von-Guericke University Magdeburg, Germany, and received his Dipl.-Ing. (M.Sc.) degree in microsystems technology in 2005. In 2010 he obtained his doctoral degree (Ph.D.) in the field of acoustic microsensors from the Johannes Kepler University Linz, Austria. From 2010 to 2013 he has been working as a Post-Doc research assistant on industry funded research projects in the fields of microsensors, novel sensor systems, and novel substrate materials such as porous silicon at the Institute for Microelectronics and Microsensors and the Austrian Center of Competence in Mechatronics (ACCM) in Linz, Austria. Since 2014 he is a senior researcher with the Institute for Microsensors, -Actuators and -Systems at the University of Bremen.

Bernhard Jakoby obtained his Dipl.-Ing. (M.Sc.) in Communication Engineering and his doctoral (Ph.D.) degree in electrical engineering from the Vienna University of Technology (VUT), Austria, in 1991 and 1994, respectively. In 2001 he obtained a venia legendi for Theoretical Electrical Engineering from the VUT. From 1991 to 1994 he worked as a Research Assistant at the Institute of General Electrical Engineering and Electronics of the VUT. Subsequently he stayed as an Erwin Schrödinger Fellow at the University of Ghent, Belgium, performing research on the electrodynamics of complex media. From 1996 to 1999 he held the position of a Research Associate and later Assistant Professor at the Delft University of Technology, The Netherlands, working in the field of microacoustic sensors. From 1999 to 2001 he was with the Automotive Electronics Division of the Robert Bosch GmbH, Germany, where he conducted development projects in the field of automotive liquid sensors. In 2001 he joined the newly formed Industrial Sensor Systems group of the VUT as an Associate Professor. In 2005 he was appointed Full Professor of Microelectronics at the Johannes Kepler University Linz, Austria. He is currently working in the field of liquid sensors and monitoring systems.