

## **Wide Bandgap Semiconductors for Power Electronics**

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Materials, Devices, Applications

*Volume 1*

*Edited by*

*Peter Wellmann*

*Noboru Ohtani*

*Roland Rupp*

**WILEY-VCH**

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## Preface

### Introduction

The scope of this edited book is to provide a state of the art of the technology and application of SiC and related wide bandgap materials. The focus lies on the material SiC with 16 review articles from internationally well-known experts covering major aspects of fundamental physics, applied science, as well as industrial development and manufacturing. In addition, five experts are reporting on the technological status of further wide bandgap materials GaN, diamond, and  $\text{Ga}_2\text{O}_3$ , which have the potential to even outperform SiC with respect to certain physical properties relevant for power electronics.

The semiconductor Si has dominated the fabrication of electronic devices for switching of electrical currents or for the application in microelectronics almost since the beginning of semiconductor technology in the early 1950s. For the application in power electronic devices, however, two major material properties limit the performance of Si: the medium breakdown field limits the achievable conductivity at a certain desired breakdown voltage as well as the medium heat conductivity hinders the release of excess power during device operation (e.g. overcurrent, short circuit, avalanche) and, hence, may cause thermal failure. From a physical point of view, wide bandgap materials like SiC, Diamond, GaN, AlN, and  $\text{Ga}_2\text{O}_3$  exhibit a much higher breakdown field that outperform their medium bandgap counterparts like Si and GaAs by a factor of 10 and more (see Table 1). Due to their strong covalent chemical bonding, the wide bandgap semiconductors diamond and SiC show a significant higher heat conductivity than the standard semiconductor Si. Hence, SiC- and diamond-based power electronic devices can handle much higher power densities than Si devices would do.

A key parameter for the choice of the proper semiconductor in power electronics is the so-called on-resistance of a power semiconductor device (Figure 1). Related to this, the Baliga's figure of merit (BFOM) defined as  $\epsilon \mu E_C^3$  ( $\epsilon$  = dielectric strength,  $\mu$  = charge carrier mobility,  $E_C$  = breakdown field) provides a selection rule for the proper choice of a semiconductor material for power electronic transistors. In literature, BFOM values are often calculated from idealized material properties that do not reflect the conditions under real device operation. Nevertheless, the BFOM value allows to rate the ultimate potential of each semiconductor related

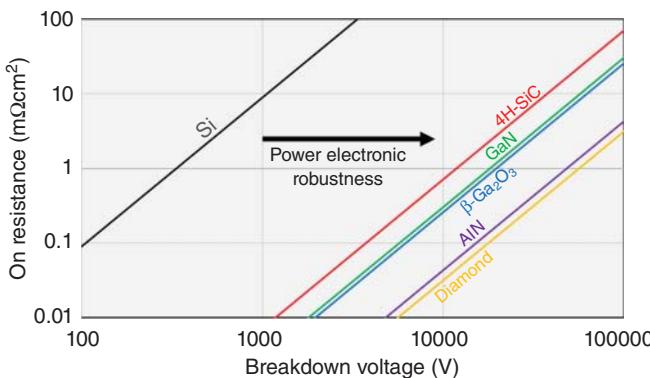
**Table 1** Physical properties (room temperature values) of wide bandgap semiconductors for power electronic applications in comparison to classic semiconductor materials (data from [1–3]).

	<b>4H-SiC</b>	<b>GaN</b>	<b>AlN</b>	<b><math>\beta\text{-Ga}_2\text{O}_3</math></b>	<b>C</b>	<b>Si</b>
Lattice parameter (Å)	$a = 3.08$ Hexagonal	$a = 3.19$ Hexagonal	$a = 3.11$ Hexagonal	$b = 3.04$ $c = 5.80$ $\beta = 103.7^\circ$ Monoclinic	3.57 Cubic	5.43 Cubic
$E_G$ (eV)	3.2	3.44	6.2	4.8	5.5	1.1
$E_B$ ( $10^5$ V/cm)	40	50	150	80	100	3
$\epsilon$	9.7	10.4	9.1	10	5.7	11.9
$\lambda$ (W /cm/K)	3–5	1.3	2.9	0.23	20	1.5
$v_S$ ( $10^7$ cm/s)	2.5	2.5	2.5 <sup>approx.</sup>	2	2.7	1
$\mu_n$ (cm <sup>2</sup> /V/s)	<900	<1000	300	250	<2200	1400
$E_D$ (meV)	60 (N)	22 (Si)	90–250 (Si)	20–30 (Sn)		45 (P)
$E_A$ (meV)	250 (Al)	160 (Mg)	500 (Mg))		400 (B)	44 (B)
$T_S$ (°C)	2830	2500	3000	1740	3900	1420
Doping capability	n-type <sup>med</sup> p-type <sup>high</sup>	n-type <sup>med</sup> p-type <sup>high</sup>	n-type <sup>high</sup> p-type difficult	n-type <sup>med</sup> No p-type	p-type <sup>high</sup> p-type	n-type
Baliga FOM $\epsilon \mu E_B^3$ with relation to Si	500	1100	8100	1350	11,000	1
Johnson FOM $v_S E_B / 2\pi$ with relation to Si	25	31	75	40	68	1
Native wafer material size	150 mm 200 mm <sup>dem</sup>	50 mm <sup>lowav</sup> 100 mm <sup>lowav</sup>	50 mm <sup>dem</sup>	150 mm <sup>dem</sup>	c. 100 mm <sup>dem,lim</sup> 300 mm 450 mm <sup>dev</sup>	200 mm 300 mm
Maturity of technology	c) Power <sup>b)</sup> High frequency <sup>c)</sup> Optoelectronics <sup>d)</sup>	a)	a), b)	a)	a)	d)

approx., approximated value; med, medium excitation energy; high, high excitation energy; dev, developed; dem, demonstrated; lim, limited crystal quality; lowav, low availability

The calculated Baliga FOM is based on idealized charge carrier transport properties that are usually not realized in a real electronic device. The usage of the materials breakdown field  $E_B$  as critical breakdown field  $E_C$  is an overestimation. Also, in the case of the Johnson FOM, the critical electrical field  $E_C$  was approximated by the breakdown field  $E_B$ , which is the upper limit.

- a) R&D.
- b) Demonstrators.
- c) Well developed.
- d) Mature.



**Figure 1** Relation of the on-resistance and the breakdown voltage of a power semiconductor device. The underlying material properties have been listed in Table 1. In general, a larger bandgap causes a significant reduction of the on-resistance at a given device operation voltage.

to power electronics. In addition to the BFOM value, a large heat conductivity of the semiconductor material is quite favorable in power electronics. Among the wide bandgap semiconductors listed in Figure 1 and Table 1, SiC outperforms its counterpart by simultaneously exhibiting a large BFOM value (compared to Si), a great heat conductivity (compared to GaN and  $\beta\text{-Ga}_2\text{O}_3$ ), and a quite mature device-processing technology that makes use of major parts of Si processing lines. In addition, high-quality SiC wafer substrates are available with a diameter of 150 mm, and even the 200 mm size has been demonstrated. Further, a quite significant cost down for the SiC substrate costs (US\$/mm<sup>2</sup>) in the range of 10%/a-12%/a has been observed in the last two decades since the introduction of the very first SiC diode to the market in year 2001.

Another important issue for the application of a wide bandgap material in an electronic device is the capability to carry out intentional doping by donor and acceptor atoms to tailor electron and hole transport and to establish bipolar device operation. From the application point of view, at least one kind of doping, i.e. by donor or acceptor atoms, is necessary to establish unipolar device operation. In this context, SiC exhibits reasonable n-type and p-type doping options using the donor nitrogen and the acceptors boron and aluminum, respectively.

Wide bandgap semiconductors also exhibit superior physical properties for the application in high-frequency switching devices. In this context, the Johnson figure of merit  $v_s E_C / 2\pi$  ( $v_s$  = charge carrier saturation velocity,  $E_C$  = critical electrical field in the device structure) may be applied for materials selection (Table 1). From the application point of view, GaN epitaxial layers grown on semi-insulating SiC substrates are widely used for the fabrication of high-frequency and medium-power switches, as they are needed in mobile communication networks. This kind of application of SiC profits from the progress in bulk growth of conductive n-type conducting 4H-SiC substrates.

To link the high potential of the wide bandgap semiconductor SiC with the technologic implementation capabilities, all chapters on defects, bulk growth, epitaxial growth, and device processing stemming from fundamental physics and/or materials science and engineering are combined with chapters that comprise the status of the industrial-driven technology development. Following this structure in Part I of the book, the reader gains a comprehensive insight into today's SiC technology. The strong focus on the semiconductor SiC is related to the fact that the well-developed technology is ready to replace the standard semiconductor Si in power electronics. To point out that the materials focus on SiC is not dogmatic, also related wide bandgap materials featuring extraordinary power electronic-related properties, i.e. GaN, diamond, and  $\text{Ga}_2\text{O}_3$ , are surveyed in the shorter Part II of the book.

September 2021

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## Part I

### **Silicon Carbide (SiC)**

**1**

## **Dislocation Formation During Physical Vapor Transport Growth of 4H-SiC Crystals**

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### **1.1 Introduction**

Silicon carbide (SiC) is the leading candidate among wide-bandgap semiconductor materials for next-generation power semiconductor devices. Over recent decades, the quality of SiC single crystals has improved considerably, thereby making it feasible to fabricate high-performance SiC power devices. 4H-SiC epitaxial wafers of 100 and 150 mm in diameter, with low dislocation density are already available in the market and have been used to fabricate high-performance SiC power devices [1]. However, the widespread commercialization of such devices remains hindered by technological issues related to SiC crystal growth. It is abundantly clear that further successful development of SiC semiconductor technology relies on understanding the process of SiC crystal growth and thus improving the technology for manufacturing large high-quality SiC crystals.

In this chapter, I describe recent progress in understanding the formation of defects during physical vapor transport (PVT) growth of SiC, focusing particularly on the formation of dislocations in 4H-SiC. Currently, commercially available SiC bulk crystals are almost always grown by PVT, namely, by the modified Lely method [2]. However, dislocation formation during the PVT growth of bulk SiC crystals remains a major obstacle to realizing high-performance SiC power devices. Certain types of dislocation are detrimental to the yield and reliability of SiC power devices. Dislocations in PVT-grown SiC crystals are classified broadly into two types, namely, (i) threading dislocations extending along the *c*-axis and (ii) basal plane dislocations (BPDs) lying in the basal plane. Threading dislocations, particularly threading screw dislocations (TSDs), degrade the blocking capabilities of SiC diodes [3–5], whereas BPDs have a serious impact on the reliability of unipolar devices such as SiC metal oxide semiconductor field-effect transistors (MOSFETs) and junction gate field-effect transistors (JFETs) [6, 7] as well as SiC bipolar devices [8, 9]. Therefore, over the decades, considerable effort has gone into reducing the TSD and BPD densities in SiC crystals.

TSDs and BPDs differ markedly in how they form during the PVT growth of SiC crystals. Most TSDs are inherited from the seed crystal and often form in the initial

stage of crystal growth [10–12]. BPDs can also be inherited from the seed crystal and form during the initial seeding process, but they do not propagate throughout the entire crystal because their propagation or extension directions are restricted to the basal plane, almost normal to the growth direction. Therefore, the high density of BPDs in the top and middle portions of SiC crystals cannot be explained by the aforementioned mechanisms, and the causes of the BPDs observed in these portions remain poorly understood.

A plausible explanation is that BPDs are nucleated at the growth front (growing crystal surface) and then incorporated into the growing crystal. In general, defect formation at the growth front is closely related to the shape and morphology of the growing crystal surface; the crystal shape determines the magnitude and distribution of the thermoelastic stresses imposed on the grown crystals [13–16], and the surface morphology at the growth front largely affects the defect formation kinetics. Therefore, control of these growth parameters is crucial to obtain high-quality SiC single crystals.

In Section 1.2, I discuss the BPD formation during the PVT growth of 4H-SiC crystals. SiC single crystals of the 4H polytype are the ones studied and implemented most intensively by the industry. The present author's group investigated the BPD formation by characterizing the BPD distributions at the growth front as well as inside 4H-SiC single-crystal boules grown by PVT. The investigation was focused to identify where and how BPDs are nucleated and multiplied in PVT-grown 4H-SiC crystals. As described earlier, the growth front of 4H-SiC crystals is the most plausible location where BPDs are nucleated. The growth front comprises the  $(000\bar{1})$  facet and its outer (non-facet [NF]) regions; they exhibit characteristic surface morphologies in terms of the step-terrace structure. The morphologies of these two regions are quite different [17, 18], and thus different defect formation kinetics would govern the defect formation on the two surface regions. Furthermore, these two regions grow into different crystal shapes; the facet is fairly flat and has a temperature distribution across the surface during PVT growth [18], whereas the non-facet regions are convex-shaped toward the growth direction and are assumed to be roughly isothermal during growth [19]. The degree of the convexity of the growth front is also a crucial parameter for defect formation during the PVT growth of SiC. As such, investigating the crystalline properties of the facet and non-facet regions at the growth front provides valuable information about the formation of defects during the PVT growth of SiC crystals.

As described earlier in this section, another relevant issue for dislocation formation during the PVT growth of 4H-SiC crystals is the seeding process. In general, the seeding process, namely, how crystal growth is initiated on the seed crystal, is a key issue for reproducible growth of high-quality single crystals. This is also true for the PVT growth of 4H-SiC single crystals, and thus, establishing a well-controlled seeding process for the PVT growth of SiC is necessary for obtaining high-quality 4H-SiC bulk single crystals. Several authors have tried to reveal the growth mode and the defect formation process during the initial stage of PVT growth [10–12, 20–25]. However, detailed knowledge about the seeding process of SiC PVT growth remains lacking, and further intensive study is required to explore

this important technological issue in SiC PVT growth. An obstacle to investigating the seeding process of SiC PVT growth is that defect formation occurs within a very narrow range near the interface between the seed and grown crystal, and this greatly hinders detailed observations and analyses of the defect formation at the interface.

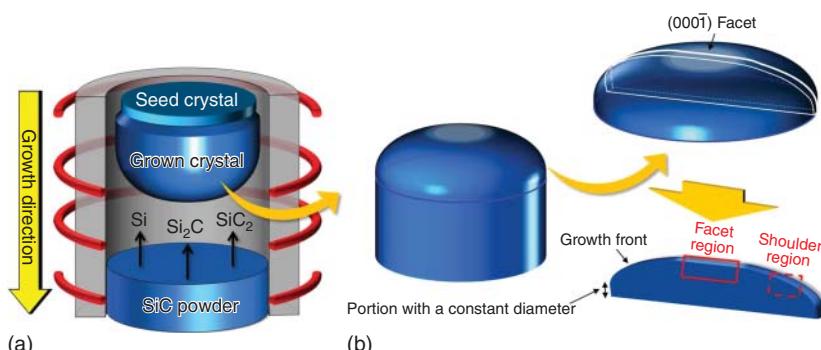
Another reason why it is difficult to study the defect formation at and near the grown-crystal/seed interface is the complexity of causes of defect formation during the initial stage of SiC PVT growth, such as thermoelastic stress [10, 12], growth kinetics [10, 11, 21], surface conditions of the seed crystal [20], and nitrogen doping enrichment near the grown-crystal/seed interface [12, 22–25]. Section 1.3 is dedicated to this issue, and recent studies of the dislocation formation at the grown-crystal/seed interface during PVT growth of 4H-SiC crystals are described. Slightly off-oriented ( $000\bar{1}$ ) wafers containing the beveled interface between the grown crystal and seed crystal were prepared, which revealed a characteristic dislocation structure formed at the interface and indicated the important role of vacancy injection during the initial stage of the PVT growth of 4H-SiC crystals.

In Section 1.4, I summarize this chapter and draw some conclusions.

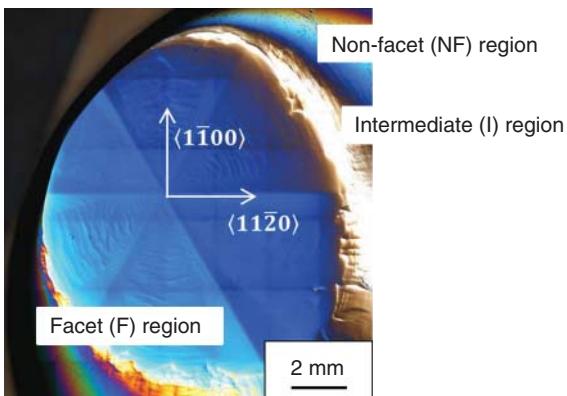
## 1.2 Formation of Basal Plane Dislocations During PVT Growth of 4H-SiC Crystals

### 1.2.1 Plan-View X-ray Topography Observations of Growth Front

Figure 1.1 shows schematically (a) the PVT growth reactor of 4H-SiC crystals and (b) the scheme for preparing the top portion of the grown crystal with the ( $000\bar{1}$ ) facet and a 4H-SiC ( $1\bar{1}00$ ) or ( $11\bar{2}0$ ) wafer sliced vertically along the growth direction from a 4H-SiC single crystal. The crystal was grown on an on-axis or off-oriented 4H-SiC ( $000\bar{1}$ )C seed crystal. The vertically sliced ( $1\bar{1}00$ ) or ( $11\bar{2}0$ ) wafer consisted of two



**Figure 1.1** Schematics of (a) physical vapor transport (PVT) growth reactor and (b) preparation scheme of top portion of grown crystal with ( $000\bar{1}$ ) facet and a 4H-SiC ( $1\bar{1}00$ ) or ( $11\bar{2}0$ ) wafer sliced vertically in the growth direction from a 4H-SiC single-crystal boule grown on a 4H-SiC ( $000\bar{1}$ )C seed crystal. The areas in the wafer examined by transmission X-ray topography are indicated by red open rectangles. Source: Nakano et al. [26]. © 2019, Elsevier.

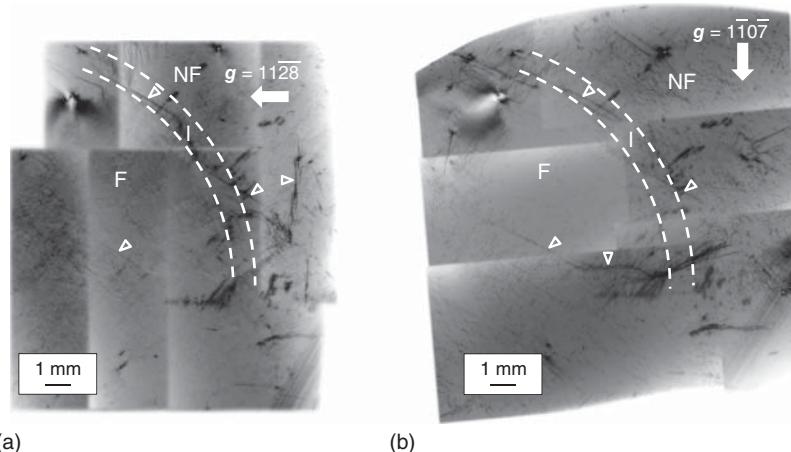


**Figure 1.2** Differential interference contrast (DIC) optical microscopy image of growth front of nitrogen-doped ( $\text{mid-}10^{18} \text{ cm}^{-3}$ ) 4H-SiC single-crystal boule examined in this study. The growth front consists of three distinct morphological regions, namely, the  $(000\bar{1})\text{C}$  facet (F) and non-facet (NF) regions and the intermediate (I) region between them (after [27]). Source: Sonoda et al.

portions that are classified from the perspective of crystal growth. One was accompanied by the growth front that showed a domed shape (convex toward the growth direction). In this portion, crystal growth occurred during PVT growth. The other portion contained the side surfaces of the crystal, on which there was nominally no crystal growth, and thus it had a constant diameter.

Figure 1.2 shows a differential interference contrast (DIC) optical microscopy image of the growth front of a nitrogen-doped ( $\text{mid-}10^{18} \text{ cm}^{-3}$ ) 4H-SiC boule examined by Sonoda et al. [27]. The figure reveals that the growth front of the nitrogen-doped 4H-SiC single-crystal boule comprised three distinct morphological regions, namely, (i) the  $(000\bar{1})\text{C}$  facet region (denoted as F in the figure), (ii) the non-facet (NF) region, and (iii) the intermediate (I) region between F and NF. The facet region exhibited hexagonal symmetry comprising six vicinal  $(000\bar{1})\text{C}$  surfaces tilted toward the  $<1\bar{1}00>$  direction. The vicinal surfaces were separated by six crystallographically equivalent ridges extending along the  $<11\bar{2}0>$  direction. The non-facet region exhibited macroscopically smooth morphology, and the convexity of the region varied depending on the growth conditions, particularly, the temperature distribution in the growth cell. The intermediate region was arranged on the perimeter of the facet region, was narrow, and exhibited a macroscopically slightly rough morphology.

Figure 1.3 shows reflection X-ray topographs of the growth front of a nitrogen-doped 4H-SiC boule in the diffraction conditions (a)  $\mathbf{g} = 11\bar{2}\bar{8}$  and (b)  $1\bar{1}0\bar{7}$ , obtained by Sonoda et al. [27]. In the topographs, the boundaries of the facet, intermediate, and non-facet regions are marked by dashed lines. Both topographs contain relatively intense linear contrasts extending roughly along the  $<1100>$  direction; some of them are marked with open triangles in the topographs. They correspond to low-angle grain boundaries consisting of threading edge dislocations (TEDs) penetrating the crystal along the  $c$ -axis. Small dot-like contrasts were also observed in both topographs. They had two possible origins, namely, TSDs and TEDs, but were ascribed to TSDs based on their estimated density ( $\sim 10^3 \text{ cm}^{-2}$ ). As shown in Figure 1.3, no marked difference in the defect structure was found among the three regions of the as-grown surface, namely, the facet, intermediate,



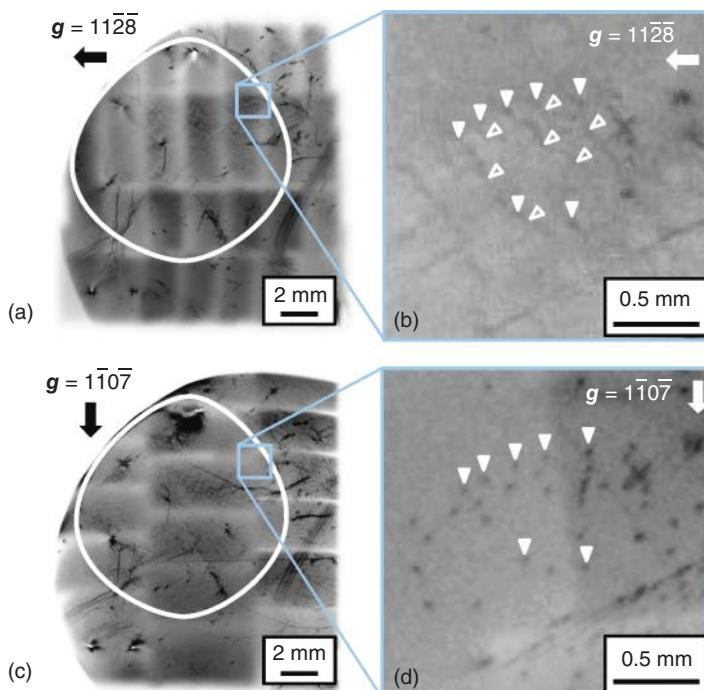
**Figure 1.3** Reflection X-ray topographs from the three regions at the growth front of a PVT-grown 4H-SiC crystal. The diffraction vector was (a)  $11\bar{2}8$  and (b)  $1\bar{1}0\bar{7}$ . In the topographs, the facet, non-facet, and intermediate regions are denoted as F, NF, and I, respectively, and their boundaries are marked by dashed lines. Source: Sonoda et al. [27].

and non-facet regions, implying that the faceted growth front hardly affects the formation of extended defects during PVT growth of 4H-SiC boules.

The topographs with diffraction vectors  $\mathbf{g} = 11\bar{2}8$  and  $1\bar{1}0\bar{7}$  shown in Figure 1.3a,b exhibit slightly different image textures. This is thought to be due to BPDs existing in the crystal portion just beneath the as-grown surface of the boule. BPDs, which have Burger vectors within the basal plane, are out of contrast when the diffraction vector is perpendicular to their Burgers vector, and thus, the two topographs taken with different diffraction vectors exhibit slightly different contrast patterns (image textures).

Figure 1.4 shows enlarged X-ray topographs for more detailed investigation of the dislocation structure underneath the facet and near-facet regions [27]. In the figure, wider-area topographs (Figure 1.4a,c) are also presented, in which the  $(000\bar{1})$  facet region is marked by a white circle, and the positions at which the enlarged X-ray topographs (Figure 1.4b,d) were taken are indicated by open squares. The topographs shown in Figure 1.4a,b were taken with the diffraction vector  $\mathbf{g} = 11\bar{2}8$ , whereas those in Figure 1.4c,d were taken in the diffraction vector  $\mathbf{g} = 1\bar{1}0\bar{7}$ . Figure 1.4b,d was acquired from the same area in the as-grown crystal surface of a 4H-SiC single-crystal boule (indicated by open squares in Figure 1.4a,c). In Figure 1.4b, both TSDs and BPDs were observed; they are indicated by closed and open triangles, respectively. By contrast, only TSDs were detected in Figure 1.4d in which BPDs exhibited no distinct contrast because the diffraction vector was set perpendicular to their Burgers vectors. These observations indicate that at this particular region of the grown crystal, most BPDs had the same Burgers vector, which implies that they arose from the same cause during the PVT growth process.

In Figure 1.4b, note that many of the observed BPDs seem to emanate from TSDs. Sonoda et al. examined other areas on the as-grown surface and found similar cases of BPDs emanating from TSDs [27]. These results suggest that the existence of



**Figure 1.4** Reflection X-ray topographs of the growth front in the diffraction conditions (a)  $g = 11\bar{2}\bar{8}$  and (c)  $\bar{1}10\bar{7}$ . (b, d) Enlarged X-ray topographs of the areas indicated by open squares in (a, c), respectively. In (b, d), some of the dot-like and line contrasts due to threading screw dislocations (TSDs) and basal plane dislocations (BPDs) are marked by closed and open triangles, respectively. Source: Sonoda et al. [27].

TSDs is related to the BPD formation at the growth front, and TSDs intersecting the growing crystal surface would induce the nucleation of BPDs at the surface during PVT growth of 4H-SiC boules. The mechanism is yet to be clarified, but the elastic interaction between TSDs and the growing crystal surface would play a crucial role in this phenomenon. In this respect, Wang et al. reported an important result that is helpful when considering the origin of this phenomenon [28]. They found that BPDs existing in commercially available 6H-SiC substrates connect or emanate from micropipes (super screw dislocations), comprising dislocation networks in the substrates. Similar BPD structures have also been reported in 4H-SiC epitaxial layers [29]. Micropipes and TSDs extending along the *c*-axis in an infinite crystal do not have a shear stress component parallel to the basal plane, and hence, they could not be the cause of BPDs in an infinite crystal. However, in a finite crystal, they interact elastically with the free surface, and the resultant surface relaxation due to the image force effect of dislocations [30] can provide a shear stress parallel to the basal plane. Compared to micropipes, TSDs provide lower shear stress because of their relatively smaller Burgers vector. However, the Burgers vector of TSDs would be still large enough for them to provide a shear stress exceeding the critical resolved shear stress for BPD formation at the PVT growth temperature (2300–2400 °C) and

nucleate BPD loops and/or half loops at the growing crystal surface during PVT growth of 4H-SiC crystals.

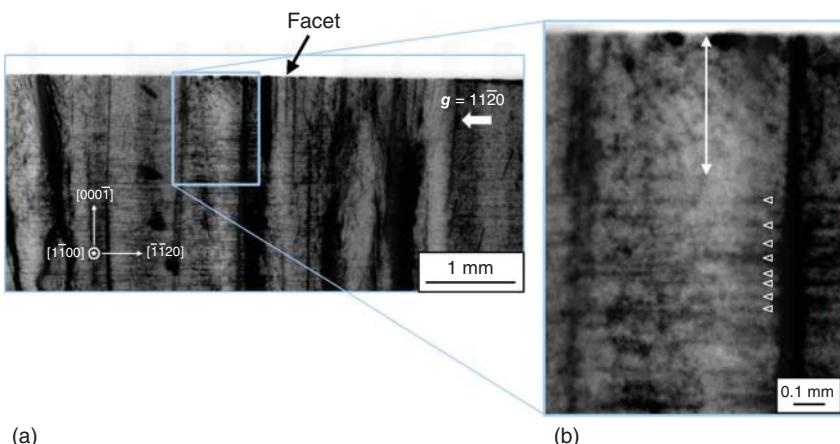
Another important finding made in the X-ray topographs shown in Figures 1.3 and 1.4 is that the density of BPDs in the facet and near-facet regions of the as-grown crystal is significantly lower than the typical BPD densities in commercially available 4H-SiC substrates. The densities of BPDs in 4H-SiC substrates are typically  $10^4\text{--}10^5\text{ cm}^{-2}$  [31, 32] and of the order of  $10^3\text{ cm}^{-2}$  for state-of-the-art 4H-SiC substrates [33]. By contrast, the estimated BPD density in the facet and near-facet regions of the crystal was less than  $10^3\text{ cm}^{-2}$ . Sonoda et al. also examined two other 4H-SiC boules and found similar BPD densities in the crystal portion just beneath the facet and near-facet regions of the boules, although 4H-SiC substrates sliced out from the portions of the boules far from the growth front had typical BPD densities ( $10^4\text{--}10^5\text{ cm}^{-2}$ ) [27]. These results indicate that although BPDs could nucleate at the growing crystal surface, they hardly multiply in the facet and near-facet regions of PVT-grown 4H-SiC boules.

### 1.2.2 Cross-Sectional X-ray Topography Observations of Growth Front

To examine in more detail the BPD formation at the growth front, cross-sectional X-ray topography observations of PVT-grown 4H-SiC boules were performed [27]. The two portions in a vertically sliced wafer examined by transmission X-ray topography are illustrated schematically by open rectangles in Figure 1.1b. The solid-line rectangle corresponds to a portion right beneath the facet, whereas the dashed-line rectangle corresponds to a crystal portion near the shoulder region of the grown front.

Figure 1.5a shows a cross-sectional transmission X-ray topograph for the diffraction condition  $\mathbf{g} = 11\bar{2}0$  of the portion right beneath the  $(000\bar{1})$  facet, obtained by Sonoda et al. [27]. The topograph shows several dark vertical band and line contrasts, which correspond to low-angle boundaries and threading dislocations, respectively, penetrating the boule along the growth direction (*c*-axis). In addition to these vertical band and line contrasts, a number of horizontal line contrasts are also observed in the topograph. Figure 1.5b shows an enlarged topograph of the portion indicated by an open rectangle in Figure 1.5a. In Figure 1.5b, some of the horizontal line contrasts are marked by open triangles. The  $\mathbf{g} \cdot \mathbf{b}$  contrast analysis revealed that these contrasts were caused by BPDs in the boule. Note here that a portion very close to the as-grown surface (facet), marked by a double-headed arrow in Figure 1.5b, is almost free of BPDs. This implies that BPDs hardly multiply in the facet and near-facet regions of the grown boule during PVT growth of 4H-SiC, which agrees well with the results of the plan-view X-ray topography observations shown in Figures 1.3 and 1.4.

Figure 1.5a also reveals that a number of BPDs exist in crystal portions distant from the growth front. This is consistent with the fact that 4H-SiC substrates prepared from these portions contain a high density of BPDs ( $10^4\text{--}10^5\text{ cm}^{-2}$ ). An important question here is where they came from. To clarify this point, a series of X-ray topographs (not shown) was taken from the center to the edge of the boule, and it was found that many BPDs extended continuously toward the edge of the

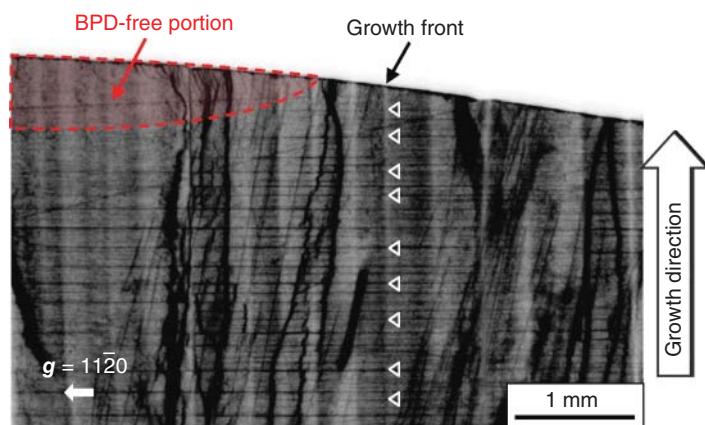
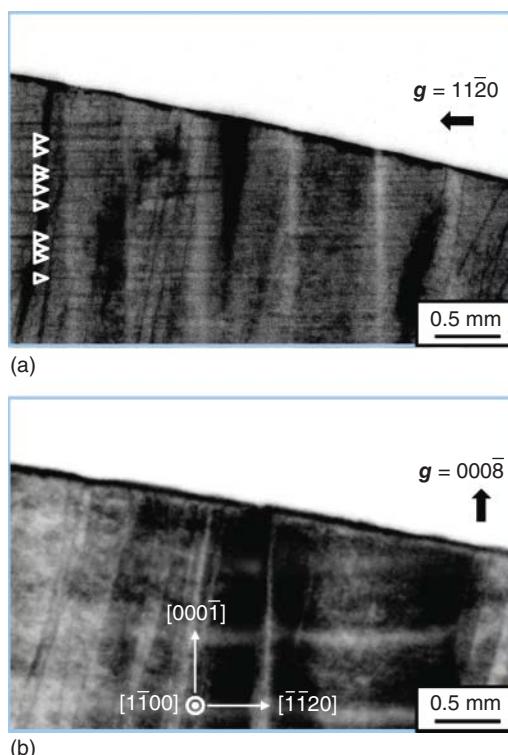


**Figure 1.5** Cross-sectional X-ray topographs for diffraction condition  $\mathbf{g} = 1\bar{1}20$  of a crystal portion right beneath the (0001) facet of a PVT-grown 4H-SiC boule. (b) An enlarged topography image of the portion indicated by an open rectangle in (a). In (b), some of the horizontal line contrasts caused by BPDs are marked by open triangles. Source: Sonoda et al. [27].

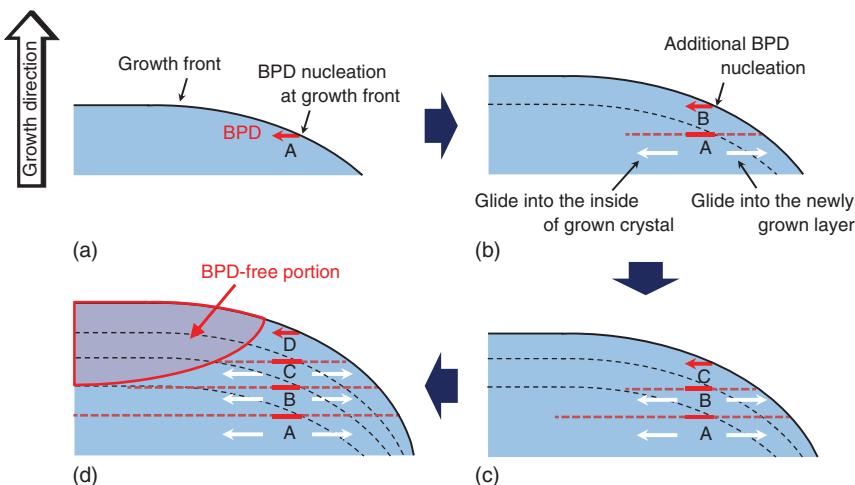
boule and terminated at the shoulder region of the growth front. Figure 1.6 shows X-ray topographs of a crystal portion underneath the shoulder region of a 4H-SiC single-crystal boule [27]. The location of the crystal portion in the boule is indicated by a dashed-line rectangle in Figure 1.1b. Figure 1.6a,b shows X-ray topographs of the portion for the diffraction conditions  $\mathbf{g} = 1\bar{1}20$  and  $0008\bar{1}$ , respectively. As shown in Figure 1.6a ( $1\bar{1}20$  topograph), a number of horizontal line contrasts extend along the basal plane; some of them are marked by open triangles in the figure. As shown in the figure, the horizontal line contrasts terminate at the as-grown surface of the boule. By contrast, they are lost in Figure 1.6b ( $0008\bar{1}$  topograph), and thus, they were ascribed to BPDs. To elaborate the BPD formation process, Sonoda et al. examined the other ends of these horizontal line contrasts and found that many of them terminated within the crystal at positions roughly below the facet. They observed a similar distribution of BPDs in the other half of the wafer and thus inferred that BPDs were nucleated at the shoulder region of the growth front and extended toward the inside of the grown boule via dislocation glide and multiplication processes during PVT growth. By contrast, such BPD glide and multiplication processes hardly occur in the facet and near-facet regions, resulting in a very low BPD density in the crystal portion right beneath these regions.

These BPD behaviors are illustrated more clearly in a wider-area transmission X-ray topograph shown in Figure 1.7, where the BPD-free crystal portion right beneath the facet and near-facet regions is bounded by a dashed line. In the figure, some of the BPDs extending along the basal plane in the grown crystal are indicated by open triangles. As shown in the figure, the boundary between the BPD-free portion and the other portions has a characteristic “round neck” shape that indicates that the BPD distribution in PVT-grown 4H-SiC crystals is controlled

**Figure 1.6** Cross-sectional X-ray topographs for diffraction conditions (a)  $g = 11\bar{2}0$  and (b)  $000\bar{8}$  of a crystal portion underneath the shoulder region of the growth front of a PVT-grown 4H-SiC crystal, whose location in the crystal is indicated by a dashed line rectangle in Figure 1.1b. In (a), a number of horizontal line contrasts due to BPDs are observed; some of them are marked by open triangles. Source: Sonoda et al. [27].



**Figure 1.7** Wider-area transmission X-ray topograph for diffraction condition  $g = 11\bar{2}0$ , which shows the existence of an almost BPD-free crystal portion right beneath the facet and near-facet regions at the growth front. Some of the BPDs extending along the basal plane are indicated by open triangles. The “round-neck” boundary between the BPD-free portion and the other portions is indicated by a dashed line.



**Figure 1.8** Schematics of temporal change of BPD distribution in a 4H-SiC crystal during PVT growth. (a) Nucleation of BPDs at the shoulder region of the grown crystal, and (b) glides of BPDs into the crystal and also toward the growth front of the crystal through the newly grown layer, together with the nucleation of additional BPDs at the growth front. (c) Repetition of processes (a, b) at the growth front of the newly grown layer during PVT growth, and (d) resulting round-neck distribution of BPDs due to the different glide distances of BPDs nucleated at different times in the PVT growth process.

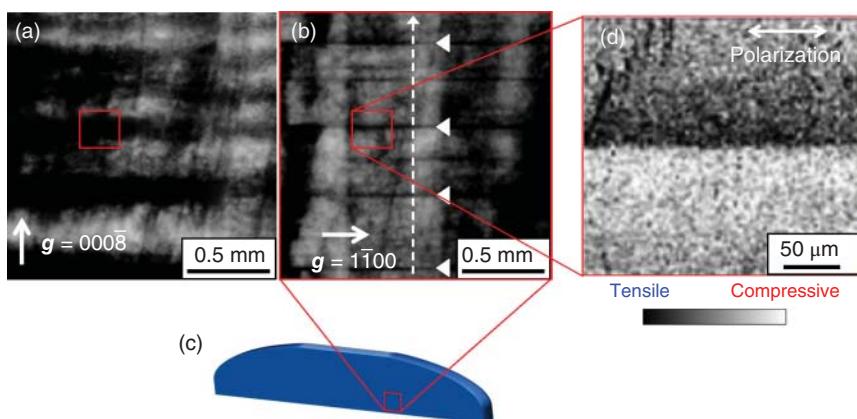
by the BPD nucleation at the shoulder region of the grown crystal. This important conclusion was drawn by considering the glide and multiplication of BPDs after they nucleate at the shoulder region. These processes are illustrated in Figure 1.8, which shows schematically how the BPD distribution in a 4H-SiC crystal changes with time during PVT growth. Figure 1.8a shows the nucleation of BPDs at the shoulder region of a PVT-grown 4H-SiC crystal, and as the PVT growth proceeds, the nucleated BPDs glide into the grown crystal and also extend toward the growth front through the newly grown layer (Figure 1.8b). At this stage, additional BPDs nucleate at the growth front of the newly grown layer, and the aforementioned processes are repeated during PVT growth (Figure 1.8c), resulting in the round-neck distribution of BPDs (Figure 1.8d) because of the different glide distances of BPDs nucleated at different stages of the PVT growth process.

The BPD formation at the shoulder region of the PVT-grown SiC crystals coincides well with numerical results by Gao and Kakimoto [16]. They conducted three-dimensional numerical modeling of BPD multiplication in 4H-SiC bulk crystals. They calculated the resolved thermoelastic shear stresses on the basal plane during PVT growth of 4H-SiC and then substituted them into the Alexander-Hassen model to obtain the BPD distribution in PVT-grown 4H-SiC crystals. Their results showed that the shape of the growth front is key for BPD multiplication, with a largely convex growth front giving rise to a high resolved shear stress on the basal plane at the shoulder region of 4H-SiC boules during PVT growth, thus introducing many BPDs from the region. Their results also suggested that BPD multiplication occurs mainly in the crystal growth stage of the PVT growth process rather than in

the cooling stage. I believe that some irregularities at the growing crystal surface, such as TSD outcrops, become the nucleation sites of BPDs and lead to dislocation multiplication if a sufficiently high thermoelastic shear stress is imposed at these sites during PVT growth. The observed characteristic distribution of BPDs in the growth-front portion of 4H-SiC single-crystal boules corroborates this assumption.

### 1.2.3 Characteristic BPD Distribution in PVT-Grown 4H-SiC Crystals

In Section 1.2.2, it was revealed that many BPDs are introduced from the shoulder region of 4H-SiC crystals grown in the  $[000\bar{1}]$  direction. However, it remains unclear how these BPDs behave in the crystals after their introduction. To clarify their behaviors, X-ray topography and Raman microscopy were conducted on a vertically sliced 4H-SiC (11 $\bar{2}$ 0) wafer, which is shown schematically in Figure 1.1b. Figure 1.9a,b shows transmission X-ray topographs of a 4H-SiC (11 $\bar{2}$ 0) wafer for the diffraction conditions  $\mathbf{g} = 000\bar{8}$  and 1 $\bar{1}00$ , respectively, obtained by Nakano et al. [26]. The area where the topographs were taken is indicated schematically by a red open square in Figure 1.9c. As shown in the topographs, strong horizontal line contrasts are observed in Figure 1.9b (diffraction vector: 1 $\bar{1}00$ ), which almost diminish in Figure 1.9a (diffraction vector: 000 $\bar{8}$ ). By contrast, in Figure 1.9a, line contrasts extending along the  $c$ -axis (growth direction) are observed, which correspond to TSDs. In Figure 1.9a, broad band contrasts are also observed at the positions where the strong horizontal line contrasts are observed in Figure 1.9b. The strong horizontal line contrasts observed in Figure 1.9b were caused by either BPDs or basal plane stacking faults in the crystal. To clarify the origin of the strong horizontal line contrasts observed in Figure 1.9b, Nakano et al. performed defect-selective etching

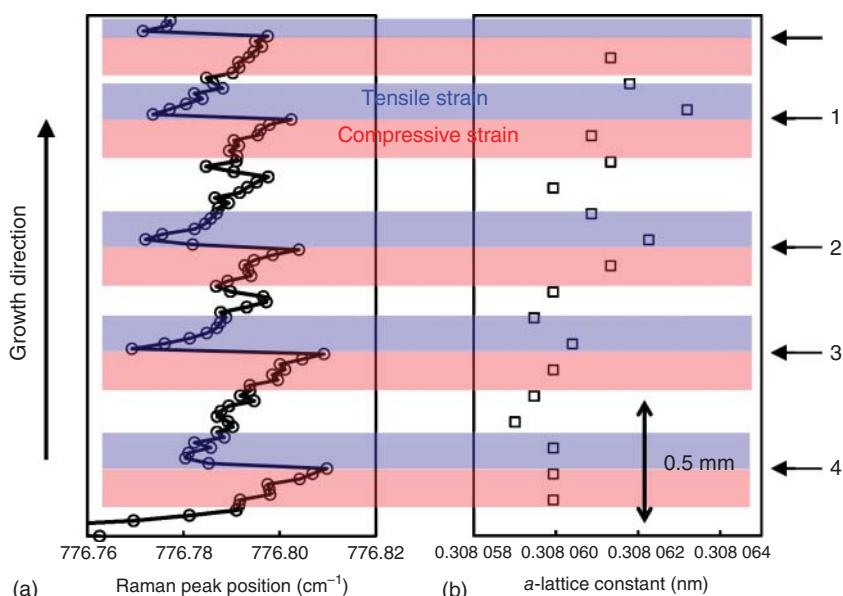


**Figure 1.9** Transmission X-ray topographs for diffraction conditions (a)  $\mathbf{g} = 000\bar{8}$  and (b)  $1\bar{1}00$  of a vertically sliced 4H-SiC (11 $\bar{2}$ 0) wafer. In (c), the area in the wafer examined by transmission X-ray topography is shown as an open rectangle. (d) Raman microscopy image of a layer with a high density of BPDs (bunched BPDs). The white dashed arrow in (b) indicates the points and direction where the variations of the  $E_2$  mode peak position and the  $a$ -lattice constant (Figure 1.10) were measured. Source: Nakano et al. [26]. © 2019, Elsevier.

(molten KOH etching) and found that they were caused by a high density of BPDs; Nakano et al. referred to this type of BPDs as “bunched BPDs” [26]. Note here that such bunched BPDs are arranged almost periodically along the growth direction in the grown crystal, as revealed in Figure 1.9b, where some of the bunched BPDs are indicated by closed white triangles.

To examine the structure of bunched BPDs in more detail, Raman microscopy imaging of bunched BPDs was conducted. The imaged area is indicated by a red open square in Figure 1.9a,b, and the peak position of the  $E_2$  mode at  $\sim 776 \text{ cm}^{-1}$  was plotted across this area with the polarization vectors of the incident and scattered light parallel to the basal plane. The obtained image is shown in Figure 1.9d, in which the light polarization is indicated by a double-headed arrow. As shown in the figure, there is a clear difference in the peak position between the upper and lower sides of bunched BPDs. In the upper side, the peak of the  $E_2$  mode shifts to a lower position, while the peak is positioned at higher wavenumbers in the lower side, implying the existence of tensile (compressive) strain in the upper (lower) side of bunched BPDs.

Figure 1.10 shows how (i) the  $E_2$  peak position and (ii) the  $a$ -lattice constant (lattice constant within the basal plane) vary in the growth direction as measured by high-resolution X-ray diffraction (HRXRD). These variations were measured along the line indicated by a white dashed arrow in Figure 1.9b. As shown in Figure 1.10a, the peak position shifted abruptly where bunched BPDs existed. The



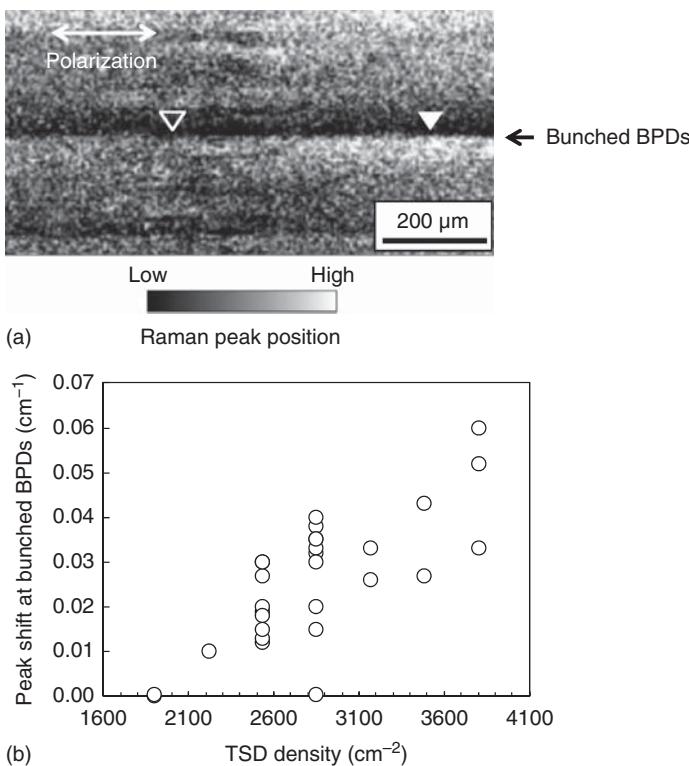
**Figure 1.10** Variations of (a) peak position of Raman-active  $E_2$  mode around  $776 \text{ cm}^{-1}$  and (b) the  $a$ -lattice constant measured using HRXRD in the growth direction on a vertically sliced 4H-SiC (11 $\bar{2}$ 0) wafer. The measured points and direction are indicated by a white dashed arrow in Figure 1.9b. (a) shows clearly that abrupt shifts of the  $E_2$  peak position occurred at bunched BPDs; the positions of some of the bunched BPDs are indicated by arrows in the right-hand side of the figure (after [26]).

positions of some of the bunched BPDs are indicated by arrows in the right-hand side of Figure 1.10; those indicated by the arrows numbered from 1 to 4 correspond to the bunched BPDs indicated by closed white triangles in Figure 1.9b. The shift at bunched BPDs always occurred toward lower wavenumbers when the light beam was scanned from the bottom to the top of the grown crystal, implying that tensile strain within the basal plane always exists in the upper side of bunched BPDs [34–36]. The  $a$ -lattice constant also varied in the growth direction and increased in the upper side of bunched BPDs. This is consistent with the variation of the  $E_2$  mode peak position, and it can be concluded that the tensile strain within the basal plane existing in the upper side of bunched BPDs resulted in a larger  $a$ -lattice constant.

The aforementioned results indicate that bunched BPDs are accompanied by extra half-planes pointing toward the seed crystal. This is reasonable if bunched BPDs are introduced by the thermoelastic stress imposed on the growing crystal during the PVT growth of SiC. The SiC PVT growth process is driven primarily by the temperature gradient along the  $c$ -axis (growth direction), and thus, a high  $\sigma_{rz}$  shear stress is imposed on the growing crystal during PVT growth, where  $r$  and  $z$  denote the radial and axial directions, respectively, of the grown crystal ( $z$  is parallel to the  $c$ -axis). At typical PVT growth temperatures ( $>2300^\circ\text{C}$ ), SiC crystals deform plastically and the  $\sigma_{rz}$  shear stress is relieved considerably by the introduction of BPDs into the crystal. During the PVT growth process, a positive temperature gradient is maintained in the growth direction, and thus when the thermoelastic stress is relieved, BPDs are introduced that have extra half-planes pointing toward the seed crystal.

#### 1.2.4 BPD Multiplication During PVT Growth

To investigate in more detail how BPDs behave during the PVT growth of 4H-SiC crystals, further extended Raman microscopy imaging of bunched BPDs in the lateral direction (parallel to the basal plane) was performed. The result of the Raman microscopy imaging is shown in Figure 1.11a. The image is a two-dimensional mapping of the peak position of the  $E_2$  mode around  $776\text{ cm}^{-1}$  on a vertically sliced 4H-SiC (11̄20) wafer. Similarly to Figure 1.9d, the peak position differs clearly between the upper and lower sides of bunched BPDs. Note in this figure that the contrast difference between the upper and lower sides of bunched BPDs varies along the basal plane. In Figure 1.11a, portions with larger and smaller contrast differences are indicated by closed and open triangles, respectively. Nakano et al. found that the observed variation of the contrast difference (magnitude of the abrupt shift of the  $E_2$  mode peak position at bunched BPDs) along the basal plane was correlated with the TSD density in the crystal [26]. Figure 1.11b shows the relationship between the contrast difference and the TSD density; the latter was estimated from the density of the line contrasts extending along the  $c$ -axis in X-ray topographs with the diffraction vector  $\mathbf{g} = 000\bar{8}$  (e.g. Figure 1.9a) at the position where the contrast difference was measured by Raman microscopy. As shown in the figure, the magnitude of the abrupt peak shift at bunched BPDs is correlated well with TSD density: as the TSD density increases, the abrupt peak shift at bunched



**Figure 1.11** (a) Extended Raman microscopy image of bunched BPDs along the basal plane. The image shows variation of the  $E_2$  mode peak position around bunched BPDs. The open and closed triangles in the image indicate portions that exhibited smaller and larger abrupt peak shifts, respectively, at the bunched BPDs. (b) A positive correlation between the magnitude of the abrupt peak shift at the bunched BPDs and the TSD density. Source: Nakano et al. [26]. © 2019, Elsevier.

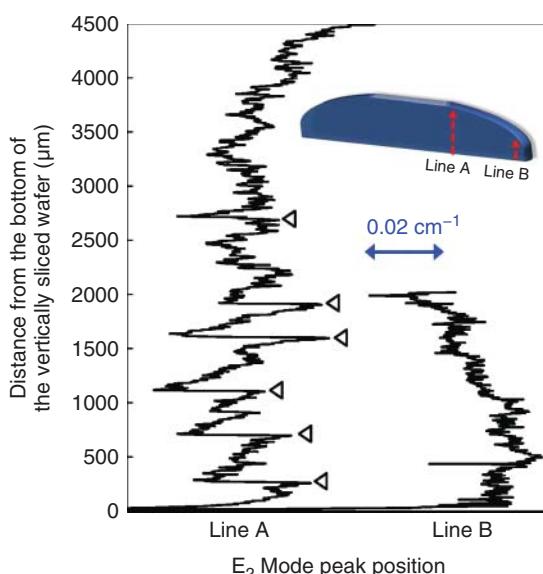
BPDs becomes larger, which implies that the TSD and BPD densities in PVT-grown 4H-SiC crystals are correlated positively.

Ohtani et al. [37] reported a similar positive correlation between the TSD and BPD densities in PVT-grown 4H-SiC crystals. They conducted defect-selective etching using molten KOH to estimate the TSD and BPD densities in PVT-grown 4H-SiC crystals and found that the BPD density increased with the TSD density in the crystals. They ascribed this positive correlation to BPD multiplication around TSDs. Temperature gradients in 4H-SiC crystals during PVT growth cause BPDs to glide on the basal plane and cut through a forest of TSDs extending along the  $c$ -axis in the crystals. After crossing TSDs, BPDs have super jogs parallel to the  $c$ -axis, which are immobile and anchored in the crystal. When the BPDs glide further under thermoelastic stress during PVT growth and/or post-growth cooling, the well-known Frank–Read-type BPD multiplication occurs, and consequently the BPD density increases significantly around TSDs [32, 38]. This is why the BPD and TSD densities are correlated positively in 4H-SiC crystals.

As described in Section 1.2.3, BPDs have a characteristic distribution in the growth direction in PVT-grown 4H-SiC crystals; layers exist with a high density of BPDs (bunched BPDs) arranged almost periodically in the growth direction. As for the BPD formation in PVT-grown 4H-SiC crystals, it was also revealed in Section 1.2.2 that a number of BPDs are introduced from the shoulder region of the grown crystal during PVT growth. In this respect, it is noteworthy that bunched BPDs were observed relatively far from the shoulder region of the grown crystal. Given these results, an important question arises as to where and when bunched BPDs are introduced in crystals. A possible mechanism is that bunched BPDs are introduced from the side surfaces of grown crystals. The constant-diameter portion of a grown crystal has side surfaces that are located very close to the crucible inner walls, and under certain growth conditions, they can come into contact with the walls during PVT growth or cooling because of the different coefficients of thermal expansion of SiC and graphite. Therefore, the side surfaces of the grown crystal could be subject to high stress during PVT growth, thereby introducing a number of BPDs from the side surfaces. However, X-ray topography observations of a crystal portion near the side surfaces of 4H-SiC grown crystals revealed no bunched BPDs near the side surfaces [26].

To examine further the origin of bunched BPDs, further extended Raman microscopy analysis was performed in the growth direction. Figure 1.12 shows how the  $E_2$  peak position varies in the growth direction [26]. The variations were measured along two lines, one that started from the bottom of a vertically sliced wafer and ended near the  $(000\bar{1})$  facet region at the growth front (denoted by line A) and one that was close to the side surface (edge) of a grown crystal (denoted by line B). The locations of these two lines (lines A and B) in a vertically sliced  $(11\bar{2}0)$  wafer are indicated schematically by dashed arrows in the inset of Figure 1.12. As shown in Figure 1.12, the  $E_2$  peak position often shifted abruptly along line A;

**Figure 1.12** Variations of  $E_2$  mode peak position in growth direction measured in the near-facet (line A) and edge (line B) portions of a vertically sliced 4H-SiC  $(11\bar{2}0)$  wafer. The locations of the two measured portions (lines A and B) in the wafer are indicated by dashed arrows in the inset figure.  
Source: Nakano et al. [26].  
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some of the shifts are indicated by open triangles in the figure. By contrast, no such abrupt shifts were seen along line B. Note here that the abrupt shift intensified as the measured point approached the bottom of the vertically sliced wafer, implying that the BPD density in bunched BPDs increases gradually toward the seed crystal. Such an increase in BPD density toward the seed crystal is reasonable if bunched BPDs are introduced from the growth front (top surface of the growing crystal) during PVT growth. Once bunched BPDs are introduced from the growth front, their BPD density increases gradually as the growth proceeds, this being because the total duration of thermoelastic stress imposed on the growing crystal increases with the growth time.

The abovementioned discussions combine to give the important conclusion that bunched BPDs or their nuclei would be introduced at the growth front (domed surface) but hardly so from the side surfaces of grown crystals. The most plausible location where bunched BPDs are introduced would be the shoulder region of the growing crystal. Gao and Kakimoto [16] showed theoretically that the domed shape of the growth front gives rise to a high resolved shear stress on the basal plane in the shoulder region of the grown crystal during PVT growth of 4H-SiC, thus causing many BPDs to be introduced from that region. This theoretical prediction was subsequently confirmed experimentally by Sonoda et al. using X-ray topography [27]. The aforementioned results of Nakano et al. [26] indicate that the shoulder region of the growing crystal is a major source of BPDs, including bunched BPDs or their nuclei, and the BPDs introduced from that region would determine the distribution of BPDs throughout PVT-grown 4H-SiC crystals.

## 1.3 Dislocation Formation During Initial Stage of PVT Growth of 4H-SiC Crystals

### 1.3.1 Preparation of 4H-SiC Wafers with Beveled Interface Between Grown Crystal and Seed Crystal

In this section, I describe the formation of dislocations at the grown-crystal/seed interface of PVT-grown 4H-SiC crystals. As described in Section 1.1, most threading dislocations in PVT-grown 4H-SiC crystals form during the initial stage of PVT growth, and thus, it is essential to control the growth initiation to obtain high-quality 4H-SiC crystals. To reveal the processes for dislocation formation in the initial stage of 4H-SiC PVT growth, Shioura et al. [39] prepared 4H-SiC wafers containing a beveled interface between the grown crystal and the seed crystal and used them to examine the detailed distribution of crystallographic defects at and near the interface. Figure 1.13 shows schematics of the slicing geometry of a 4H-SiC crystal grown on a  $4^\circ$  off-oriented  $(000\bar{1})$  seed crystal, providing a  $1.5^\circ$  off-oriented  $(000\bar{1})$  wafer, which has a beveled interface between the grown crystal and seed crystal [39]. Figure 1.13a is a schematic side view of a nitrogen-doped 4H-SiC crystal grown on a  $4^\circ$  off-oriented  $(000\bar{1})$  seed crystal and a slightly off-oriented ( $1.5^\circ$  off-oriented approximately toward  $[11\bar{2}0]$ )  $(000\bar{1})$  wafer sliced out from the grown crystal, while

**Figure 1.13** Schematics of slicing geometry of a nitrogen-doped 4H-SiC crystal grown on a 4° off-oriented  $(000\bar{1})$  seed crystal, providing a 1.5° off-oriented  $(000\bar{1})$  wafer, which has a beveled interface between the grown crystal and the seed crystal. (a) Side view of grown crystal and 1.5° off-oriented  $(000\bar{1})$  wafer sliced out from the crystal. (b) Top view of sliced wafer. Source: Shioura et al. [39]. © 2019, Elsevier.

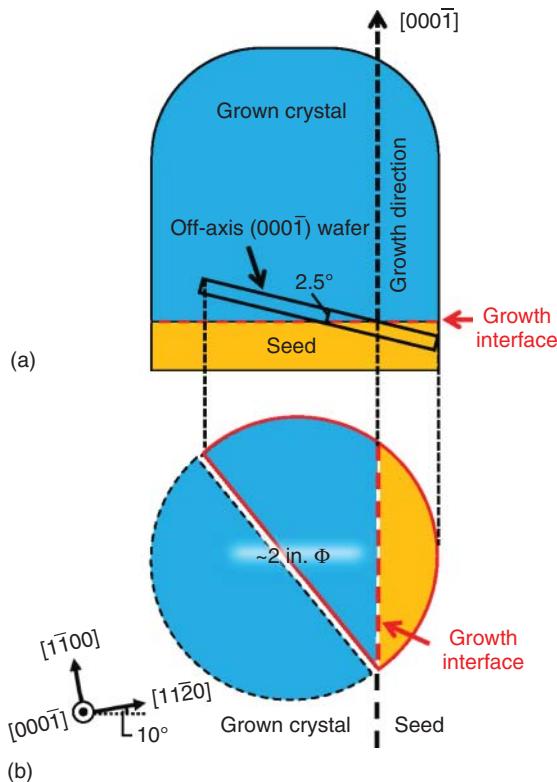
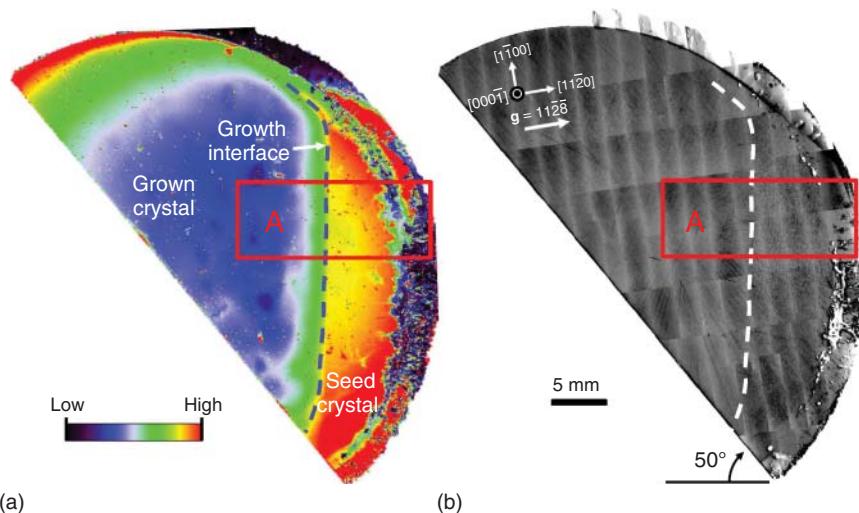


Figure 1.13b shows a top view of the sliced wafer. The angle between the wafer surface and the grown-crystal/seed interface was relatively shallow (2.5°), and thus, the defective near-interface region was substantially enlarged to facilitate detailed observations and analyses of defects at and near the interface. Shioura et al. examined this substantially enlarged interfacial region between the grown crystal and seed crystal using Raman microscopy and X-ray topography, and on the basis of the obtained results elucidated the formation mechanisms of crystallographic defects during the initial stage of PVT growth of 4H-SiC crystals [39].

### 1.3.2 Determination of Grown-Crystal/Seed Interface by Raman Microscopy

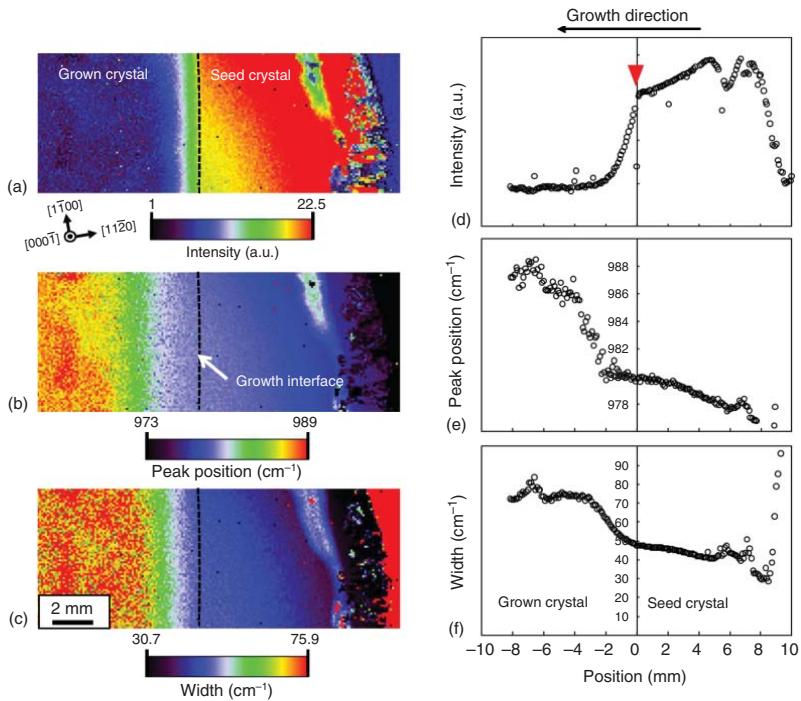
Figure 1.14 shows (a) an intensity mapping image of the whole 1.5° off-oriented 4H-SiC  $(000\bar{1})$  wafer containing the grown-crystal/seed interface, acquired using the intensity of the longitudinal optical phonon–plasmon-coupled (LOPC) mode around  $983\text{ cm}^{-1}$ , and (b) a reflection X-ray topograph of the wafer for the diffraction condition  $\mathbf{g} = 11\bar{2}\bar{8}$  [39]. The intensity of the LOPC mode is known to be very sensitive to the carrier (electron) concentration in 4H-SiC crystals: as the electron concentration increases, the intensity decreases rapidly [40, 41]. As shown in Figure 1.14a, the LOPC mode scattering intensity differs markedly between the seed



**Figure 1.14** (a) Raman mapping image using longitudinal optical phonon-plasmon-coupled (LOPC) mode intensity of a 1.5° off-oriented 4H-SiC (0001) wafer with a beveled interface between the grown crystal and the seed crystal, which corresponds to the upper right part of the wafer illustrated schematically in Figure 1.13b. (b) Reflection X-ray topograph of the 1.5° off-oriented 4H-SiC (0001) wafer in the diffraction condition  $\mathbf{g} = 11\bar{2}\bar{8}$ . The position of the interface between the grown crystal and seed crystal is indicated by a dashed line, and the region used for subsequent Raman microscopy and X-ray topography analyses is indicated by a red open rectangle (region A) in both (a, b). Source: Shioura et al. [39]. © 2019, Elsevier.

and grown crystal regions, and thus, their interface can be determined by Raman microscopy. Figure 1.15 shows enlarged Raman microscopy images across region A in the wafer, whose location is indicated by a red open rectangle in Figure 1.14a,b. In Figure 1.15, mapping images of (a) Raman scattering intensity, (b) peak position, and (c) width of the LOPC asymmetric peak are shown, together with their line profiles across the grown-crystal/seed interface, namely, (d) intensity, (e) peak position, and (f) peak width. As shown in Figure 1.15d, the Raman scattering intensity decreases rapidly from the point indicated by a red triangle in the figure toward the left-hand side of the figure (in the growth direction). Ohshige et al. reported that the electron concentration in PVT-grown 4H-SiC crystals increases abruptly at the grown-crystal/seed interface because of the enrichment of nitrogen donors in the crystal in its initial growth stage [23]. The rapid decrease in the scattering intensity shown in Figure 1.15d is thought to be due to the nitrogen enrichment at the grown-crystal/seed interface, and thus, using the LOPC intensity profile, the location of the interface between the grown crystal and the seed crystal can be determined reasonably as the point indicated by a red triangle in Figure 1.15d.

According to the scheme described earlier, the grown-crystal/seed interface was determined and indicated as a dashed line in Figures 1.14 and 1.15a–c [39]. In all the figures, the left-hand side of the dashed line is the grown crystal, while the right-hand side corresponds to the seed crystal.

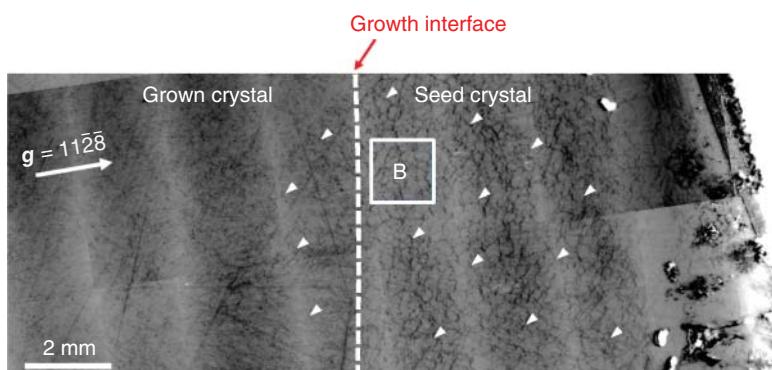


**Figure 1.15** Raman microscopy images of region A, which is indicated by a red open rectangle in Figure 1.14: (a) scattering intensity, (b) peak position, and (c) width of the asymmetric LOPC peak around  $983 \text{ cm}^{-1}$ , where the position of the grown-crystal/seed interface is indicated by a dashed line in each image. The variations of the intensity, peak position, and width of the LOPC peak across the interface are shown in (d–f), respectively, where the data were averaged in the direction parallel to the grown-crystal/seed interface (after [39]). Source: Shioura et al.

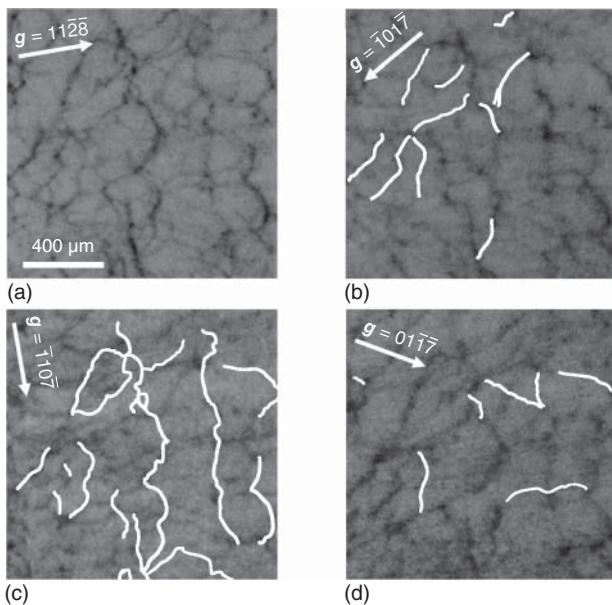
### 1.3.3 X-ray Topography Observations of Dislocation Structure at Grown-Crystal/Seed Interface

To examine more clearly the defect structure near the grown-crystal/seed interface, an enlarged X-ray topograph from the interface region was taken and is shown in Figure 1.16 [39], which is a reflection X-ray topography image for the diffraction condition  $\mathbf{g} = 1\bar{1}\bar{2}\bar{8}$  acquired from region A indicated by a red open rectangle in Figure 1.14. The grown-crystal/seed interface determined by Raman microscopy imaging is indicated by a dashed line in Figure 1.16. The image shows the existence of widespread networks of BPDs near the grown-crystal/seed interface; some of them are marked by white triangles in Figure 1.16. Similar BPD networks have been reported by Tani et al. [24]. They conducted high-voltage transmission electron microscopy (HVTEM) observations and found that BPDs in the networks connected to each other to form cell-like structures and decomposed into stacking faults at the triple nodes of the networks. In Figure 1.16, a cell-like feature of the BPD networks formed at the grown-crystal/seed interface is also observed, and more interestingly, it was found that the networks extended considerably into the seed crystal.

Shioura et al. conducted  $\mathbf{g} \cdot \mathbf{b}$  contrast analyses of the BPD networks observed at the grown-crystal/seed interface to determine the nature of the networks [39]. The results are shown in Figure 1.17, where reflection X-ray topographs of region B, which is indicated by an open square in Figure 1.16, are shown; they were taken for the diffraction conditions (a)  $\mathbf{g} = 1\bar{1}\bar{2}\bar{8}$ , (b)  $\bar{1}01\bar{7}$ , (c)  $\bar{1}10\bar{7}$ , and (d)  $011\bar{7}$ . Figure 1.17 reveals that under each diffraction condition, some parts of the BPD networks become out of contrast; the parts that are out of contrast under each diffraction condition are indicated by white lines in each topograph. The extinction of the diffraction contrast means that the Burgers vectors associated with these parts of the BPD networks are perpendicular to the diffraction vector, and thus, the results of the  $\mathbf{g} \cdot \mathbf{b}$  contrast analyses shown in Figure 1.17 demonstrate that the BPD networks



**Figure 1.16** Reflection X-ray topograph for diffraction condition  $\mathbf{g} = 1\bar{1}\bar{2}\bar{8}$  of region A in 1.5° off-oriented 4H-SiC (0001) wafer, where the position of the grown-crystal/seed interface is indicated by a white dashed line. In this figure, the region used for subsequent  $\mathbf{g} \cdot \mathbf{b}$  analyses (see Figure 1.17) is indicated by a white open square (region B). Source: Shioura et al. [39].



**Figure 1.17** Reflection X-ray topographs of BPD networks observed in region B of 1.5° off-oriented 4H-SiC (0001) wafer for diffraction conditions (a)  $g = 11\bar{2}\bar{8}$ , (b)  $\bar{1}01\bar{7}$ , (c)  $\bar{1}10\bar{7}$ , and (d)  $01\bar{1}\bar{7}$ . The diminished parts of the BPD networks under each diffraction condition are indicated by white solid lines in each topograph. Source: Shioura et al. [39].

consist mainly of edge-type BPDs that have a Burgers vector perpendicular to the dislocation line. This result suggests that a high density of BPDs observed at the grown-crystal/seed interface would have been caused by some form of misfit stress within the basal plane imposed at the interface during the initial stage of PVT growth.

To investigate further the nature of the BPD networks, the bending of the (0001) basal plane was examined by means of measurements of the peak position shift of the  $\omega$ -scan 0008 HRXRD rocking curve across the grown-crystal/seed interface [39]. The results indicated that the (0001) basal plane in the slightly off-oriented (0001) wafer contained the beveled interface between the grown crystal and seed crystal bent in a concave manner in the  $[000\bar{1}]$  growth direction, which implies that the crystal near the grown-crystal/seed interface contained extra half-planes pointing in the  $[0001]$  direction (the backside of the seed crystal).

### 1.3.4 Formation Mechanism of BPD Networks and Their Migration into Seed Crystal

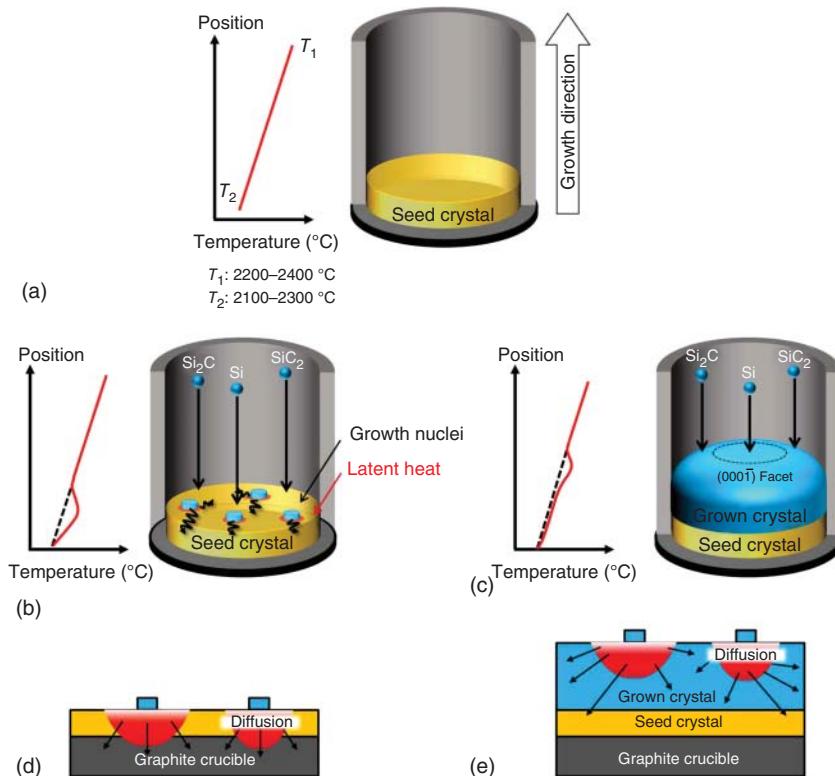
It was revealed by HRXRD measurements that there were extra half-planes pointing in the  $[0001]$  direction in the crystal near the grown-crystal/seed interface [39]. These extra half-planes are thought to be associated with the BPD networks existing near the grown-crystal/seed interface. It was also revealed that most parts of BPDs comprising the networks have an edge component, and thus, they are likely to have

been caused by misfit strain accommodated at the interface during the initial stage of SiC PVT growth.

The misfit strain within the basal plane at the grown-crystal/seed interface has two possible origins, namely, (i) nitrogen enrichment at the interface and (ii) the temperature gradient in the growth direction imposed on the growing crystal in the initial stage of PVT growth. The nitrogen enrichment at the grown-crystal/seed interface has been reported by several authors [12, 22–25]. The grown crystal was doped intentionally with nitrogen in the same concentration as the seed crystal; however, residual nitrogen impurities in the growth atmosphere and/or those adsorbed on the source powder surface could give rise to a relative enrichment of nitrogen in the crystal grown during the early stage of PVT growth. Nitrogen doping has been reported to give rise to a smaller lattice spacing [42] and also a smaller coefficient of thermal expansion [43] within the basal plane for 4H-SiC crystals; thus, a higher nitrogen concentration in the grown crystal than that of the underlying seed crystal would give rise to misfit strain between the grown crystal and the seed. However, in this case, the sign of the misfit strain is opposite to that having caused the BPD networks; the nitrogen enrichment in the grown crystal results in a smaller lattice constant within the basal plane at the PVT growth temperature ( $\sim 2300^\circ\text{C}$ ), yielding BPDs with extra half-planes pointing in the growth direction when the misfit strain is relieved. This is contradictory to the result of the HRXRD measurements.

Another possible origin of the misfit strain at the grown-crystal/seed interface is the temperature gradient at the interface. Usually, during SiC PVT growth, a positive temperature gradient in the growth direction is set in the growth zone by placing the growth crucible asymmetrically in the radio-frequency (RF) induction coil or the heating furnace (see Figures 1.1a and 1.18a). In addition to this intentionally imposed temperature gradient, the latent heat dissipation associated with the condensation of Si- and C-bearing species sublimed from the source powder would result in an enhanced positive temperature gradient during PVT growth. In this respect, note that SiC has an extremely large latent heat of phase transition from the vapor to the solid (heat of condensation/sublimation), which is estimated to be 580 kJ/mol [44] and more than 10 times larger than that of Si solidification from the melt (50.6 kJ/mol) [45].

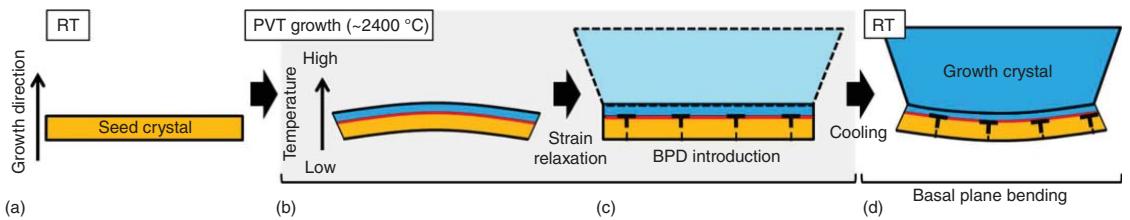
With respect to the heating due to the latent heat, another important factor that should be considered is the thickness of the grown crystal in the initial stage of growth. Figure 1.18 explains schematically how the thickness of the grown crystal affects the dissipation of latent heat. Upon condensation of the Si- and C-bearing species, the latent heat is released on the growing crystal surface. The seed crystal is usually placed on a graphite holder, which has a much lower thermal conductivity than that of 4H-SiC at the PVT growth temperature. In the initial stage of PVT growth, the SiC crystal (seed crystal plus grown crystal) is very thin, and thus, all the heat generated by the condensation of Si- and C-bearing species must be dissipated through the backside of the seed crystal (Figure 1.18d). However, the low thermal conductivity of the graphite seed holder means that the generated heat is not dissipated efficiently, and thus, an even larger positive temperature gradient is established at the growing crystal surface during the initial stage of PVT



**Figure 1.18** Schematics of latent heat dissipation during PVT growth of 4H-SiC crystals. (a) Positive temperature gradient in the growth direction imposed intentionally in the growth crucible by placing it asymmetrically in the RF induction coil or the heating furnace. (b) Enhancement of temperature gradient at growth front of the grown crystal caused by the poor latent heat dissipation in the initial stage of PVT growth because of the low thermal conductivity of the graphite seed holder; this effect is shown schematically in (d). (c) Case of a thick grown crystal after sufficient time of crystal growth; the enhanced temperature gradient at the growth front is lessened considerably because the generated latent heat can be dissipated efficiently through the thickly grown SiC crystal, as shown schematically in (e).

growth (Figure 1.18b). This large positive temperature gradient causes a large misfit strain within the basal plane at and near the grown-crystal/seed interface, which is relieved by the introduction of BPDs during growth. By contrast, as the grown crystal becomes thicker as it grows, the latent heat is dissipated more efficiently through the body of the thick grown crystal (Figure 1.18e). This lessens considerably the enhanced temperature gradient at the growth front due to the condensation of the Si- and C-bearing species (Figure 1.18c).

The aforementioned strain generation and relaxation processes due to the latent heat are illustrated schematically in Figure 1.19. The figure depicts sequentially (a) the seed crystal prior to PVT growth, (b) the basal plane bending associated with the large temperature gradient in the initial stage of growth, which occurs in a convex manner in the growth direction, (c) the introduction of BPDs to relieve the



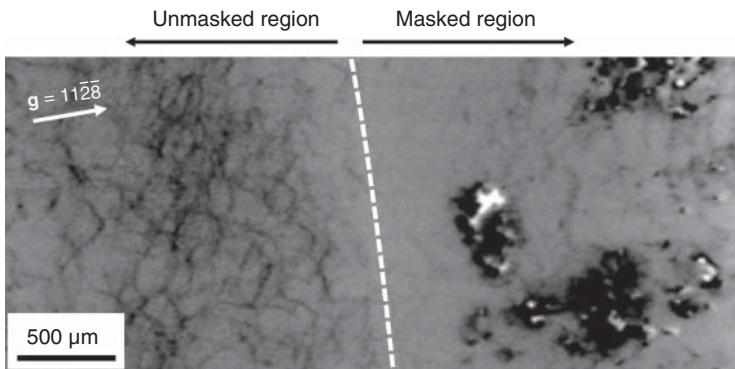
**Figure 1.19** Schematic of introduction of BPDs at grown-crystal/seed interface during PVT growth process, and the resulting basal plane bending after the growth process. Source: Shioura et al. [39]. © 2019, Elsevier; (a) seed crystal prior to PVT growth, (b) basal plane bending associated the large temperature gradient at the initial stage of growth, which occurs in a convex manner toward the growth direction, (c) introduction of BPDs to relax the misfit strain within the basal plane at the grown-crystal/seed interface, and (d) concave-shape basal plane bending toward the growth direction after cooling to room temperature.

misfit strain within the basal plane at the grown-crystal/seed interface, and (d) the resultant concave-shaped basal plane bending in the growth direction after PVT growth. The large basal plane bending due to the poor heat dissipation in the initial stage of PVT growth of SiC was observed experimentally by Hock et al. using *in situ* X-ray diffraction [46]. They found that the degree of basal plane bending increased with the growth rate, implying that the latent heating due to the condensation of source gas species plays an important role in the basal plane bending in the initial stage of PVT growth.

The final concave shape of the basal plane in the growth direction shown in Figure 1.19d is consistent with the lattice bending observed by HRXRD, and thus, the large positive temperature gradient established at the growing crystal surface during the initial stage of PVT growth would be the most plausible cause of the observed BPD networks. The relationship between the observed BPD networks and the formation of threading dislocations in the initial stage of PVT growth [10–12] is yet to be clarified. However, in Figure 1.17, in addition to the BPD networks, dot-like features are also observed at the nodes of the BPD networks. They are likely to correspond to threading dislocations and suggest that the BPD networks are related closely to them and would be an important source of threading dislocations in PVT-grown 4H-SiC crystals.

As revealed in Figure 1.16, the BPD networks extended fairly deeply in the seed crystal. The maximum depth of the networks in the seed crystal can be estimated from their positions on the surface of the  $1.5^\circ$  off-oriented  $(000\bar{1})$  wafer; the networks extended up to 7 mm on the wafer surface from the grown-crystal/seed interface toward the backside of the seed crystal. The distance of 7 mm on the wafer surface corresponds to a depth of 300  $\mu\text{m}$  from the grown-crystal/seed interface toward the backside of the seed crystal. In the initial stage of PVT growth, growth islands are likely to nucleate on the seed crystal surface and then coalesce as the crystal growth proceeds (see Figure 1.18b). Under a large positive temperature gradient, the growth islands tend to incorporate BPDs to relieve the misfit strain due to the temperature gradient, and when the islands coalesce, the BPDs are rearranged and form networks at the grown-crystal/seed interface. The results obtained by Shioura et al. indicated that these BPD networks at the interface were accompanied by extra half-planes pointing toward the backside of the seed crystal and caused the  $(000\bar{1})$  basal plane to bend in a concave manner in the growth direction after the PVT growth process [39]. An important question here is how and why these BPD networks migrated into the seed crystal during PVT growth.

There are two possible mechanisms for the migration of the BPD networks into the seed crystal, namely, (i) the glide motion of BPDs on the basal plane and (ii) the climb motion of BPDs across the basal plane. To clarify the mechanism for BPD migration into the seed crystal during PVT growth, Shioura et al. conducted a masked PVT growth experiment on a  $4^\circ$  off-oriented  $(000\bar{1})$  seed crystal [39]. The result is shown in Figure 1.20, where a reflection X-ray topograph for the diffraction condition  $\mathbf{g} = 11\bar{2}\bar{8}$  acquired from the boundary area between the masked and unmasked regions of the seed crystal is shown. The masked region (right-hand side of the figure) was covered with a graphite plate during PVT growth to prevent



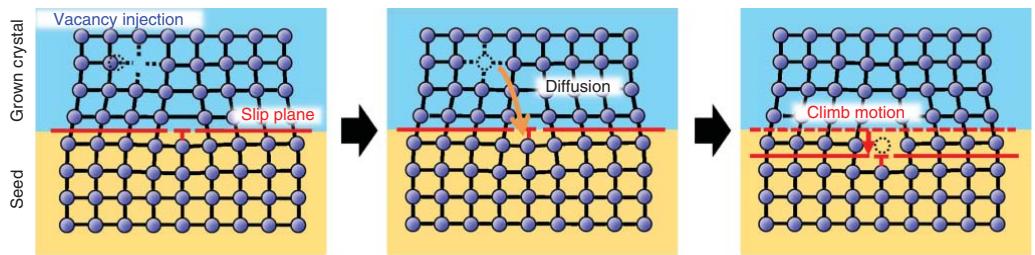
**Figure 1.20** Enlarged reflection X-ray topograph for diffraction condition  $g = 11\bar{2}\bar{8}$  acquired from the boundary area between the masked and unmasked regions of the seed crystal; the 4H-SiC crystal was grown on the unmasked region (left-hand side of the dashed line in the topograph), whereas no crystal growth occurred on the masked region (right-hand side of the dashed line). The topograph shows clearly that the BPD networks in the seed crystal existed only in the unmasked region of the seed crystal. Source: Shioura et al. [39].

crystal growth. As shown in the figure, BPD networks exist only in the unmasked region and do not extend into the masked region. This result shows clearly that the observed BPD networks migrated into the seed crystal through the climb motion of dislocations, as schematically illustrated in Figure 1.21, rather than the glide motion. This is because, had the glide motion been the dominant mechanism for BPD migration, then the BPD networks formed during the initial stage of PVT growth should have glided on the basal plane into the masked region beyond the boundary between the unmasked and masked regions and then been observed in the masked region of the seed crystal after the crystal growth.

The climb motion of dislocations is driven by the injection, diffusion, and incorporation of intrinsic point defects, such as vacancies and interstitials, to the dislocations [47]. As described in Section 1.3.3, the observed BPD networks were accompanied by extra half-planes pointing toward the backside of the seed crystal, and thus, their migration toward the backside of the seed crystal requires vacancies to be incorporated in the dislocations as illustrated schematically in Figure 1.20. Given the migration depth of the BPD networks, it is clear that a large number of vacancies were injected during the initial stage of PVT growth. The mechanism for this remains unclear, but the poor dissipation of the latent heat in the initial stage of PVT growth (see Figure 1.18b,d) would cause local heating of the growing crystal surface, which may induce the injection of a large number of vacancies into the growing crystal.

## 1.4 Conclusions

SiC is a promising material for the next generation of power semiconductor devices, and the adoption of SiC power devices is critical for enabling faster, smaller, lighter,



**Figure 1.21** Schematic of the climb motion of a BPD toward the backside of the seed crystal due to the vacancy injection into the growing crystal during PVT growth. Source: Shioura et al. [39]. © 2019, Elsevier.

and more powerful power electronic systems. However, it is amply clear that such a successful adoption of SiC power devices for a wide range of power electronics systems relies considerably on establishing the manufacturing technology for large-diameter high-quality SiC single crystals. This chapter described recent progress in understanding the dislocation formation processes in PVT-grown SiC crystals, which is essential for obtaining high-quality SiC crystals.

After a brief introduction (Section 1.1), Section 1.2 was dedicated to understanding the BPD nucleation and multiplication processes during the PVT growth of 4H-SiC crystals. A large number of BPDs are introduced from the shoulder region of the growth front of 4H-SiC crystals, where a large thermoelastic shear stress is thought to be imposed during PVT growth. Detailed investigations of the BPD distribution in grown crystals suggest that BPDs nucleated at the shoulder region of a growing crystal largely determine the BPD distribution across the entire crystal.

In Section 1.3, the defect structure at the grown-crystal/seed interface of PVT-grown 4H-SiC crystals was investigated using 4H-SiC wafers with a beveled interface between the grown crystal and seed crystal. The existence of BPD networks at the grown-crystal/seed interface was revealed, and they extended considerably into the seed crystal. Such networks were likely to be caused by a large positive temperature gradient imposed on the growing crystal surface because of the local heating by the latent heat dissipation associated with the condensation of Si- and C-bearing species from the vapor during the initial stage of PVT growth. It was also revealed by masked-growth experiments that the migration of the BPD networks deep into the seed crystal was caused by the injection of a large number of vacancies during the initial stage of PVT growth of 4H-SiC crystals.

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## 2

### Industrial Perspectives of SiC Bulk Growth

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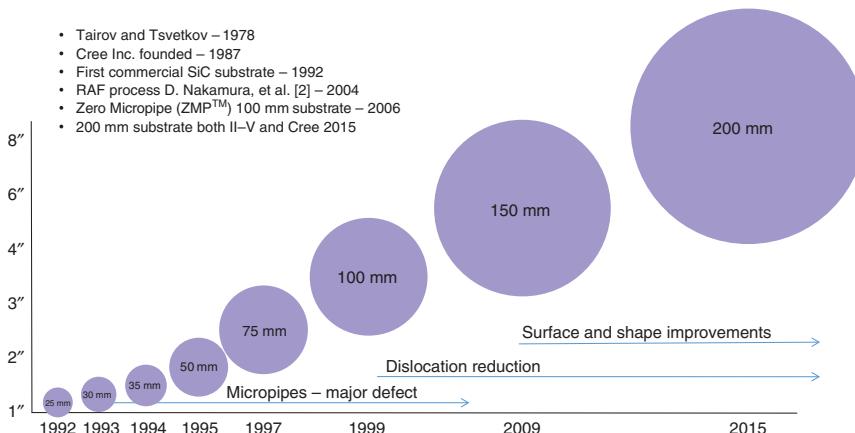
#### 2.1 Introduction

In this chapter, we discuss the inherent differences between growing SiC wafers for specialized high-end niche markets and the production of SiC wafers substrates for large-volume manufacturing. Both are critical in developing a robust commercial market. In the case of SiC, many academic and industrial players have contributed to the impressive ramp in quality and diameter that SiC wafers have experienced over the last 30 years. Figure 2.1 shows how the maximum diameter of SiC wafers has increased since the first commercial release in 1991 along with some of the critical milestones [1–4].

Currently, there are three primary markets for SiC wafers: (i) low-doped substrates for GaN light-emitting diode (LED) structures, (ii) high-doped substrates for high-power SiC device structures, and (iii) semi-insulating substrates for high-frequency GaN devices. In the following sections, we will discuss the commercial needs of each of these in turn. For each, we will address the key question of price vs. quality. For commercialization, it is important to remember that the perfect substrate is the one that meets all the customer needs at the lowest cost to produce. It is this balance between providing substrates that meet all customer requirements and are priced as low as possible that distinguishes industrial development from academic research.

#### 2.2 SiC Substrates for GaN LEDs

The first high-volume usage of SiC substrates was driven by the release of high-brightness blue and green LEDs in the early 2000s by both Cree and Osram. This was the product that took the production of SiC substrates into true commercialization. GaN LEDs are fabricated on SiC substrates through heteroepitaxy. The unit cells and thermal expansion of SiC and GaN are not perfectly matched;



**Figure 2.1** Progression of demonstrated single-crystal wafer diameter.

however, the match is superior to other available substrates (Si or Sapphire), and the nucleation of high-quality GaN layers can be achieved.

The primary factor that controls this nucleation is the offcut angle of the substrate. Thus, tight tolerances to  $<0.25^\circ$  are required here, and any curvature of the lattice planes within the substrate must be avoided. However, even with optimal nucleation conditions, the interface between SiC and GaN introduces many, typically greater than  $10^5 \text{ cm}^{-2}$  dislocations [5, 6], which are subsequently controlled by complex buffer structures in the GaN epitaxial growth. The consequence of this for the SiC substrate manufacturer is that dislocation densities in the substrates become non-critical at substrate values below  $10^5 \text{ cm}^{-2}$ . The final critical parameter for LED substrates is their optical characteristics. Many of the LED chip structures rely upon the generated light traveling through the substrate and therefore a transparent substrate is desired, this in turn defines a purity level required. In the case of SiC, the most problematic impurities are nitrogen, boron, and aluminum. Since all three of these are electrically active and cause absorption of the light emitted by the LED, in general the level of impurities in the substrates must be kept below  $10^{17} \text{ cm}^{-3}$ . In the most recent decade, the ability to produce these LED diode structures on Sapphire substrates has improved, and so it is anticipated that further market growth of this segment will be static due to the lower price point of Sapphire substrates.

### 2.3 SiC Substrates for Power SiC Devices

LEDs allowed the first commercialization of SiC substrates; however, as we enter the next decade, it is expected that the volume of the power product will expand. In 2019, over 1 billion dollars of expansion was announced by various SiC substrate manufacturers mostly directed toward power device structures. SiC power devices include Schottky and MOSFET diodes. These devices are fabricated in SiC epitaxy grown directly on SiC substrates. For SiC epitaxy, the growth is carried out on

$4^\circ$  offcut surfaces, and this in turn reduces the requirement for very low lattice plane curvature. However, the quality requirements of the epitaxial SiC on SiC substrates are extremely high, and therefore, any defects in the substrate that thread into the epitaxy are a great concern. This leads to stringent limits on defect densities in the substrate with micropipes typically below  $1\text{ cm}^{-2}$  and dislocations  $<10^3\text{ cm}^{-2}$ . Unlike LEDs, these device structures electrically connect through the substrate requiring highly doped, low resistivity material. Generally, nitrogen is the active dopant, and resistivity values are desired to be as low as possible ( $0.015\text{--}0.028\text{ }\Omega\text{-cm}$ ) so as to minimize device on resistance. It is known that a higher doping concentration leads to the occurrence of stacking fault defects in the active devices [7] and so this sets the minimum wafer resistivity.

## 2.4 SiC Substrates for High-Frequency Devices

High-frequency power devices are made from GaN on SiC; consequentially, the demands are similar to those of LED structures with the additional requirement that the substrate must not electrically couple to the active device. Thus, a very high resistivity substrate is desired. This can be achieved either through the addition of a deep level impurity such as vanadium [8] or by reducing the level of all impurities to a level less than  $2 \times 10^{-16}\text{ cm}^{-3}$  [9]. Table 2.1 shows the key aspects of substrate quality that must be present to allow high-yielding stable device structures to be manufactured for all three product types.

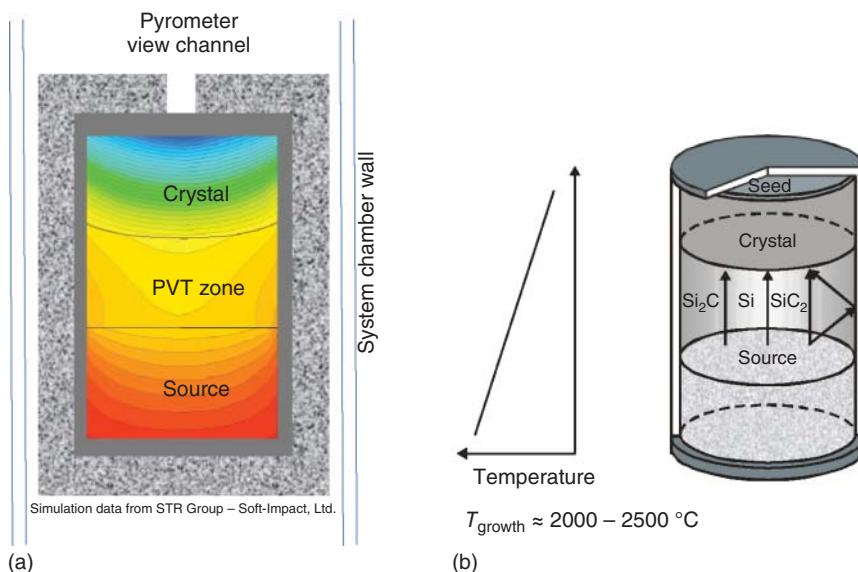
## 2.5 Cost Considerations for Commercial Production of SiC

The basic wafer supplier question is “how to provide high quality wafers, at a minimal cost.” For SiC, that means that the manufacturer must consider where the

**Table 2.1** Indicating substrate characteristics beyond which significant final device yield hits might be expected<sup>a)</sup>.

Characteristic	LED (GaN on SiC)	Power (SiC on SiC)	High frequency (GaN on SiC)
Surface orientation	$0.0 \pm 0.25$	$4.0 \pm 0.5$	$0.0 \pm 0.25$
Micropipe density	$<5\text{ cm}^{-2}$	$<1\text{ cm}^{-2}$	$<1\text{ cm}^{-2}$
Basal plane	$<10^5\text{ cm}^{-2}$	$<10^3\text{ cm}^{-2}$	$<10^5\text{ cm}^{-2}$
Threading screw	$<10^5\text{ cm}^{-2}$	$<10^3\text{ cm}^{-2}$	$<10^5\text{ cm}^{-2}$
Threading edge	$<10^5\text{ cm}^{-2}$	$<10^5\text{ cm}^{-2}$	$<10^5\text{ cm}^{-2}$
Resistivity	$>0.2\text{ }\Omega\text{-cm}$	$0.015 < x < 0.03\text{ }\Omega\text{-cm}$	$>10^5\text{ }\Omega\text{-cm}$

a) Commercial specs are often set well inside these limits.



**Figure 2.2** (a) Schematic of a SiC growth system, (b) schematic of gases present during growth. Source: Tairov and Tsvetkov [1].

main cost drivers are in the process and reduce them. Currently, in 2020, virtually all commercial SiC production utilizes the modified Lely technique, shown in Figure 2.2. Here, a seed wafer of SiC is placed at the top of the crucible and SiC source material placed at the base. The crucible is then heated to temperatures in excess of 2000 °C. The overall temperature is controlled by pyrometer feedback to the power supply, and the thermal field shape is controlled both by the positioning of the thermal insulation and by where the heat energy is coupled into the crucible. In a typical growth, both the absolute temperature and the axial thermal gradient are adjusted to maintain optimal thermal fields. As the seed/crystal region is kept cooler than the source region, the SiC sublimation gases sublime from the source and condense on the growing crystal.

From a cost point of view, we have several items to consider and these are outlined in Table 2.2.

## 2.6 Raw Materials

For modified Lely growth, one requires a seed of similar diameter to the final grown crystal. This of course has a cost similar to that of a completed SiC wafer. In this style of growth (unlike Si growth), there is no necking down of the crystal diameter, and therefore, any threading defects or misoriented regions in the seed wafer will be propagated into the growing crystal. This difficulty in producing crystals with significantly larger diameter than the seed used is one of the factors that has slowed the increase in SiC wafer diameter available to the commercial market. Two main approaches have been used for seed diameter expansion; the

**Table 2.2** Cost considerations for SiC bulk growth.

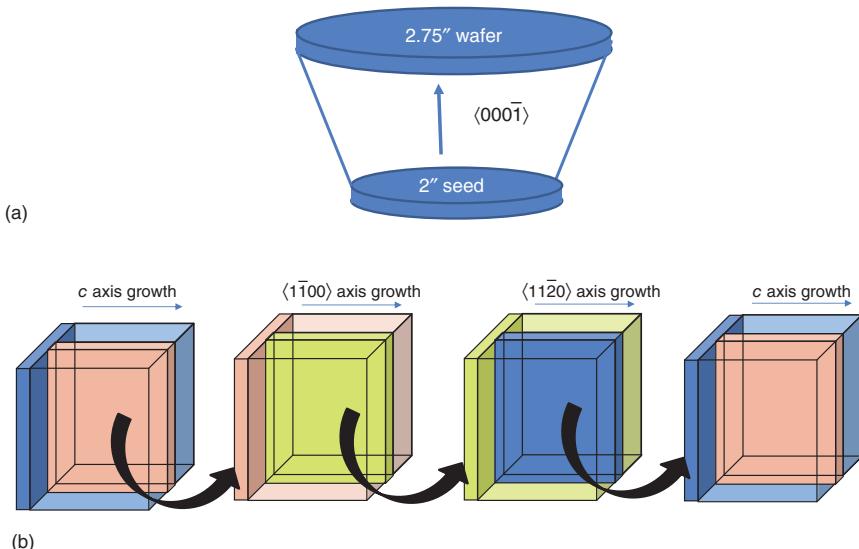
Requirement	Subsystem	Cost is a function of
Raw materials	Seed, SiC source material	Part purity and efficiency of conversion to final crystal
Reactor hot zone	Graphite crucible, insulation	Part purity, part size, part lifetime
Equipment	Crystal growth system	Time required for growth process (turns per year)
Wafer manufacture	Wafering and polish	Equipment cost and throughput, slurry cost
Yield	Fraction of high-quality product per start	Bulk crystallographic defects, boule and processing machining errors, kerf loss, and wafer thickness

first is a gradual increase in crystal diameter, here the region of high-quality crystal is expanded, growth after growth, where the general orientation of the growth direction is in the “*c*” axis direction, an example of a 2" to 2.75" diameter expansion was shown by II-VI Inc. [10] (Figure 2.3a), and the second approach was pioneered by Denso Inc. [2] and termed “Repeated A Face” growth (Figure 2.3b). In this second approach, a crystal is first grown on the “*c*” axis direction; however, instead of slicing perpendicularly to the “*c*” axis, an orthogonal slice is taken perpendicular to the  $\langle\bar{1}\bar{1}00\rangle$  plane, this slice is used as a seed to grow a second crystal in the  $\langle\bar{1}\bar{1}00\rangle$  direction, from which an orthogonal slice is also taken, this time allowing growth in the  $\langle\bar{1}\bar{1}\bar{2}0\rangle$  direction, again this slice is then used to grow a crystal and an orthogonal slice taken, this time the slice is perpendicular to the  $\langle000\bar{1}\rangle$  direction and it is suitable to be a seed for a conventional growth, and thus a high-quality *c*-axis seed boule can be produced. It should be noted that due to the challenges involved in creating high-quality seeds, many manufacturers place restrictions on their wafer sales, preventing the use of a commercially sold wafer as a seed substitute.

The other primary input is the source material; in the modified Lely process, this is SiC powder, and the key cost parameter here is what fraction of powder is transported to grow the crystal, rather than to create parasitic deposits elsewhere in the crucible, gas leakage out of the crucible, or simply residual source not consumed during growth.

## 2.7 Reactor Hot Zone

The modified Lely approach for SiC is unusual compared to other commercial crystal growth processes in that it operates at very high temperatures 2200–2400 °C [11, 12]. At these temperatures, there is a limited pallet of materials available that (i) withstand the temperature without decomposing and (ii) can be fabricated at high purity levels. The most commonly used material for both crucible and insulation is graphite. Figure 2.2a shows a typical reactor configuration for the hot zone showing



**Figure 2.3** Two differing methods for expanding SiC seed: (a) schematic of gradual expansion and (b) schematic of repeated A-face growth (RAF) technique.

(i) crystal location, (ii) source location, (iii) crucible walls, (iv) insulation materials, and (v) reactor walls.

The challenge with graphite for the crucible build at these high growth temperatures, and in the presence of typical gases Si, Si<sub>2</sub>C, and SiC<sub>2</sub>, is that serious etching can occur on the inside walls of the crucible. It is key that the crucible remains whole for the entirety of the growth process. This etching behavior is enhanced at higher temperatures, again leading to a compromise choice between costs in terms of crucible parts lifetime vs. the savings achieved through increasing the growth rate by increasing growth temperatures.

Next out from the crucible is the insulation package that serves two major functions. The first of these is to keep the heat in the hot zone, to avoid high power consumption levels, without any insulation; the simple crucible shown in Figure 2.2a would need about 700 kW to maintain its temperature, this would not be financially viable. The second function is to allow control of the thermal profile within the growth crucible, by variation of the thickness and thermal properties of the insulating material surrounding that crucible. For example, it can be seen in Figure 2.2a that the gap in the insulation at the top of the crucible provides both a clear path for temperature control via a pyrometer and an exit route for energy in the crucible. This in turn locally cools the crystal directly below the "pyrometer view channel," thus providing a concave thermal field in the crystal region. Since SiC will deposit preferentially at the coolest location, this configuration would be expected to grow a convex SiC crystal as suggested by the schematic.

As one moves away from the hot zone, other more standard insulation materials become more viable, and the system design tends toward more standard low-pressure grower designs.

## 2.8 System Equipment

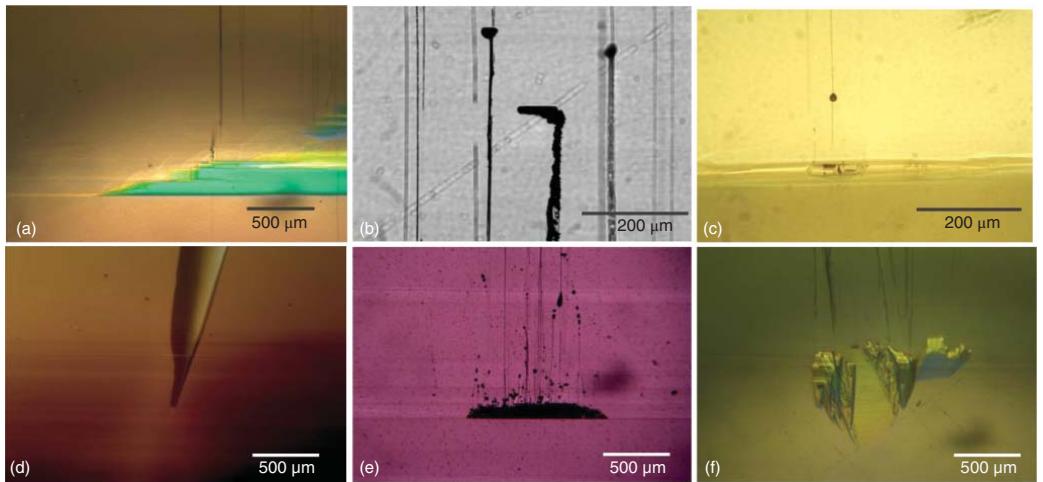
Many SiC wafer vendors keep their reactor geometry proprietary, though some early images are available [13]; in addition, there are currently several commercial vendors of SiC furnaces. However, whatever the source of the reactor, the cost of ownership is high and the factory floor space requirement is substantial. As an example, consider a published growth rate of 0.1 mm/h [14]. Assuming very effective reactor turn around, one might then grow 800 mm of crystal in a year from this grower. If one then assumes a US\$ 1 million grower cost, a five-year depreciation, and excellent yields, a typical wafer slice would have a contributory cost of over US\$ 200 from the grower equipment alone. This high cost drives the desire to increase the SiC growth rate. However, as the growth rate is pushed up, there is a tradeoff between high growth rates and induced crystalline defects. This will be discussed in the following section.

## 2.9 Yield

Left till last, but as in all processes, the yield is of immense importance. The cost of growing a defective crystal is the same as that of growing a high-quality crystal, so we must ensure that our growth process creates few defective crystals. Unfortunately, the need to produce a high-growth-rate, long-length crystal from a low-cost starting set of raw materials is often in direct competition to growing low defectivity crystals. The science of production is to create the optimal balance between these competing factors. Figure 2.4 shows many of the defects associated with the growth of SiC boules. Some of these have been well characterized by the scientific community and the mechanisms of their formation well understood. However, the nucleation mechanisms of others are still not fully explained, and much exciting work remains in the field to identify root causes and optimal ways to prevent the defect formation in standard growths.

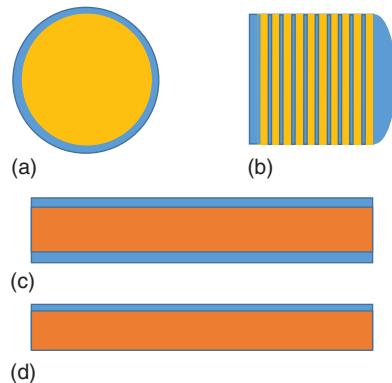
The creation of a new product or process requires several stages – each with a unique focus. Originating in research phase, where researchers champion the few excellent crystals to highlight where the process can go, the process typically moves through to early production where the focus changes to how to increase the total number of passing wafers, i.e. yield enhancement. From there, the process typically moves on to full production, where reducing process cost is of primary concern. For SiC, this yield and cost improvement is generally split into three categories: (i) Reduction of total failures: typical causes of these are equipment failure and nucleation of differing polytypes and orientations near the start of growth (Figure 2.4a,d,f). (ii) Reduction of mid boule fails: typical causes are incorporation of particles and local switching of polytype (Figure 2.4c,e). (iii) Finally, overall tightening of slicing and surface finish processes help to boost the yield to acceptable levels.

As the understanding of how the input materials, and process variables, effect the different fail modes, the overall process yield can be continually increased whilst simultaneously allowing some loosening of non-key input specifications to allow for lower cost inputs.



**Figure 2.4** Images of six defect modes that are commonly observed in SiC growth, in all cases the growth direction is upward. (a) Polytype switch from 4H, to 6H, 15R, and back, (b) large voids migrating through the crystal, (c) defect inclusion generating a small tear-shaped void, (d) initiation point of an inclusion of different orientation of SiC, (e) large growth disruption introducing many pipes and dislocations, (f) 3C inclusion, here some of the side facets of the 3C inclusion are clearly visible with the center region showing a characteristic yellow color.

**Figure 2.5** Schematic illustrating overall kerf loss for wafer manufacture processes, (a) OD grind loss from outer perimeter, (b) saw loss, (c) loss in double side polish, and (d) loss in final single side CMP.



## 2.10 Turning Boules into Wafers

Once a SiC boule has been grown, it must then be converted into high-quality wafers. For SiC, there are challenges here due to its high hardness value of 9.4 Mohs and general chemical inertness. The general process is as follows:

- Grind the crystal down to the desired diameter
- Slice this boule into wafers
- Mark the wafers with identification, orientation flats, and appropriate edge shape
- Rough polish the wafers
- Final chemical mechanical polish (CMP) step
- Characterize and supply to customer

From a cost point of view, it is worth considering that each processing step removes SiC crystal and thus represents a kerf loss. Typical kerf loss mechanisms and values are shown in Figure 2.5: Outer diameter (OD) grind 3–10%, seed and dome removal 1–5%, wafer slicing 30–40%, rough double side polish 10–20%, and final CMP <1%. Together, these can easily represent more than half of the grown crystal mass. Kerf loss has a critical role to play in the final cost of SiC wafer product and is particularly hurtful to crystal growers, as it represents the loss of high-quality material to the shaping operations. Much development work has gone into improving processing techniques to reduce overall kerf losses and increase the yield of these processes.

## 2.11 Crystal Grind

This is a fairly typical process for bulk crystal processing, where the SiC crystal is rotated and brought into proximity with a high-speed diamond grind wheel. The diamond cutting teeth on the wheel will then locally scrape away the SiC crystal material; however, SiC is unusual in that for most crystal materials, the local heating caused by the cutting diamond tooth causes the crystal to exceed the ductile to brittle transition temperature. Thus, the material removal is conducted in the

ductile domain where cracking is eliminated. For SiC, since the ductile to brittle transformation is high [15], the grind operation is generally in the brittle domain, and consequently, cracks are initiated at the outer grind surface. Care must be taken to ensure that these cracks do not propagate deeply into the crystal. In practice, to minimize this crack depth, a low grind rate is used, and the final outer edge of the crystal is effectively cleaned up later in the wafer edge grind and polish steps.

## 2.12 Wafer Slicing

Wafer slicing is where the thickness, orientation, and much of the final wafer shape are determined. Over the past two decades, multi-wire slicing has become the dominant process for slicing boules (<http://www.takatori-g.co.jp/english>). In multi-wire slicing, a thin steel wire is coated with a diamond slurry, and this wire is pulled backward and forward across the SiC surface at a speed up to 10 m/s. The process is essentially a lapping process directly between the wire and the SiC surface, with the diamond slurry providing the abrasive material and the wire acting to provide both the downforce and the lateral velocity to the diamond particles. This process creates a trench at each wire location that gradually becomes deeper as the operation continues. This operation is inherently slow since the removal rate for the lapping process is roughly 5 mm/h. Thus, many hours are needed to cut through a 150-mm-diameter boule. To effectively speed up this process, the wire is wrapped around rollers such that a wire web is created with several hundred parallel wires; consequentially, although the slicing process itself is slow, the ability to cut several hundred slices concurrently alleviates this (Figure 2.6).

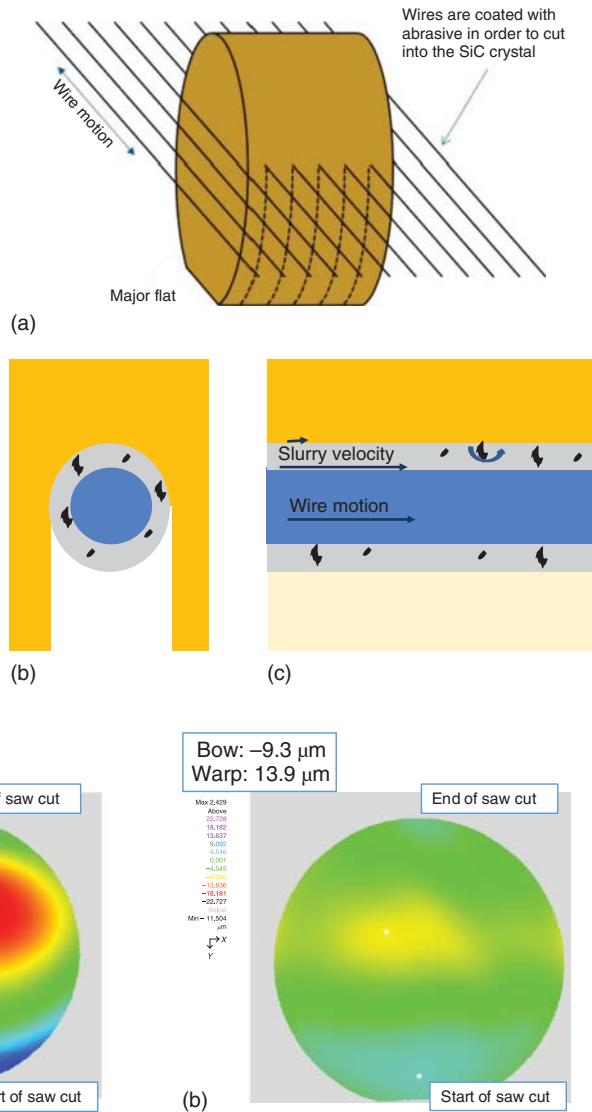
While this slicing process is simple in concept, many parameters such as wire tension, wire speed, diamond slurry composition, downforce applied to the wire, and wire diameter must be tightly controlled to cut the crystal successfully without imparting excessive shape into the sliced wafers. One further consideration is the need to maintain a stable cutting zone. Effects such as differential temperatures or nonoptimal thermal expansion loops will tend to cause the wires to move sideways during the cut which will often cause displacement of wires w.r.t. the crystal and poor wafer shape particularly at the start and end of a cut where the rapidly changing cut length makes it more difficult to hold slicing conditions stable.

In addition to wafer shape induced by the saw, there is additional shape induced due to both residual stress in the grown crystal and due to differential damage depths on the Si face vs. the C face of the wafers. This tends to impart a radially symmetric shape into the wafer. Figure 2.7 shows how the shape of 150 mm wafers have been improved through the optimization of growth and slicing processes.

There is interest in other slicing techniques predominantly due to the potential of lower kerf loss. These include laser splitting [16], electrical discharge machining (EDM) [17] slicing, and diamond impregnated wire slicing.

Laser splitting utilizes a high-power laser to locally heat a region of the crystal beneath the surface, and this thermal expansion in turn creates microcracks that are predominantly in the basal plane direction. Through careful control, this heating

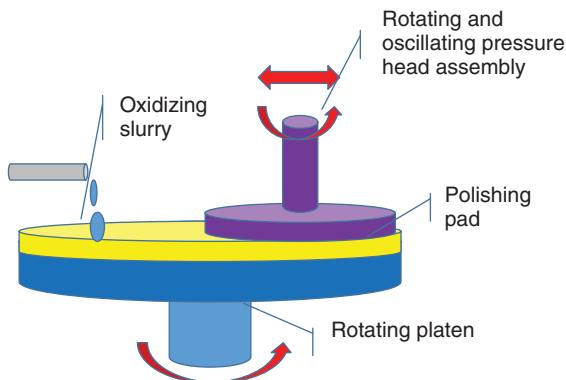
**Figure 2.6** Schematic showing modern wire saw configuration:  
 (a) configuration of boule with respect to wire web,  
 (b) cross section of wire coated in slurry cutting crystal,  
 (c) lateral cross section showing slurry velocity causing a rolling motion in the diamond particles. Note for many commercial saws, the wire cuts upward into the crystal as shown in the figure.



**Figure 2.7** (a) A 150 mm wafer shape obtained from an unoptimized cut, (b) 150 mm wafer shape obtained once slicing parameters are optimized.

can be maintained within a very tight depth window from the surface of the boule, and thereby, as this laser is scanned across the wafer, a “sheet of cracks” can be produced. It then becomes possible to peel or pull this top wafer from the boule. This technique could in principle reduce kerf loss to below 50  $\mu\text{m}$  and is only limited by the accuracy of the optical system controlling the depth of penetration and the degree of localization of the cracking behavior.

EDM slicing is similar to wire slicing except that in this case a high voltage in the wire is used to strike a plasma between the wire and the crystal. This plasma in turn



**Figure 2.8** Schematic of a CMP process.

etches the crystal to create the slicing operation. Since the wire is not being required to both carry slurry and provide the downforce, it may be possible to reduce wire diameter significantly and therefore reduce material kerf loss.

Diamond impregnated wire slicing, as oppose to diamond slurry wire slicing, is gaining in popularity due to the potential of reduced wire tension, and thus the reduced diameter wire required, thereby producing reduced kerf loss. As the name implies, this technique is very similar to typical wire slicing, except that the abrasive (diamond) is actually bonded to the wire before the cutting operation.

## 2.13 Wafer Polish

Once the crystals have been sliced into wafers, the processing becomes similar to that of other semiconductors in that a series of surface finishing steps are used that typically consist of polishing with successive steps of abrasive material reducing the abrasive diameter with each step (diamond for SiC wafers). This type of removal will always leave a damaged sublayer in the wafer whose depth is proportional to the abrasive size. Consequentially, the final finish is provided by a CMP step, Figure 2.8, where an oxidizer is combined with a soft abrasive. The oxidizer converts the surface layer of SiC to  $\text{SiO}_2$ , and this oxide layer is then removed by the soft abrasive. Fortunately, the soft abrasive is not aggressive enough to scratch SiC, and so a high-quality surface can be achieved.

## 2.14 Summary

Over the last 30 years, SiC materials growth has developed into a mature industry with multiple manufacturers of high-quality wafers who have supplied millions of wafers to the market. This industry has also increased the diameter of these wafers from 25 mm up to as large as 200 mm representing an almost two-order-of-magnitude increase in surface area available for device manufacture on each wafer. Simultaneously, these manufacturers have increased the wafer quality

to enable the creation of large power devices of 1 cm<sup>2</sup> area and above. It is expected that over the next decade the SiC will blossom into a very significant industry, with many commercial players and significant impact on future technology.

## Acknowledgments

One of the key aspects to consider when transitioning from a research environment to a development and production process is that the entire effort relies upon the skills and expertise of a large group of individuals. For this work, I am immensely grateful to the entire Cree/Wolfspeed materials team and feel that the role I played here should be considered as a scribe outlining aspects of the process that takes an R&D development and creates a commercial product out of it.

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# 3

## Homoepitaxial Growth of 4H-SiC on Vicinal Substrates

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### 3.1 Introduction

Many review papers [1–3] and text books, e.g. [4, 5]), have been published over the decades on SiC epitaxial growth and defect characterization. These publications are mirroring the great advance that has been made with regard to structural quality of substrate and epitaxial layer, epitaxial growth process, and scientific insights. This technological progress brought the focusing on *4H-SiC polytype by step-flow growth mode* on vicinal substrates with a specified off-cut using a *CVD process for SiC power electronic applications*. Still, there are ongoing activities worldwide for epitaxial growth of 3C-SiC on the silicon substrate for other applications than power electronics and solution growth of 4H-SiC, which promises an even better structural quality of the epilayer and deeper scientific insights into SiC growth in general. However, this paper is dealing with 4H-SiC homoepitaxial growth for power applications only.

This chapter about epigrowth and carrier lifetime is written for new comers in the SiC technology, draws a bow across the basic relations, and explains basic knowledge and the current state of the art. For the very details of epigrowth, readers are referred to the very comprehensive review on the SiC epitaxial process in the textbook edited by Kimoto and Cooper [5].

It summarizes briefly the fundamentals of 4H-SiC homoepitaxial growth and then focuses on the very important topics of extended defects (mainly dislocations and stacking faults) and point defects in epilayers – their origin, properties, and strategies for avoidance.

### 3.2 Fundamentals of 4H-SiC Homoepitaxy for Power Electronic Devices

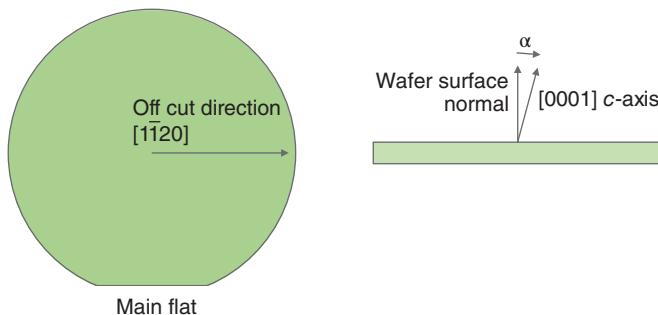
The production of today's power electronic devices demands for an 4H-SiC epilayer (stack) with specified doping concentrations and thicknesses, excellent doping and

thickness homogeneities, and (ideally) freedom of any defects grown on the Si-face of a low-resistive/highly doped 4H-SiC substrate. These aspects will be explained in the following, except the doping and thickness homogeneity, which is described in the book chapter “Industrial Perspective of SiC Epitaxy” from Al Burk.

### 3.2.1 4H-SiC Polytype Replication for Homoepitaxial Growth on Vicinal Substrates

Silicon carbide is famous for existing in various crystallographic structures with the same stoichiometry of 50 at % Si and 50 at % C, called polytypes. Under typical epitaxial growth conditions (see later in the chapter for more details), polycrystalline epilayers of 3C-SiC polytype are forming on on-axis, c-plane 4H-SiC substrates, which is an undesired heteroepitaxial growth and useless for power electronic devices. In the 1990s, Kimoto and Matsunami transferred the concept of step-flow growth mode by using vicinal (off-cut) substrates [1, 6] from other semiconductors to SiC epitaxial growth – and succeeded in a proper polytype replication from the 4H-SiC substrate to the 4H-SiC epilayer and a much more robust epitaxial growth process at lower temperatures. Initially, they used 8° off-cut substrates and got very smooth epilayers consisting mainly of micro steps with  $c/4$  step height ( $c$ : unit cell height of 4H-SiC,  $c = 1.008$  nm). As the substrates became larger in diameter and reached 3 inch diameter in 2005, the off-cut angle was reduced from 8° to 4° because of severe cost aspects in cutting out “large” tilted substrates from short on-axis grown crystals. This technological change brought drawbacks such as higher defect densities (especially stacking faults, carrots, and comets) and higher epilayer surface roughness (especially on the Si-face) due to intensified step bunching. Today, rough epilayers can be smoothened by post-epi chemo-mechanical polishing (CMP) processes, but the defect densities are still an important issue. On the other hand, the density of so-called basal-plane dislocations (BPDs) in the epilayer has been reduced dramatically by reducing the off-cut angle from 8° to 4° due to image force effects [7, 8], which is of much greater technological importance than the increased surface roughness and higher densities of other defects. The attention in epigrowth process development shifted to BPDs at that time as they were identified being the root cause of the so-called bipolar degradation, which was feared as showstopper of any bipolar SiC power electronic device including the body diode of SiC metal oxide semiconductor field-effect transistors (MOSFETs) and therefore SiC power electronic devices with blocking voltages larger than 3 kV. BPDs in the epilayer can be eliminated by using substrates with even smaller off-cut angle (such as 2° or less [7, 9]). Vicinal SiC substrates are usually off-oriented towards [1120] direction (see Figure 3.1), other off-cut directions, e.g. the [1100] direction, influence the step morphology and surface roughness [1, 10–12], but are not of technological relevance today.

Proper polytype reproduction from the 4H-SiC substrate to the growing epilayer is achieved by maintaining step-flow growth mode. This in turns means that the supersaturation on the growth terraces is kept in a reasonable range to avoid 2D seeding. The basic processes for stable step-flow growth have been described in a



**Figure 3.1** Schematic drawing of off-cut angle  $\alpha$  and off-cut direction on a vicinal 4H-SiC wafer relative to main flat. The off-cut direction coincides with the resulting step-flow direction during step-controlled epigrowth.

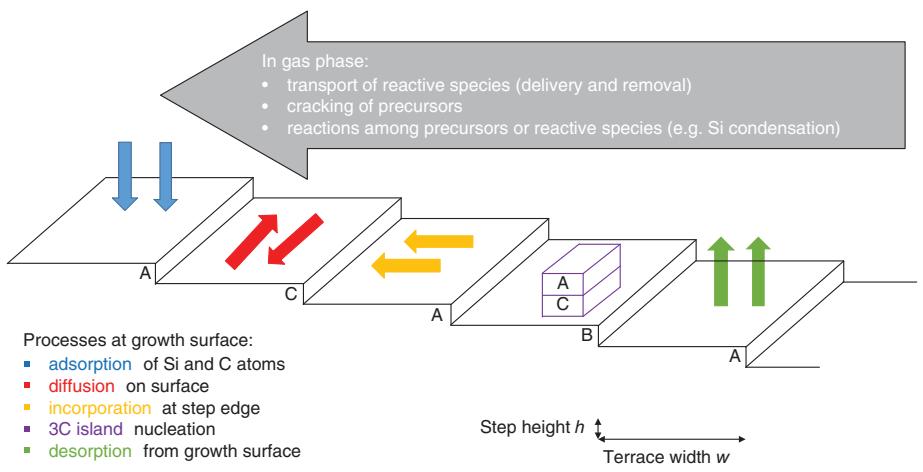
general perspective by Burton, Cabrera, and Frank (BCF model, [13]), and this BCF model has been applied to SiC epitaxy by Matsunami and Kimoto [1].

During epitaxial growth, several reactions and processes are taking place simultaneously as briefly summarized in Figure 3.2: the precursor molecules (e.g. silane  $\text{SiH}_4$  and propane  $\text{C}_3\text{H}_8$ ) are transported in the reactor to the growth zone by carrier gas (typically hydrogen [ $\text{H}_2$ ]) and start cracking to reactive species (Si and C atoms) as they reach the hot zone of the reactor. Side reactions can take place such as the condensation of Si atoms to dimers or small clusters, which is undesired as it reduces both the growth rate and the layer quality. Then, reactive Si and C atoms are adsorbed on the growth surface, diffuse on the terraces for a certain while or distance  $\lambda$ , and then incorporate at the step edge, nucleate 3C-SiC growth islands, or desorb from the growth surface. To find a suitable incorporation site, it is typically assumed that the actual diffusion length  $\lambda$  needs to be at least half of the terrace width ( $w/2$ ). The terrace width  $w$  is a simple function of the off-cut angle  $\alpha$  of the substrate and the step height  $h$ :

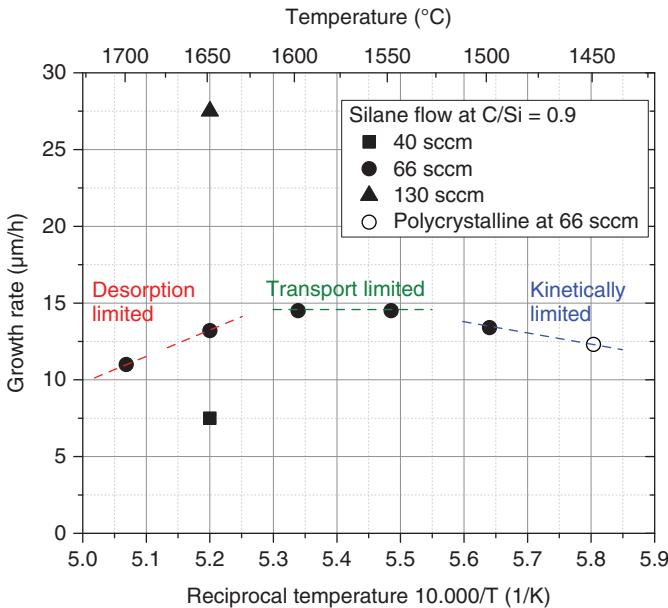
$$\tan \alpha = \frac{w}{h} \quad (3.1)$$

The diffusion length  $\lambda$  has a more complex dependence, e.g. on growth temperature, concentration of species on the terrace, chemical reactions, and ambient. If the concentrations of reactive species (either only Si atoms or both Si and C atoms) exceed a critical limit, Si droplets or SiC islands nucleate on the terraces; both are destroying the proper step-flow growth mode and degrade the epilayer quality dramatically. To avoid such nucleation on the growth terrace, either the supply with reactive species can be reduced (e.g. precursor and/or carrier gas flows, process pressure) or the growth temperature can be increased as higher temperature forces desorption of adatoms from the surface. All these basic reactions and processes have their specific temperature dependence; hence, the growth temperature is a key parameter in the growth process.

Based on the growth temperature, three different growth regimes can be determined: at low growth temperatures  $<1500^\circ\text{C}$  for 4H-SiC growth, the growth rate is kinetically limited. That means the precursor molecules provided in the process cannot be thermally decomposed completely as the temperature is too low and the



**Figure 3.2** Sketch of the BCF theory for 4H-SiC homoepitaxy on the vicinal surface.



**Figure 3.3** Epitaxial growth rate vs. reciprocal growth temperature showing different growth regimes. Polycrystalline growth occurs at very low growth temperatures below 1500 °C. Higher precursor gas flows lead to higher growth rates.

precursors are not used efficiently. As the precursor cracking becomes more efficient with increasing growth temperature, the growth rate is increasing accordingly in the kinetically limited growth regime. In a temperature window from 1500 to 1650 °C, the growth rate is transport limited. That means all precursor molecules can be cracked and contribute to the epilayer growth. Therefore, the growth rate increases proportionally to the supply of precursors (up to a certain limit at which step-flow growth turns into polycrystalline growth, see above), but is constant (for a certain precursor supply) within this temperature range. This is the desired growth regime for exact control of the growth rate and hence, the epilayer thickness. At even higher temperatures, adatoms leave the growth surface faster than they can be incorporated – or in other words: thermal back-etching competes with epilayer deposition. Therefore, the growth rate drops with increasing growth temperature within the desorption-limited growth regime (Figure 3.3).

These basics have several implications and consequences for the design of the growth step:

- Growth steps need to be present at the Si-face of the polished wafer from the very beginning of the growth phase: suitable back-etching of the off-cut substrate is required already during heat up/before growth starts.
- Growth on substrates with small off-cut angles (e.g. 4° instead of 8°): As can be seen from Eq. (3.1), the terrace width increases with decreasing off-cut angle; hence, the diffusion length of adatoms needs to become larger for smaller off-cut angles such as 4° or even 2°. That means, in turn, for growth on 4° off-cut

substrates, either the growth temperature needs to be set higher and/or the concentration of reactive species (and hence, the growth rate) has to be reduced in comparison to growth on 8° off-cut substrates.

- For step-flow growth in the transport-limited growth regime, the maximum growth rate depends on the onset of Si droplet and/or SiC island nucleation on the growth terraces, which in turn depends on the critical Si concentration. To push the maximum growth rate and hence, the maximum Si concentration to larger values, either the process pressure can be reduced and/or chloride species can be added, e.g. in terms of hydrogen chloride (HCl) or trichlorosilane (TCS,  $\text{SiHCl}_3$ ) [14]. Chloride atoms can bond even stronger to Si atoms than other Si atoms and release the Si atoms at the surface again; therefore, higher Si concentrations become tolerable without Si condensation.

The use of vicinal substrates in epitaxial growth has several implications on the epitaxial growth process:

- step-flow growth mode needs reasonable supersaturation on terraces, realized by balancing growth temperature and precursor supply for a given terrace width or off-cut angle;
- basal planes are intersecting the growth surface, and hence, defects on the basal plane are “transferrable” from substrate to epilayer.

### **3.2.2 Homoepitaxial Growth by Chemical Vapor Deposition (CVD) Process**

Based on the scientific understanding as briefly summarized in the previous section (3.2.1), a typical SiC epitaxial growth process should follow this general setup:

1. Wafer loading and conditioning of the reactor: the wafer is loaded (either manually or automated) into the reactor, and the reactor is evacuated to remove oxygen, nitrogen, and moisture residuals for low doping background and safety reasons. The wafers need to be handled carefully to avoid any scratches/damage/contamination on the wafer surface and to avoid particle generation from the sidewalls of the reactor.
2. The reactor is purged with carrier gas, typically high-purity (> 6N) hydrogen ( $\text{H}_2$ ), and starts heating up toward growth temperature.
3. During heating up in hydrogen-containing atmosphere, back-etching is taking place, which transforms the polished and smooth surface to a stepped surface and removes surface contaminations and native oxide. Back-etching can be tuned by adding C-containing precursors with regard to surface morphology (occurrence of pits and defects) and the back-etching rate [15, 16]. Depending on the reactor type, the growth process, and the substrates used, a dedicated process step for back-etching is used at growth temperature or slightly lower temperature with a specific growth atmosphere.
4. Growth step: Si- and C-precursors (e.g. silane ( $\text{SiH}_4$ ), propane ( $\text{C}_3\text{H}_8$ ), trichlorosilane ( $\text{SiHCl}_3$ )) are introduced as well as dopants ( $\text{N}_2$  for n-type doping with nitrogen, trimethylaluminum (TMA) for p-type doping with aluminium) and

any additional species such as chlorine (HCl, Cl<sub>2</sub>, and TCS), under large carrier gas flow (typically > 99% of total gas flow). Epilayer stacks are grown by adapting the dopant gas flow and/or the mixture of Si- and C-precursors.

5. Cooling down: typically in H<sub>2</sub>-containing atmosphere. Back-etching and condensation/crystallization of excess Si species may occur and can degrade the surface quality (e.g. pit formation and Si droplets) of the grown epilayer. Therefore, rapid cooling until  $T < 1400$  °C and fast removal of reactive species from the growth front are favored.
6. Wafer unload and reactor maintenance (if needed after a certain accumulated growth thickness due to parasitic Si-C compound growth on reactor components).

Growth processes are usually characterized by growth temperature and important gas-mixing ratios, such as Si concentration in carrier gas (SiH<sub>4</sub>/H<sub>2</sub>) and the precursor-mixing ratio (“C/Si”, i.e. 1/3 C<sub>3</sub>H<sub>8</sub>/SiH<sub>4</sub>), relevant for supersaturation/growth mode, growth rate, and defects, and incorporation of dopants (see below). These gas-mixing ratios are calculated for cold gases at the reactor inlet/in gas-mixing cabinet. The true gas-mixing ratios, or better concentration profiles for reactive species (elements), can only be accessed by numerical simulation of each reactor and process (needs temperature distribution, gas flows, process pressure, chemical reactions, and growth model) [14]. The process pressure is also of great importance as it distinguishes between turbulent and laminar gas flow, determines the decomposition of gaseous precursors according to the mass action law, and enters directly in the calculations of the species’ partial pressures.

### 3.2.3 Doping in Homoepitaxial Growth

Today, 4H-SiC is doped with nitrogen (N) and aluminum (Al) atoms for n-type and p-type doping, respectively. These elements have acceptable ionization energies and are technologically well controllable. As can be easily seen from the covalent radii given in Table 3.1 for the elements, N has a similar size as C and is incorporated on the C site, analogously Al on the Si site. Therefore, N competes with C about the lattice site and Al with Si. This so-called site-competition effect [18] can be used in epitaxial growth to either suppress or promote the incorporation of dopant atoms to

**Table 3.1** Properties of silicon (Si) and carbon (C) host atoms and nitrogen (N) and aluminum (Al) doping atoms.

Element	Function	Covalent radius [17] (pm)	(preferred) Incorporation site	Ionization energy
C	Host atom	77		n.a.
N	Donor	70	On C site	35–100 meV
Al	Acceptor	125	On Si site	190–240 meV
Si	Host atom	117	—	n.a.

the growing layer – simply by providing more or less C- or Si-precursor in the growth step. Suppressing the incorporation of a dopant means that the doping background can be kept very low and promoting can help to grow highly doped epilayers.

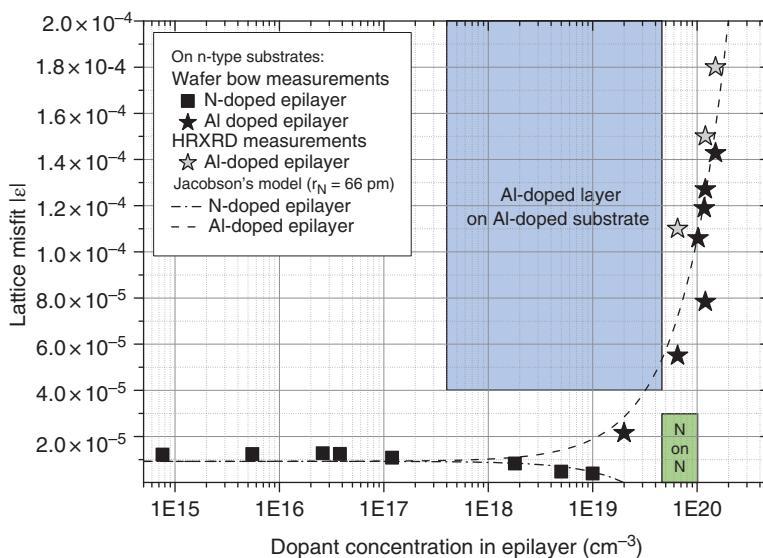
Moreover, Al has a so-called memory effect. Once a highly Al-doped epilayer was grown in the epi reactor, Al remains in the parasitic SiC deposition on the reactor parts and emits continuously Al atoms during the subsequent growth processes. Consequently, the Al doping concentration in the subsequent growth runs is higher than that expected from the relevant gas-mixing ratios (Al/Si, C/Si). This memory effect can be reduced or suppressed by mechanical cleaning of the reactor parts and deposition of undoped SiC – or by a chemical cleaning process with chloride-containing precursors at elevated temperatures, such as HCl etching. Some (older) reactor types provide dedicated chambers for n- and p-type doping, but – in combination with cleaning of reactor parts – it can be sufficient to use dedicated n- or p-type reactor kits for the growth chamber.

As mentioned at the beginning of the chapter, SiC homoepitaxial layers are grown on low-resistive, highly N-doped 4H-SiC substrates. Nitrogen doping leads – as the covalent radius of N is smaller than that of C [17, 19] – to a contraction of the SiC unit cell. High N dopant concentrations (as for substrates) lead to a stronger contraction of the unit cell than moderate or low N concentrations (as for epilayers). Therefore, highly N-doped SiC substrates have the smallest unit cell (volume), followed by moderate or low N-doped epilayers. Contrarily, Al incorporation leads to a dilation of the SiC unit cell as Al has the larger covalent radius than the substituted Si atom [17, 19]. Additional size effects might occur due to electronic effects [20], but they seem to be negligible compared to the atomic size effect for 4H-SiC. The unit cell volume V follows the general doping rule:

$$V_{\text{highly N-doped}} < V_{\text{moderate N-doped}} < V_{\text{undoped}} < V_{\text{moderate Al-doped}} < V_{\text{highly Al-doped}}$$

Several working groups worldwide have been already dealing with doping-induced crystal lattice misfit. It is challenging to measure and determine the small values of doping-induced misfit, and classical as well as innovative attempts have been made: reciprocal space maps obtained by high-resolution X-ray diffraction and high-precision lattice constant determination [20–22], wafer bow measurements on epilayers grown on thin substrates [19], and theoretical models [21, 23]. The reported misfit values are summarized in Figure 3.4.

Therefore, any combination of highly N-doped substrate and epilayer with different N or Al doping concentration has different lattice constants and hence, a doping-induced lattice misfit. Of course, the misfit is very small in the order of  $10^{-5}$  to  $10^{-6}$  (especially if compared to heteroepitaxy), but relatively thick epilayer (stacks) is grown in the SiC technology: 10 µm epilayer thickness on 350 µm substrate (thickness ratio 1 : 35 for 1200 V devices) up to 65 µm epilayer on 350 µm substrate (~1 : 5 for 6.5 kV devices). For simple comparison, in GaN-on-Si heteroepitaxy, a <5 µm thick GaN layer is grown on a stress management layer stack on a 750 µm thick Si substrate (1 : 150). Therefore, wafer bowing occurs in



**Figure 3.4** Summary of reported doping-induced misfit values as a function of epilayer doping concentration. Misfit data for N- and Al-doped epilayers grown on N-doped substrates taken from [19, 21] and for Al-doped epilayers grown on Al-doped substrates from [22].

4H-SiC homoepitaxial growth, but even misfit dislocation generation is possible for large misfits (abrupt doping gradients) in combination with thick layers. It can be shown that – in case of misfit dislocation generation – BPDs are generated as they have the appropriate configuration (line direction, Burgers vector direction) to reduce the strain energy at the substrate–epilayer interface (if critical shear stress at the respective epi growth temperature is exceeded). The classical models about the onset of misfit dislocation generation by Matthews–Blakeslee [24, 25] and People–Bean [26] predict different critical values for the epilayer thickness/doping difference and need to be adapted and reproven.

### 3.3 Extended Defects in Homoepitaxial Layers

This section deals with extended defects in the 4H-SiC substrate and homoepitaxially grown material, i.e. dislocations, stacking faults, and complexes thereof. These types of defects range from microscopic to macroscopic level and are relevant for device performance and device production yield. First, extended defects are classified, i.e. which defect types can occur in the hexagonal lattice of 4H-SiC, followed by an introduction which defect types do occur under real conditions. Their origins will be discussed as well as their behavior during homoepitaxial growth because these two factors often determine the actual morphology of the defects. Finally, common characterization techniques for extended defects in epilayers are briefly introduced.

### 3.3.1 Classification of Extended Defects According to Glide Systems in 4H-SiC

Dislocations have a specific Burgers ( $\vec{b}$ ) and line ( $\vec{l}$ ) vector, which represent the distance and direction of displacement ( $\vec{b}$ ) and the orientation ( $\vec{l}$ ) of the actual disturbance, respectively. Due to energetic reasons, the Burgers vector needs to be a closely packed direction and the glide plane (which contains the line vector) a closely packed plane. Hence, discrete glide systems occur in crystal structures, and dislocations cannot form with “random” configuration. From a theoretical perspective [27], six different glide systems are possible in a hexagonal lattice (with stacking sequence AB). These glide systems need to be adapted to the actual stacking sequence ABAC of 4H-SiC, resulting in the six independent glide systems as summarized in Table 3.2.

**Table 3.2** Glide systems in hexagonal lattice (as given in textbook from Hull and Bacon [27] for stacking sequence AB) adapted to the 4H stacking sequence of 4H-SiC. BPD, basal-plane dislocation; TED, threading edge dislocation; TSD, threading screw dislocation; TMD, threading mixed dislocation.

Type	$a$	$c$	$\sqrt{c^2 + a^2}$	$a/\sqrt{3}$	$c/4$	$\sqrt{\frac{a^2}{3} + \frac{c^2}{16}}$
$\vec{b}$	$\frac{1}{3}\langle 11\bar{2}0 \rangle$	$\langle 0001 \rangle$	$\frac{1}{3}\langle 11\bar{2}3 \rangle$	$\frac{1}{3}\langle 1\bar{1}00 \rangle$	$\frac{1}{4}\langle 0001 \rangle$	$\frac{1}{6}\langle \bar{2}203 \rangle$
$ b $	0.308 nm	1.008 nm	1.054 nm	0.178 nm	0.252 nm	0.308 nm
Glide plane	$\langle 0001 \rangle$ $\{1\bar{1}00\}$ $\{1\bar{1}00\} \{1\bar{1}01\}$	$\{1\bar{1}00\}$	$\{\bar{1}100\}$ $\{\bar{1}112\}$	$\langle 0001 \rangle$	$\{1\bar{1}00\}$	$\{\bar{2}112\}$
Examples	BPD, TED	TSD, MP	TMD	Shockley partial	Frank partial	

There are two closely packed directions and hence, Burgers vectors, in the hexagonal lattice, called  $a$  and  $c$ , and their combination  $\sqrt{c^2 + a^2}$ . Additionally, partial dislocations can occur with Burgers vectors of types  $a/\sqrt{3}$  and  $c/4$  and their combination  $\sqrt{\frac{a^2}{3} + \frac{c^2}{16}}$ . Partial dislocations always surround stacking faults, i.e. planar defects.

Dislocations with  $a$ -type Burgers vector have prominent representatives such as the before-mentioned BPDs and threading edge dislocations (TEDs). BPDs are lying on the basal plane (0001) and can occur in edge, screw, or mixed configuration. TEDs have a distinct line direction of [0001]; hence, they are in edge configuration, and their line vector is part of the prismatic m-plane {1100}. Dislocations with  $c$ -type Burgers vector mainly occur with the dislocation line along [0001] direction, i.e. they are in screw configuration and called threading screw dislocation (TSD). Threading mixed dislocations (TMDs), i.e. with line direction [0001] but mixed ( $a + c$ )-Burgers vector, have been reported recently [28, 29], but occur quite seldom.

Shockley partial dislocations with a Burgers vector of type  $\vec{b} = a/\sqrt{3}$  always surround a stacking fault; the latter ones are often called Shockley stacking faults (SSF) in the SiC terminology. A certain subtype (those with Si core) of these partial dislocations is mobile and the leading actor of the so-called bipolar degradation [30]. Analogously, Frank partials with Burgers vectors of type  $\vec{b} = c/4$  border Frank

stacking faults (FSF). Frank partials and hence, FSF, are sessile and cannot grow during device operation etc. The SiC-specific “carrot” defect is a certain combination of FSF and SSF [31, 32]. Representatives of the sixth glide system  $\sqrt{\frac{a^2}{3} + \frac{c^2}{16}}$  have been reported by Mike Dudley’s group [33]. This fault can be generated by macrostep overgrowth of a TSD.

### 3.3.2 Dislocation Reactions During Epitaxial Growth

Dislocations cannot simply end inside a crystal volume, as their distortion energy needs to be conserved. Hence, all dislocations present at the surface of the substrate need to proceed somehow during epitaxial growth. Today, commercially available 4H-SiC substrate contain BPDs, TEDs, TSDs, TMDs, but hardly any micropipes. As the dislocation density of substrates depends on multiple factors, such as the grade of the substrate quality and the substrate vendor, and has been continuously reduced over the years, it is very difficult to provide exact numbers, but the following data can be taken as a rough indication: TSDs occur usually with a density of  $10^2$  to low  $10^3/\text{cm}^2$ , TEDs with low  $10^4/\text{cm}^2$  and BPDs with  $10^2$  to low  $10^3/\text{cm}^2$ . During epitaxial growth, beside the propagation of dislocations without any change to the dislocation line or Burgers vector, several dislocation reactions can take place at the growth surface. All these dislocation reactions can only take place if the total energy can be minimized by the dislocation reaction (driving force) and if a critical stress level is exceeded. The following dislocation reactions can occur:

- change of the dislocation line direction (while keeping the Burgers vector), e.g. the *conversion* of BPDs to TEDs,
- splitting of the Burgers vector from perfect to partial type (and vice versa), known as *stacking fault generation* (or annihilation),
- the *recombination* of two dislocations, such as the formation of superscrew dislocations or micropipes with  $n*c$  Burgers vectors or the recombination of a TED and TSD to a mixed type dislocation with Burgers vector  $\sqrt{c^2 + a^2}$ ,
- the *annihilation* of two dislocations with similar Burgers vectors, but different sign,
- the *generation of misfit dislocations* due to (local) lattice strain.
- Multiplication of existing dislocations due to high local strain (local dislocation source e.g. Frank–Read type).

In case of *dislocation propagation* during homoepitaxial growth, the dislocation goes on straightforward without any change to its line or Burgers vector. Typically, all kinds of threading dislocations (TEDs, TSDs, and TMDs) propagate as they cannot further minimize their dislocation line energy during growth. Some of the BPDs, usually < 5% of the substrate BPDs, propagate as well. It has been discussed that the line vector of the propagating BPDs is parallel to the step-flow direction [7, 8, 34]. Most of the BPDs, typically more than 95%, from the substrate *convert* to TEDs during epitaxial growth within the first grown micrometers. The propagation and conversion of dislocations can be described adequately by the model of Klapper [7, 8, 35], which is based on the idea of image forces acting on dislocations close to

the growth surface. This model was first invented for bulk crystal growth [35] and has been applied successfully to epitaxial growth of other semiconductors, such as GaN [36]. In case of propagation and conversion of dislocations, the dislocation density (in terms of intersection points on a certain surface area, given in  $\text{cm}^{-2}$ ) remains unchanged.

*Stacking faults* can either propagate from the substrate to the epilayer – analogously to dislocations – or be generated by dislocations: an a-type Burgers vector, i.e. as for BPDs and TEDs, can split into Shockley partials, and a c-type Burgers vector, as for TSDs, can split into Frank partials. This stacking fault generation is energetically possible and favorable in SiC due to its low stacking fault energy [37]. Other semiconductor materials have a much higher stacking fault energy and thus a much weaker tendency to form any stacking faults.

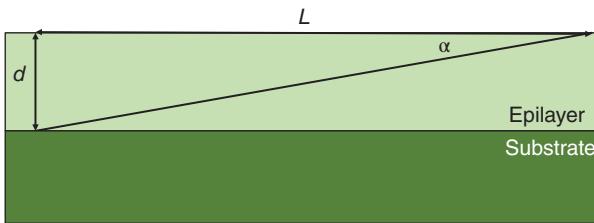
*Generation of misfit dislocations and multiplication of dislocations* happen if a critical strain level is exceeded (locally), due to doping-induced lattice misfit or interactions of dislocations with growth steps, such as pinning. Dislocations generated by such mechanisms are of a distinct type and geometric arrangement: misfit dislocations in 4H-SiC epilayers are BPDs lying at the substrate–epilayer interface, or the so-called TED half loop arrays [38, 39] are generated by pinned BPDs, which are acting as Frank–Read sources. Such dislocation generation mechanisms do not necessarily lead to a higher dislocation density at the wafer surface (in terms of dislocation intersection points on a certain surface area), but increase the total length of dislocations inside a crystal volume (also given in  $\text{cm}/\text{cm}^3 = \text{cm}^{-2}!$ ).

The *annihilation*, i.e. the recombination of 2 TSDs with c-type Burgers vectors of different sign, and/or the *combination of dislocations*, i.e. TED and TSD combine to a TMD, is possible in SiC, but very unlikely. The two involved dislocations need to be within an interaction distance, which can be estimated based on the Peierls barrier (as lattice resistance against dislocation movement) [40] and Peach–Köhler force (interaction force between two dislocations) [27, 41] and is in the order of single micrometers [42]. For comparison: for a typical dislocation density of  $1 \times 10^4 \text{ cm}^{-2}$ , the average distance between two dislocations amounts to  $100 \mu\text{m}$ , which is much too far for any interaction of dislocations.

The types of defects lying on the (0001) basal plane of SiC, such as BPDs, SSF, carrots, can “grow” very large due to the substrate’s off-cut. There is a simple geometric relation between the depth ( $d$ ), at which the defect starts growing, its projected length ( $L$ ) and the wafer off-cut angle  $\alpha$ :

$$d = L \cdot \tan \alpha \quad (3.2)$$

This relation implies that defects on the basal plane become larger, the thicker the epilayer grows and can be used to analyze the origin of defects within epilayers, i.e. if the defect was generated at the substrate–epilayer interface or during epitaxial growth (see Figure 3.5). Hence, the defect density can be minimized by tuning the back-etching and initial epigrowth conditions or by changing epitaxial growth conditions.



**Figure 3.5** Schematic drawing for illustrating the relationship between depth ( $d$ ) of defect nucleation on the basal plane and its projected length ( $L$ ) for a certain off-cut angle  $\alpha$  of the wafer. Source: Kallinger et al. [19].

### 3.3.3 Characterization Methods for Extended Defects in 4H-SiC Epilayers

Among a broad spectrum of characterization methods for extended defects in 4H-SiC, there are three methods of great importance and commonly used: defect-selective etching (DSE), X-ray topography (XRT), and UV-excited photoluminescence (UVPL) imaging. They are briefly introduced in this section.

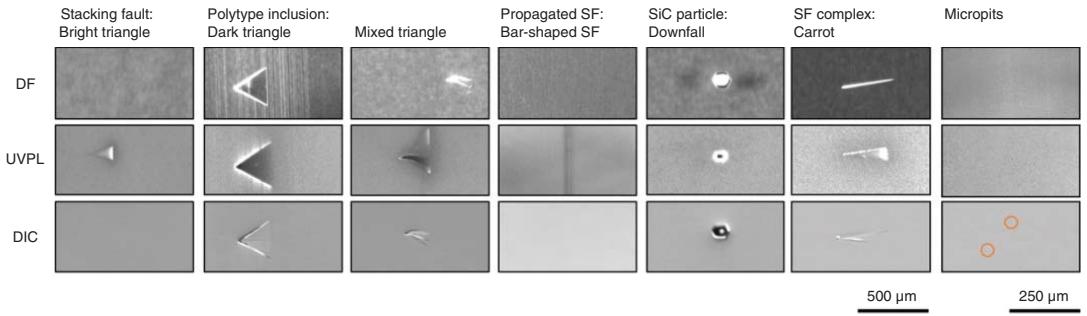
DSE is a simple, robust, and well-established method for the determination of the dislocation density and distribution on a 4H-SiC wafer. It has been used since the beginning of 4H-SiC commercialization. The intersection points of dislocations on the (Si-face of the) wafer surface are more strongly attacked by a chemical etchant than the undisturbed wafer area between these intersection points. Hence, etch pits are forming at these intersection points of dislocations. It is commonly expected that the size and shape of the etch pits are characteristics for the dislocation type due to the size and form of the dislocation strain field, which again goes back to the Burgers vector and type of the dislocation [3]. Hence, oval-shaped etch pits are expected for BPDs and small and large hexagonally shaped etch pits for TEDs and TSDs, respectively. This expectation holds for 4H-SiC with moderate N doping, Al doping, and undoped materials [43]. For highly N-doped material like low-resistive substrates, this classification for TEDs and TSDs is not true if etched with the standard etchant, molten potassium hydroxide (KOH). It has been reported that the selectivity of the etching process can be improved by adding  $\text{Na}_2\text{O}_2$  to KOH (KN etching) [44] instead of pure KOH melt. Nevertheless, the density and lateral distribution of BPDs and all threading dislocations (TEDs + TSDs + TMDs) as well as micropipes (if present) can be determined routinely. The etching process of wafers (substrates as well as epi-wafers), image recording of the etched surface, and image analysis with regard to etch pit densities can be automated and is a cost-effective, reliable method. But, it is a destructive method as it destroys the wafer surface and it can only reveal defects intersecting the wafer surface.

XRT is based on the diffraction imaging of X-rays at crystal (defects) and is able to identify the dislocations including their Burgers and line vectors. Moreover, it is a nondestructive method and needs no special sample preparation despite of good surface quality. However, for long time, XRT had to be done at synchrotron facilities to record images with good contrast in reasonable time. Generally, defect

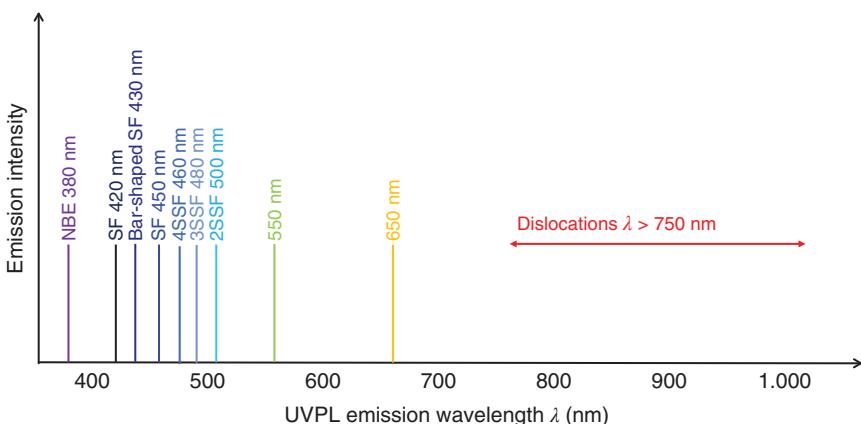
identification, as well as Burgers vector analysis by XRT, needs images from different diffraction reflexes, which need to be compared and analyzed in detail. These conditions were time-consuming and expensive; hence, it was a method only for scientific studies of dislocation types, dislocation reactions, and stacking faults inside the wafer (or bulk crystal). Today, XRT studies can be done with lab tools with micro-focus X-ray tubes, high-resolution charge-coupled device (CCD) cameras, facilitating the access to XRT images and bringing down the time for image recording. For example, a 150 mm wafer can be scanned within two hours with an image resolution sufficient for dislocation analysis, like TSD counting based on the symmetric 0008 reflex. XRT can image and identify dislocations, stacking faults, and complexes thereof such as carrots, giving the possibility to generate expected yield maps for devices based on these killing defects. Still, the determination of the dislocation type and their densities by automated image analysis is very demanding.

In the last decade, UVPL imaging has been developed to a methodologically sound and fully automated method, which can provide data on density and distribution of stacking faults, defect complexes, and particles across the epiwafer without sample preparation or damage. Current systems like the Lasertec SICA or the Intego AQUILA can scan a 150 mm wafer and deduce the defect density and distribution within a few minutes. Hence, these systems can be used as inline monitoring systems for quality control and improvement of epilayers and epitaxial growth. However, UVPL imaging cannot provide reasonable data for threading dislocation (TEDs and TSDs) densities and distributions, only for BPDs, and can hardly image defects in highly N-doped substrates. In UVPL imaging, the 4H-SiC material is excited with a wavelength in the UV range (typically 305, 313, 340, or 365 nm) and the emitted photoluminescence (PL) signal is recorded by a CCD camera in imaging mode (not in spectral resolution). As 4H-SiC is a semiconductor with an indirect band gap, the defect-free material remains quite dark (it has a very small probability to emit near band edge radiation, and hence, the SiC background in the pictures is not completely black, but gray). On this dark background, some defects are actively emitting light and, hence, appear as bright features with a specific emission wavelength, size, and shape. Still, the defects have a large variance in appearance and that complicates the automated defect detection. Examples for typical defects in epiwafers are summarized in Figure 3.6, for the UVPL channel as well as for surface sensitive channels as dark field (DF) and differential interference contrast (DIC) imaging.

Moreover, there is no common, standardized classification of defects available yet for the different measurement systems and SiC suppliers worldwide. Defects are often named according to their appearance, e.g. dark or bright triangles, but this naming is purely phenomenological, since the appearance of defects is determined by the measurement conditions. Some attempts of standardization have been done, e.g. SEMI standards [45] or the Japanese standard from JEITA [46], but they are not yet commonly applied. Therefore, it remains difficult to translate defect densities from one system or wafer supplier to another. The basic UVPL imaging method is not spectrally resolved, but the systems offer the opportunity to insert optical filters to collect UVPL emission in a specific wavelength range, such as near-infrared (NIR, suitable for dislocations), visible spectrum (VIS, for stacking faults), or near band



**Figure 3.6** Examples for typical epilayer defects: appearance in dark field (DF), UVPL imaging, and differential interference contrast (DIC) mode. Pictures recorded with an Intego AQUILA at Fraunhofer IISB. DF, dark field; UVPL, UV-excited photoluminescence; DIC, differential interference contrast; SF, stacking fault.



**Figure 3.7** Summary of room-temperature luminescence data from stacking faults (SF) after UV excitation according to [9, 37, 47–50]: near band edge emission (NBE), double Shockley stacking fault (2SSF), triple Shockley stacking fault (3SSF), and quadrupole Shockley stacking fault (4SSF).

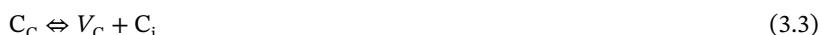
edge emission (NBE). A comprehensive overview to reported emission wavelengths of defects is given in Figure 3.7.

Besides these difficulties in defect classification and counting, UVPL imaging has become the standard characterization method for extended defects in epiwafers and it can be used for estimating the device production yield for a certain device type on a certain wafer and allows for inking out defective devices.

## 3.4 Point Defects and Carrier Lifetime in Epilayers

### 3.4.1 Classification and General Properties of Point Defects in 4H-SiC

Point defects are 0-dimensional defects in the crystal lattice and classified into intrinsic and extrinsic point defects. **Intrinsic defects** are “misaligned” host atoms, i.e. Si and C atoms, which are either missing on their regular lattice sites (“vacancies”) or placed on an interstitial site (“interstitials”). There are four basic intrinsic point defects, such as Si and C vacancy ( $V_{Si}$  and  $V_C$ ) as well as Si and C interstitials ( $Si_i$  and  $C_i$ ). They can occur as single defects or as complexes, such as  $V_{Si}C_i$ . In a compound semiconductor like SiC, antisite defects like  $Si_C C_{Si}$  can occur. Intrinsic point defects have various origins: They have a thermodynamical probability of formation (at the high growth temperature and quenched during fast cool down), but they can also form during nonequilibrium processes like irradiation with ions, electrons, high-energetic photons, and particles. Point defect annihilation during thermal annealing can be considered as back reaction of the so-called Frenkel pair formation reaction:



A Frenkel pair is generated when a C (or Si) atom is leaving its regular lattice site ( $C_C$ ) and therefore, generating a C (or Si) vacancy and a C (or Si) interstitial simultaneously and in close distance. The C vacancy is sessile, whereas the C interstitial is quite mobile. As the formation of a Frenkel pair is taking place at elevated temperatures, the C interstitial is diffusing away; therefore, the Frenkel pair is not stable and cannot easily recombine (i.e. annihilate). The mobile C interstitials might diffuse to other defects, e.g. other point or extended defects, and agglomerate there or vanish if they reach a crystal surface. Hence, the originally stoichiometric concentration of  $V_C : C_i = 1 : 1$  is not necessarily conserved, but changes to an excess of C vacancies in the material volume. This is the challenge of point defect annealing: bringing the reaction partners back together, which will be discussed later in this section.

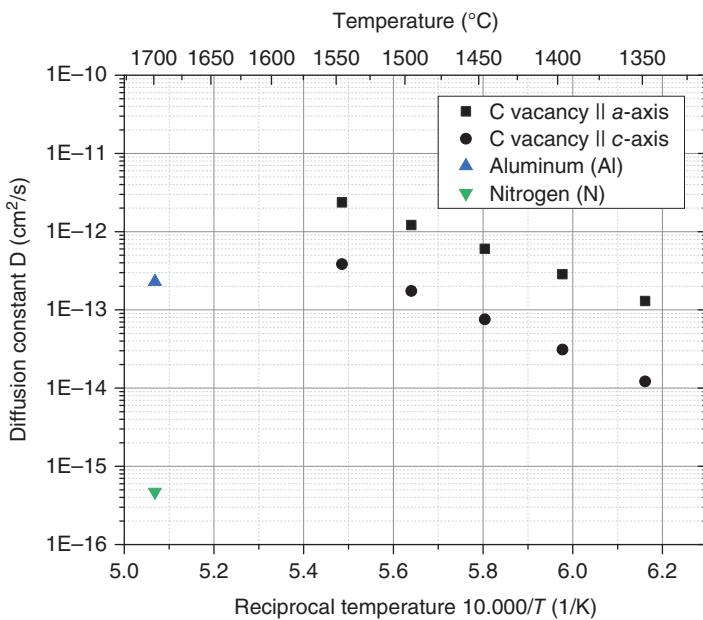
To make a complex process like the Frenkel pair generation more simple, Eq. (3.4) shows the Arrhenius-type equation for C vacancy formation – although we already know that a *pair* of C vacancy and interstitial is formed:

$$[V_C] = N_C \cdot \exp\left(\frac{S_F}{k}\right) \cdot \exp\left(\frac{-H_F}{kT}\right) \quad (3.4)$$

The concentration of C vacancies  $[V_C]$  and regular C lattice sites  $N_C$ , the formation entropy  $S_F$ , the formation enthalpy  $H_F$  and the absolute temperature  $T$  enter Eq. (3.4). As the formation entropy of point defects is usually not known, a value of  $5k_B$  is a reasonable assumption for further calculations [51, 52]. The formation enthalpy for a Si vacancy (8 eV) is much larger than that of a C vacancy (5 eV, [51]); hence, in any processes at elevated temperature such as epitaxial or bulk growth or thermal annealing, much more C vacancies are generated than Si vacancies.

Besides the intrinsic point defects, **extrinsic point defects** are present in SiC material such as dopant atoms, which are intentionally incorporated, or impurity atoms (unintentional incorporation). Extrinsic defects can either substitute host atoms (like for doping) or incorporate on interstitial sites, if the impurity's covalent radius does not fit to those of the host atoms. Extrinsic point defects have extremely low diffusion constants in 4H-SiC (as shown in Figure 3.8) and are, hence, quite sessile. Consequently, the growth conditions, especially the purity of the growth environment in bulk and epitaxial growth, are decisive for the concentration of extrinsic point defects in SiC substrates and epilayers.

Point defects can be charged with electrons and/or holes and, therefore, show (several) steps of charging. Some have acceptor-like character if they trap an additional electron and become negatively charged; others have a donor-like character. This charging and de-charging of defects under defined external conditions (temperature, voltage, ...) can be used for defect characterization – either by electrical methods such as deep level transient spectroscopy (DLTS) or optical methods like (deep temperature) PL spectroscopy. Magnetic properties of point defects can be investigated by means of electronic spin resonance (ESR) and similar methods. As this chapter is dedicated to the relationship between point defects and carrier lifetime in epitaxially grown material, hence, it is focused on the electrical properties (i.e. energetic level and capture cross section) of point defects, which are usually determined by DLTS measurements.



**Figure 3.8** Diffusion constants for carbon vacancies (parallel to  $a$ - and  $c$ -axis) [53], N donor [54], and Al acceptor [55].

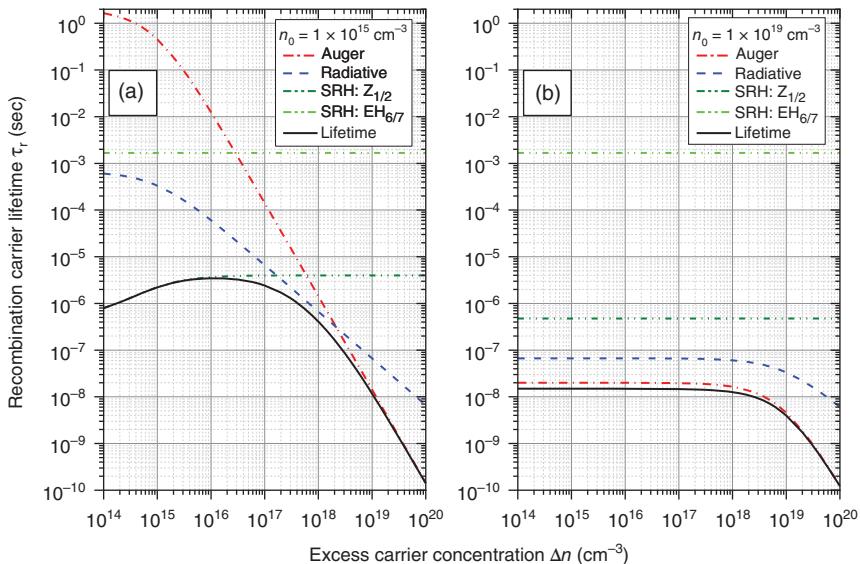
### 3.4.2 Basics on Recombination Carrier Lifetime in 4H-SiC

There are three recombination processes in semiconductors, called Auger, radiative, and Shockley–Read–Hall (SRH) recombination [56]. Auger recombination takes place under high injection conditions and at high doping concentrations, whereas radiative recombination is dominant at low doping and moderate injection conditions. SRH recombination is a model describing the recombination processes at point defects, and it includes both radiative and non-radiative recombination processes at the point defects. As all these basic recombination processes (and multiple point defects in SRH recombination) concur, the overall reciprocal recombination carrier lifetime is the sum of all reciprocal lifetimes:

$$\frac{1}{\tau_{\text{SiC}}} = \frac{1}{\tau_{\text{Auger}}} + \frac{1}{\tau_{\text{rad}}} + \frac{1}{\tau_{\text{SRH}}} \quad (3.5)$$

The physical nature of these recombination processes is explained in textbooks, e.g. Schroder [56] or review papers [57]. Figure 3.9 shows exemplarily the overall recombination carrier lifetime as well as Auger, radiative, and SRH lifetimes calculated for 4H-SiC substrates and epilayers.

For the calculation of the recombination lifetimes shown in Figure 3.9, basic equations given in the textbook from Schroder [56] have been used together with recombination coefficients for Auger [58] and radiative [59] recombination, as well as the capture cross sections and energetic levels of the carbon vacancy and its typical point defect concentrations of  $10^{12}\text{--}10^{13} \text{ cm}^{-3}$ . The C vacancy is represented by the  $Z_{1/2}$  and  $\text{EH}_{6/7}$  defects, which are the electronic signatures of



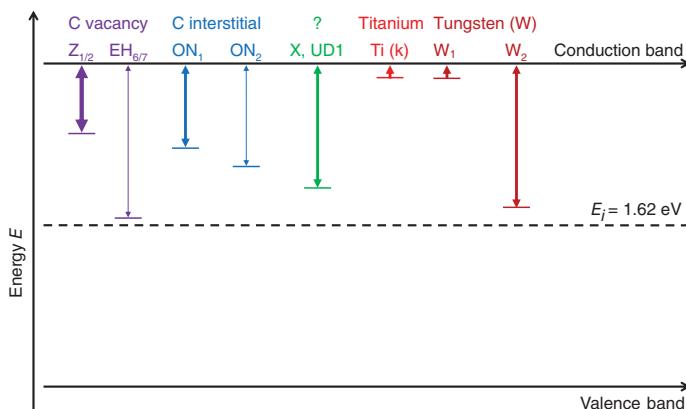
**Figure 3.9** Calculated recombination carrier lifetime in a typical low N-doped epilayer (a, doping concentration  $n_0 = 1 \times 10^{15} \text{ cm}^{-3}$ ) and a highly N-doped substrate (b, doping concentration  $n_0 = 1 \times 10^{19} \text{ cm}^{-3}$ ) as a function of excess carrier concentration. A trap concentration  $N_T = 5 \times 10^{12} \text{ cm}^{-3}$  is assumed for  $Z_{1/2}$  and  $EH_{6/7}$ .

$V_C$  in DLTS measurements [60, 61]. In case of a low doped epilayer (Figure 3.9a), the SRH-lifetime obtained for the  $Z_{1/2}$  defect is the shortest and therefore, limiting carrier lifetime for low to moderate carrier injection. As the carrier injection becomes larger than approximately  $1 \times 10^{17} \text{ cm}^{-3}$ , radiative recombination comes into play, but Auger recombination becomes the dominant recombination process for injected carrier concentrations larger than  $2 \times 10^{18} \text{ cm}^{-3}$ . As such high injection conditions are typically found in forward operation of bipolar devices, point defects are not the limiting factor for poor lifetimes in forward operation, but the intrinsic recombination processes, Auger and radiative recombination. N-type substrates have very short carrier lifetimes due to their high doping concentration as can be seen from Figure 3.9b and their overall lifetime value is dominated by Auger recombination for all magnitudes of carrier injection.

### 3.4.3 Carrier Lifetime-Affecting Point Defects

Auger and radiative recombination are intrinsic properties of the SiC material, which cannot be tuned or improved by material development, but point defects, which determine the SRH lifetime, can be controlled in epitaxial growth and post-epi processes. This section deals with the current state of the art and knowledge.

The impact of point defects on the SRH lifetime is characterized by their capture cross sections for electrons ( $\sigma_n$ ) and holes ( $\sigma_p$ ) as well as their trap energy ( $E_T$ ) and naturally their defect concentration. Lifetime-affecting point defects have a large trap energy, i.e. are close to the mid of the band gap, and have both large capture



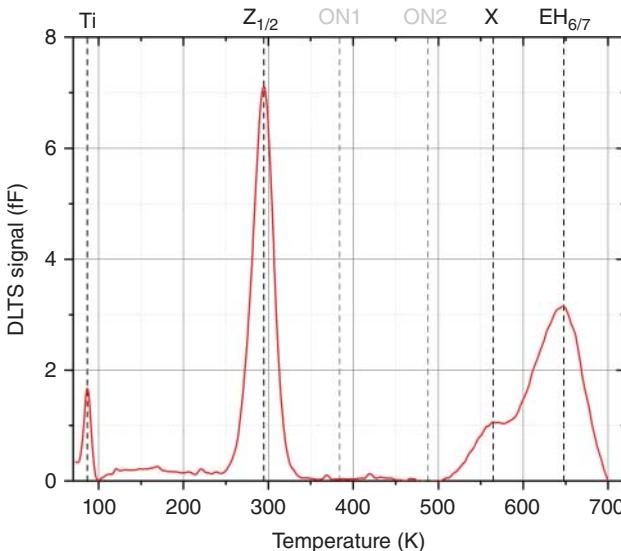
**Figure 3.10** Trap energies and capture cross sections of intrinsic and extrinsic point defects in n-type 4H-SiC. Thicker arrows indicate larger capture cross sections; thinner arrows smaller capture cross sections.

cross sections for electrons and holes. For example,  $Z_{1/2}$  has a smaller trap energy, but larger capture cross sections for electrons and holes than  $\text{EH}_{6/7}$ , and therefore, causes a much shorter SRH lifetime (for the same trap concentration) as can be seen from Figure 3.9. It has been shown by several work groups that both  $Z_{1/2}$  and  $\text{EH}_{6/7}$  are signatures of the C vacancy in 4H-SiC [60, 61].

Figure 3.10 summarizes the trap energies and capture cross sections of technologically relevant intrinsic and extrinsic point defects in n-type 4H-SiC, which have been discussed recently in relation to carrier lifetime. More detailed information about electronic properties of point defects can be found in the book chapter “Intrinsic and Extrinsic Electrically Active Point Defects in SiC” from Ulrike Grossner.

In highly N-doped 4H-SiC substrates, the Auger and radiative recombination are the dominant recombination processes, resulting in very short carrier lifetimes of nanoseconds or tens of nanoseconds. Besides the high doping concentration, considerable concentrations of intrinsic and extrinsic point defects might be present in the substrate material. Intrinsic defects, e.g. C and Si vacancies are generated due to high growth temperatures  $> 2000^\circ\text{C}$  in bulk crystal growth and their thermodynamical probability of formation. Extrinsic defects such as tungsten (W) [62, 63] and titanium (Ti) [64] can be incorporated at high growth temperatures from graphite parts and typically originate in the SiC seed powder. However, these point defects play a minor part in lifetime considerations of the substrates.

On these substrates, epilayers are deposited typically at epigrowth temperatures around  $1600^\circ\text{C}$  from highly pure precursors. Therefore, extrinsic defects are quite unlikely being incorporated or at very low concentrations. Intrinsic defects can be formed, and the concentration of the C vacancy is expected to be larger than that of the Si vacancy due to their different formation enthalpies. It has been shown that the concentration of C vacancies (in terms of  $Z_{1/2}$  defect measured by DLTS) follows the growth temperature, which fits to the general thermodynamic model [65, 66]. Additionally, if the epigrowth is performed in deficiency of C, e.g. at small C/Si ratios,



**Figure 3.11** Typical DLTS spectrum for an as-grown n-type epilayer. Common point defect signatures are indicated by broken vertical lines in the spectrum, such as Titanium,  $Z_{1/2}$ , X, and  $EH_{6/7}$ . Commonly observed peaks like the ON1 and ON2, which are absent in this sample, are indicated by gray broken lines.

even more C vacancies are present. Conclusively, the concentration of C vacancies or,  $Z_{1/2}$  in DLTS measurements can be controlled by the epitaxial growth parameters temperature and C/Si ratio. In epigrowth, the  $Z_{1/2}$  concentrations can be reduced to  $2 \times 10^{12} \text{ cm}^{-3}$  [65–67], corresponding to a SRH lifetime of  $10 \mu\text{s}$ . For proper current modulation in bipolar devices, such a SRH lifetime is still too short and needs further optimization, e.g. by post-epi processes.

Besides the lifetime-limiting  $Z_{1/2}$  defect and the  $EH_{6/7}$  defect, titanium (Ti) and the so-called X defect are commonly observed in DLTS spectra of as-grown epilayers (as shown in Figure 3.11). Ti is a very common impurity in SiC epilayers, although its origin is not really clear. It has one peak in DLTS spectra at  $\sim 80 \text{ K}$ . The UT1 [68] or X defect [69] occurs only in epilayers grown on n-type substrates from a few vendors, suggesting a relation to a substrate property. It is characterized by a single peak in DLTS spectra around  $560 \text{ K}$  and is a lifetime-affecting defect in n-type 4H-SiC. A recent study [70] indicates that it might be an extrinsic impurity in the substrate, which agglomerates on the growth surface during back-etching at the beginning of epitaxial growth and is incorporated into the growing epilayer with a specific segregation coefficient. Currently, this thesis needs more experimental and theoretical proofs and publication.

In post-epi lifetime engineering, the basic idea is to insert excess C atoms to annihilate the C vacancies. This can be realized by thermal oxidation of the epilayer [71, 72], annealing [51], and ion implantation [73]. Thermal oxidation consumes the Si atoms of SiC for the formation of the silicon oxide, whereas the C atoms leave the material as long as they can diffuse through the thin oxide layer. As the oxide is growing

thicker, the C atoms can hardly leave anymore, but enrich at the oxide–epilayer interface as C interstitials or C clusters [74]. In case of ion-implanted N atoms (as well as other C substituting elements) and subsequent annealing, N displaces C atoms from their regular lattices sites and hence, generates C interstitials. Both thermal oxidation and ion implantation insert excess C atoms, i.e. C interstitials, close to the epilayer surface and these C interstitials need to diffuse into the epilayer to recombine with C vacancies. Hence, the resulting  $Z_{1/2}$  concentration profile is increasing with increasing depth in the epilayer. Annealing of the samples is another alternative for minimizing the C vacancy concentration and hence, the carrier lifetime, in as-grown epilayers. Due to the thermodynamics of Frenkel pairs, a post-epi annealing process can reduce C vacancy concentration, when it is performed at a temperature lower than the epigrowth temperature, i.e. less than 1600 °C. The lower the annealing temperature, the lower the resulting C vacancy concentration – but, the longer the annealing time as the C interstitials need to diffuse and diffusion velocity slows down at low temperatures. The advantage of annealing compared to thermal oxidation and ion implantation might be that it happens throughout the material volume simultaneously. Several annealing steps are performed at several stages of device production, also at late stages e.g. for contact formation etc. Here, annealing temperatures higher than the epigrowth temperature increase the C vacancy concentration again, and hence, degrade the carrier lifetime. Therefore, the annealing temperatures in the device processing need to be adapted to maintain high carrier lifetimes.

#### 3.4.4 Carrier Lifetime Measurement in Epiwafers and Devices

There are many techniques established for measuring the recombination carrier lifetime in substrates, epiwafers, and devices. Today, recombination carrier lifetime of *epiwafers* is usually measured by optical methods such as time-resolved photoluminescence (TR-PL) or microwave-detected photoconductivity decay ( $\mu$ -PCD) because these methods are fast, contactless, and do not need any sample preparation. They are called optical methods because they use optical excitation of the SiC material with UV light, i.e. a photon energy larger than the band gap, with a certain light intensity. The wavelength and the intensity of the UV light determine the excess carrier concentration profile in the sample during the measurement, which is a key factor for the recombination process taking place (see above). Only a small spot of the sample can be excited at one time; hence, the wafer needs to be scanned to get a full wafer lifetime distribution map. Real samples consist of both the low doped epilayer (stack), with certain doping concentration and thickness profiles, and the highly doped substrate as well as the epilayer surface and the back side of the wafer. Therefore, the lifetime values determined by optical measurement techniques are a kind of mean lifetime value and usually called *effective lifetimes*. Kimoto [67] has proven that the reciprocal effective lifetime is the sum of the reciprocal SRH lifetime and another reciprocal lifetime term ( $\tau_{\text{other}}$ ), which covers all other recombination mechanisms, e.g. surface recombination of the sample, and all other effects on the optical lifetime measurement. Moreover, the injected carrier concentration is not constant throughout the sample thickness and decreases during the measurement, which brings

many locally and timely shifting measurement conditions. The resulting transient curve has several regimes, representing different stages of the measurement and recombination processes, and their slopes yield the carrier lifetime value. Therefore, from a single measurement or transient, different lifetime values can be extracted. Hence, the measured lifetime values are not easy to understand or even to compare. Deeper insights into this complex situation can be gained from the simulation of the recombination carrier lifetime based on the physical equations, true doping and thickness data of the epilayer stack and substrate, as well as available recombination data [75]. The user is able to play around with surface recombination velocities, defect types, and their concentration profiles as well as intrinsic properties of the SiC material and epiwafer and check their impact on the resulting lifetime values.

Besides the optical measurements on epiwafers, the recombination carrier lifetime can be characterized at pn junctions, e.g. in bipolar power devices or the body diode in MOSFETs, by electrical methods such as the open-circuit voltage decay (OCVD). This is important as this measurement yields the actual carrier lifetime during device operation – however, the measurement takes place under high injection conditions at the pn junction. Such measurements often reveal recombination carrier lifetimes in the order of single nanoseconds or tens of nanoseconds, which are to be expected for the dominant radiative and Auger recombination processes under high injection conditions. Hence, it is probable that an epiwafer has been characterized several times during bipolar device processing with optical methods, yielding effective carrier lifetimes in the order of microseconds, and the final lifetime test in the operating device reveals much shorter carrier lifetimes during device operation.

Conclusively, recombination carrier lifetime depends on many factors, e.g. sample doping and thickness, surface recombination velocities, carrier injection, types, and their concentrations of point defects. Consequently, carrier lifetimes cannot be characterized adequately by a single lifetime value. This is the reason, why different measurement setups or measurement techniques provide different lifetime values for the same sample – the measured values are correct, but represent different measurement conditions.

## 3.5 Conclusion

This chapter summarizes and explains the main inventions in 4H-SiC homoepitaxial growth, such as step-flow growth on vicinal substrates by a CVD process, and its implications on the design of the growth process. Moreover, the most important extended defects such as dislocations and stacking faults are introduced as well as point defects, which are relevant for carrier lifetime. It has been shown that 4H-SiC homoepitaxy is a mature technology today, which reached a technological level that has been inconceivable some years ago with respect to doping control and epilayer quality. Many researchers around the world contributed to a deep understanding of phenomena and relations, e.g. the bipolar degradation mechanism and strategies for BPD avoidance and the relation between point defects and (minority) carrier lifetimes. Besides this, new characterization methods such as the UVPL imaging and

$\mu$ -PCD for extended defects and carrier lifetime have been established within the last years and useful measurement tools are commercially available – allowing for high wafer throughput and short feedback times. Hence, SiC has been established as *the* semiconductor material for power electronic applications – and will be a main part of future technologies such as electric mobility.

## Acknowledgments

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## 4

### Industrial Perspective of SiC Epitaxy

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#### 4.1 Introduction

In this chapter, the status of high-throughput production of large-area silicon carbide (SiC) epitaxial wafers for advanced SiC power devices is addressed. Because of the nature of this compound semiconductor, and high temperatures required, SiC epitaxial growth is very challenging. While maturing into a reliable manufacturing technology, it is still a highly competitive and rapidly developing field, making any review difficult. The authors of this paper apologize in advance for any inadvertent omission. A companion paper in this volume will focus more deeply on several of the important theoretical and scientific developments in the field of SiC epitaxy. However, as the performance, device parameter distributions, cost, and even reliability depend critically on the SiC epitaxial active layer properties, these topics will also be touched on here. More specifically, even after the layer metallurgical uniformity and quality, growth chamber capacity, layer growth rate, fixed growth cycle times, up time, and throughput are optimized, it is the throughput of the actual device quality epitaxy that meets the requisite device input specifications that matters. For example, one could relax epitaxial layer uniformity or defectivity for higher epi yield and lower epitaxial wafer cost, but there is so much value added in the subsequent device processing that these epi trade-offs are often overwhelmed by the final device yields to specification, pressing SiC epi to ever tightening requirements.

In large part, however, these technical challenges have been satisfied for the high-throughput supply of SiC epitaxial layers capable of producing 3.3 kV power devices ( $\sim 0.1 \text{ kV}/\mu\text{m}$ ) even demonstrating 6.5 kV [1] with low background doping concentrations  $< 1 \times 10^{14} \text{ cm}^{-3}$  and intentional n-type doping from  $\sim 1 \times 10^{15} \text{ cm}^{-3}$  to  $> 1 \times 10^{19} \text{ cm}^{-3}$ . These most recent SiC epitaxial layer growth results, particularly those from the still highest reported throughput, 8 × 150-mm, warm-wall planetary vapor phase epitaxial (VPE) reactor, will be presented in detail. The epitaxial layers have intrawafer thickness and n-type doping uniformity ( $\sigma/\text{mean}$ ) of 1.17% and 4.99%. While under active process control to counter small run-to-run systematic drifts, long-term run-to-run variations ( $\sigma/\text{mean}$ ) are currently 1.01% for thickness and 5.13% for doping (*vide infra*) [2].

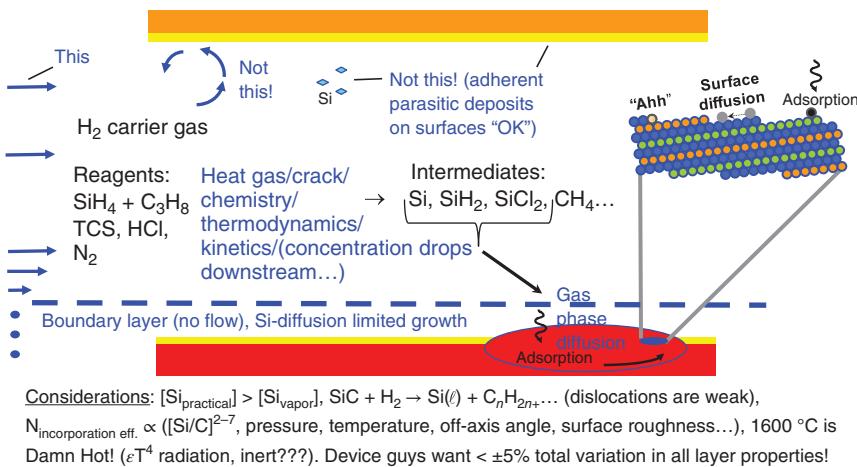
Multi-wafer SiC epitaxial layer throughput has been increased by almost 2 orders of magnitude over the past 20 years with continuously improving layer quality characteristics with further improvements underway. This and other reactor configurations will be discussed. These new SiC epitaxial growth capacities have greatly enabled the economical production of advanced SiC devices for the marketplace.

## 4.2 Background

SiC is now a preferred semiconductor material for high-power, high-temperature, and microwave devices because of its superior thermal and electrical properties [3]. SiC substrates with a diameter of 150 mm and epitaxy are commercially available, and larger 200 mm diameter SiC materials are in the early stage of development. SiC metal-semiconductor field-effect transistor (MESFETs) [4], static induction transistors (SITs) [5], BJTs [6], metal oxide semiconductor field-effect transistors (MOSFETs) [7], PiN diodes [8], insulated gate bipolar transistors (IGBTs) [9], and gate turn-off thyristers (GTOs) [10] fabricated on epitaxial grown layers have demonstrated performance far exceeding than that of Si- and GaAs-based devices, and SiC Schottky diodes and MOSFET power devices have reached widespread commercial acceptance [7], with even greater adoption projected with regard to electric vehicle applications. The development of these advanced wide-bandgap (WBG) devices has been greatly aided by the development of economical device-quality SiC epitaxial layers. These SiC epitaxial layers are the active layers of controlled thickness and doping that form the heart of all advanced WBG power semiconductor devices. The economical production of these layers has been made possible by the large area, high capacity VPE reactors with continuing and new developments described herein.

## 4.3 The Basics of SiC Epitaxy

Figure 4.1 contains a cartoon of the SiC epitaxial layer deposition process [11]. Chemical reagents such as silane and propane are delivered into the growth chamber by a carrier gas, typically hydrogen. The reagents flow over an inductively heated graphite susceptor (or directly over the SiC wafer, *vide infra*) at a temperature of  $\sim 1600^{\circ}\text{C}$ . In the ideal case, the reagents quickly heat and crack into intermediate chemical compounds that flow in a controlled laminar fashion over the SiC substrates to be deposited on. Tendencies for the gas to recirculate from convection or turbulence and silicon agglomeration in the gas phase (and on cold surfaces) due to supersaturation reduce epitaxial layer growth rates and increase layer defectivity. These undesirable characteristics are inhibited by increased growth temperature, reduced chamber pressure, and the addition of chlorine- containing compounds [12]. The natural depletion of the reagents in the gas stream must be compensated for by geometrical (including wafer rotation) or gas flow means to obtain uniform layer thickness across the substrates. Under the typical growth conditions employed



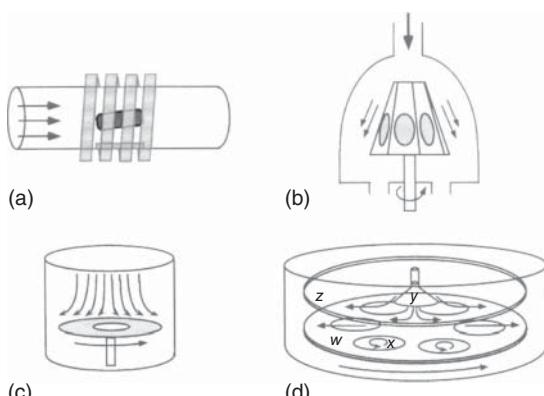
**Figure 4.1** SiC epi growth mechanism cartoon.

(~100 mbar, 1600 °C, >20 μm/h), partially cracked chemical intermediaries such as  $\text{SiCl}_2$  and  $\text{SiCl}$  [13] diffuse through a boundary layer of stagnant gas flow typically depleted of silicon (i.e. Si-diffusion growth rate limited conditions). Once adsorbed on the surface, the surface adatoms diffuse to an appropriate atomic step to correctly replicate the underlying SiC polytype or a polytype inclusion or other morphological defect will ensue.

Additional critical considerations are that the concentration of silicon-containing species for a practical growth rate will certainly at some location and temperature in the reactor exceed the allowed silicon vapor pressure as the gas heats (hence the tendency for silicon supersaturation). At the temperatures of SiC epitaxy, the hydrogen carrier gas etches the SiC substrate [14]. Despite significant improvement, unlike silicon, the SiC substrate and its surface still contain hundreds of crystallographic dislocations per square centimeter that are chemically weaker than the surrounding surface, so some pitting and other surface roughness typically result. Certain of these features can adversely impact devices [15]. Further, while the growth rate only depends linearly on the naturally reducing silicon concentration, dopant incorporation (nitrogen for n-type) is exponentially dependent upon the local Si/C ratio [16] at the growing surface and also depends on pressure, temperature, off-axis crystal angle, and atomic surface roughness. To further complicate matters, all of these diverse physical and chemical steps occur at temperatures where most supposed refractory materials and coatings are not truly physically stable to thermal gradients or shock nor chemically inert to hydrogen, chlorine, or certainly liquid silicon. Despite these challenging factors, device designers require very tight epitaxial thickness and doping distributions  $\sim \pm 5\%$  total variation and low defectivity ( $\ll 0.5 \text{ defects/cm}^2$ ) to within 5 mm of the wafer edge, and in the case for bipolar devices, zero basal plane crystallographic dislocations (both of materials and processing origins [17]) to satisfy their equally demanding device performance, yield, and reliability specifications.

## 4.4 SiC Epi Historical Origins

While interest in SiC has its origins in the late 1950s, alongside the elemental semiconductors Si and Ge, its technological development has been delayed by the extreme temperatures ( $\sim 1600^\circ\text{C}$ ) required to grow good-quality SiC epitaxial layers, the late development of suitable substrates, and the various polytypes that can form in SiC. Several reactor geometries have been successfully employed for the growth of SiC epitaxial layers. They include basic “cylindrical”-horizontal and vertical (or chimney) reactors, barrel reactors, rapidly rotating disk reactors, and “planetary”-horizontal (hereafter referred to only as planetary) reactors. Figure 4.2 contains a schematic of the basic reactor geometries. A historic distinction between these reactor geometries is whether the input gas flows perpendicular or parallel to the surface as it approaches the wafer. While either flow condition can be realized regardless of the gross orientation of the reactor, conventionally gases flow roughly horizontally over the wafers in cylindrical-horizontal, barrel, and planetary reactors and perpendicularly in vertical reactors. An important distinction used here between “cylindrical” and planetary reactors for multi-wafer configurations is that the gas must flow longitudinally over two or more wafer diameters in the former whereas it need only flow over one in the latter (*vide infra*). Note also that this distinction still holds true even if planetary motion is used in a cylindrical-horizontal reactor (hereafter referred to as horizontal). While the rapidly rotating reactor has a vertical orientation, the rapid rotation drags the gas flow stream lines horizontally by viscous pumping [18]. These reactor configurations can also be further categorized with regard to the temperature of the surfaces opposite to the wafer. These are referred to as either cold or hot “walls” where the hot wall is actively heated or “warm-wall” where the surface is passively heated yet is still hotter than silicon’s melting point,  $1410^\circ\text{C}$ . Both greatly reduce



**Figure 4.2** Schematic drawings of (a) cylindrical-horizontal (shown with inductive coil), (b) barrel, (c) rapidly rotating, and (d) planetary-horizontal-VPE SiC reactors. All employ inductively heated graphite susceptors to reach the extreme,  $\sim 1600^\circ\text{C}$ , epitaxial growth temperature. Critical components of the planetary reactor are the susceptor (*w*), wafer holders (*x*), reagent injection nozzle (*y*), and ceiling (*z*).

gas phase Si-supersaturation and surface Si-condensation which damage both reactor components and increase epitaxial layer defectivity. While in theory either condition can be realized for all of the reactor geometries, the extreme  $\sim 1600^{\circ}\text{C}$  temperatures required for SiC epitaxial growth have in practice limited barrel (and until recently, *vide infra*) rapidly rotating geometries to the cold-wall condition.

Prior to 1980, SiC epitaxial growths were still primarily performed in small, single  $\mu\text{m}/\text{h}$  growth rate, home-made horizontal and vertical quartz cold-wall reactors capable of growing only on very small, several millimeter on a side, SiC crystals. Given the high temperatures, all reactors were necessarily constructed with high-temperature-tolerant materials and coatings, such as quartz, graphite, SiC, Ta, and TaC and were normally inductively heated. Even with these refractory materials, judicious use of active water cooling and thermal insulation was required to enable growth temperature to be reached while still protecting the reactor and its components from degradation and even catastrophic mechanical failure. Moreover, in contrast to conventional semiconductors such as Si and GaAs, at growth temperatures required for SiC, none of the reactor components are truly inert; quartz devitrifies, graphite, and SiC coatings are susceptible to reaction with hydrogen, and refractory metals suffer hydrogen embrittlement and also react with hydrocarbons and silicon to form metal carbides and silicides depending upon the local environment. Unlike narrow bandgap semiconductors, the inherent chemical strength and attributes above of SiC make *in situ* cleaning of parasitic deposits highly problematic. Also, SiC readily sublimes from hotter to colder surfaces in contact or close proximity. Additionally, given the superlinear  $T^4$  dependence of radiative heating, changes in component coating thickness, composition, and emissivity by parasitic deposition or reaction can significantly change both reactor component and wafer temperatures for a fixed reactor input power.

Early SiC epitaxial growths by Jennings et al. [19] and Campbell and Chu [20] used silicon and carbon tetrachloride for silicon and carbon sources, respectively, with hydrogen as the carrier gas. Rai-Choudhury and Formigoni [21] employed dimethyldichlorosilane with argon carrier gas. Minagawa and Gatos [22] used the now more typical silane and propane reagents with hydrogen carrier gas. Nitrogen and trimethylaluminum are conventionally used for n-type and p-type doping. However, arsine, phosphine, and diborane have also been employed [20]. Some reactors also incorporated HCl as a complementary means (in addition to hydrogen) to etch substrates prior to [14, 23], or more recently, during [24–26] growth. HCl also helps avoid Si-droplet formation on the wafer surface and in the gas phase by the formation of various gaseous chlorosilanes [14]. Initially, researchers had available only very small (several millimeter on a side) 6H on-axis (0001) Lely or Acheson crystals for their SiC epitaxial growths and required high growth temperatures ( $\sim 1650^{\circ}\text{C}$ ). Slightly lower temperatures yielded unwanted yellow cubic SiC deposits. Slightly higher temperatures resulted in net etching not growth. Both extremes were also a function of reagent concentrations. Even in the relatively narrow process window where epitaxial growth was observed, the layers had relatively poor quality, suffering various polytype inclusions, and double positioning grain boundaries [27]. Nonetheless, epitaxially grown pn junctions in

such layers still exhibited basic rectification and even low levels of light emission [20]. Foreshadowing the promise of SiC-based WBG devices, these early devices blocked 50 V at 500 °C [20].

Kuroda et al. [28], Matsunami et al. [29], and Kong et al. [30] obtained specular homoepitaxial growth at reduced temperature (e.g. <1600 °C) by using 6H-SiC substrates off-oriented from the *c*-axis by several degrees toward the  $\langle 11\bar{2}0 \rangle$  *a*-axis direction, thus facilitating atomic step flow. While the two-dimensional step-flow growth model of Frank and van der Merwe [31] is well known in crystal growth, in SiC epitaxial growth, the use of off-axis substrates has the critical added benefit of exposing the atomic stacking sequence of the substrate, thereby facilitating effective polytype replication [32]. In particular, the  $\langle 11\bar{2}0 \rangle$  “*a*-axis” directions have been shown to yield improved epitaxial layer morphology [33] and to be the fast growth direction for SiC [34].

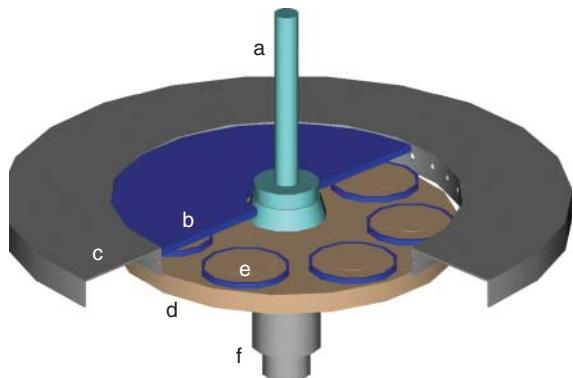
Itoh et al. successfully grew 4H-SiC epitaxial layers using 5–10° off-oriented 4H-SiC substrates [35]. Larkin et al. [36] first observed the large dependence of dopant incorporation efficiency on input Si/C ratio for both 6H, 4H, and 3C-SiC (analogous to the impact of III/V ratio in that semiconductor family [37]) helping to both reduce background doping density and extend the range of intentionally doped SiC layers.

Continued investigations of SiC epitaxial growth proceeded primarily using basic single wafer cold-wall horizontal reactors. Kong et al. [38], however, developed a cold-wall multi-wafer barrel reactor. This reactor, capable of growing epitaxial layers simultaneously on eight 10 mm diameter wafers, was the largest capacity reactor during the early 1990s. In 1993, Kordina et al. [39] developed a hot-wall reactor primarily for the purpose of reducing the perceived large (20–40 kW) power requirements of the other reactors by using a hollow, inductively heated susceptor in an otherwise basic horizontal reactor. Later, this hot-wall configuration would prove to have other beneficial attributes for the growth of thick epitaxial layers (*vide infra*). Investigating an alternate approach, Rupp et al. [40] developed the cold-wall, single-wafer, rapidly rotating vertical reactor.

## 4.5 Planetary Multi-wafer Epitaxial Reactor Design Considerations

With the exception of the barrel reactor, all of the above SiC reactors were initially designed for single wafer use. Historically, however, it has proven very difficult to achieve the  $<\pm 5\%$  total variation of epitaxial layer doping and thickness desired for high yield production of solid-state power or microwave devices in scaled-up horizontal reactors or barrel reactors when using large diameter wafers. In III/V epitaxial growth, two basic types of multiwafer metal-organic chemical vapor deposition (MOCVD) reactors produced the most uniform 3 and 4-in. diameter wafers, the rapidly rotating vertical reactor [41] commercialized by Emcore and the planetary reactor [42] commercialized by Aixtron. Two key benefits sometimes overlooked regarding planetary reactors are the high reagent efficiency, and more importantly,

**Figure 4.3** Detailed view of the 8–100 mm warm-wall planetary VPE reactor including, (a) water-cooled gas injector, (b) warm-wall (ceiling), (c) exhaust gas collector, (d) susceptor, (e) wafer holder, and (f) rotating susceptor support.



that ideal epitaxial growth conditions need only be maintained over a little more than one wafer diameter as opposed to two or more in horizontal cylindrical configurations. This is particularly challenging at the extreme temperatures of SiC growth.

First reports on the extension of the planetary design to the much higher temperatures of SiC epitaxial growth were reported by Burk in 1997 [43, 44] for a 7 × 35-mm and 7 × 2-in. warm-wall configuration. In the warm-wall configuration shown in Figure 4.3, a passively heated insulating ceiling is used. The temperature of the ceiling's bottom surface is determined by the thickness and thermal conductivity of the insulation, radiative and conductive heating from the susceptor, and conduction through a gas present in a thin gap between the back of the insulated ceiling and a water-cooled flange. The conductivity of this gap can be actively controlled by varying the relative concentrations of hydrogen and argon gas in the gap. To minimize susceptor mass, and thereby reduce thermal cycle times, mechanical rotation is used for the susceptor, and gas is used only to rotate the wafer holders. Initial growth rates for this warm-wall configuration were relatively low, between 2 and 5  $\mu\text{m}/\text{h}$  [43, 44]; however, specular morphology, reasonable background doping ( $\sim 1 \times 10^{15} \text{ cm}^{-3}$ ), and 2%  $\sigma/\text{mean}$  thickness and 8%  $\sigma/\text{mean}$  doping intrawafer uniformity were cited for 8 × 100-mm wafers [45]. The latest results for a significantly scaled up 8 × 150 mm warm-wall reactor are reported in [2, 11] and Section 4.6.

#### 4.5.1 Rapidly Rotating Reactors

Rupp [46] successfully extended his single-wafer, rapidly rotating, cold-wall reactor to 6 × 2-in. configuration for Schottky layer production. Further scaling of this configuration, however, presents many challenges. In SiC epitaxial growth, cold-wall reactors in general have suffered limited growth rate (<5  $\mu\text{m}/\text{h}$ ) and poor layer uniformity due to significant silicon supersaturation in the gas phase [47]. This is caused by silicon's very low vapor pressure, at temperatures at which silane is readily decomposed ( $\sim 10^{-9}$  Torr at  $\sim 900^\circ\text{C}$ ). Supersaturation can also result in morphology degradation if the ensuing Si and SiC clusters come into contact with the wafer surface. Silicon supersaturation can be significantly reduced by using a “hot-wall” configuration; however, until recently, this was not implemented in the rapidly rotating reactor as the reactor is designed to have the gases enter uniformly through

the ceiling, making pre-reaction and clogging very problematic if heated. Another challenge for the rapidly rotating reactor is that planetary rotation is not likely to be achieved due to the enormous centripetal forces from the >500 RPM required to obtain stable and laminar flow patterns for consistent and uniform epitaxial growth and depending upon *in situ* wafer flatness, wafers can literally fly off of the susceptor.

#### 4.5.2 Horizontal Hot-Wall Reactors

Horizontal hot-wall reactors evolved from small single wafer reactors but have been successfully scaled up to as large as  $3 \times 150$  mm configuration including the addition of planetary rotation, using gas levitation for susceptor and wafer rotation [48, 49]. These reactors historically reported the best combination of purity (low background doping concentration  $<1\text{E}14 \text{ cm}^{-3}$ ), layer thickness uniformity, and defectivity ( $\sim<0.25 \text{ defects/cm}^2$ ), particularly for epitaxial layers with thickness greater than  $100 \mu\text{m}$  [2].

Our latest in-house  $3 \times 150$  mm hot-wall results are shown in Figure 4.4. While having challenges regarding edge doping uniformity (Table 4.1), they have demonstrated the ability to maintain good defect densities and  $5 \times 5$  mm useable areas (killer defect [KD] free area for  $5 \times 5$  mm device die) for epitaxial layers of greater than  $100 \mu\text{m}$  thickness [2], enabling the pilot-line production of 10 kV SiC power devices with high yields. As shown in Figure 4.5, even the much higher throughput  $8 \times 150$  mm warm-wall reactor have demonstrated 6.5 kV suitable layers with similar, 89%  $5 \times 5$  mm useful areas showing a path to future production of higher power devices [1].

Externally, Hochbauer et al. reported on a  $3 \times 150$  mm Tokyo Electron Ltd. (TEL) hot-wall reactor with 0.68% sigma/mean thickness and 4.92% doping uniformity with a 5-mm edge exclusion and fixed cycle times as low as 1.5 hours (excluding epitaxial growth time) [53]. Wada et al. [54] have also reported on a custom made  $3 \times 150$  mm hot-wall horizontal hot-wall reactor with equally impressive 1.9% sigma/mean thickness and 2.2% doping uniformity trade-off but without independent wafer rotation,  $<0.1 \text{ defects/cm}^2$  and 99%  $5 \times 5$  mm useful area for albeit thin,  $10 \mu\text{m}$ -thick, epitaxial layers. While certainly possible, further scaling of the horizontal configuration to  $3 \times 200$  mm capacity, where, as mentioned previously, the carrier gas has to flow longitudinally over two or more wafer diameters while still maintaining optimum epitaxial growth conditions, may result in higher than desired carrier gas flow and cycle time requirements.

### 4.6 Latest High-Throughput Epitaxial Reactor Status

Of course, many of the above reactors were considered state-of-the-art, high-capacity, and even high-throughput reactors for their time. Table 4.1 includes a list of the salient properties for several of these production proven

**Table 4.1** SiC epitaxial growth reactor comparisons.

Reactor family	Wolfspeed planetary warm-wall reactors					Wolfspeed hot-wall		Rapidly rotating vertical	
	7 × 35-mm		8 × 100-mm		8 × 150-mm (manual)	5 × 200-mm (automated) (projection!)	3 × 150-mm (projection!)	3 × 150-mm (automated) (projection!)	1 × 150 (automated)
Reactor	7 × 35-mm	8 × 100-mm							
Reference(s)	[45]	[45]	[2]	[50]	[2]	na	Current [51, 52]	na	na
Wafer count per run (capacity)	7	8	8	5	3	3	1	1	1
Wafer OD (mm)	35	100	150	200	150	150	150	150	200
Single wafer area (cm <sup>2</sup> )	10	79	177	314	177	177	177	177	314
Single useful wafer area (cm <sup>2</sup> a)	4.9	63.6	153.9	283.5	153.9	153.9	153.9	153.9	283.5
Total useful wafer area (cm <sup>2</sup> a)	34	509	1232	1418	462	462	154	154	284
Growth rate (mm/h)	3	10.0	45	60	14	20	60	60	60
Approximate fixed heat/cool cycle time (h)	1.00	3.00	2.00	0.75	5.50	1.00	0.38	0.38	0.38
Unloading/loading time	0.50	0.50	0.50	0.19	0.50	0.25	0.08	0.08	0.08
Total time per 17-μm thick epi run, h (~1200 V blocking + buffer)	7.17	5.20	2.88	1.22	7.21	2.10	0.75	0.75	0.75
Yielded cm <sup>2</sup> of 17 mm-thick epi/day	84	1712	7487	20 317	1120	3848	3594	6620	
<b>Normalized 17 μm layer throughput</b>	<b>1</b>	<b>20</b>	<b>89</b>	<b>242</b>	<b>13</b>	<b>46</b>	<b>43</b>	<b>79</b>	
Thickness uniformity (% sigma/mean)	2.4	2	1.17		1.03		1.3		
Doping uniformity, 5 mm EE (% sigma/mean)	3.6	8	4.99		11.7		2.6		
Defectivity <sup>b)</sup> (“killer” defects/cm <sup>2</sup> ) (Candela CS20 or equivalent)	~5	~2	0.29		0.47		<~0.1 <sup>d)</sup>		
% 5 × 5-mm useful area (Candela)	na	na	93.0		90.5		na		
% 5 × 5-mm useful area (SICA KD4 <sup>c)</sup>	na	na	95.3		93.4		>~98 <sup>d)</sup> [52]		
% 5 × 5-mm useful area (SICA KD1 <sup>e)</sup>	na	na	83.9		78.8		na		

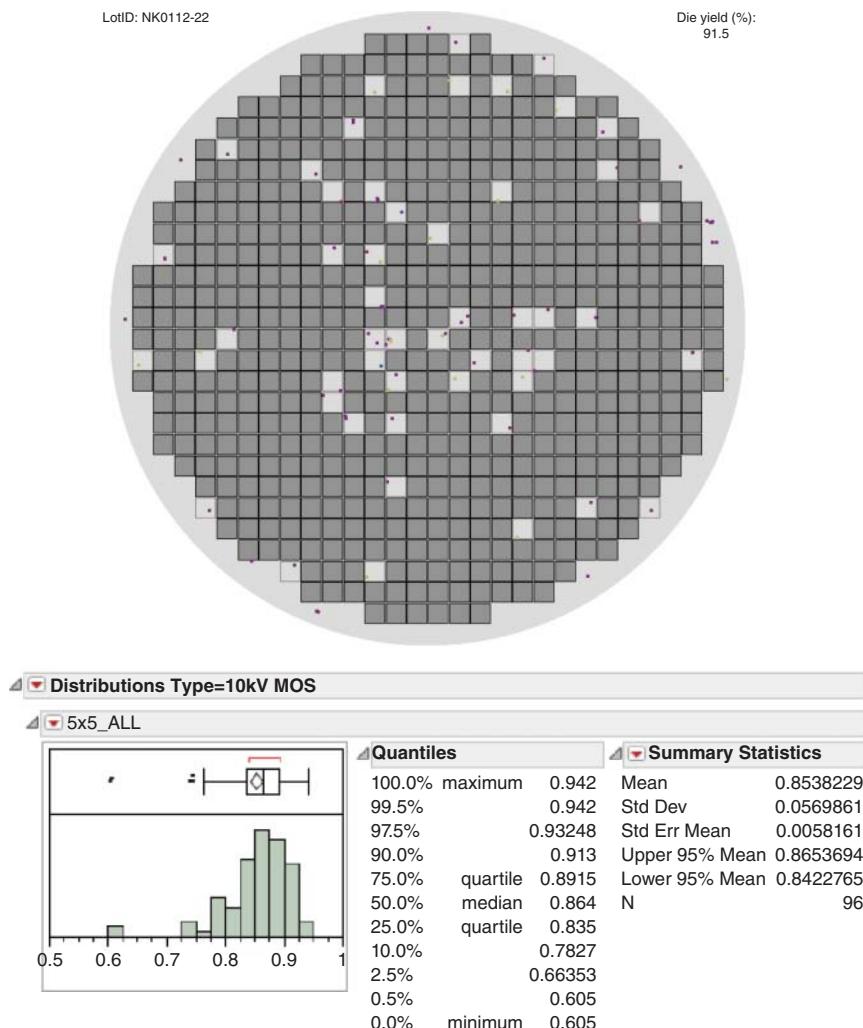
a) 5 mm edge exclusion. Assuming 90% each for % Uptime, % Production, and % Yield to epi specification.

b) Calculated by Poisson equation.

c) Lascertec System 88 (Triangles + Falldown).

d) Lascertec SICA (Triangles + “Large” Pits + Diagonal).

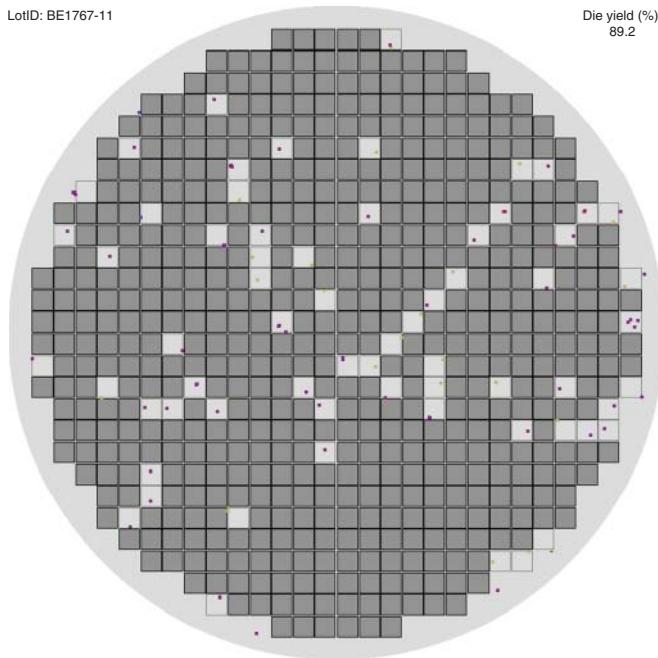
e) Lascertec System 88 (Triangles + Carrots + Falldown + Particles).



**Figure 4.4** Candela optical surface analyzer (CS20) defect map and typical defect distribution for 100  $\mu\text{m}$  thick epi wafers from a 3  $\times$  150 hot-wall epi reactor averaging 85% useful area.

high-throughput reactor configurations along with more modern developments and as will be discussed later, projections for 200 mm diameter capability. The projections assume the same 90% uptime, percent product time, and yield to epi layer specification so are only approximations. We do include the latest reported uniformity, defectivity, and cycle times and attempt to project reasonable cycle times when scaling to 200 mm diameter wafers.

There are many different ways to achieve high epitaxial layer areal throughput. First and most desirable is increasing wafer diameter as that has the greatest direct benefit to device processing costs, which accrue on a per wafer basis almost regardless of the actual die count per wafer. Second would be the epitaxial reactor



**Figure 4.5** Candela optical surface analyzer (CS20) defect map for an example 65  $\mu\text{m}$  thick epi wafer from a 8  $\times$  150 warm-wall epi reactor with 89% useful area.

capacity (number of wafers of a certain size per run). The third typically addressed and included here is increased epitaxial layer growth rates. However, given the high 1600 °C temperatures, significant heat up and cool down times can dominate overall growth run cycle times particularly for thinner epitaxial layers. These “fixed” cycle times can be reduced somewhat by automation, but most importantly, can be cut in half by allowing 600 or even 900 °C temperature hot loading and unloading. Heat up times can of course be reduced to a point with increased heater power, however, at the risk of thermal shock to reactor components and larger capacity reactors already tend to have much more thermal mass. For all reactors, the passive cool-down driving force ( $\Delta T$ ) is naturally reduced in the final stages of cooling well before wafers can be manually manipulated. Automation has been emphasized first in single and lower capacity wafer reactors perhaps in an attempt to catch up to the inherent through-put advantage of higher capacity multi-wafer reactors); however, automation [50] is now being applied to these too.

In addition, any of the reactors described in this paper could be combined in a cluster of two or more growth chambers for certain hardware and cost efficiency, but for truly independent operation, it is assumed that any cost savings per chamber would be modest (and likely similar for competing reactor styles), so comparisons in Table 4.1 have been made for single reactor chambers only. Not included but very important for eventual real-world cost consideration is of course the footprint of a given reactor and capital cost.

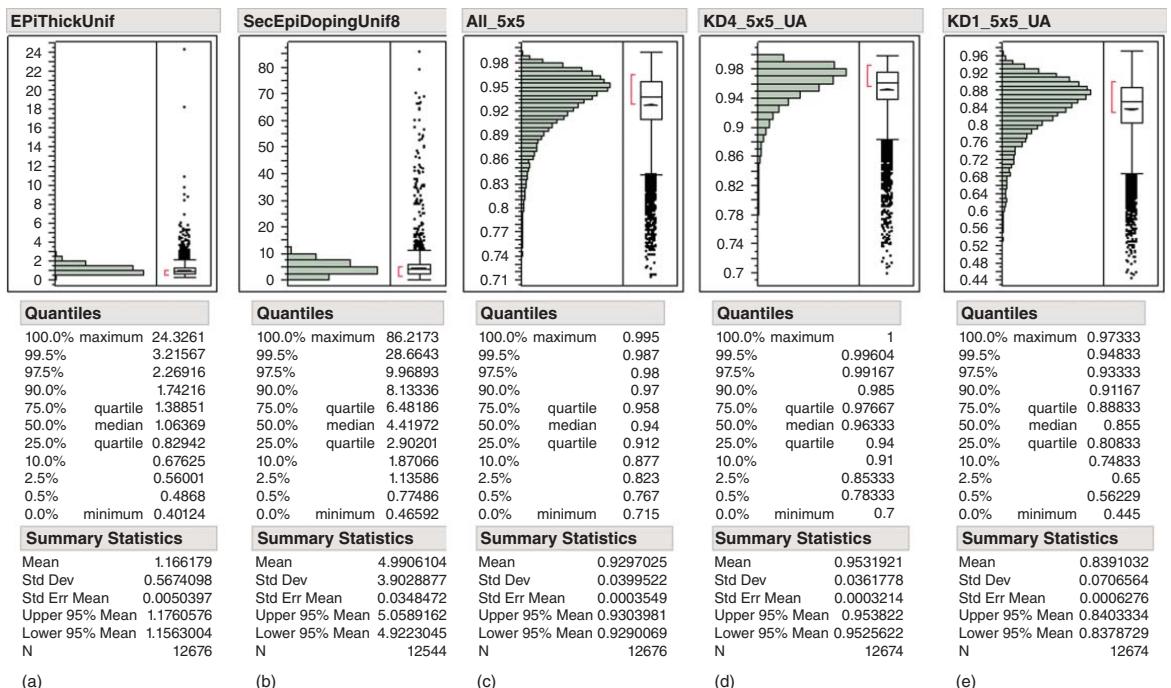
## 4.7 Benefits and Challenges for Increasing Growth Rate in all Reactors

Increasing growth rate obviously offers important throughput benefits for all wafer sizes and reactor configurations particularly for thicker layers where the fixed cycle times are less significant. Layer defectivity, however, can increase if supersaturation limits are exceeded and/or surface adatom diffusivity is inadequate for the rate, causing stacking faults and other defects to increase [55]. Increasing temperature to counter these undesirable trends can unfortunately cause dislocation etch pitting and subsequent defectivity [56–58]. Despite this, horizontal hot-wall reactors had already demonstrated increased growth rates [24] reportedly as high as 18  $\mu\text{m}/\text{h}$ . [25]. Extreme growth rates as high as 250  $\mu\text{m}/\text{h}$  by Ito [59] have been reported in horizontal hot-wall reactors and 380  $\mu\text{m}/\text{h}$  by Ellison et al. for high temperature chemical vapor deposition (HTCVD) [60]. Despite these promising demonstrations, there have been no reports that these impressive growth rates have been extended to large diameter or multi-wafer production reactors. Most conventional epitaxial growths are still typically performed at 1600 °C at approximately a tenth of these rates, likely due to the remaining (and increasingly stringent) device layer defectivity requirements.

## 4.8 Increasing Wafer Diameters, Device Processing Considerations, and Projections

Given the current 150 mm diameter SiC wafer standard, increasing wafer diameter to 200 mm alone would nearly double the number of device die per wafer if the epitaxial layer uniformity and defectivity requirements can still be satisfied. Moreover, in true production quantities, even larger area SiC epitaxial wafers should eventually represent the same or less epi cost per unit area (and represent only a quarter of the final device cost).

Table 4.1 includes some projections for automated growth on 200 mm wafers (to compare to the results from the current 150 mm state of the-art). All of the configurations included in the table show significant increases in areal throughput. On balance, the factors discussed in this paper still favor the throughput of high-capacity, multi-wafer, larger diameter epitaxial growth reactors in SiC epitaxy, particularly the 8 × 150 mm (and projected 5 × 200 mm configuration) Planetary reactor [2]. Figure 4.6, shows the thickness, doping, and defectivity distributions for a subset of over 10 000 150 mm wafers we have grown in our 8 × 150 mm reactors. Good thickness 1.17% and doping 4.99% uniformity (5-mm edge exclusion) were achieved. While not shown, long-term run-to-run reproducibility is 1.01% and 5.13% for thickness and doping, respectively. About 93% 5 × 5 mm useful Candela (CS20) KD areas, 83.9% Lasertec System 88 KD1 (the sum of Triangles, Carrots, Fall-down and Particles), and 95.3% KD4 (Triangles + Falldown) were also observed. Not surprisingly, the newer Lasertec optical surface analyzer is able to detect more defects (even down to nm-scale dimension [not shown here]), but by our experience



**Figure 4.6** Epitaxial layer distributions for over 10 000 150 mm epitaxial wafers grown in our 8 x 150 mm warm-wall epi reactors; (a) thickness uniformity (%  $\sigma/\text{mean}$ ), (b) doping uniformity (%  $\sigma/\text{mean}$ ), (c) Candela CS20, (d) Lasertec System 88 KD4, and (e) KD1 5 x 5 mm useful areas.

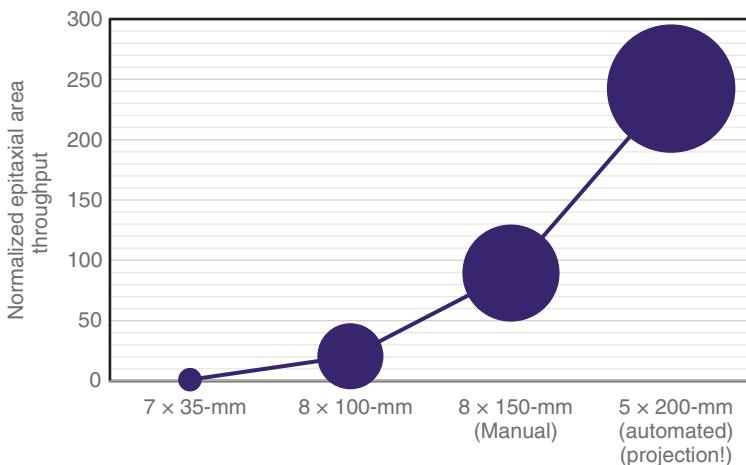
entitled device yield is reasonably well predicted by both the total Candela CS20 and Lasertec KD4 counts. Similar to these results, Epi World has generously provided in a private communication (G. Feng and Epi World, private communication) very similar uniformity values of 1.32% and 4.95% for thickness and doping, respectively, and 98% 2 × 2-mm useful areas (projected to be ~88% @5 × 5-mm by the Poisson equation) for over 5000 150 mm epi wafers.

Mauceri et al. [61] reported 30 µm/h growth rates and 10 µm thick 150 mm Schottky wafers with 1.1% thickness and 2.7% doping uniformity with <0.5 defects/cm<sup>2</sup> grown in “less than one hour” utilizing automation and 900 °C hot loads in a LPE PE1O6 hot-wall reactor. In a private communication, D. Crippa [62] relayed that a 200-mm cassette-to-cassette epitaxial reactor will be developed and ready for installation by the second quarter of 2020 as part of the European REACTION project. TEL and users [53, 63] have also reported on 3 × 150 mm automation incorporating hot loads in *Probus*<sup>TM</sup> horizontal hot-wall reactors but have not yet commented on 200 mm solutions.

In a re-emergence of rapidly rotating single wafer-epi reactors, Tsuchida et al. [64] and later Daigo et al. [51, 65] and Showa Denko (SDK) [52] have adapted single wafer rapidly rotating reactors to incorporate a hot wall with the ceiling apparently sufficiently removed and cool enough to avoid previously experienced Si-condensation, parasitic deposition, and fall down [40]. Regardless of the mechanism, this has resulted in greatly reduced defectivity and reportedly enabled the growth of several millimeters of epi before requiring maintenance at >50 µm/h growth rates. Even though currently (*and probably*) limited to single wafer configuration (150 mm diameter with as of yet unconfirmed plans for 200 mm), the incorporation of automation for very quick (few minutes) and also 900 °C hot loading for short fixed heat and cool cycle times (23 minutes) makes the total time per epitaxial wafer growth 37 minutes for a 10-µm thick layer. As shown in Table 4.1, this suggests throughput is within a factor of 2 of the higher capacity manually loaded multi-wafer planetary reactors. An estimated scaling to 1 × 200 mm would match the throughput of the manual 8 × 150 mm planetary reactor. Moreover, Showa Denko (SDK) recently presented a very impressive 280-µm thick epitaxial wafer with only one visible defect on an entire 100 mm wafer [52] reportedly using a *NuFlare*<sup>TM</sup> reactor [51].

As mentioned previously, throughput enhancement from automation or hot loads can in theory be equally well applied to a multi-wafer reactor (e.g. an 8 × 150 mm or projected 5 × 200 mm planetary warm-wall reactor in Table 4.1) [50]; however, given the significant capital expense of all production reactors, this will only be cost effective if epitaxial wafer demand supports full epitaxial wafer loads and efficient capacity utilization. Also, if new epitaxial wafer layer requirements cannot be met by any configuration with high yield, this will obviously detract from the basic throughput projections provided here. The yield of key attributes such as epitaxial layer uniformity, reproducibility, flatness, surface roughness, defectivity, and dislocation density to specification can dramatically impact the effective throughput of epitaxial reactors to a required specification (Figure 4.7).

With regard to morphological defectivity and crystallographic dislocations, even with great advances in metrologies, such as confocal optical microscopy



**Figure 4.7** Normalized plot of epitaxial area throughput vs. SiC warm-wall reactor generation (data label diameter is proportional to the wafer diameter).

and photoluminescence by Lasertec (<https://www.lasertec.co.jp/en/products/environment/sic/sica88.html>) and X-ray topography by Rigaku (<https://www.rigaku.com/en/products/xrm/xrtmicron>), details of which are beyond the scope of this chapter, it is still perhaps not surprising that predicting the suitability of a particular epitaxial layer growth process is not a simple matter. Defects are by nature highly variable in morphology impacting both identification and counting for differing generations of metrology hardware and analysis recipes and subsequent correlation with device yield [15]. There is often sufficient ambiguity and interactivity with various device manufacture processes and design that only the final device yield and performance of a given tuned epi process can conclusively determine the suitability for a particular device type (or even for different manufacturers of the same device type). There are of course cost trade-offs between epitaxial layer yield to needed layer specifications but given that the majority of device processing cost occurs after epitaxy, ultimately these allow little room for epitaxial layer specification relief.

## 4.9 Summary

The development of SiC epitaxial growth for industrial-scale production has been reviewed from small home-made quartz reactors to modern multi-wafer reactors capable of supporting commercial device production. The highest-throughput device-qualified manual SiC epitaxial growth reactor developed to date is capable of growth upon eight 150-mm wafers at a time at 45  $\mu\text{m}/\text{h}$ . The layers produced by this reactor exhibit specular morphology, high purity, and good uniformity. Long-term run-to-run reproducibility is 1.01% for thickness and 5.13% for doping [2].

Epitaxial area throughput has been increased by almost 2 orders of magnitude from that of the earliest 7  $\times$  35-mm configuration while increasing layer quality and

uniformity. Particularly for layers of  $\sim 50 \mu\text{m}$  or less, where epitaxial run cycle time considerations dominate growth rate limitations, thus far the warm-wall planetary configuration has had the superior overall throughput enabling economical SiC device production. It is projected that even a scaled, manually loaded  $5 \times 200 \text{ mm}$  epitaxial reactor could double throughput yet again, and if needed, will likely be capable of growing thicker epitaxial layers for higher voltage power devices [1].

This production capability, however, has now been significantly challenged by epitaxial reactor automation and hot loading even in single-wafer reactors but this too is being developed on multi-wafer reactors for yet higher throughputs. Regardless of the ultimate configuration for  $200 \text{ mm}$  diameter epitaxial wafer production, and despite ever tightening epitaxial layer requirements, current developments in SiC epitaxial layer reactors and processes still promise factors more epitaxial layer throughputs and hence significant cost reductions over the next few years.

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## 5

### Status of 3C-SiC Growth and Device Technology

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### 5.1 Introduction, Motivation, Short Review on 3C-SiC

The cubic polytype of silicon carbide (3C-SiC) has attracted particular interest since the early days of research and development in the field of SiC technology. Knippenberg [1] elaborated already in the year 1963 in detail stability criteria for the growth of various SiC polytypes and presented process conditions that favorably lead to the formation of 3C-SiC. Later, this work was further elaborated by Fissel [2] who presented in the year 2000 a comprehensive study on thermodynamic considerations of the epitaxial growth of SiC. From the point of view of electronic device applications, the cubic polytype of SiC was considered in the 1980s and 1990s because of the greater electron mobility compared to the hexagonal counterparts, i.e. 4H-SiC and 6H-SiC (Table 5.1).

From a crystal growth point of view, the process development progressed much faster for the hexagonal polytypes 6H-SiC and 4H-SiC which is the main reason that the 4H-SiC is being applied as state of the art in Schottky-junction diodes (SJD) as well as in power switches based on metal oxide semiconductor field-effect transistors (MOSFET). The interest in the cubic polytype, however, remained high throughout the years. The 4H-SiC metal-oxide-semiconductor (MOS) interface exhibits a high defect density in the upper band gap of 4H-SiC and a limited long-term stability. Due to the smaller electronic band gap of the cubic polytype, those interface-related electron traps are mainly located in the conduction band of 3C-SiC and, hence, enable better device performance in the mid-voltage regime of 300–800 V devices [14–16]. Up to date, the major barrier for the application of 3C-SiC in power electronic devices

**Table 5.1** Physical properties of Si, 3C-SiC, 6H-SiC, and 4H-SiC [3–13].

	<b>Si</b>	<b>3C-SiC</b>	<b>6H-SiC</b>	<b>4H-SiC</b>
<i>Lattice parameter</i> (Å)	5.43 cubic	4.36 cubic		$a = 3.08$ hexagonal
$E_G$ (eV)	1.1	2.36	2.98	3.2
$E_B$ ( $10^5$ V/cm) at $N_D = 5 \cdot 10^{15}$ cm $^{-3}$	3	15	22	23
$n_i$ (cm $^{-3}$ ) at 300 K	$1 \cdot 10^{10}$	$1.5 \cdot 10^{-1}$	$1.6 \cdot 10^{-6}$	$5 \cdot 10^{-9}$
$\lambda$ (W/cm K)	1.5	3...5	3...5	3...5
$v_s$ (10 $^7$ cm/s)	1	2	2	2
$\mu_n$ (cm $^2$ /V s)	1500	900	370	800
$\mu_p$ (cm $^2$ /V s)	480	40	80	120
$E_D$ (meV)	45 (P)	48 (N)	71/124 (N)	52/92 (N)
$E_A$ (meV)	44 (B)	242 (Al)	242 (Al)	242 (Al)
$\epsilon$	11.7	9.7	9.6	9.6
$T_s$ (°C)	1420	2830	2830	2830

is related to the lack of high-quality large wafer material that serves as the basis for the electronic device manufacturing process.

In recent years, further potential applications of 3C-SiC originated that make use of its unique physical properties. 3C-SiC co-doped with the deep boron acceptor and shallow nitrogen donor is a strong candidate for an intermediate band solar cell material that may reach a theoretical light conversion efficiencies above 50% [17, 18]. In addition, p-type doped 3C-SiC using the acceptor aluminum is intensively studied for the application in solar-driven electrochemical water splitting [19, 20]. Beside the hexagonal polytypes, also cubic SiC is under research for the future application in quantum computing [21]. The intentional incorporation and tailoring of point defects during growth of 3C-SiC as well as their annealing behavior have been demonstrated by Schöler et al. [22, 23]. Other important applications of 3C-SiC related to its chemical inertness and mechanical hardness lie in the field of biomedical coating and in general for sensing. In the latter cases, also microcrystalline layers may be applied beside single crystalline materials.

Bulk growth of 3C-SiC that could be performed with some rare, so-called small Lely platelets as seeding material, either using sublimation or solution growth, turned out to be very difficult. However, pioneering work for the nucleation and epitaxial growth of 3C-SiC on Si using chemical vapor deposition (CVD) was already performed in 1983 by Nishino et al. [24]. First attempts to grow bulk 3C-SiC also followed a hetero-epitaxial approach for the seeding process on either (100) oriented 3C-SiC layers that stem from 3C-SiC CVD deposition on Si [25, 26] or as (111) oriented 3C-SiC on (0001) oriented 6H-SiC [27]. In recent years, a number of research teams have elaborated the key process parameters that allow a stable growth of the cubic SiC polytype using sublimation growth [25–37]. Among those

process parameters, a silicon-rich gas atmosphere, a high supersaturation, and a temperature below 2000 °C are most important. The common challenges to realize bulk 3C-SiC are related to the 3C-SiC nucleation and preservation of the 3C-SiC polytype throughout the growth process. Often stacking faults (SFs), double positioning boundaries (DPBs), and anti-phase boundaries (APBs) alter crystalline quality and limit the technological application of 3C-SiC in electronic devices. Regarding the planar defects like SFs and APBs, a significant reduction and even elimination was demonstrated when 3C-SiC nucleation that was carried out on undulant, off-axis (100) oriented Si substrates was already presented [38]. For a review of hetero-epitaxial growth of 3C-SiC layers on Si substrates, see [39].

Merging the above-mentioned knowledge in literature [24–39], it is concluded by the authors of the current work that the growth of high-quality cubic SiC may be achieved by the application of high-quality 3C-SiC template layers initially grown by CVD on (100) silicon followed by a physical vapor sublimation growth method.

In this overview paper, recent progress in the fabrication of large area 3C-SiC substrates and homo-epitaxial layers with a diameter of 100 and 150 mm as well as electronic device processing will be presented. In Section 5.2, the main problems of the hetero-epitaxial process (defects and stress), the evolution of defects and the interaction of different defects, and the effect of these defects on the electrical characteristics of the material will be reported. Section 5.3 discusses the different processes to realize bulk 3C-SiC wafers. In Section 5.4, the main developments on the processing of 3C-SiC for the realization of power devices will be reviewed.

## 5.2 Nucleation and Epitaxial Growth of 3C-SiC on Si

### 5.2.1 Growth Process

The scientific and technological attraction to 3C-SiC dates back to 1959, when Spitzer et al. [40] published the first report of 3C-SiC growth on a silicon wafer by heating the silicon with a gaseous hydrocarbon. This paper represents the first milestone in 3C-SiC hetero-epitaxy on Si. Later, the real breakthrough in the 3C-SiC/Si hetero-epitaxy was achieved in 1983, when Nishino et al. [24] proposed a multi-step CVD process able to improve the crystal quality in the 3C-SiC epilayers. Their method for the 3C-SiC growth was composed of three different steps: (i) an etching process by flowing HCl at 1100 °C was performed in order to prepare the Si substrate surface; (ii) a buffer layer growth, necessary to obtain good SiC crystal quality, was performed at 1360 °C for a short time under propane ( $C_3H_8$ ) flow; and (iii) the crystal growth with both silane and propane was carried out at 1330 °C under a flowing  $H_2$  carrier gas. Using this recipe, a single-crystal 3C-SiC layer can be grown on the buffer layer, which is used as the seed for subsequent SiC growth. Coined the “buffer layer method” as used by Nishino revitalized the race toward the ideal material for 3C-SiC electronic applications started in the 1950s. Several universities and semiconductor R&D departments industries tried to improve the scientific knowledge and to develop and optimize an industrial growth process after 1982. Researchers have obtained many improvements due to

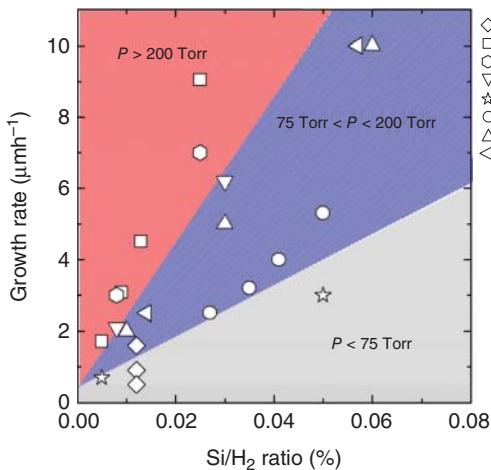
their efforts in following many different paths in the labyrinth of 3C-SiC chemical vapor deposition. SiC reactors growing on Si are complicated and a wide range of parameters are involved in the growth process, such as temperature, gaseous precursor composition, pressure, and gaseous partial pressures. A huge number of published works, not only by CVD but also by sputtering or molecular beam epitaxy (MBE) [41, 42], are devoted to the growth of SiC on Si. Over the decades, CVD reactor development involved the enlargement of the reaction chamber allowing epitaxial growth on Si wafers with a diameter of 200 mm (8 in.) [43].

Among many variables, the composition of the *gaseous precursors* is crucial in determining which will be the experimental conditions of several parameters inside the CVD reaction chamber in order to achieve good quality 3C-SiC films. This is of course related to the different behavior of reactants in their dissociation from gaseous phase molecules to solid phase adatoms that will arrive, migrate, and bond with the dangling bonds available at substrate surface steps or terraces. An overview of possible reactions can be found in literature [44–46]. Thus, changes in gaseous precursor chemistries will determine significant differences in the growth temperature range, in the gas partial pressures during the growth, and in the cracking efficiency of reactant species in the gaseous phase. The temperature of gasses determines the rate of production of the various radicals. For instance, in the silane–propane system, a widely used chemistry for SiC CVD epitaxy, silane dissociates at a lower temperature than propane. This means that, as the chamber is heated up to growth temperature, the effective C/Si ratio changes so that the real amount of adatoms to form SiC film is unknown. As a consequence, due to the higher thermal stability of CH species compared to the SiH ones [47], the growth process requires a higher amount of C-containing supply in the gas phase to obtain stoichiometric SiC. On the other hand, being Si the reaction-limited element in the gas phase participating to the reaction, a linear dependence of the growth rate on the Si-precursor gaseous flux is commonly observed.

The dependence of the growth rate with the Si/H<sub>2</sub> ratio is reported in Figure 5.1. From this plot, the linear dependence is clearly evidenced. Moreover, a strong dependency of both parameters with the total pressure can also be observed [49]. In detail, the higher the reactor pressure, the steeper the experimental slope. The higher growth rate at lower Si/H<sub>2</sub> ratio for pressure regime above 200 Torr (eventually at atmospheric pressure) is related to the lower gas velocity and to the longer time that adatoms need to reach the solid surface. When the pressure is reduced, the gas velocity increases and more Si (higher Si/H<sub>2</sub> ratio) is required to maintain the same growth rate.

However, the silane–propane system is affected by homogeneous gas phase nucleation, where solid/liquid particulates (usually of Si) are formed in the gas phase. This phenomenon causes the depletion of the gas phase precursor available for the deposition and the worsening of the surface quality, due to particulates impinging on the deposition surface. To remove the homogeneous gas phase nucleation, the use of chlorinated silicon precursors, or simply the addition of HCl, was suggested [50–53]. Using these precursors, it is possible to obtain a high growth rate (30 μm/h) at low temperature (1370 °C) [54].

**Figure 5.1** Dependence of the growth rate with the Si/H<sub>2</sub> ratio. This dependence is strongly influenced by the total pressure within the reaction chamber. Growth temperatures used are similar. Source: Severino [48]. © 2012, Andrea Severino.



Since before Nishino et al. introduced the two-step growth method for the 3C-SiC hetero-epitaxy on Si by CVD, a relevant interest was placed on the effect of a hydrocarbon gas on a Si surface at high temperatures. Different models and experimental observations were proposed in the 1970s, with the evidence that a thin 3C-SiC layer was formed on a Si surface by the conversion of Si into SiC.

Even though single-crystal 3C-SiC films have been obtained by the two-step CVD technique, the SiC/Si interface remains a plague due to the formation of voids in the Si substrate. Voids are usually hollow inverted pyramids, with the shape depending from the orientation of the substrate, lying just beneath the interface. Their presence poses a severe problem in several applications based on 3C-SiC hetero-epitaxy such as hetero-junction bipolar transistors or hetero-junction solar cells with 3C-SiC emitter layer as these devices require an excellent interface morphology. In a work published in 2007 [55], author's group has correlated void density and size with the process temperature and reaction time for 3C-SiC buffer layer formation on differently oriented Si substrates. A statistical study of voids at the interface has been conducted as a function of the process temperature for the buffer layer formation. First, the temperature strongly influences the surface and interface morphology and the film thickness with the observation of an incomplete film formation and occurrence of cavities in the substrate if the temperature is too low. Void shape is, as expected, strictly related to the orientation of the silicon substrate used for the growth. In a diamond cubic crystal structure such as for Si, the atomic lattice packing density and the available bonds in the crystallographic plane strongly affect both the removal and the addition of the atoms on the surface. Voids on the silicon surface during the growth of a 3C-SiC layer could be seen as an etching process of atoms from the substrate contributing to the formation of the growing 3C-SiC layer. The (111) oriented Si surface shows the highest atomic packing density, which is less for the (001) Si surface and is even less dense for the (110) Si surface. Since etch and deposition rates depend on this density, one would expect a faster process in the  $\langle 110 \rangle$  direction than in the other directions. This assumption is confirmed by measurements, in which the thicknesses of 3C-SiC films grown at 1120 °C are reported as a function

of reaction time and the highest growth rate corresponds to the (110) surface [55]. The trend found here predicts a squared dependence of the thickness vs. the process time, suggesting that the reaction is limited by the diffusion of one of the species (atoms of Si in 3C-SiC buffer layer) involved in the growth.

In a recent paper [56], it has been shown that the main parameter for the reduction of voids at the interface is the C/H ratio. In fact, increasing the C/H ratio the voids density decreases and finally even voids free interface can be obtained. With this process even the density of the carbonization layer increases and the morphology of the layer is largely improved resulting more flat.

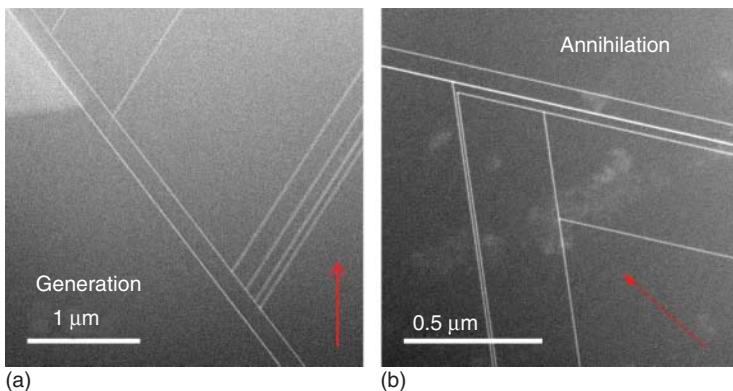
Another step that has a large impact on the final quality of the grown layer is the buffer layer grown during the temperature ramp between the carbonization step and the growth one [56]. In fact, it has been observed that the ramp time can have a large impact on the reduction of the final stress, [56] while the C/Si ratio in this step can have an impact on the formation of protrusions in the layer [57].

### 5.2.2 Defects

Considerable efforts have been made to improve the quality of CVD-grown 3C-SiC. Significant reduction in the defect density in cubic SiC thin films has come with the introduction of a buffer layer [58–60] and the use of patterned Si substrates [38, 61–63], but has also introduced new problems during the growth. The CVD process suffers from an intrinsic drawback, whereby, at typical growth temperatures, between 1550 and 1700 °C, on free-standing 3C-SiC surface diffusion limits the growth rate to approximately 100 µm/h [64]. Instead, growth on Si substrates is limited to temperatures below 1350 °C [65] with correspondingly lower growth rates. High growth temperatures are favorable, as stated above, for the reduction of defects, especially SFs.

Hetero-epitaxial growth of 3C-SiC on Si appears to be an ideal solution to obtain large wafers at low cost, but efforts must be made to reduce the density of crystallographic defects in the 3C-SiC films. Large lattice mismatches (19% at RT) and differences in the thermal expansion coefficients (TECs) (~23% at deposition temperatures and 8% at RT) between the two materials are the causes of defects.

In fact, lattice mismatch produces a misfit dislocation in every fifth SiC plane. The 5 : 4 SiC-to-Si lattice plane matching, defined as the “magic” by Long et al. [66], was reported by Ernst and Pirouz [67] for selected, away-from-voids, regions of a 3C-SiC thin layer. Li et al. [68] reported that when void-free film growth conditions were employed, this 5 : 4 match was extended over the length of the entire layer. Méndez et al. [69] observed with cross-section transmission electron microscopy (TEM) linear misfit dislocations with a density that corresponded to one dislocation on each four [70] Si planes and then on each five [70] SiC planes. These dislocations, as observed by filtered TEM micrographs, are mainly Lömer (90° type) dislocations and spaced about 1.61 nm from each other. Furthermore, the Lömer dislocations are much more efficient than a 60° type for relaxing the strain produced by the 20% lattice mismatch. However, misfit dislocations are not able to



**Figure 5.2** (a) STEM cross-section of a sample region where the generation process is evident. The red arrow shows the direction of the growth. (b) STEM cross-section of a sample region where the annihilation process is evident. The red arrow shows the direction of the growth.

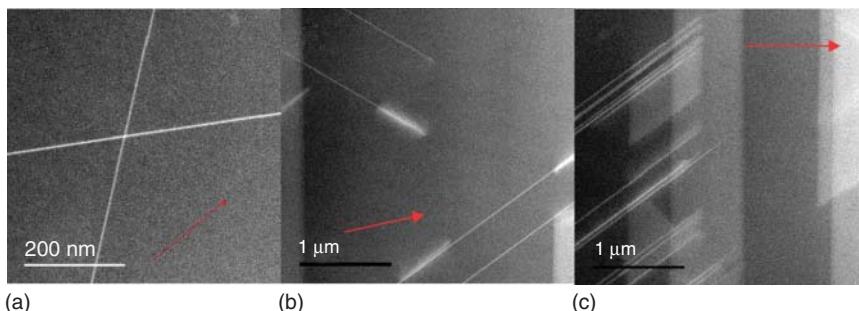
completely relieve the residual strain generated, whereby grain misorientations and SF generation are then involved.

The 3C-SiC/Si interface gives rise to a high density of planar and volume defects, such as micro-twins, APBs, and SFs in the epilayer, and voids in Si underneath the hetero-interface. Most of these defects that are considered device killers will however reduce their density, or be annihilated, when very thick (several tens of microns) 3C-SiC epitaxial films are grown. Furthermore, the orientation of the Si substrate strongly influences the defect density and surface morphology.

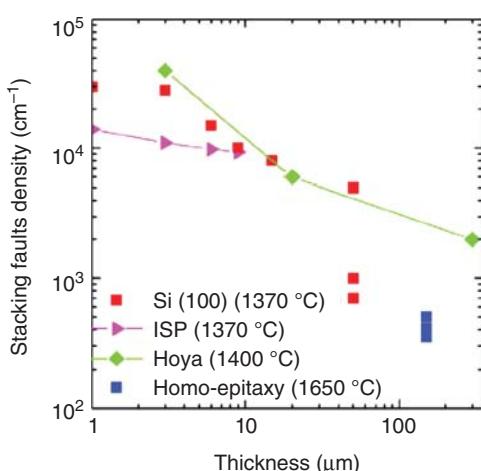
The SFs are the main defects present in 3C-SiC. Their density is typically very high and, after the fast reduction of their density in the first nanometers from the interface, the density reduction is much less evident and almost a saturation occurs close to  $10^4/\text{cm}^2$  [48]. This saturation occurs essentially because during the growth an equilibrium is reached between the annihilation and the generation of SFs. In Figure 5.2, these two phenomena are evident. In Figure 5.2a, one SF generates several SFs during the growth, while in Figure 5.2b from seven SFs only two survive after the annihilation process.

The SFs can interact in several ways. Two SFs can cross (Figure 5.3a) without annihilation, or a SF can close without interaction with another SF (Figure 5.3b) or finally can interact with a SF of different polarity (Figure 5.3c). Then the behavior and the interactions of these SFs are extremely different and probably depend strongly on the type of SFs and on the surface structure during the growth. A more detailed understanding of the SFs behavior is important to try to reduce this kind of defect that has been shown that has a big effect on the electrical characteristics of the material [61].

The trend of SF linear density (per unit length) as a function of the film thickness is displayed in Figure 5.4. Experimental data reported in the figure show an exponential decaying trend of SF density as the 3C-SiC film thickness increases. The reduction rate of SFs due to their self-annihilation is roughly inversely proportional to their density.



**Figure 5.3** (a) STEM cross-section of two SFs crossing. (b) STEM cross-section of two SFs that are closing without annihilation. (c) STEM cross-section of several SFs stopped from a SF of different polarity.



**Figure 5.4** Stacking faults density vs. grown thickness. Different processes or different substrates give different SFs densities. Source: La Via et al. [71]. © 2018, Elsevier.

This statement is further supported by Polychroniadis et al. [32], where a detailed study on the propagation of SFs using TEM in cross-section is presented. The annihilation rate of SFs is high where a very dense network of SFs is detected and the mutual closure mechanism is stimulated. As the SF density decreases, SFs are much further each other so that their annihilation rate falls and their density tends to a saturation value. Furthermore, for relatively thin ( $<5\text{ }\mu\text{m}$ ) 3C-SiC films, the APB density is high enough to ensure another closure mechanism to SFs while the density of APB in thicker films is drastically reduced so that their contribution to the reduction of SFs fails.

Using a compliance substrate as inverted silicon pyramids (ISPs)[62], a large reduction of SFs is observed for thin layer because this type of substrate concentrates SFs in small regions increasing the probability of SFs annihilation. After about 10 times the dimension of the silicon inverted pyramid ( $1\text{ }\mu\text{m}$ ), the SFs density saturates at almost the same value of the layers grown on a flat substrate because the concentration of SFs is not working anymore.

Increasing the temperature at 1400 °C, as in the HOYA experiment [32] a further reduction of the SFs density is observed. This reduction is even larger if the silicon substrate is removed and the epitaxy process is realized at temperatures higher than the silicon melting temperature as reported in Figure 5.4 for the samples grown by CVD.

From these data, it is clear that increasing the growth temperature the SFs density decreases. In a previous paper [72], it has been shown by ab initio quantum transport calculations, that SFs give rise to highly dispersive bands within both the valence and the conduction bands that can be distinguished for their enhanced density of states at particular wavenumber subspaces. The consequent localized perturbation potential significantly scatters the propagating electron waves and strongly increases the resistance for n-doped systems. No formation of levels inside the band gap has been observed by these calculations.

In addition, it is not clear which physical mechanism causes a high leakage current when a high density of SFs is observed in the material.

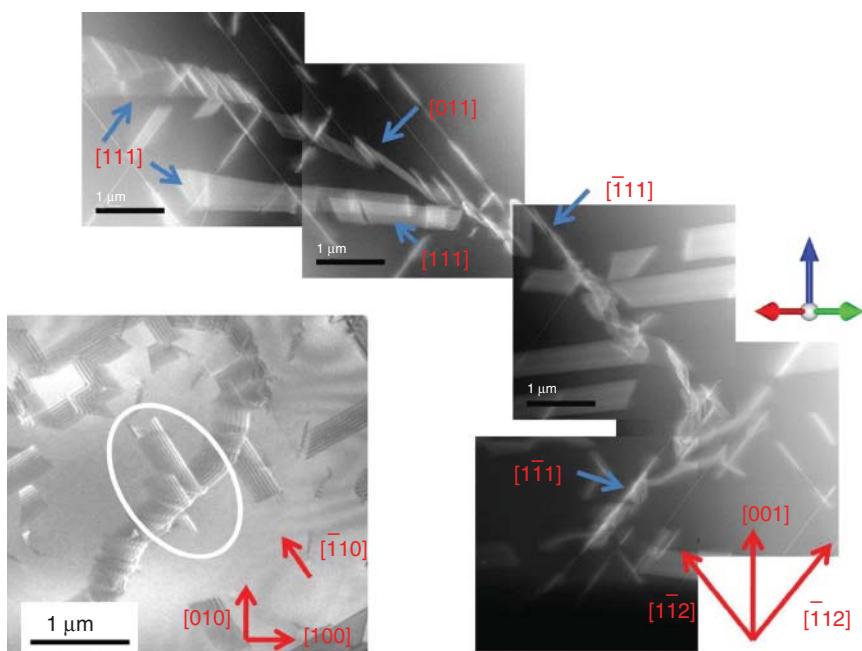
The SFs can interact also with a different kind of defect: the APB. This defect is at the edge of two different domains rotated of 90° between each other.

In order to understand the behavior of the APBs, we followed one of these boundaries through a series of cross view STEM images shown in Figure 5.5 on the right.

The growth direction ([001]) is indicated in the lower part of the image. The SFs lie always in the {111} planes and in cross view STEM images (as in Figure 5.4 right side). SFs lying in the (1–11) and (–111) plane are observed as lines in the <112> directions while SFs in the (111) and (–1–11) are observed as almost trapezoidal shaped bright zones. In the same figure, an APB is shown. APB has different lying planes: the APB lies in (1–11) plane in the bottom image of the series then it changes to (–111) plane in the third image of the series. Moreover, in the fourth image the APB lies in (011) plane and in the top left image it lies again in the (111) plane. It is worth nothing that APBs lying in the (100) plane are also observed. Additionally, in Figure 5.4 we included a STEM plane view of an APB “running” through the surface and interacting with SFs. The plan and cross view images show APBs changing their lying plane. A detailed inspection of the image shows that the APB lying planes are only specific planes (i.e. the {111}, {011}, and {001}) and a process of faceting occurs when a GB curves. In such a way, at low magnification, it is able to “curve” through the sample. Another very important fact that can be understood from this image is that APBs and SFs strongly interact as highlighted with the white circle in the bottom left image.

Another defect that has a large influence on the growth of thick layers is the protrusion [57]. This defect is a small polycrystalline region that starts to grow in the first instants of the growth and becomes bigger and bigger increasing the thickness.

We observed that the presence of the protrusion was not strongly correlated with voids commonly observed at the SiC/Si interface. Instead, we found that seeds for protrusions lie 10 nm into the SiC layer above the SiC/Si interface. This finding indicated that protrusion seeds form during or just after the carbonization process [57].



**Figure 5.5** The sequence of STEM images shows an APB and its effect on SFs. Image is the projection of the lamellae in the (110) plane. The growth direction ( $[001]$ ) is indicated at the bottom, the lying plane of the GB for each image is also indicated, and the scale bar is the same for all images. The growth was performed in the  $[001]$  direction and  $(110)$  is the cross view STEM projection plane. In the left bottom, a plane view STEM image shows an APB interacting with SFs in the highlighted regions.

### 5.2.3 Stress

Growing 3C-SiC films on a Si substrate inherently means two dissimilar materials are forced together creating several results in the subsequent epitaxy. First, a large strain is generated at the hetero-interface due to a misfit,  $\Delta a/a$ , of about 19.7% resulting from the difference in bulk lattice parameters of 3C-SiC and Si of 4.3589 and  $5.4311\text{ \AA}$ , respectively [46]. This strain is called the “intrinsic strain,” which contributes to the residual strain field and a high density of crystallographic defects close to the interface is generated in the 3C-SiC film in order to relieve the most of it.

The large mismatch in TECs between Si and SiC is the second contribution to the strain field. The thermal strain acts mainly during the cool down from the growth temperature to room temperature. TECs of Si and SiC at room temperature are  $2.77 \times 10^{-6}\text{ K}^{-1}$  and  $2.57 \times 10^{-6}\text{ K}^{-1}$ , respectively, as tabulated by Slack and Bartram [73], leading to a TEC mismatch of about 8% at RT. At growth temperature, the difference in the TECs between SiC and Si increases reaching percentages above 20%, which is dependent on the growth technique used and gaseous precursors involved, but often over  $1000^\circ\text{C}$ . The stress generated during the cooling down from growth temperature is of a tensile nature and causes an upward bending in the wafer and, often, the generation of cracks in the epitaxy and in the substrate. The

bending, referred to “wafer bow,” depends on the thickness of the 3C-SiC epitaxy, thickness of the Si substrate, symmetry (orientation) of the epitaxial crystal and substrate, and elastic modulus.

The curvature resulting from the residual stress can be calculated using a modified Stoney equation that takes into account the film elastic relation to wafer bending: [74]

$$\sigma = \frac{M_{\text{film}} h}{\Delta R} \left( \frac{1 + 4mn + 6mn^2 + 4mn^3 + m^2n^4}{6mn(1+n)} \right) \quad (5.1)$$

where  $m = M_{\text{film}}/M_{\text{sub}}$  is the biaxial modulus ( $M = E/(1-\nu)$ ) of the film substrate and  $n = t/h$ , where  $t$  and  $h$  are the thicknesses of the substrate and film, respectively. The Young's modulus ( $E$ ) and Poisson's ratio ( $\nu$ ) are related to the film orientation.  $\Delta R$  is the change in curvature radius determined from  $(1/R) = (1/R_2) - (1/R_1)$ , where  $R_1$  is the average radius of the substrate prior to film deposition and  $R_2$  after the film is deposited.

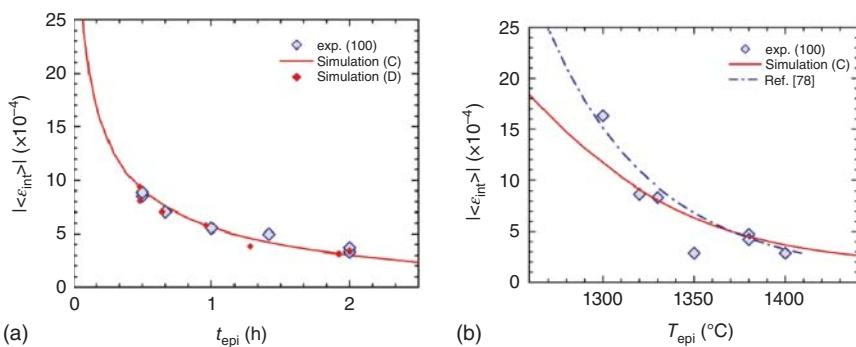
A micro-machined planar rotating probe was developed for residual stress analysis to split the stress into the following two components: (i) the gradient residual stress ( $\sigma_1$ ) related to the film defects and (ii) the uniform stress ( $\sigma_0$ ) related to the substrate [75]. TEM characterization studies about the defect formation and the defect evolution as a function of thickness on 3C-SiC on the Si substrate revealed the problems due to the incorrect linear stress approximation in a hetero-epitaxial thin film. With FEM, an exponential approximation of the stress relationship was studied, yielding a better fit with the experimental data.

Another important aspect that has been observed in 3C-SiC and that has a large influence on both the bow of the wafer and on the use of this material for micro-electron mechanical systems (MEMS) is the variation of the Young's modulus ( $E$ ) as a function of the thickness. In fact, due to the presence of a large density of defects at the interface with silicon which is slowly decreasing with the increasing of the layer thickness, the Young's modulus varies from  $1.5 \times 10^{11}$  Pa to  $4.1 \times 10^{11}$  Pa. Then the interface region of the 3C-SiC layer is less rigid with respect to the surface region.

The main parameters for the reduction of the intrinsic stress are the growth rate [76] or the growth time (for the same thickness) and the growth temperature [77]. In fact, it has been observed (Figure 5.6) that decreasing the growth rate and increasing the growth temperature we can observe a decrease of the stress. This effect is probably due to the “creep effect,” i.e. the slow, plastic relaxation of the material occurring through the continuous introduction and/or movement of extended defects (SFs, twins, and dislocations) within the material volume, and not only at the growth front.

## 5.3 Bulk Growth of 3C-SiC

Bulk growth of hexagonal polytypes (4H- and 6H-SiC) using physical vapor transport (PVT) method can be considered mature. Today, wafers with diameters of 200 mm and dislocation densities as low as  $2800 \text{ cm}^{-2}$  [79–81] can be called



**Figure 5.6** Mean intrinsic strain in 3C-SiC(100) as a function of the growth duration  $t_{\text{epi}}$  (a) and of the growth temperature  $T_{\text{epi}}$  (b). Source: Zielinski et al. [77]. © 2012, AIP Publishing.

standard for 4H-SiC. However, the method of continuous growth and enlargement as it is performed in PVT growth of hexagonal SiC cannot be employed for 3C-SiC. This is due to the growth conditions required to achieve stable growth of 3C-SiC, namely high vertical temperature gradients and a sufficient supersaturation of the silicon-containing gas phase. Therefore, the epitaxial sublimation growth (SE) method using a sublimation sandwich approach as presented by Tairov et al. [82] in 1976 was implemented and demonstrated the suitability to grow 3C-SiC [26, 83]. Besides that, various other bulk growth processes for 3C-SiC have been presented over the last decades, such as the modified PVT (M-PVT) or the continuous-feed PVT (CF-PVT) method [33, 84]. Up to now, only the epitaxial sublimation growth approach has generated 3C-SiC material with dimensions which can be called bulk [71, 85–88]. All these bulk growth methods have in common that they suffer from a lack of appropriate high-quality seeds, which hindered the development of such approaches for many years. However, such seeding material can be obtained by using 3C-SiC layers, which were hetero-epitaxially grown on silicon substrates by CVD [57, 71, 89]. Even though this approach still faces some challenges in the handling of the fragile CVD-grown seeds, reasonable results could be obtained in recent years [71, 85–88].

Indeed, one of the main challenges for the bulk growth of 3C-SiC by epitaxial sublimation growth, as well as for CVD, lies in CVD growth of the seeding material. Differences in the lattice parameters and TECs between 3C-SiC and silicon lead to CVD layers that feature high levels of stress which can result in the bending of the whole wafer and even cracking of the material. The subsequent processing of such bended layers in order to use them as seeds for SE still slows down the upscaling of this approach.

### 5.3.1 Sublimation Growth of (111)-oriented 3C-SiC on Hexagonal SiC Substrates

In the past, valuable work has also been done on the growth of (111)-oriented 3C-SiC on hexagonal SiC substrates [31, 37]. It shall be pointed out that this material was of very high crystalline quality. However, the high-quality material could only be

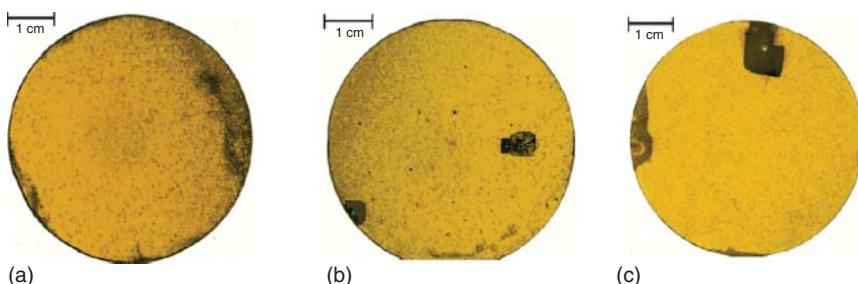
obtained on small areas (<2-in.) as DPBs propagate the material. As DPBs as well as the limitation to (111)-oriented material are not favorable for electrical devices, this approach could not demonstrate its practicability so far.

### 5.3.2 Sublimation Growth of 3C-SiC on 3C-SiC CVD Seeding Layers

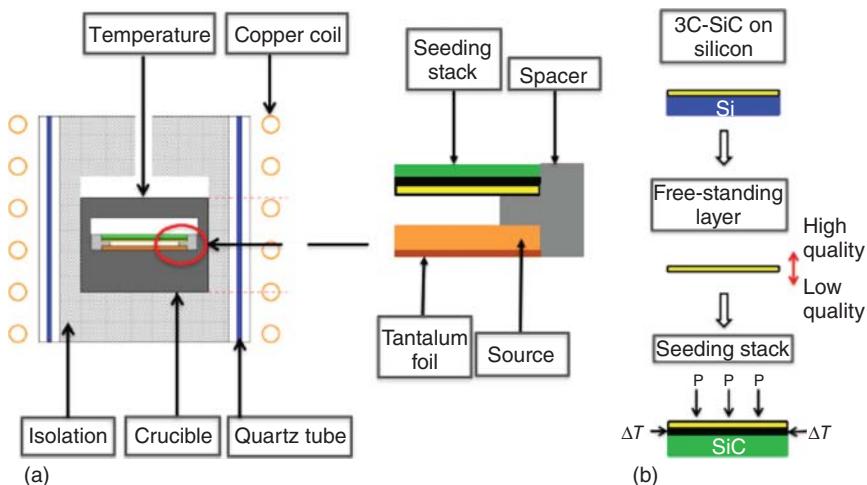
On the other hand, applying epitaxial sublimation growth on CVD-grown seeds led to remarkable results, namely the reproducible growth of (100)-oriented 2-in. 3C-SiC with thickness up to 870 µm as can be seen from Figure 5.7. The growth rates for such layers typically lie between 160 and 320 µm/h. These results represent a milestone in the growth of large area bulk 3C-SiC as such layers with a thickness of approximately 1 mm will in principle allow the consecutive growth using methods like M-PVT or CF-PVT.

The layers depicted in Figure 5.7 represent the first quasi-bulk 3C-SiC material of relevant size produced by sublimation method on a regular base. The optical appearance of all crystals features a bright yellow color which is typical for cubic SiC. X-ray diffraction (XRD) and Raman spectroscopy confirm the growth of 3C-SiC. However, as can be seen from Figure 5.7 the layers still suffer from many defects. The typical defects in (100)-oriented 3C-SiC crystals are SFs, APBs and protrusions. Therefore, the small dark spots on the 3C-SiC layers in Figure 5.7 can be mainly assigned to protrusions which were already present on the CVD-grown seeds and increase in size during epitaxial sublimation growth. Dark areas on the outer edges of the layers can be assigned to defects which were generated by carbon contaminations on the seed surface. Such contaminations originate from the seed-mounting process and insufficient cleaning of the seed. The large dark areas in Figure 5.7b,c arose from areas featuring a burst of the seed layer.

The hot-zone for epitaxial sublimation growth can be realized in a state-of-the-art PVT reactor. In order to meet the aforementioned requirements for stable growth of cubic SiC, the hot-zone for a sublimation sandwich features some typical characteristics [36, 85]. High vertical temperature gradients are realized by a small distance



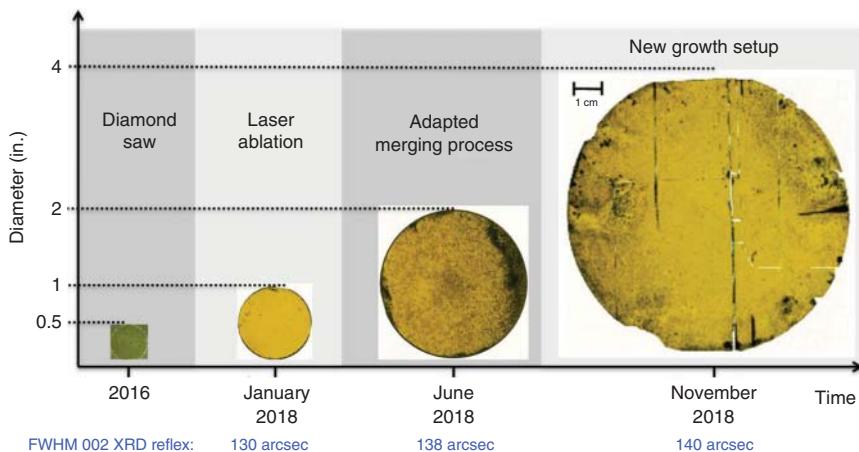
**Figure 5.7** Transmitted light images of free-standing 2-in. wafers with thickness of (a) 870 µm, (b) 780 µm, and (c) 500 µm. The small dark spots on the samples can be mainly assigned to defects like protrusions and carbon inclusions. The larger dark areas in (b) and (c) can be assigned to burst areas of the seed layer. Source: Reproduced with permission of Schuh et al. [86].



**Figure 5.8** Growth-setup for epitaxial sublimation growth and transfer-process for the preparation of seeding-stacks. (a) Schematic of a physical vapor transport (PVT) setup used for epitaxial sublimation growth with the reactor (left) and the hot-zone (right). (b) Schematic manufacturing process for seeding-stacks used in the hot-zone for epitaxial sublimation growth. Source: Schuh et al. [88]. Licensed under CC BY 4.0.

between source material and seed. Usually, both are separated by a thin graphite spacer. A silicon-rich gas phase can be achieved by introducing a carbon getter, namely tantalum, into the growth cell. The supersaturation goes along with the temperature gradient. Hence, starting from the bottom of the growth cell in Figure 5.8a, a tantalum foil lies below the sandwich. On top, a SiC source material, usually polycrystalline SiC, is placed. A graphite spacer determines the distance between source and seeding-stack.

In order to use CVD-grown 3C-SiC layers as seed, a seeding-stack needs to be prepared according to Figure 5.8b. This is necessary to mechanically stabilize the thin (typically  $20\text{ }\mu\text{m}$ ) 3C-layers and to prevent backside sublimation of the seed during sublimation growth. Starting from 3C-SiC-on-Si wafers that were produced by CVD, a seed of the desired dimensions is prepared by using a multi-pulse laser ablation technique [90, 91]. Subsequently, the silicon substrate is removed using wet-chemical etching by HNA ( $\text{HF}:\text{HNO}_3:\text{H}_2\text{O}$ ) resulting in a free-standing 3C-SiC layer with a high-quality growth front and a low-quality former 3C-SiC/Si interface. The free-standing 3C-SiC seed is attached to polycrystalline SiC carrier using a carbon glue. The carrier serves as mechanical support and backside protection. With that transfer process, crystals of 2-in. in diameter have been grown reproducibly. The preparation of 4-in. layers has in principle been demonstrated, too, as can be seen from Figure 5.9. However, at present the transfer of seeding layers with diameters  $>2$ -in. is still subject to some difficulties. On the one hand, the handling of the fragile 3C-SiC seeds becomes more difficult with increasing diameter. This obstacle could partly be overcome by a reduction of stress and bow in the CVD seeds. On the other hand, the processing of the seeding stacks for SE growth needs to be adapted for

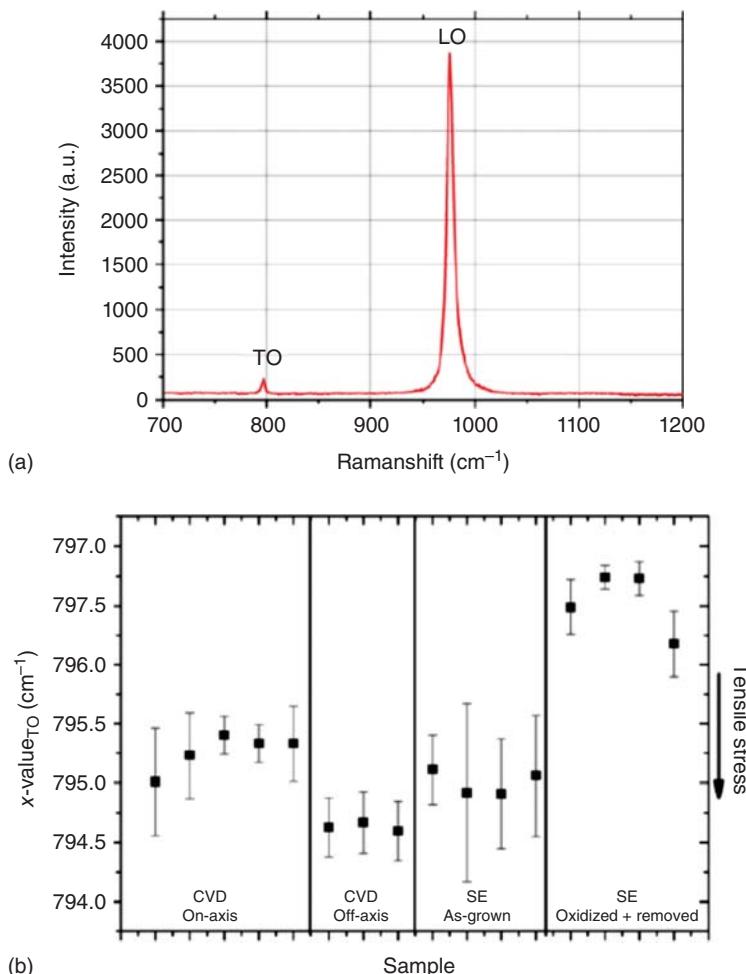


**Figure 5.9** Evolution of diameters for bulk 3C-SiC crystals grown by epitaxial sublimation growth. The timeline and the full-width-at-half-maximum (FWHM) values from XRD-rocking curve measurements are indicated.

large diameters. All these challenges are likely to be solved by adaptions concerning the wet-chemical etching procedure and the geometry of the sublimation sandwich.

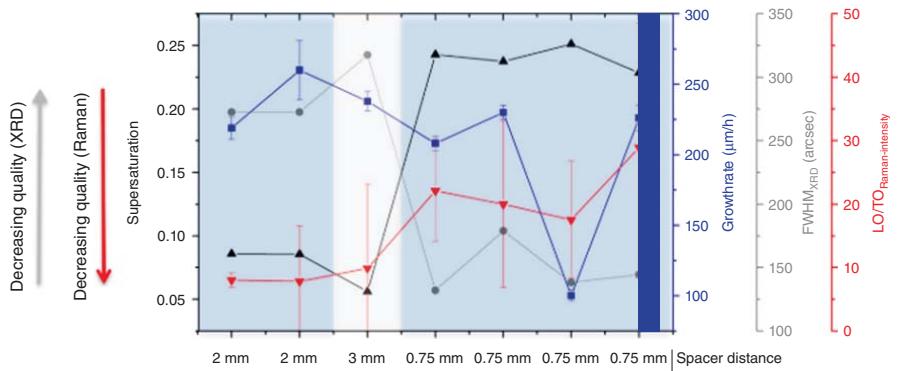
Even if there are still many defects present in the material, the quality of sublimation grown bulk 3C-SiC can be designated as “high-quality.” Raman analysis of a defect-free surface area on a SE-grown material is depicted in Figure 5.10a. For defect-free (100)-oriented on-axis material, the transverse optical (TO) mode is forbidden. If the TO-mode is visible anyway, its position can be used as a measure for the stress within the material [92]. The diagram in Figure 5.10b shows the wavenumbers of the TO-mode for typically stressed CVD-grown material on on-axis and off-axis silicon substrates as it was used as seeds for the aforementioned sublimation grown crystals. From these data, a tensile stress is visible in both materials. In comparison, as-grown SE-material features similar values as CVD material which was grown on on-axis substrates. If sublimation growth on seeding-stacks is applied, a temperature treatment at 800 °C is usually performed after the growth in order to oxidize the carbon glue and remove the SE layer from the remaining part of the carrier. Such material features a reduction of stress toward 797 cm<sup>-1</sup>, as obvious from Figure 5.10b. Therefore, free-standing sublimation grown bulk 3C-SiC can be considered as quasi stress free.

When it comes to real bulk growth, the thickness of the crystals is the significant value of interest. Therefore, the source-to-seed distance which is set by the spacer determines the maximum achievable thickness. Figure 5.11 depicts calculated values of the supersaturation for different source-to-seed distances (0.75, 2, and 3 mm). The supersaturation which is influenced by the temperature gradient and therefore depends on the source-to-seed distance is the critical parameter in order to evaluate the conditions for stable growth of 3C-SiC. Besides supersaturation, data from Raman spectroscopy and XRD are shown. For the analysis of XRD-rocking curve data, the full-width-at-half-maximum (FWHM) of the 002 reflex is used. Raman



**Figure 5.10** (a) Raman spectrum of typical sublimation grown material acquired in a protrusion-free surface area. (b) Comparison of the  $x$ -value for the transverse optical (TO) Raman mode of 3C-SiC epitaxial layers grown by chemical vapor deposition (CVD) on on-axis and 4° off-axis substrates, homo-epitaxial as-grown material produced by epitaxial sublimation growth (SE), and SE material after temperature treatment. Source: Schuh et al. [86].

results were obtained using the ratio of the intensities of the longitudinal mode (LO) and the TO-mode. From both characterization methods follows a similar trend. A decrease of supersaturation, created by an increase of the source-to-seed distance, results in a decrease of overall material quality. The FWHM values vary from close to 120 arcsec for 0.75 mm spacer to 325 arcsec for 3 mm spacer. In Figure 5.9, the FWHM values for XRD-rocking curve measurements are given for bulk 3C-SiC of different diameters. FWHM values between 130 and 140 arcsec are almost comparable with those of high-quality material grown on hexagonal SiC substrates, which can be lower than 120 arcsec [83].



**Figure 5.11** Calculated supersaturation of the  $\text{SiC}_2$  gas species for experiments with different source-to-seed distances (black). The intensity ratio of the LO and TO-mode from Raman spectroscopy (red), XRD measurements of the 002 peak and the FWHM (gray), as well as the growth rate (blue) is given. Source: Schuh et al. [88]. Licensed under CC BY 4.0.

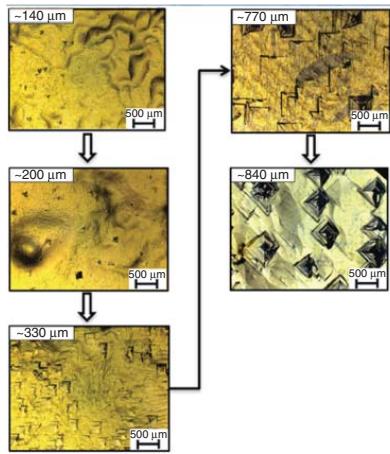
It should be noted that bulk growth of 3C-SiC by epitaxial sublimation growth is subject to some limitations. Up to now, the main problem is the protrusions defect as already mentioned. This three-dimensional defect occurs during the initial stage of 3C-SiC growth on silicon substrates by CVD. As such material is used as seed for epitaxial sublimation growth, these defects are present in sublimation grown 3C-SiC, too. Zimbone et al. [57] reported that this kind of defect already tends to increase in size with increasing 3C-SiC thickness during CVD growth. This trend can also be observed for subsequent SE growth [93] as the protrusions continue to grow. A set of optical images of SE layers with different thickness are depicted in Figure 5.12a. A continuous increase of protrusion dimensions can be observed for increasing thickness of the bulk material. The diagram in Figure 5.12b shows the length of the protrusion base derived from as-grown surfaces of 3C-SiC vs. the thickness of the layer. At least for the investigated parameter range, a linear behavior can be observed. As a consequence, as long as protrusions cannot be initially avoided, the amount of high-quality protrusion-free material is limited by the density of protrusions on the seeds used for bulk growth of 3C-SiC. Bulk layers with thickness of 2.7 mm have been grown which showed a macroscopic surface roughening due to a complete covering with protrusions. In this context, it is pointed out that keeping stable growth conditions for 3C-SiC, in particular regarding supersaturation, for larger source-to-seed distances is still a matter of research. With numerical simulation, the temperature gradients within the sublimation sandwich can be calculated. Using these gradients, the partial pressure of the growth-limiting SiC<sub>2</sub> gas species can be accessed in order to approximate the supersaturation. Hence, for the growth of 3C-SiC on 3C-SiC seed layers, a supersaturation of 0.1 or above is assumed to be necessary in order to ensure stable growth conditions [88].

While protrusions can be considered a serious issue to be solved in future, the quality of SE layers is quite good regarding SF. If CVD-grown 3C-SiC is used as seed for epitaxial sublimation growth, a defect-rich transition layer is formed between CVD seed and SE layer. Within this area, the SF density increases significantly. However, with increasing 3C-SiC thickness the SF density decreases again during SE growth. As soon as a total thickness of approximately 175 µm is exceeded, the SF density of the SE-layer lies below the value for the used CVD seed (Figure 5.13) [93].

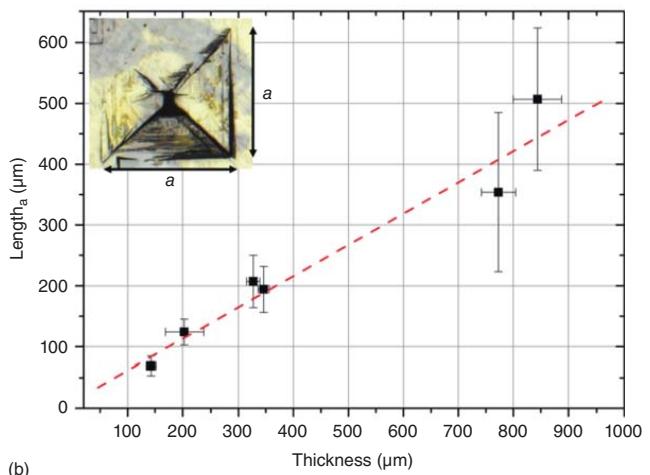
From Raman, XRD, and SF characterization follows, that epitaxial sublimation growth can considerably improve the quality of material grown by CVD. If the density of protrusion defects as well as the wafer bow can be reduced or even avoided in future, the growth of high-quality bulk 3C-SiC comes within tangible reach.

### 5.3.3 Continuous Fast CVD Growth of 3C-SiC on 3C-SiC CVD Seeding Layers

The main issue to develop the 3C-SiC devices is the lack of available material [71]. Bulk crystal with good crystal quality is not yet commercially available. This limitation is probably due to the fact that almost all of the studies related to 3C-SiC growth were performed using Si as substrate for the epitaxial process. Actually, the hetero-epitaxial system is limited by the high lattice mismatch between SiC and Si

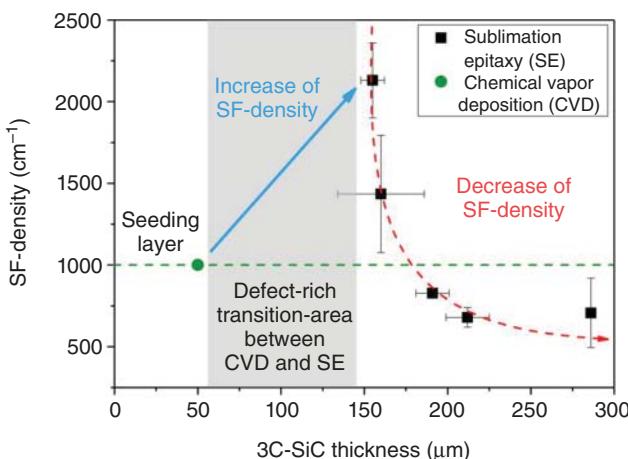


(a)



(b)

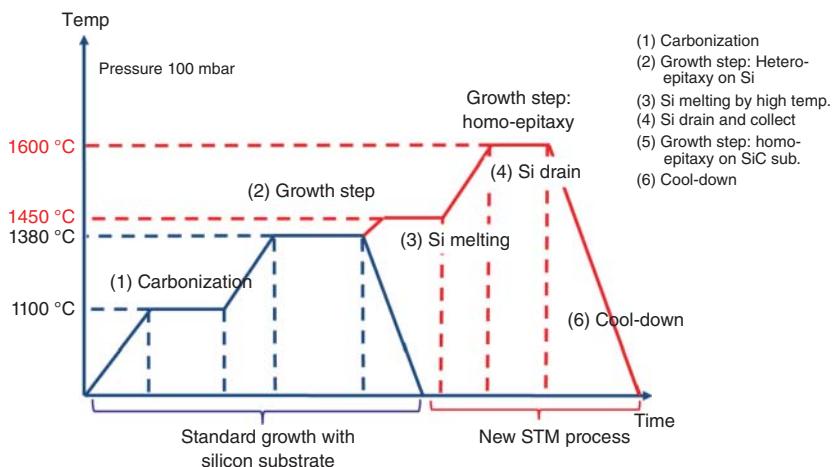
**Figure 5.12** (a) Evolution of protrusion dimensions for bulk 3C-SiC layers with different thickness. (b) Edge-length of protrusions plotted vs. 3C-SiC thickness. Source: Reproduced with permission of Schuh et al. [88].



**Figure 5.13** Stacking fault (SF) density vs. thickness of SE-grown 3C-SiC layers extracted from KOH etched samples. After an initial rise of SF-density within the transition area between CVD and SE, the density of SFs decreases with increasing 3C-SiC thickness and declines below the value of the used CVD seed. For comparison, the SF-density of HOYA sample grown by Switch-Back-Epitaxy is presented [61]. Source: Adapted from Schoeler et al. [93].

(20%), and the difference in TEC that generates a very high density of defects during the growth of the layers and the cool down, respectively [56, 73]. In the last decades, many efforts have been devoted to search technologic feasible growth techniques to overcome such limitation.

After the initial attempt by Nishino et al. [94], when he proposed a multi-step CVD process able to ensure an improvement in the crystal quality of the 3C-SiC epitaxial layers, and today thick 3C-SiC films have been commonly grown on carbonized Si substrates by CVD. Important progresses have been demonstrated using patterned (undulant) silicon substrates [65] followed by the switch-back epitaxy process. This technique seems to be promising but the wafer bending issue remains unsolved. Another way is to use a silicon substrate with ISPs [62]. Using ISP substrate, a reduction of SFs is observed for thin layer because this substrate allows the probability of SFs annihilation, but the substrate manufacturing is not easy. Different approaches are being developed to find a convincing alternative to 3C-SiC/Si hetero-epitaxial system. In order to grow 3C-SiC bulk material of 4 and 6 in., a new epitaxial reactor chamber has been designed and tested. The main idea is to grow a hetero-epitaxial layer as seed, melt the silicon substrate, and continue the growth at high temperature. In this way, it will be possible to grow a bulk substrate of 3C-SiC with a low density of SFs and low wafer bow. In fact, the bow can be strongly decreased, because by removing silicon, one of the main components of the stress due to the different TEC between the two materials is completely eliminated. The removal of silicon gives also the possibility of a large increase in the growth temperature and in the growth rate, and then thicker wafers and better material can be grown.



**Figure 5.14** Schematic of the new CVD growth process of the 3C-SiC bulk wafer with the silicon melting after the first epitaxial growth on silicon substrate.

In order to grow bulk material of 4 and 6 in., a new chamber for the CVD hot wall commercial reactor has been designed and tested. The main idea described in the patents submitted by STMicroelectronics [95–97], is to grow a thick hetero-epitaxial layer on silicon substrate (4 or 6 in.) with a standard process, melt the silicon substrate by a dedicated new reaction chamber within the CVD reactor, where the Si can drain through the susceptor and continue the growth at high temperature (standard homo-epitaxial process). In this way, it will be possible to grow a bulk substrate of 3C-SiC with a low density of SFs and low bow.

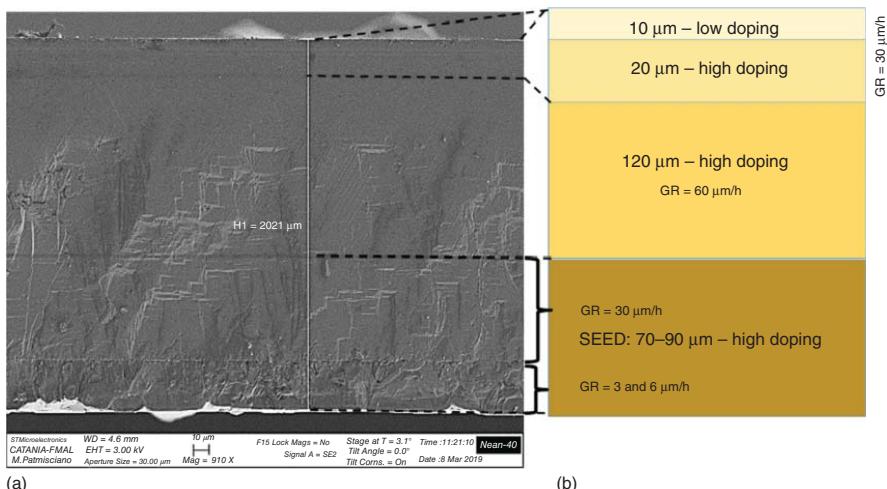
A large set of experiments have been performed to understand how to melt the silicon substrate, how to drain it, how to etch the remaining silicon, and how to grow the homo-epitaxial layer on the 3C-SiC substrate obtained after the silicon melting. In Figure 5.14, a scheme of the entire process is reported. The first two steps are the standard ones (well reported and described in literature). The growth of 3C-SiC seed was performed with an epitaxial CVD process, in a horizontal hot-wall reactor (LPE) on Si(100) substrate. Trichlorosilane ( $\text{SiHCl}_3$  or TCS), ethylene ( $\text{C}_2\text{H}_4$ ), and hydrogen ( $\text{H}_2$ ) were used as silicon and carbon precursors and gas carrier, respectively. The first step (i) is the carbonization steps where, after a vacuum bake of the reactor, to decrease the nitrogen contamination of the reaction chamber and a  $\text{H}_2$  etching of the silicon surface is performed at a temperature of 1100 °C for 10 minutes, at the same temperature, the carbonization was performed for a fixed time of 5 minutes with only carbon precursor inside the chamber [56, 57]. For the second step (ii), the process was carried out in a low-pressure regime (100 mbar) at a temperature of 1380–1400 °C (very close to the silicon melting temperature).

The growth starts at 3  $\mu\text{m}/\text{h}$ , then increases to 6  $\mu\text{m}/\text{h}$  and finally further increases to 30  $\mu\text{m}/\text{h}$ . With this process, a thick layer of about 90  $\mu\text{m}$  has been grown. Subsequently, the temperature was increased above the melting point of silicon and the Si substrate was completely melted inside the CVD reactor.

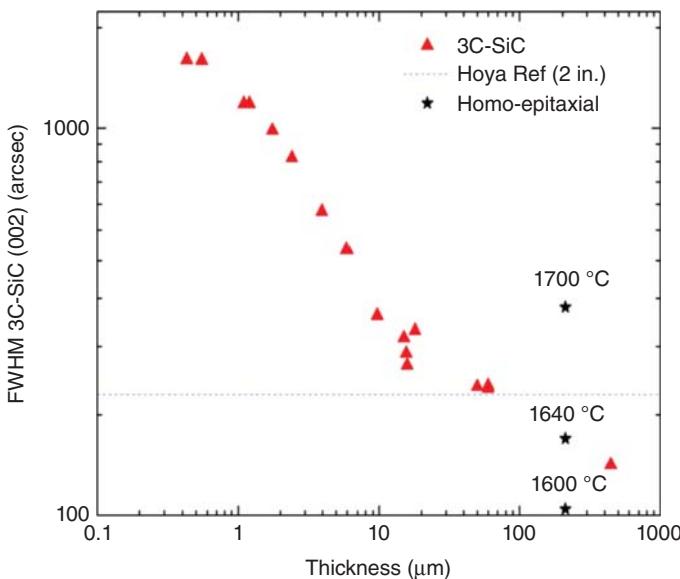
The remaining freestanding SiC layer is used as a seed layer for a subsequent homo-epitaxial growth. The processes were obtained in a low-pressure regime at different temperatures in the range between 1600 and 1700 °C. It was used a growth rate of 60 µm/h for two hours to increase the substrate thickness and at 30 µm/h for the last one hour to further improve the quality of the material as previously reported. While the first 20 µm of the last step has been highly doped, the final 10 µm is low doped for device realization. Nitrogen was used as doping species for  $n+$  and n-type layers formation. After the homo-epitaxial deposition, the total thickness of 3C-SiC samples was about 200 µm (observed by SEM analysis).

The structural investigation of the entire 200 µm thickness film was performed by SEM in cross-section, where the 3C-SiC film (seed and homo-epitaxial layer) is observed (Figure 5.15). Figure 5.15 shows different layers within the film: starting from the bottom, first the seed of 90 µm and next, the homo-epitaxial layer grown after the fusion of Si. The seed shows different layers with different growth rate, with more defects close to the old silicon interface. With increasing growth rate, the seed exhibits a decrease of the defect density. The seed shows the decreasing of defects increasing the growth rate. The second step is made up of the homo-process that reveals a lower thickness value (around 120 µm) compared to the predicted one (150 µm of Figure 5.15b). From the figure, the change in the doping concentration is also visible close to the film surface (10 µm thickness layer with low doping concentration close to the surface).

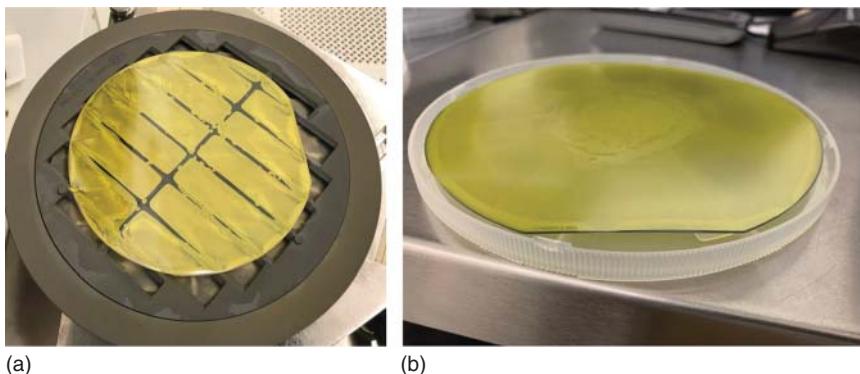
The investigation of the temperature influence on the homo-epitaxial process was evaluated by XRD analysis (Figure 5.16). The FWHM on the X-ray rocking curve of the 3C-SiC (002) peak is related to the crystal quality and defect density (decrease the FWHM increases the crystal quality). The figure shows the trend of FWHM as a function of film thickness for different samples growth also in different condition (all the samples at low value of thickness are coming from previous experiments [71]). It is well known that by increasing the film thickness, the quality of the material increases [64]. The first part of the curve (from 0 to about 20 µm of thickness) shows the 3C-SiC samples growth with Si substrate. For such samples, the crystal quality is limited by the present of silicon substrate that starting from about 20 µm of thickness introduces many cracks and extended defects during the cooling down after the growth [71]. The three points between 60 and 90 µm are the 3C-SiC samples without silicon substrate (after Si fusion) with a good crystal quality (around 200 arcsec), comparable with an old 2 in. 3C-SiC wafer provided by HOYA corporation (dotted line). These samples are the substrates used as template for the homo-epitaxial process of this experiment. The stared points (three at 200 µm) are the samples grown by using the new melting technique described in the present work. They are grown at three different temperatures (1600, 1640, and 1700 °C). The graph clearly shows the sample grown at 1600 °C is significantly better than the other two [98]. Indeed, it has a FWHM value of around 100 arcsec that is very promising also compared to a thicker sample (about 400 µm) grown by sublimation epitaxy (PVT reactor) at high temperature [87].



**Figure 5.15** (a) Cross-section SEM image of the 3C-SiC wafer (about 200  $\mu\text{m}$ ). (b) Schematic representation of the structure: hetero-epitaxial seed and homo-epitaxial layer. Layers have different doping concentration and growth rate. Source: Anzalone et al. [98]. Licensed under CC BY 4.0.



**Figure 5.16** FWHM of the X-ray rocking curve as a function of film thickness for different value of temperature and compared with other reference samples. Source: Anzalone et al. [98]. Licensed under CC BY 4.0.



**Figure 5.17** The 3C-SiC 6 in. wafer after the total process. (a) The wafer on the subsector (with silicon not totally melted) and (b) after the total silicon melting.

According to the patent [97], many melting experiments (on 4 and 6 in.) have been performed with the susceptor structure reported in Figure 5.17a. As can be observed in this figure, the main problem observed with this structure was the uncomplete etch of silicon in the internal regions of the wafer (dark zone).

In the successive experiments, using long melting process time and long etching time, it was possible to completely remove this silicon residue.

Finally, with a further susceptor structure tested, a better uniformity of the temperature with respect to the standard structure, the silicon has been successfully removed during the melting and etching process.

It has also been observed that the removal of the silicon substrate releases the tensile stress of the wafer and only the intrinsic stress is present. Then new experiments on the carbonization and growth should be done to decrease this stress and obtain a flat wafer.

## 5.4 Processing and Testing of 3C-SiC Based Power Electronic Devices

### 5.4.1 Prospects for 3C-SiC Power Electronic Devices

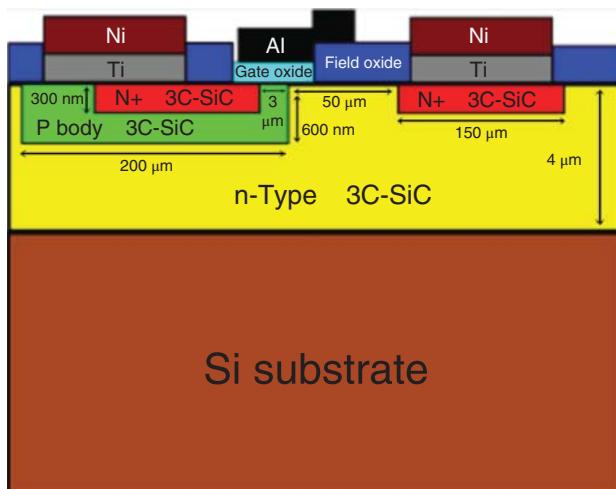
The past number of years has heralded the dawn of the electric revolution in terms of consumer products, transportation, energy generation, and distribution. Various reports have predicted that 60–80% of global energy demand will be provided in the form of electrical power [99, 100] over the coming decades. This places power electronics at the forefront of technological priorities, with the majority of this electrical energy passing through some form of converter.

It is generally accepted that 3C-SiC can occupy the 600–1000 V range, given its band gap value of 2.4 eV. Although the 3C-SiC band gap is narrower than its 4H-SiC counterpart, this brings about many positives in terms of on-state operation. A narrower band gap lowers the conduction band minimum, resulting in a reduced density of states at the  $\text{SiO}_2$ /3C-SiC interface.

Therefore, MOSFET fabricated in 3C-SiC have already achieved a channel mobility up to  $300 \text{ cm}^2/(\text{V s})$ . This is the highest realized on any of the SiC polytypes, demonstrating the potential reduction in power consumption of these promising switching devices. Furthermore, the bulk mobility for electrons,  $1000 \text{ cm}^2/(\text{V s})$  is slightly higher than that of 4H-SiC, offering a similar drift region resistance. The thermal conductivity is  $3\text{--}4 \text{ W}/(\text{cm K})$  allowing for harsh environment operation with some early reports showing the drift region temperature coefficient (bulk mobility degradation) being 10% lower compared to 4H-SiC ( $200^\circ\text{C}$ ). This offers enhanced drift region resistance and more realistic junction temperatures.

### 5.4.2 3C-SiC Device Processing

In spite of these potential advantages, the application of 3C-SiC in power device technology remains limited by the material quality, which in turn is strongly related to the growth techniques [101]. Figure 5.18 shows the cross-section of a typical research-grade 3C-SiC MOSFET fabricated by Li [102]. This device architecture for 3C-SiC is prevalent in the literature and as can be inferred from this figure, the required processing technology is similar to that of conventional silicon and 4H-SiC device topologies. On-going research into the fundamental device building blocks, including the 3C-SiC/ $\text{SiO}_2$  interface, ion implantation, and metal/semiconductor contacts, has been reported in the literature. However, these initial studies have been significantly influenced by the quality of the 3C-SiC material (e.g. defect density, surface roughness, surface preparation, etc.) [71].



**Figure 5.18** A cross-sectional representation of a 3C-SiC LDMOSFET. Source: Adapted from Li [102].

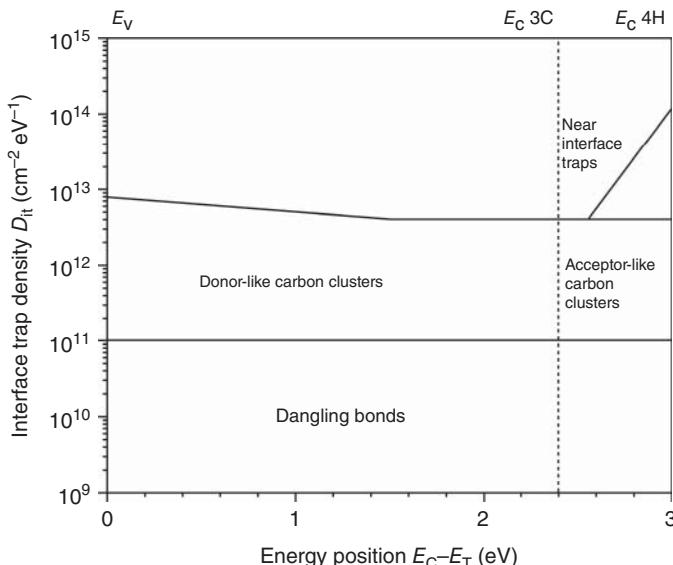
### 5.4.3 MOS Processing

With its superior electrical properties and the ability to be thermally oxidized, it is no surprise that there is positivity around the prospects for SiC MOS devices. Commercial 4H-SiC is the most prominent SiC polytype. The hexagonal lattice of 4H-SiC means there will be several faces available for oxidation. Most research has been devoted to the (0001) Si-face, the only one available in commercial wafer form. There have been studies suggesting that MOS interface traps for all SiC polytypes are similar [103]; thus, the study on the 4H-SiC/SiO<sub>2</sub> interface also provides a great insight for 3C-SiC. Unfortunately, the 4H-SiC/SiO<sub>2</sub> interface turns out to be quite poor and the electrical performance is not even close to its Si counterpart. The interface trap density ( $D_{it}$ ) on the as-grown 4H-SiC/SiO<sub>2</sub> interface is typically close to  $10^{13} \text{ cm}^2/\text{eV}$ , which is two orders of magnitude higher than more conventional Si/SiO<sub>2</sub> interfaces [104]. After decades of study, the reasons behind the poor 4H-SiC/SiO<sub>2</sub> interface are still not fully understood. Afanasev et al. [105] discussed the potential origins of this high density of interface traps, with two sources being identified, the first of which is the carbon accumulated at the MOS interface during the SiC oxidation process.

The theory of carbon failing to escape through thicker oxides naturally leads to the idea that there should be less carbon at the MOS interface with respect to thinner oxides. Indeed, a recent study [106] demonstrated an almost ideal SiC/SiO<sub>2</sub> interface with a very thin oxide layer ( $\approx 14 \text{ nm}$ ), the  $D_{it}$  value reported was less than  $10^{11} \text{ cm}^2/\text{eV}$ . However, a certain oxide thickness ( $\approx 50 \text{ nm}$  for SiC MOS devices) is necessary for a reasonable threshold voltage, which renders this thin oxide approach impractical for real device fabrication. Thin thermally grown oxides with a deposited oxide above may be an option but are still not straightforward. This is since a deposited oxide is known to contain many more defects than its more traditional thermally grown equivalent [107]. This leads to the second source of

SiC/SiO<sub>2</sub> interface traps, namely oxide defects. Oxide defect induced traps are essentially the oxide trapped charges. In SiC/SiO<sub>2</sub> studies they are also referred to as “near-interface traps” since they do not actually sit at the interface but instead are located in the SiO<sub>2</sub>, very close to the interface. For Si, energy levels of oxide trapped states are in the conduction band, thus not electrically active. For SiC, however, whose band gaps are two to three times wider, many of the oxide trapped charges are located in the band gap, meaning they are electrically active, as has been confirmed by photon stimulated electron tunneling [108]. The near-interface traps have time constants much smaller than the carbon clusters, thus are called fast traps while the latter are known as slow traps.

A schematic representation of the carbon cluster mode is in Figure 5.19 with corresponding energy levels of the specified traps. Due to the significantly low mobility of holes compared to electrons, SiC MOS devices are almost exclusively based on an n-channel design. Therefore, the traps providing the scattering mechanism acting upon electron carriers within the channel are the ones located close to the conduction band edge. Figure 5.19 illustrates the fact that the 4H-SiC conduction band edge is mostly troubled by near-interface traps and  $\pi$ -bonded carbon clusters, with the former more dominant. Both of these traps are accepter-like, namely negatively charged when occupied, which can explain the positive flat band voltage often observed for 4H-SiC MOS devices. On the other hand, 3C-SiC should be free from near-interface traps, attributed to a narrower band gap. However, the 3C-SiC/SiO<sub>2</sub> interface is still troubled by  $\pi$ -bonded carbon clusters. These carbon clusters near the 3C-SiC conduction band edge are donor-like, thus positively charged if occupied, which means the resultant flat band voltage may be more negative. Dangling bonds still contribute



**Figure 5.19** Schematic representation of the “carbon cluster model”. Source: After Esteve [109].

to some of the interface traps but are merely secondary concerns. Consequently, for SiC, H<sub>2</sub> annealing is not as effective as it is for Si. Other techniques had to be explored for SiC/SiO<sub>2</sub> interface optimization.

#### 5.4.4 3C-SiC/SiO<sub>2</sub> Interface Passivation

The efforts put into improving the SiC/SiO<sub>2</sub> interface can be divided into three directions, namely post-oxidation annealing (POA), channel counter-doping, and high temperature oxidation. Up to this point, nitridation may be the most widely used method to improve the 4H-SiC/SiO<sub>2</sub> interfaces. It is usually achieved by the annealing of thermally grown gate oxides in a nitrogenous trace gas environment (NO or N<sub>2</sub>O), called POA. During the annealing process, it is believed that the N—O bond breaks at high temperature and supplies free oxygen which oxidizes 4H-SiC [110], consequently nitridation by POA is accompanied by a further growth of oxide, although this is not significant. Occasionally, gate oxides can be directly grown within such an atmosphere to obtain similar benefits. Previous X-ray photoelectron spectroscopy (XPS) results demonstrated that after NO/N<sub>2</sub>O POA, there were fixed nitrogen atoms near the interface with an area density around  $1 \times 10^{14} \text{ cm}^{-2}$  [111], even after removing all the oxide by thorough HF etching. This suggests that the nitrogen atoms were strongly bonded to the 4H-SiC substrate. There had been evidence showing the nitridation process reduced both carbon-related traps and near-interface traps [112], even though there is still no complete theory established to explain these findings. The near-interface traps are probably reduced by the formation of an oxynitride layer between the 4H-SiC and gate oxide, which redefines the oxide/semiconductor boundary [113] and the oxide trapped charges no longer near the interface. In terms of carbon clusters, they are probably decomposed by inserted nitrogen atoms, which shift the energy levels of remaining clusters deeper into the band gap, further away from the conduction band edge. The result is that these carbon clusters are nullified and are less effective in terms of scattering channel carriers [114]. Apart from N<sub>2</sub>O/NO, it was reported that annealing the gate oxide in a phosphorous trace atmosphere (POCl<sub>3</sub> [115] or P<sub>2</sub>O<sub>5</sub> [116]) also led to a channel mobility improvement. However, this technique introduced severe threshold voltage instability as a result of SiO<sub>2</sub> being converted into phosphor silicate glass. Reducing the number of traps via the introduction of extra atoms into the interface is called passivation, and regardless of the source (N or P), the key-enabler is that enough foreign atoms diffuse through the gate oxide and reach the interface. Certainly higher annealing temperature and time duration will help with that, as long as the SiO<sub>2</sub> crystal structure is still well preserved. However, due to the very low diffusion coefficient of nitrogen in SiC, nitrogen atoms incorporated through POA saturates only within a monolayer deeper into the interface [117], and consequently the mobility value does not increase further and the peak value typically stays around  $40 \text{ cm}^2/(\text{V s})$  [118]. Phosphorous has a higher saturation density than nitrogen in 4H-SiC, but still, the peak mobility value stays around  $80 \text{ cm}^2/(\text{V s})$  [119] regardless of further increased annealing time durations. In summary, the proposed mechanisms for the increased 4H-SiC/SiO<sub>2</sub> channel mobility are defect passivation, channel counter-doping [120–122], and reduced surface roughness scattering [123].

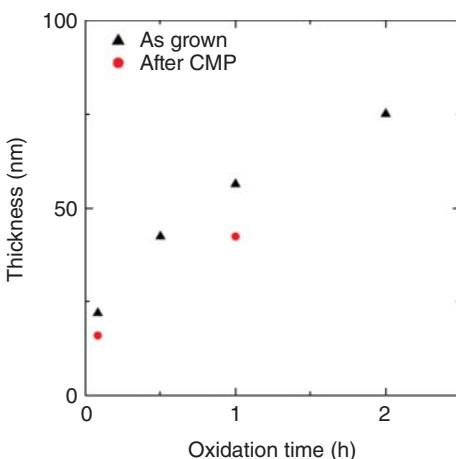
**Table 5.2** Recent results on 3C-SiC MOSFET fabrication.

Substrate material	Channel doping	Gate oxidation	Extra treatment	Peak mobility ( $\text{cm}^2/\text{V s}$ )	References
3C-SiC(001) on Si (CVD)	$2 \times 10^{17} \text{ cm}^{-3}$ p-type epilayer	O <sub>2</sub> wet oxidation at 1150 °C for 2.5 h followed by Ar annealing at 1150 °C for 30 min	O <sub>2</sub> wet re-oxidation at 950 °C for 2 h	≈165	[127]
Free-standing 3C-SiC(001)	$1 \times 10^{16} \text{ cm}^{-3}$ p-type epilayer	O <sub>2</sub> dry oxidation at 1100 °C, followed by Ar annealing at 1150 °C for 30 min	O <sub>2</sub> wet re-oxidation at 800 °C for 30 min	≈229	[128]
Free-standing 3C-SiC(001)	$7 \times 10^{16} \text{ cm}^{-3}$ p-type epilayer	O <sub>2</sub> dry oxidation at 1100 °C for 90 min	O <sub>2</sub> wet re-oxidation at 950 °C for 3 h	5–10	[129]
Free-standing 3C-SiC(001)	$1 \times 10^{18} \text{ cm}^{-3}$ Al implanted	O <sub>2</sub> dry oxidation at 1100 °C for 90 min	O <sub>2</sub> wet re-oxidation at 950 °C for 3 h	≈40	[130]
Free-standing 3C-SiC(001)	Not known, Al implanted	O <sub>2</sub> wet oxidation at 1150 °C	None	≈150 for [110] and ≈300 for [1̄10]	[131]

The 3C-SiC/SiO<sub>2</sub> interface is much less studied when compared to 4H-SiC. The literature revealed the benefits of including hydrogenation processes either during gate oxidation or via POA, which decreases the density of interface states as well as effectively reducing positive fixed charges [15, 124]. Thus, wet oxidation or POA is frequently used in 3C-SiC MOSFET fabrication [124, 125]. Regarding nitridation, extra deep interface traps revealed by the double peak conductance spectra were found from MOS capacitors fabricated using direct N<sub>2</sub>O oxidation and pure oxidation on nitrogen implanted films [124, 126]. The inefficiency of the nitridation process for 3C-SiC is curious since according to the carbon cluster model shown in Figure 5.19, the 3C-SiC/SiO<sub>2</sub> interface should be dominated by  $\pi$ -bonded carbon clusters. The effect of which should be reduced by the nitridation process just as 4H-SiC. The electrical performance of fabricated 3C-SiC MOSFET devices is heavily dependent on the quality of the wafer, making it difficult to directly compare. Recent fabrication results relating to 3C-SiC MOSFETs are summarized in Table 5.2. As can be seen, the peak mobility value covers a huge range from as low as 5–229  $\text{cm}^2/(\text{V s})$ .

#### 5.4.5 Surface Morphology Effects on 3C-SiC Thermal Oxidation

As is the case with all semiconductor materials, the surface morphology and corresponding preparation methods have a profound impact on the quality of any



**Figure 5.20** Oxide thickness as a function of oxidation time at 1150 °C for as-grown and CMP polished 3C-SiC samples. Source: Fiorenza et al. [132]. © 2019, Trans Tech Publications Ltd.

thermally grown oxide ( $\text{SiO}_2$ ). Moreover, the fact that 3C-SiC typically requires some form of chemical mechanical polishing (CMP) process after hetero-epitaxial growth complicates matters further. Figure 5.20 reports the oxide thicknesses as a function of the oxidation time for as grown and CMP processed 3C-SiC hetero-epitaxial layers [132]. These 3C-SiC layers were grown on 4-in. Si(100) substrates by hot-wall CVD at temperatures in the region of 1350 °C (or above). Silane ( $\text{SiH}_4$ ) and ethylene ( $\text{C}_2\text{H}_4$ ) or propane ( $\text{C}_3\text{H}_8$ ) are typically used as supplier gases for Si and C, respectively (see section 2). The thickness of these layers was in the range of 5–10  $\mu\text{m}$ . Standard cleaning (SC) was performed on the samples prior to thermal oxidation. Lateral MOS capacitors based on nickel (Ni)/gold (Au) contacts were fabricated and the oxidation rate was estimated by performing a selective oxide wet etch on lithographic patterns and subsequently measuring the height difference between the oxidized and the etched regions with an atomic force microscopy (AFM) microscope. It can be inferred that the oxidation rate follows an approximate linear behavior, at least for the sample without CMP. A similar linear behavior is observed on examination of the two experimental points collected on the sample after the CMP. Observed thickness fluctuations can be due to the large roughness of the 3C-SiC substrate. For this reason, the step height has been averaged between the minimum and maximum values. From Figure 5.20, after the growth of the first 15–20 nm of  $\text{SiO}_2$ , an oxidation rate of approximately 25 nm/h was estimated.

#### 5.4.6 Thermal Oxidation Temperature Effects for 3C-SiC

Some recently reported results on the temperature varying thermal oxidation properties of 3C-SiC layers are given in this section [133]. Lateral MOS capacitors were fabricated on 14  $\text{mm}^2$  chips. Apart from the solvent and RCA cleans, these samples were subjected to an additional 15 minutes Piranha clean. A unique furnace tube, made from 6H-SiC, so that very high oxide growth temperatures up to 1600 °C could be analyzed, was utilized. For more details surrounding the oxidation conditions, including idle operation, gas flow, and temperature ramp rates, see here [133].

**Table 5.3** Gate oxidation processes for the four 3C-SiC/Si lateral MOS capacitors fabricated and information extracted from high frequency C-V curves for MOS 1-4.

Sample	Gate oxidation details	POA	Oxide thickness (nm)	Flat-band voltage (V)	Fixed charge density ( $\text{cm}^{-2}$ )
MOS 1	1200 °C O <sub>2</sub> dry oxidation (60 min, O <sub>2</sub> 4 slm <sup>a)</sup>	N/A	68	-4	$1.1 \times 10^{-12}$
MOS 2	1300 °C O <sub>2</sub> dry oxidation (20 min, O <sub>2</sub> 4 slm)	N/A	73	-6	$1.6 \times 10^{-12}$
MOS 3	1400 °C O <sub>2</sub> dry oxidation (5 min, O <sub>2</sub> 4 slm)	N/A	60	-13	$4.5 \times 10^{-12}$
MOS 4	1300 °C O <sub>2</sub> dry oxidation (20 min, O <sub>2</sub> 4 slm)	1300 °C N <sub>2</sub> O anneal (2 h, N <sub>2</sub> O, 1 slm)	115	-22	$4.0 \times 10^{-12}$

a) Standard liters per minute.

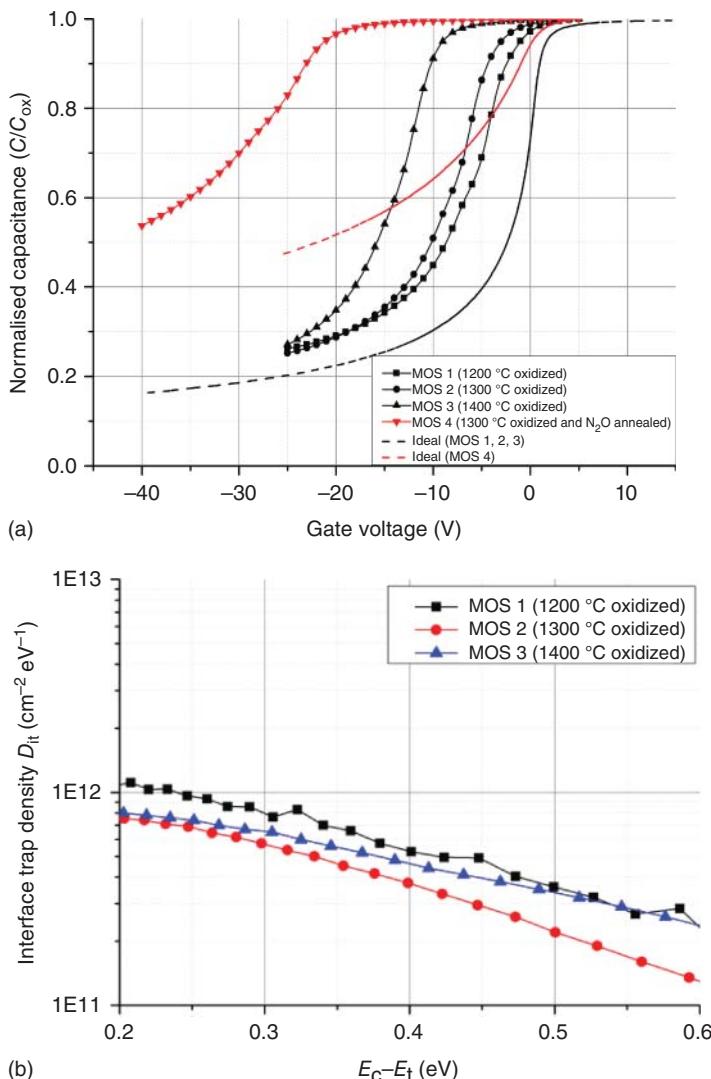
Source: Data from Nagasawa et al. [38].

Three samples were oxidized at 1200 °C, 1300 °C, and 1400 °C, respectively. A fourth sample was oxidized at 1300 °C and went through an extra N<sub>2</sub>O POA process. More detailed descriptions for oxidation conditions are summarized in Table 5.3.

Figure 5.21 shows the ideal capacitance-voltage (C-V) curves for all four samples plotted against their experimental results. A negative shift of the experimental C-V curves from the ideal ones is observed for all samples, indicating the existence of a positive fixed charge. Only donor-like states are present at the 3C-SiC/SiO<sub>2</sub> interface, and since they are positively charged when empty, these donor-like states may be responsible for the negative flat band voltage shift, extracted from the same data and shown in Table 5.3. Comparing MOS 1, 2, and 3, it can be seen that the flat band voltage shifts negatively with increasing oxidation temperature. This is different from the 4H-SiC case and the reason behind this observation is still not clear. The N<sub>2</sub>O annealed MOS 4 has the largest evidenced shift. However, by calculating the fixed charge density for all samples (see Table 5.3), it is seen that MOS 4 does not have the highest fixed charge density. Hence, the significant flat band voltage shift of MOS 4 most likely comes from the counter-doping effect. A sharp peak of nitrogen in MOS 4 compared to all other samples, evidenced by secondary mass ion spectroscopy (SIMS, not shown), demonstrates that like into the 4H-SiC system, nitrogen atoms only accumulate at a very limited depth at or around the 3C-SiC/SiO<sub>2</sub> interface.

#### 5.4.7 Ohmic Contact Metalization

The purpose of this section is to give an overview of the fundamentals of ohmic contacts onto 3C-SiC. Specific and unique contact fabrication processes from the literature will be covered. The basic steps involved in ohmic contact formation to

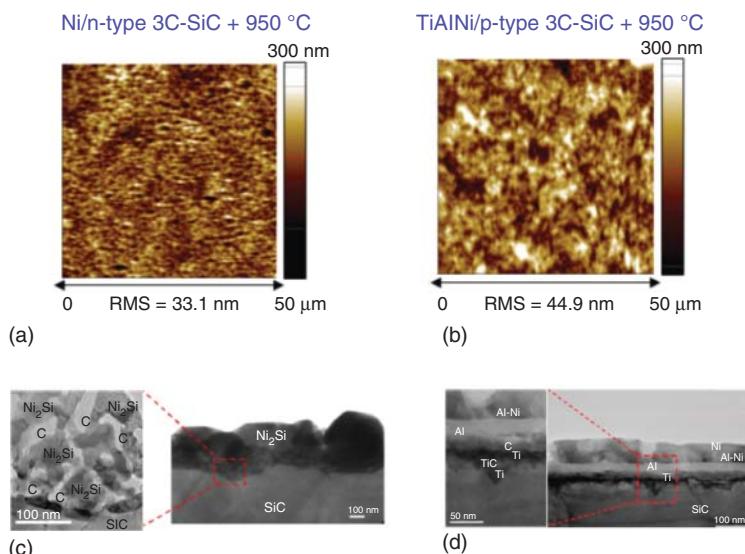


**Figure 5.21** Ideal and experimental (1 MHz) normalized  $C-V$  curves for MOS 1–4 (a) and interface state density as a function of trap depth beneath the conduction band for MOS 1–3 (conductance method) (b).

3C-SiC and how it differs from silicon and 4H-SiC technology will be covered. Creating a quality ohmic contact to 3C-SiC is challenging for many reasons, mainly the aforementioned material quality issues. It is more difficult to form ohmic contacts to p-type with respect to n-type 3C-SiC due to deeper acceptor levels. The primary challenge here is a limitation in terms of post implantation annealing (PIA) temperatures, resulting in poor dopant activation and ionization since the 3C-SiC is grown on silicon, taking the form of hetero-epitaxy wafers. The result is an ion implantation activation annealing temperature of just below 1400 °C (silicon substrate melting

temperature). As a consequence, there are less carriers (lower activation percentage of acceptor dopants) available for current transport, making it more difficult to achieve a high doping concentration, a precursor required for ohmic contact realization. A high free carrier concentration beneath the metal promotes field emission (FE, tunneling) through the metal-semiconductor junction, that is, generally accepted to be the main current transport mechanism, characteristic of ohmic contacts. Identification of the FE current transport mechanism is prevalent under the ohmic regime and is well understood by understanding the contact resistance variance as a function of temperature. Classic metal-semiconductor theory and characterization have been presented elsewhere [134, 135], whereas the concept of the characteristic energy and doping dependent current transport was introduced by Padovani and Stratton [136].

The most recent study on ohmic contacts applied to epitaxial p- and n-type 3C-SiC layers was given by Spera et al. [137, 138]. Here, Ni metallization to n-type 3C-SiC and Ti/Al/Ni metallization to p-type 3C-SiC were examined. Ohmic behavior could be observed after annealing at 950 °C, with values of the specific contact resistance varying in the range of  $10^{-3}$ – $10^{-5}\Omega\cdot\text{cm}^2$ , depending on the 3C-SiC layer and on the metal. In general, annealed Ni contacts exhibited a better surface morphology than Ti/Al/Ni ones. However, these latter are more suitable to form ohmic contacts on p-type doped material, owing to the lower work function. Figure 5.22 shows a physical analysis of both n- and p-type ohmic contacts to 3C-SiC utilizing AFM and cross-sectional TEM. Metallic phases were determined using XRD (not shown).



**Figure 5.22** AFM images of Ni (a) and TiAlNi (b) ohmic contacts onto n- and p-type 3C-SiC epitaxial layers respectively. Cross-section TEM micrographs of Ni/3C-SiC (c) and TiAlNi/3C-SiC (d) samples after annealing at 950 °C. Source: The figure has been adapted from Ref. Spera et al. [137] with kind permission of Trans Tech Publications Ltd. Copyright ©2019 Trans Tech Publications Ltd.

### 5.4.8 N-type 3C-SiC Ohmic Contacts

Ohmic contact studies on 3C-SiC have been primarily limited to n-type material with contact resistivity values ranging between  $10^{-1}$  [139] and  $10^{-5} \Omega\text{cm}^2$  [137, 140]. Many more reports are available for n-type contact resistance measurements within the literature because activation of p-type dopants has proved troublesome due to the limitation in PIA temperature to just below  $1400^\circ\text{C}$ . As was the case with other semiconductor materials such as 4H-SiC and silicon, two topics have been discussed in detail: surface preparation and contact metals. For WBG semiconductors, another topic attracts more focus, namely post metallization annealing (PMA). Depending on the growth method of the 3C-SiC epilayer, the surface roughness can be quite different from below 1 nm to as high as tens of nm. To obtain a smooth initial semiconductor surface for ohmic contact fabrication, often, CMP is performed before any further processing. Noh et al. [139] showed that when the root mean square (RMS) surface roughness value dropped from 20 nm to 7.5 nm, respectively, the contact resistivity value was reduced by one order of magnitude, from  $8.6 \times 10^{-1} \Omega\text{cm}^2$  to  $2.8 \times 10^{-2} \Omega\text{cm}^2$ . As mentioned previously, actual 3C-SiC device fabrication processing involves a high temperature ( $> 1400^\circ\text{C}$ ) PIA process, which can potentially degrade the surface further, even if polishing was performed. A thorough discussion was made on the PIA effects on the 3C-SiC surface morphology [140] and how it is related to the resultant specific contact resistivity values. It was noted that although a severe surface degradation can be a major limiting factor, the specific contact resistivity value will not be affected much so long as the surface roughness value stays below 10 nm. Quite a few metals including aluminum (Al), titanium (Ti), Ni, Ni/Ti, Au/Ti, platinum (Pt), tungsten (W), and TiW [101, 139–149] have been studied for 3C-SiC ohmic contact fabrication. Among them, Ni seems to be the most favored, not only because it can achieve a low resistance value, but also the value has been shown to decrease with elevated PMA temperature up to  $\sim 1000^\circ\text{C}$ . Even though Ti and Al can achieve the same level or even lower specific contact resistance values, an increase with rising PMA temperature was previously reported for these metals, which is an indication of Schottky barrier height increase [142]. Moreover, both Ti and Al suffer from an ease of surface oxidation during processing.

### 5.4.9 Ion Implantation

Ion implantation, which includes a mandatory post implantation thermal treatment, is a consolidated technology for the fabrication of regions with different conductivity sign and different conductivity values next to the surface of a SiC wafer. The desired acceptor and donor densities, as well as the desired shape of the doped regions, depend on the device design that is determined by the desired electrical performance. The actual possibility to achieve the desired doping levels and device geometry depends on the ion implantation parameters, the ion implantation mask design, and the PIA treatment. Presently, 4H-SiC and 6H-SiC are the most studied SiC polytypes and the achieved results are benchmarks for setting up an ion implantation technology for 3C-SiC. Common to all, the SiC polytypes are the need of hot ion

implantation processes and of ion implantation masks that takes into account the ion lateral straggling. The latter is significantly large in the case of  $\langle 0001 \rangle$  4H-SiC wafers [150]. The heating of the SiC wafer during ion implantation induces a recovery of the lattice disorder as far as such disorder accumulates. Such a dynamic annealing inhibits the formation of heavily disordered regions where the lattice reconstruction of the original SiC polytype is no longer possible during the subsequent PIA [151]. The optimal temperature for hot ion implantation depends on the ion implantation dose rate and the implanted ion species [152]. In the case of the PIA of hetero-epitaxial 3C-SiC/Si, the annealing temperature is limited by the melting temperature of the Si substrate. It has been shown that annealing times of hundreds of hours are necessary to detect the sign of an electrical activation in the case of the ion implanted p-type dopant species Al [153]. The PIA temperature is not limited in the case of homo-epitaxial 3C-SiC. Nevertheless, preliminary experiments have shown that for annealing temperatures equal to or higher than  $1700^{\circ}\text{C}$ , on bulk 3C-SiC, and very long annealing times at lower temperatures around  $1300^{\circ}\text{C}$ , in the case of 3C-SiC/Si, the structural quality of the original 3C-SiC material degrades.

## 5.5 Summary

The presented overview in the state-of-the-art materials growth and processing of SiC clearly indicates the rapid technologic progress in recent years. Based on this, cubic SiC exhibits a realistic chance to be applied in future mid-voltage power electronic devices like they are used, for example, in electric car vehicles.

## Acknowledgements

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## 6

### Intrinsic and Extrinsic Electrically Active Point Defects in SiC

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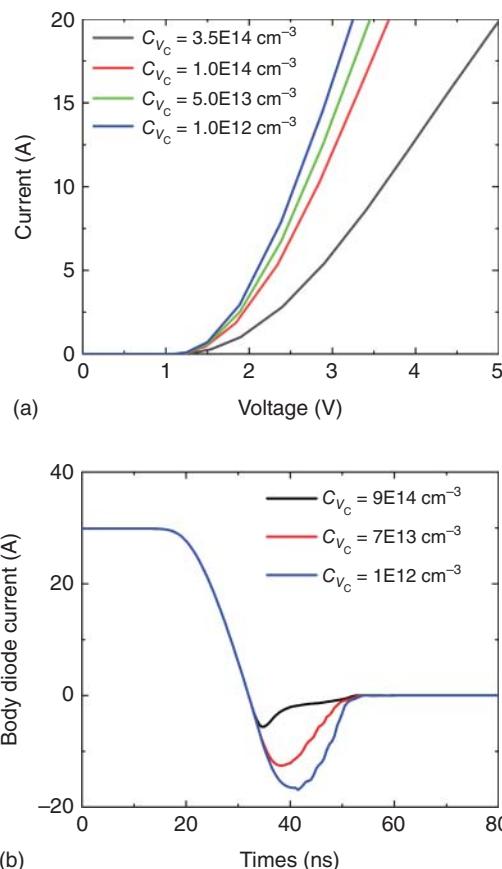
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No crystal is perfect – based on the unit of amount of substance in the International System of Units (SI), the mole [1], we typically assume a prototypical crystal to be composed of the order of  $10^{23}$  atoms. With a density of SiC of  $3.21 \text{ g/cm}^3$  and a molar mass of  $40.11 \text{ g/mol}$ , we arrive at approximately  $4.8 \times 10^{22}$  atoms per cubic centimetres SiC. Typically, SiC-based power devices in the 1.2 kV class employ active layers with a drift layer doping (nitrogen for n-type) in the range of  $10^{15}$  to  $10^{16}$  dopant atoms per cubic centimetres. Hence, the typical desired doping concentration in a power device drift layer is around 6 to 7 orders of magnitude lower than the total amount of atoms and, thus, beyond six sigma level, i.e. 3.4 defects per million (99.999 997% accuracy) [2]! These impurity elements – dopants – are essential for the performance of the devices.

Inevitable, however, are also impurities and intrinsic defects introduced during growth, processing, or even operation that may hamper the application of semiconductor devices. The general characteristics of those defects become relevant at also much lower concentration, as we will show below. The question arises, at which concentration do such defects start to play a role?

Let us first differentiate between intrinsic and extrinsic defects: with the term “intrinsic defects,” defects originating in the SiC lattice itself – missing atoms or vacancies, vacancy complexes, stacking faults, etc. – are summarized. “Extrinsic defects” are used for all impurities, i.e. atoms not being silicon or carbon. Furthermore, within this chapter, we focus on “point defects,” i.e. defects with a rather local structure involving a single or a pair of atoms. Such point defects may introduce an alteration of its surroundings within the crystal by a change of charge distribution at similar geometry or even forcing a local change of the lattice structure. Dopant impurities, on the other hand, are generally not denoted as “defects.” Furthermore, unless stated otherwise, we assume that our prototypical



**Figure 6.1** (a) TCAD simulation for the forward current of a pin diode, assuming different concentrations of the carbon vacancy,  $V_C$ . (b) Reverse recovery of the body diode in a SiC power MOSFET assuming different concentrations of  $V_C$  (TCAD simulation).

SiC to be “lightly doped n-type,” i.e. exhibiting an effective donor concentration in the range of  $3\text{--}5 \times 10^{15} \text{ cm}^{-3}$ , achieved by nitrogen doping during growth.

Now, with these definitions in place, let us get back to our initial question: at which level do impurities and defects in the crystal become relevant – the undesired, performance-altering defects, e.g. generation and recombination centers following Shockley–Read–Hall (SRH) statistics [3, 4], often called “lifetime-killing” defects?

One of the most dominant intrinsic defects in SiC is the carbon vacancy,  $V_C$ . In Section 6.2, the current state of the art of the accumulated knowledge on  $V_C$  will be presented. We know from experiments that an increasing concentration of  $V_C$  is limiting the charge carrier lifetime in n-type 4H-SiC [5].

With device simulations, we can gain further insight on the impact of the  $V_C$  concentration on the performance of SiC-based devices: In Figure 6.1, the effect of the change in charge carrier lifetime due to introduction of  $V_C$  on the forward current of a pin diode (a) and the reverse recovery current of a body diode of a power MOSFET (b) is shown. The investigation is based on TCAD simulations of a p–n test diode and a MOSFET structure representing a commercial 1.2 kV 4H-SiC-based power MOSFET (C2M0080120D) [6] using Sentaurus Device (S-Device) [7].

A simple p–n-diode is designed, where the thickness of the drift layer is 15  $\mu\text{m}$  and the effective n-type carrier concentration is  $3 \times 10^{15} \text{ cm}^{-3}$ , and simulated with

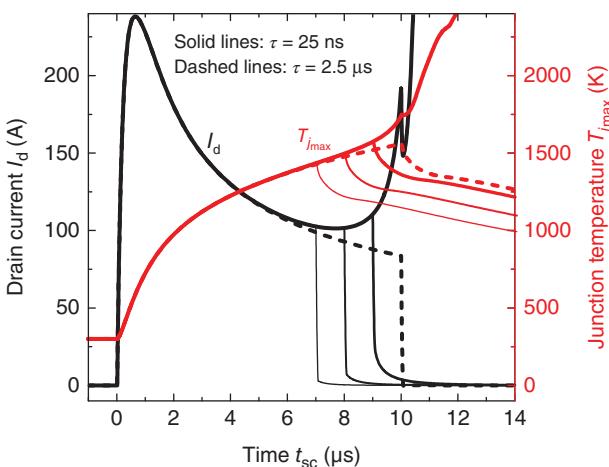
Sentaurus Technology Computer-Aided Design (TCAD) [7] in order to demonstrate the influence of the  $V_C$  concentration on the forward characteristics. Even though the defects cannot be directly incorporated in the simulation model, their effect on the carrier lifetime can be included. Extracted from Ref. [5] for different concentrations of  $V_C$ , different carrier lifetimes are used within the SRH recombination model of the device simulation which otherwise uses the default SiC models. The resulting diode current (Figure 6.1a) increases with decreasing defect concentration due to a higher carrier lifetime and thus reduced recombination rate. The effect becomes less significant at higher carrier lifetimes as other factors such as the drift doping and thickness influence the differential resistance of the diode.

Mixed mode simulations of the MOSFET model are performed to assess the influence of the defect concentration, i.e. the carrier lifetime on the reverse recovery behavior of the internal body diode. The test circuit is chosen in accordance to the datasheet of the manufacturer [6]. The default device simulation models provided by Sentaurus [7] are used, while the carrier lifetime of the SRH recombination model is adjusted to represent different  $V_C$  concentrations. The resulting body diode current (Figure 6.1b) shows a reverse recovery charge that is decreasing with increasing defect concentration as the recombination rate increases. Due to its additional dependence on drift thickness and doping the reverse recovery is not linearly dependent on the defect concentration.

Based on these rather simple estimates, we can now draw two important conclusions:

- Whereas in the case of the p–n diode the reduction of  $V_C$  in the drift layer region is strongly beneficial for achieving a higher forward current at lower bias voltages, a power MOSFET gains from an increased  $V_C$  concentration for the drift layer material in order to reduce switching losses, when utilizing the body diode. This is a classical trade-off scenario in power device design. The interested reader is pointed to [8–10].
- The impact of  $V_C$  on device performance is already pronounced at concentrations of around  $1 \times 10^{13} \text{ cm}^{-3}$  – the level determined by Danno et al. [5] as the concentration at which  $Z_{1/2}$  (we will later see the direct correlation between the level “ $Z_{1/2}$ ” and  $V_C$ ) starts acting as a recombination center – a concentration 3 to 4 orders of magnitude lower than the typical doping concentration in commonly used drift layers. Employing a statistical concept widely used in semiconductor industry: we are at a level far beyond six sigma accuracy!

The effect of recombination centers such as  $V_C$  becomes even more evident when considering conditions as observed during a short circuit (SC) event, i.e. beyond nominal operation [11]. Here, the effect of recombination on the lifetime of generated charge carriers is visible in the current decay observed after SC operation: SiC MOSFETs may exhibit a leakage current that remains after the turn-off of SC operation, which is common for bipolar Si-IGBTs (the so-called tail current), but unexpected for unipolar power devices such as power MOSFETs. Reducing the lifetimes for holes and electrons ( $\tau_p$ ,  $\tau_n$ ) enhances the SRH generation in the depletion region of the p-base/n-drift junction of the MOSFET. With a larger SRH generation, the total  $I_{\text{drain}}$  increases as the generated holes flow through the p-base to the base contact, see Figure 6.2.



**Figure 6.2** Influence of carrier lifetime ( $\tau$  corresponds to maximum SRH generation lifetime of the electron) on the short circuit current and junction temperature in a SiC MOSFET. Lower generation lifetime increases the leakage current during short circuit leading to an increase of the device temperature. Increasing thickness of the black solid lines corresponds to SC current and temperature with increasing SC time duration ( $t_{sc} = 7 \mu s, 8 \mu s, 9 \mu s, \text{ and } 10 \mu s$ ), showing an increase in tail current at SC turn-off.

Now, one further aspect should be considered: most of the currently used SiC devices are based on material with a rather thin epitaxial “active” layer, typically in the range of some  $10 \mu m$ , on top of a thicker SiC substrate (typical thickness between  $110$  and  $350 \mu m$ ), which does not contribute to the active device performance. Hence, the region of interest is the thin, high-quality, rather low-doped layer on top of the wafer. With the boundary conditions we now have established, our search for suitable characterization techniques for identification and characterization of intrinsic and extrinsic electrically active defects should, therefore, be focused on techniques sensitive to probing regions at or at least close to the surface.

The chapter is organized as follows: after a brief recapitulation of the most commonly used techniques to characterize defects in semiconductors, the most sensitive electrical characterization technique, deep level transient spectroscopy (Section 6.1.1) is described. Following, an introduction to muon spin rotation spectroscopy ( $\mu$ SR) is given – a nuclear method involving a short-lived subatomic charged particle highly promising for further analysis of surface-near defects (Section 6.1.2). In addition, the primary theoretical framework for investigating defects in semiconductors is mentioned (Section 6.1.3). Following are a review on recent findings of the two types of vacancies in SiC, the carbon vacancy  $V_C$  and the silicon vacancy  $V_{Si}$  (cf. Section 6.2), and a collective summary of all unambiguously assigned extrinsic electrically active defects, primarily the ones caused by transition metals (cf. Section 6.3). The chapter is concluded with a suggestion on how the findings presented can be used in current and further SiC research and development, both in science and technology (cf. Section 6.4).

## 6.1 Characterization of Electrically Active Defects

Very frequently, a very first approach to probe the overall quality of the crystal and its dominant types of defects is an optical method such as photoluminescence. It typically does not require any sophisticated sample preparation and is sensitive to point defects similar to the ones considered here. The investigation of luminescence in materials excited by light date back to the early 1900s, when E.L. Nichols and E. Merritt presented the first results on sidot blende (ZnS) at the meeting of the Physical Society in 1905 [12].

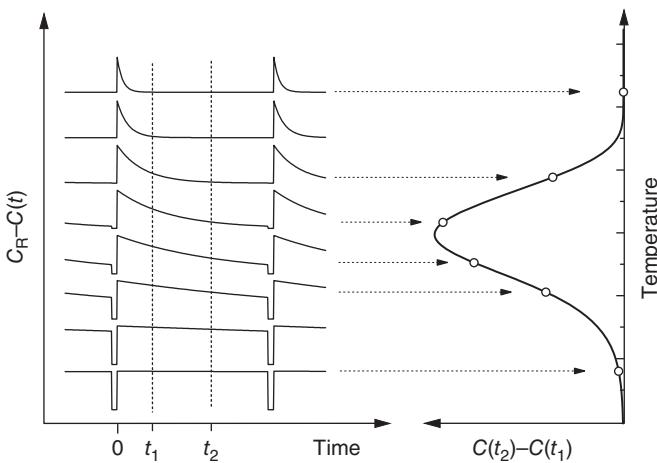
Since then, the method has been further refined and understanding of the spectroscopic response of the materials has improved tremendously; an excellent overview on the technique and data on photoluminescence in SiC can be found in [13] and the references cited therein.

Other techniques utilized for characterization of point defects in SiC are optical absorption, electron paramagnetic resonance (EPR), and optically detected magnetic resonance (ODMR). For more detailed information, we point to the most recent book publication [14] and the references cited therein, as this is not the main focus of this contribution.

These techniques are highly successfully employed for defect characterization, but cannot readily identify electrically active traps or their position in the band gap. Especially optical methods are probing at a completely different region compared to a method depending on capture and emission processes within in a depletion region, such as deep-level transient spectroscopy (DLTS); the incoming laser light in photoluminescence, for example, can excite the entire region of the sample and its detected signal is collected from several  $100 \mu\text{m}^3$  areas. Furthermore, most available research results using photoluminescence are obtained at fairly low temperatures. In order to avoid the effect of lattice vibrations and to extract clean spectra, most results have been obtained at temperatures below or at about 10 K, and spectra will not exhibit narrow features at temperatures above 100 K. This is in contrast to electrical techniques, which can reliably provide information up to 700 K (see, for example, DLTS studies on near-midgap states of Pt in SiC [15]).

### 6.1.1 Deep Level Transient Spectroscopy

DLTS is the most sensitive method for the characterization of electrically active defects in semiconductors [16]. It is based on the electron and hole trapping in the Shockley–Read–Hall model [3]. By means of DLTS, it is possible to determine the energetic position and the capture cross section for charge carriers of an electrically active trap in the space charge region of a semiconductor device. In most DLTS studies, Schottky diodes or p–n junctions are used. During a typical DLTS measurement, traps in the space charge region are filled with a pulsing voltage. Upon returning to the reverse bias condition, the traps re-emit the charge carriers due to thermal activation. The measured signal is directly proportional to the number of charge carriers involved in that particular emission.



**Figure 6.3** From capacitance transients to DLTS spectrum: the capacitance is measured at two different times  $t_1$  and  $t_2$  during the charge carrier emission (left panel). The difference  $C(t_2) - C(t_1)$  is stored for each temperature step observed. In the resulting DLTS-signal, a peak can be observed when the emission rate matches the time window (right panel).

The most frequently used technique is the so-called capacitance-DLTS (C-DLTS) that measures the width of the space charge region by observing the diode capacitance. One critical assumption that is made for the evaluation of DLTS data is that the trap concentration is much smaller than the shallow doping concentration. Furthermore, in most cases, it is assumed that the capture cross section does not depend on the energetic position of the trap in the band gap.

The simplest way to determine the emission rate is the so-called box-car method (see Figure 6.3). The capacitance is measured at two different times  $t_1$  and  $t_2$  during the charge carrier emission. The difference  $C(t_2) - C(t_1)$  is stored for each temperature step observed. In the resulting DLTS signal, a peak can be observed when the emission rate matches the time window. Applying different time windows  $t_1$  and  $t_2$  leads to different peak positions and the emission rate can be determined by  $(t_2 - t_1) / \ln(t_2/t_1)$  at each temperature position. More advanced DLTS systems also use other correlation functions like a sine wave (first Fourier factor) or a double-rectangular function [17]. This may result in spectra with a higher resolution, i.e. narrower DLTS peaks, which may aid to distinguish traps with similar parameters. One should note here that using the capacitance rather than the current transient leads to the effect that the collected charge carrier is not traveling through the junction; therefore, the capacitance-based DLTS is not sensitive to the region close to the junction interface (for a typical drift layer doping this “blind” region is around 100–300 nm thick from the top of the sample/the junction). Application of a forward bias may result in information closer to the surface; however, the validity of all assumptions made in DLTS analysis needs to be ensured.

From the linear regression of the Arrhenius plot of the resulting data, the trap energy is then determined from the slope of the curve. The capture cross section results from the intersection with the  $-\ln(T^2 t)$ -axis. It is important to note that the

latter value represents the product of the entropy factor and the true capture cross section. If the bare capture cross section is to be determined, measurements with a varying duration of the pulse voltage can be performed. Though, this places higher demands on the measurement equipment, i.e. an external pulse generator that is capable of pulses in the order of nanoseconds.

There are multiple descriptions on different flavors of DLTS and a wide range of applications available in the literature. Here, we would like to point the reader to the following, more classical publications aiming at the basics of the technique rather than its application for specific types of samples: [16–19], and, most certainly, [20].

#### 6.1.1.1 Profile Measurements

DLTS is also capable of determining the depth profile of deep levels in the space charge region. One way to observe a depth-dependent concentration is to record the DLTS signal at fixed temperature (isothermal DLTS), varying the reverse and pulse bias and thus the probed region of the device. This is also referred to as double-correlated DLTS (DDLTS).

#### 6.1.1.2 Poole–Frenkel Effect

The electric field in the space charge region affects the emission of charge carriers from a deep donor in an n-type and a deep acceptor in a p-type semiconductor [21]. A deep donor is positively charged after the emission. Therefore, the electron has to overcome the Coulomb barrier. The electric field in the space charge region superimposes the Coulomb field of the donor and thus decreases the barrier. In this case, the emission rate is reduced, and the resulting trap energy determined from DLTS spectra is too low. This is called Poole–Frenkel effect and is often neglected in studies on deep levels. In detailed studies, the Poole–Frenkel effect is determined, e.g. by varying the reverse bias and thus the electric field strength in the space charge region observed. By measuring the emission rate at different electric fields, it is possible to evaluate the correct trap position in the band gap and determine the charge state. In this case, it is necessary to measure the emission rate in a reasonably small part of the space charge region only since the electric field varies with depth. This can also be achieved with DDLTS measurements.

#### 6.1.1.3 Laplace DLTS

Laplace-DLTS has been developed for obtaining a better resolution of major traps in DLTS spectra [18]. Essentially, the data from the capacitance transient are transformed from the time to the frequency domain, enabling an increase in energy resolution by 1 order of magnitude compared to conventional DLTS. The most recent findings, both for  $V_C$  and  $V_{Si}$ , have been obtained using Laplace-DLTS and will be further discussed in Section 6.2.

All examples given for intrinsic and impurity trap levels in Sections 6.2 and 6.3 are based on one or the other flavor of DLTS analysis, as we deem this technique the most precise for determining activation energy  $E_a$  and capture cross section  $\sigma$  for the identification of extrinsic and intrinsic trap levels in the bandgap of a semiconductor, including SiC.

### 6.1.2 Low-energy Muon Spin Rotation Spectroscopy

In muon spin rotation ( $\mu$ SR) spectroscopy, charge and spin of a short-lived subatomic particle called *muon* are used as sensitive local electronic and magnetic probes of matter. Muon spin rotation (or relaxation or resonance) is a relatively young nuclear method and can be classified between nuclear magnetic resonance (NMR) and diffraction techniques [22]. In contrast to NMR or Mössbauer spectroscopy,  $\mu$ SR does not rely on internal nuclear spins of the target material but can be applied for any type of material in a large variety of environments (e.g. different temperatures, pressures, magnetic and electric fields, ...). The fact that the spin polarization of the muons is provided by the laws of particle physics also implies that the magnetic properties of the sample can be studied under zero external field. Muons are unstable leptonic particles with an electric charge of  $\pm 1 e$ , a spin of  $1/2$  and a mass of  $207 m_e$  (or  $1/9 m_p$ ) [23]. They can be obtained at high-energy proton accelerators through the decay of pions which are produced in nuclear interactions between accelerated particles and nuclear targets. At dedicated muon facilities, muons (in most cases, positive  $\mu^+$ ) are implanted into the material of interest. After a mean lifetime of  $2.2 \mu\text{s}$ , they decay again into a positron  $e^+$  (or electron in case of  $\mu^-$ ) and two neutrinos. The muon decay violates parity, with the result that the positrons are preferentially emitted along the direction of its spin [24]. By measuring the direction of the emitted positrons in a time-resolved fashion using detectors outside of the target material, conclusions on the spatial distribution and dynamical fluctuations of the muons' magnetic environment can be drawn.

A more complete description of  $\mu$ SR and the wide range of applications can be found in a number of books [23, 25–28] and review articles [22, 24, 29–32].

The main advantages compared to other nuclear methods are the extreme sensitivity of the  $\mu$ SR technique to small internal magnetic fields (reaching down to  $\sim 0.1 \text{ G}$ ) and its unique time window for the study of magnetic fluctuations between  $10^4$  and  $10^{12} \text{ Hz}$ , bridging the gap between NMR and neutron scattering techniques. In general,  $\mu$ SR experiments require high muon fluxes of more than  $10^3 \text{ muons}/(\text{s cm}^2)$  which can only be obtained at high-energy accelerators such as the proton accelerator facility at the Paul Scherrer Institute, PSI.

For applications in thin film and surface investigations, muon beams in the range of eV to several keV are needed, yielding implantation depths into the target material ranging from below-nanometer to the order of hundred nanometer [25]. The most successful method to generate low-energy (LE) muons with a decent beam intensity is an approach developed at PSI [33]. This modified  $\mu$ SR technique then also allows probing the region which is otherwise not easily accessible using DLTS, namely, the very surface-near region.

#### 6.1.2.1 $\mu$ SR and Semiconductors

Depending on the host material, the implanted  $\mu^+$  interacts differently with its environment during its short lifetime of  $2.2 \mu\text{s}$ . In metals, the positive charge of the muon is collectively screened by a cloud of conduction electrons and behaves like a free muon. In insulators, semiconductors, or molecular compounds on the other hand,

the muon will usually pick up one electron and form muonium ( $\text{Mu} = \mu^+e^-$ ) with the size of the Bohr radius and reduced mass and ionization potential very similar to a hydrogen atom. The evolution of the muon spin during Mu formation is governed by a spin Hamiltonian which includes the interaction between the muon and electron spins as well as the Zeeman interactions between the external field and the electron and muon spins [24, 26].

The muonium formation process varies significantly for different semiconductors and the particularities of each host material have to be considered carefully when interpreting the  $\mu\text{SR}$  data.

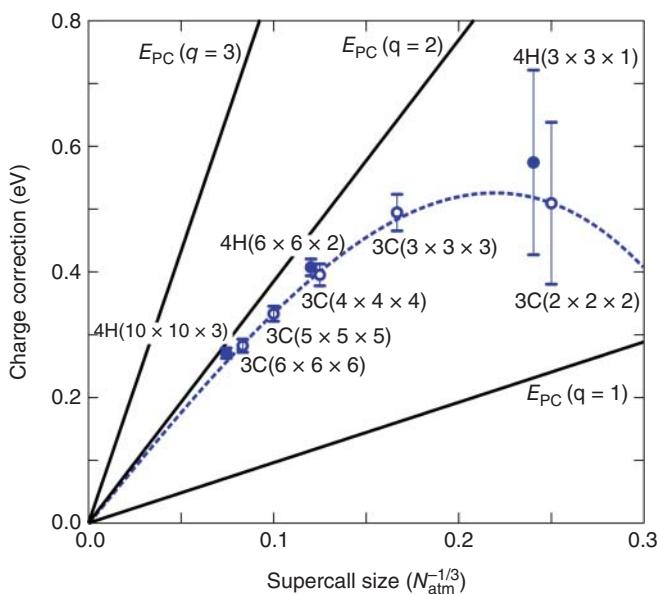
During the past few years, LE- $\mu\text{SR}$  has been successfully employed for the characterization of  $V_{\text{C}}$  [34],  $V_{\text{Si}}$  [35] as well as the  $\text{SiO}_2/4\text{H-SiC}$  interface region [36]. Considering the recent results, the LE- $\mu\text{SR}$  technique shows great promise for the characterization of defects in SiC, especially close to the surface and including the depth resolution required for the analysis of thin interface structures.

### 6.1.3 Density Functional Theory

To accompany the aforementioned experimental techniques, an *ab-initio* technique, namely, density functional theory (DFT) is widely used for assessment of potential point defects; one should note, however, that at the beginning of any such simulation there is an assumption on the shape and the characteristics of the investigated defect, which is then rather probed for its likelihood compared to another version rather than enabling a clear identification.

Also, the exact determination of the energetic position of the investigated defect structure in the bandgap requires advanced methods beyond traditional DFT techniques and should, therefore, be carefully reviewed. An excellent example is given by Jose Coutinho et al. [37], whose clear identification of the different transitions of the carbon vacancy in SiC will be discussed in more detail in the later part of this chapter. Here, we would like to turn the focus of the reader on a rather basic problem of DFT-based methods - the choice of the correct setup of the initial supercell to simulate the defect in question and the charge correction required. In Figure 6.4, the effect of the size of the so-called supercell (the collectively treated sum of all unit cells multiplied toward all reciprocal coordinate directions) on the necessary charge correction is presented. As discussed in the very beginning of this chapter, the typical defect concentrations are in the range of  $1 \times 10^{12} \text{ cm}^{-3}$  to  $1 \times 10^{14} \text{ cm}^{-3}$ , i.e. up to only approximately 0.0001 defects per million atoms. It is very obvious that both potential corrections of charges as well as the effect of supercells being systematically smaller than real crystals have to be carefully taken into account.

As both optical measurements as well as ab initio simulations are based on completely different areas and even orders of magnitude in size compared to the probed volumes in DLTS or LE- $\mu\text{SR}$ , in most publications on defect characterization using optical or ab initio methods the values obtained may differ compared to the ones obtained by direct electrical measurement using DLTS, complicating the successful correlation to final device performance.



**Figure 6.4** Variation of the charge correction,  $E_{\text{corr}}$ , obtained for a double positively charged carbon vacancy in 4H-SiC (closed circles) and 3C-SiC (open circles) supercells sized by the number of atoms,  $N_{\text{atm}}$ . Error bars are standard deviations obtained from the averaging of  $\Delta\Psi_{\text{PC,ind}}$ . Integer triplets  $(l \times m \times n)$  are scaling factors applied to the lattice vectors of each unit cell to obtain the respective supercell. The dashed line represents a function of the form  $a N_{\text{atm}}^{-1} + b N_{\text{atm}}^{-1/3}$  fitted to the data. Solid lines represent simple point charge corrections for  $q = 1, 2$ , and  $3$ . Source: Reprinted with permission from [37]. Copyright (2017) by the American Physical Society.

## 6.2 Intrinsic Electrically Active Defects in SiC

In recent years, the understanding of the behavior and stability of the silicon and carbon vacancy in SiC has significantly improved. These two types of intrinsic defects are now very well understood – the focus of this section is, therefore, a careful review of the current state of the art, as found both in experiment as well as theory.

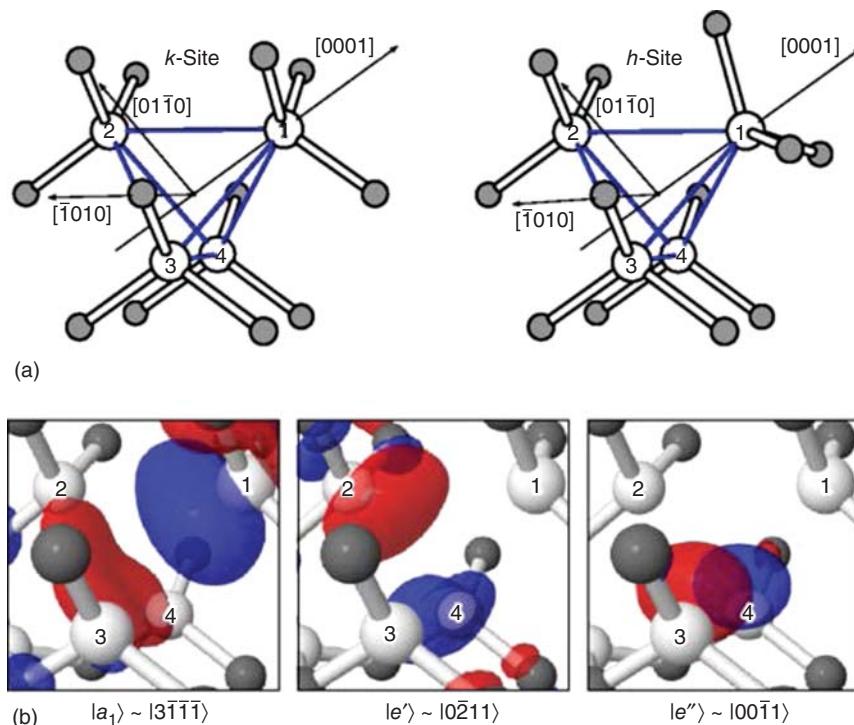
Prior to geometric relaxation,  $V_{\text{Si}}$  and  $V_{\text{C}}$  exhibit a nearly tetrahedral  $C_{3v}$  symmetry. Although  $V_{\text{Si}}$  and  $V_{\text{C}}$  initially appear similar, variations in their local environment lead to drastically different behavior.

$V_{\text{C}}$  is surrounded by Si atoms having extended dangling bonds that overlap, and the degenerate ground state makes  $V_{\text{C}}$  susceptible to a symmetry-lowering Jahn-Teller distortion. The overlapping Si orbitals neighboring  $V_{\text{C}}$  drive a strong inward displacement to increase the overlap, and pairwise Si-Si dimer formation reduces the  $V_{\text{C}}$  symmetry to  $C_{1h}$  in the neutral charge state [38–42]. As a result,  $V_{\text{C}}$  exhibits negative- $U$  characteristics [43] and becomes a deep-level carrier trap responsible for limiting carrier lifetimes in 4H-SiC, thereby lowering the performance of 4H-SiC power electronic devices [44].

$V_{\text{Si}}$ , on the other hand, is surrounded by highly localized C orbitals with negligible overlap, similar to the vacancy in diamond. Without nearest-neighbor bonding, there is no driving force for a JT distortion in  $V_{\text{Si}}$  and a high energetic cost for inward displacement. Instead, the Si–C bonds shorten, yielding a symmetry conserving outward-breathing relaxation.  $V_{\text{Si}}^-$  exhibits  $S = 3/2$ , long spin coherence times, and single-photon emission [45], in contrast to the low-spin ( $S = 0$ ) and negative- $U$  character of  $V_{\text{C}}$  [37, 43]. Owing to these properties, the  $V_{\text{Si}}$  has been identified as a promising candidate for a wide range of quantum applications, including quantum communication, computing, and sensing [45–47].

### 6.2.1 The Carbon Vacancy, $V_{\text{C}}$

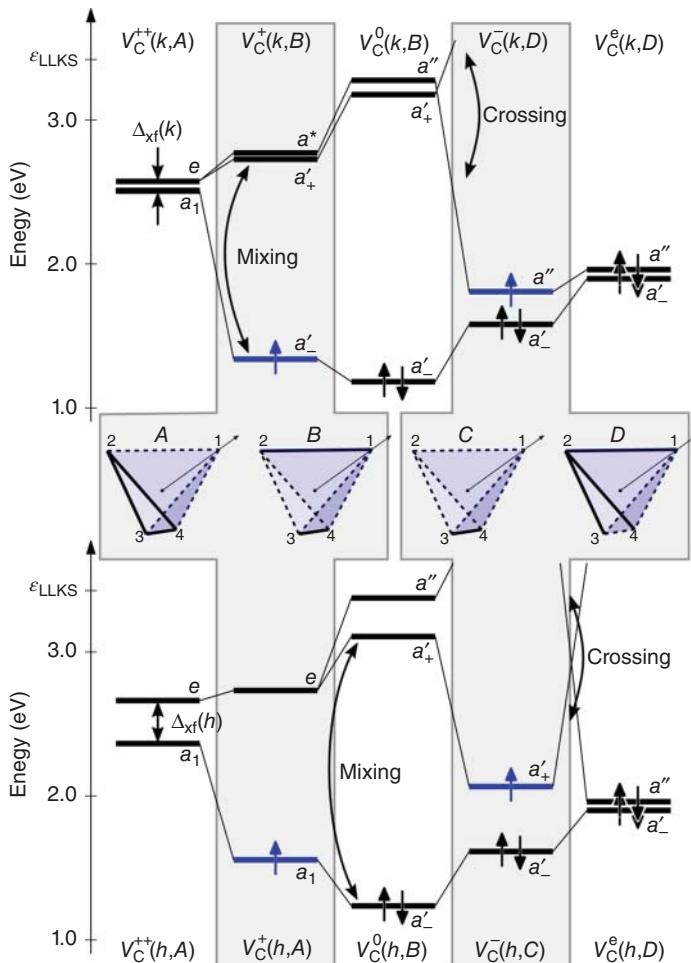
The DLTS levels finally assigned to the different charge states of  $V_{\text{C}}$ ,  $Z_{1/2}$  and  $\text{EH}_{6/7}$  [48], have long been under discussion. Originally, the first description of a deep level in SiC named  $Z_1$  was given in [49]. Over the years, this level has been assigned to  $V_{\text{C}}^-$  or carbon-interstitial complexes involving nitrogen [50, 51] or hydrogen [52].



**Figure 6.5** (a) Atomic structure of perfect carbon vacancies at *k* and *h* sites of a 4H-SiC crystal. Si and C atoms are white and gray, respectively.  $1_{\text{Si}}$  is axial (located on the [0001] crystallographic axis), whereas  $2_{\text{Si}}, 3, 4$  atoms lie on the basal plane. (b) Representation of the one-electron states in the gap ( $a_1 + e$ ) arising from an undistorted  $V_{\text{C}}$  defect at the *k* site. Red and blue isosurfaces denote negative and positive phases, respectively. Source: Reprinted with permission from [37]. Copyright (2017) by the American Physical Society.

Also, the thermal stability of the trap level was under discussion for a very long time – initial studies even suggested annealing at temperatures as low as 1300 °C [53]. The final assignment of  $Z_{1/2}$  and  $\text{EH}_{6/7}$  to  $V_C$  has been presented by Son et al. [43].

Since then, the focus has been on developing further understanding of properties, annealing behavior, and migration. We will start our discussion at the point in time represented in detail in [13] – around 2014. Whereas at this stage the state of the art



**Figure 6.6** Kohn-Sham electronic states at  $k = \left(\frac{001}{2}\right)$  for the carbon vacancy at the cubic (upper half) and hexagonal (lower half) sites. The zero of the energy scale is at the  $\epsilon_{\text{HOKS}}$  energy in bulk (using the HSE06 functional). Electrons are represented by upward (spin-up) and downward (spin-down) arrows. Each state is accompanied by symmetry labels (see text for details). The central region displays the structures found for positively charged (A and B) and negatively charged (C and D) defects. Contracted/elongated Si–Si distances are represented as solid/dashed lines, respectively. Source: Reprinted with permission from [37]. Copyright (2017) by the American Physical Society.

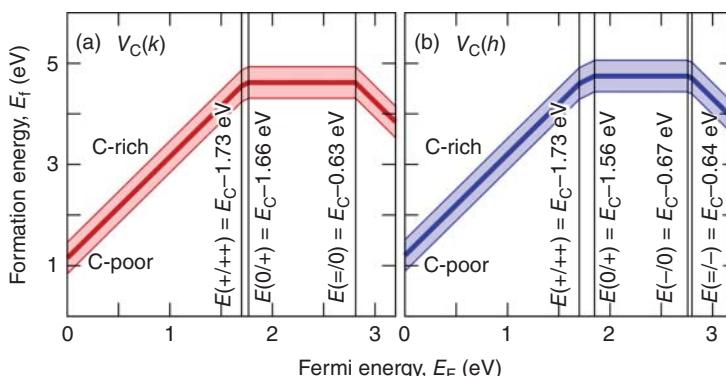
was represented by decreasing the  $V_C$  concentration using oxidation [56, 57] showed that  $V_C$  can also be generated in high-temperature annealing above 1600 °C. From these experiments, kinetics of  $V_C$  was determined and the generation rate of  $V_C$ , the diffusivity of  $V_C$  and carbon interstitials,  $C_i$ , was determined to be 6.3, 2.5, and 1.5 eV, respectively [58]. This triggered also a more detailed analysis of the correct treatment of the  $V_C$  in DFT calculations, especially with respect to the correct representation of lattice distortions. Starting from the ideal crystal configuration (cf. Figure 6.5), the relaxation and resulting mixing of the different states is determined (cf. Fig 6.6). Finally, the formation energies for the charge states and their dependence on growth conditions (C- or Si-rich) are investigated (see Figure 6.7), and the configuration coordinate diagrams of  $V_C$  defects in 4H-SiC are presented (see Figure 6.8).

In a combination of Laplace-DLTS and DFT, the capture and emission behavior of the acceptor states of  $V_C$  could then be directly determined with great precision [54]. Interestingly, the suggested fast capture process of the second electron seems to confirm the findings made recently in LE- $\mu$ SR experiments [35]: Here, a two-electron capture process at the  $V_C$  needs to be considered where a  $Mu^+$  forms  $Mu^-$  via a short-lived  $Mu^0$  state (Figure 6.9).

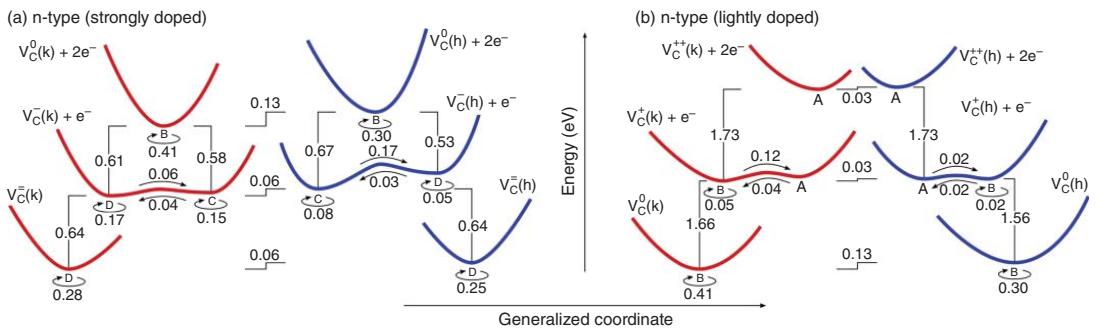
Migration of  $V_C$  was further investigated in [55]; the  $V_C$  shows a different migration pattern for  $a$ -cut vs.  $c$ -cut SiC wafers. Diffusion of  $V_C$  along the  $a$ -direction is found to exhibit a lower activation energy than migration along  $c$ -direction. Furthermore, although the formation energy of  $V_C$  is lower than the one for  $C_i$ , the energy required for diffusion is higher for  $V_C$  than for  $C_i$ .

The authors find that although  $V_C$  has a lower formation energy than  $C_i$ , it is still less mobile, so that self-diffusion of carbon in SiC is most likely governed by carbon interstitial migration (Figures 6.10 and 6.11).

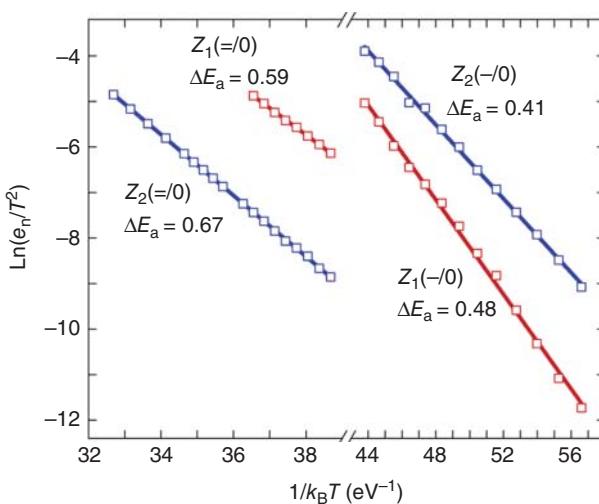
In summary, the recent advances in understanding of the carbon vacancy in SiC have been achieved by the combination of various experimental and theoretical



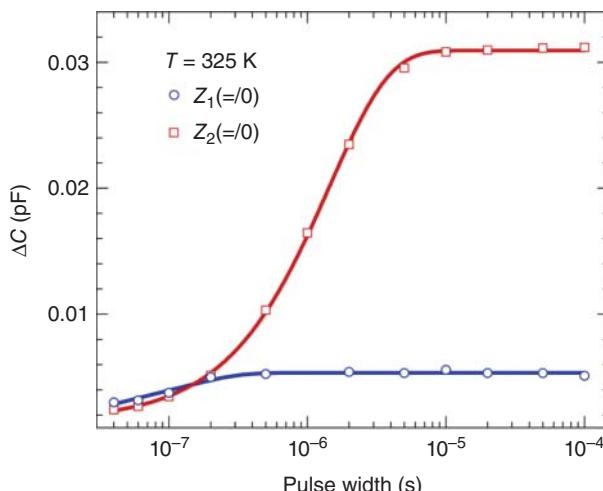
**Figure 6.7** Formation energy ( $E_f$ ) of the carbon vacancy at the cubic (a) and hexagonal (b) sites as a function of the Fermi energy ( $E_F$ ). Lower, central, and upper lines represent  $E_f$  values for crystals grown under C-poor (or Si-rich), stoichiometric, and C-rich conditions. Source: Reprinted with permission from [37]. Copyright (2017) by the American Physical Society.



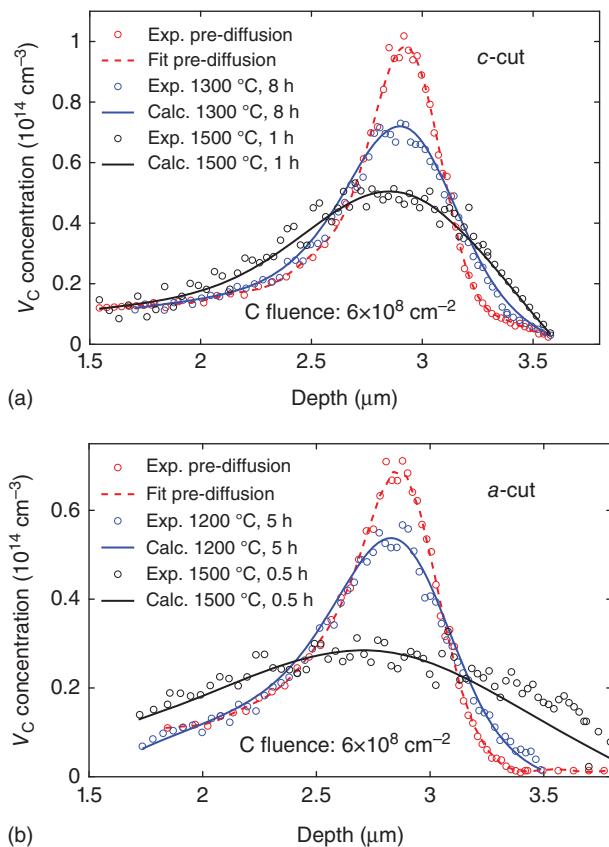
**Figure 6.8** Configuration coordinate diagram of  $V_C$  defects in 4H-SiC. Acceptor and donor transitions are shown in (a) and (b), representing strongly doped and lightly doped n-type material, respectively. Electronic transitions (up in energy) involve the emission of one electron to the conduction band ( $e^-$ ). Insets (a) and (b) include two diagrams, one for each sublattice site. Energies (in eV) are accompanied with guidelines for better perception. Forward/backward transformation and rotation barrier energies are indicated by right/left and spinning arrows, respectively. Steplike guidelines indicate the energy difference between ground states of defects in  $k$  and  $h$  sites. Minima of the potential curves represent stable/metastable structures and are identified with labels A–D. Source: Reprinted with permission from [37]. Copyright (2017) by the American Physical Society.



**Figure 6.9** Arrhenius plots of electron emission rates for  $Z_1(=0)$ ,  $Z_2(=0)$ ,  $Z_1(-0)$ , and  $Z_2(-0)$  transitions in 4H-SiC obtained by L-DLTS measurements. Activation energies for electron emission are also shown for each peak. The horizontal axis is broken and separates double from single emissions. Source: Reprinted from [54], with the permission of AIP Publishing.



**Figure 6.10** Capture kinetics measured for  $Z_1(=0)$  and  $Z_2(=0)$  transitions by L-DLTS at  $T = 325$  K. Data points are the magnitude of the L-DLTS peaks for different durations of the filling pulse. Source: Reprinted from [54], with the permission of AIP Publishing.



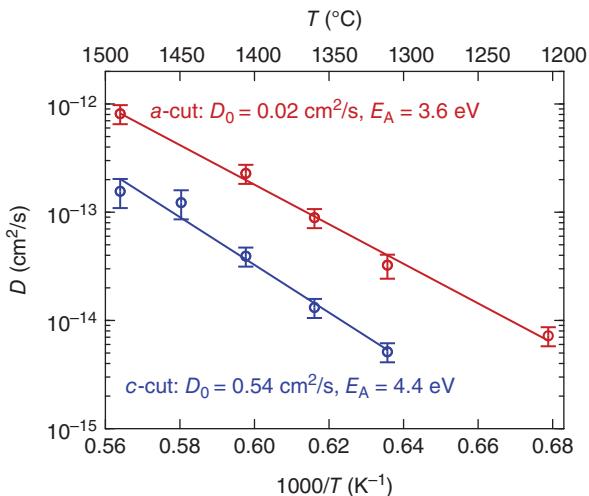
**Figure 6.11**  $V_C$  concentration vs depth profiles along the (a) *c* and (b) *a* direction before (red) and after (blue and black) annealing at temperatures between 1200 and 1500 °C. Circular marks represent experimental data, red dashed lines are fits to the initial profiles, and solid lines are the diffused profiles calculated by solving the diffusion equation. Source: Reprinted with permission from [55]. Copyright (2019) by the American Physical Society.

approaches.  $V_C$  has been unambiguously correlated to the well-known  $Z_{1/2}$  and  $\text{EH}_{6/7}$  levels as seen in DLTS. The fast capture process also has been observed experimentally using LE- $\mu$ SR, and the theoretical framework developed in the course of the various studies allows the correct prediction of formation and activation energy. This has enabled also a good understanding of annealing conditions where either a generation or an annealing of  $V_C$  can be expected, delivering a useful processing method toward lifetime control in power devices (Figure 6.12).

### 6.2.2 The Silicon Vacancy, $V_{\text{Si}}$

For a very long time, the electronic signature of the Si vacancy was unknown. In photoluminescence spectroscopy, the  $V_{\text{Si}}$  exhibits a well-known fingerprint [60, 61]. Only very recently, the DLTS signature of the silicon vacancy in 4H-SiC has been identified [59].

**Figure 6.12** Temperature dependence of  $V_C$  diffusivity ( $D$ ) along the  $c$  direction (blue) and  $a$  direction (red), with  $D$  clearly obeying Arrhenius behavior. Circular marks represent  $D$ , and solid lines are linear fits to the data. The extracted fitting parameters ( $D_0$  and  $E_A$ ) are included in the figure. Source: Reprinted with permission from [55]. Copyright (2019) by the American Physical Society.



A so-called  $S_1$  level has first been observed in 4H SiC after electron irradiation with 2 MeV electrons [62]. This first study raised a lot of questions as the defect appeared to be comparably unstable in irradiation and subsequent annealing experiments (especially compared to what we now know to be the signature of  $V_C$ ). Hence, in a further study [63], the trap level was named “S” (as in sporadic, not Si), and the behavior remained a “mystery” for quite some time. In retrospect, a truly visionary choice of naming this level!  $S_1$  and  $S_2$  have first been identified as different charge states of one and the same defect in [64] and were further investigated in [65].

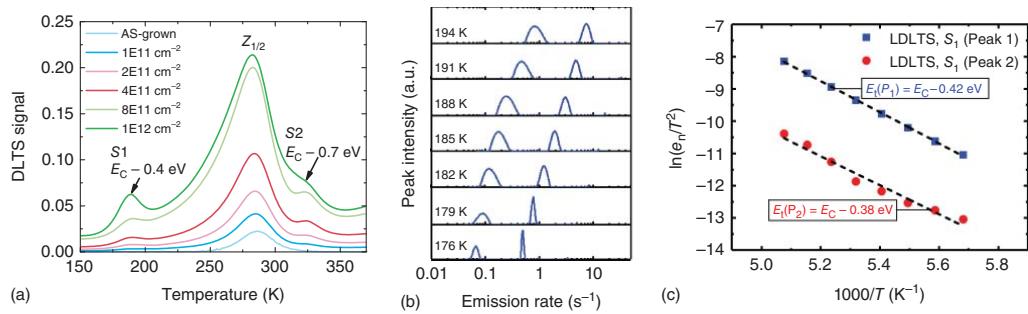
A definite assignment of  $S_1$  and  $S_2$  to  $V_{Si}$  and the identification of the  $(-/2-)$  and  $(2-/-3-)$  charge transition levels of  $V_{Si}$  using DLTS and a combination of proton irradiation, photoluminescence and DFT was presented by Bathen et al. [59].

LE- $\mu$ SR investigations show that a  $\mu^+$  in the vicinity of  $V_{Si}$  is captured to form an isolated and stable  $Mu^0$ , which does not interact further with the environment [35], an effect corroborated by the stability of the hydrogen- $V_{Si}$  complex found recently [66].

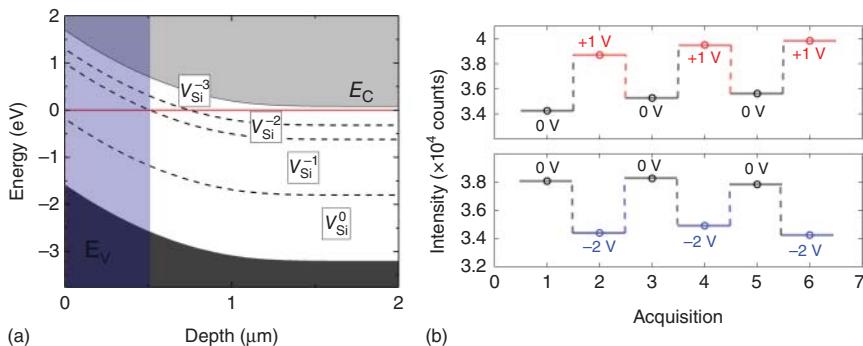
From optical measurements and DFT calculations,  $V_{Si}$  has for a long time now attracted a lot of attention as a high-spin qubit candidate with long spin lifetimes. From recent Laplace-DLTS, two contributions for the  $S_1$  state were identified, assigned to the hexagonal and cubic lattice site (see Figure 6.13). With the identification of the electronic signature, it is now possible to access the  $V_{Si}$  also electrically, as shown in Figure 6.14 and [59]. This may allow a good electrical spin control in a spintronic application in the true sense of the word.

## 6.3 Transition Metal and Other Impurity Levels in SiC

Transition metals (TM) are a common impurity in semiconductor material, often introduced during growth (see also other chapters in this book). Furthermore, intended doping with transitions metals is aimed at formation of recombination



**Figure 6.13** Experimental characterization of  $V_{Si}$  charge state transitions. (a) DLTS spectra of proton-irradiated n-type 4H-SiC samples, evidencing an increase in  $S_1$ ,  $Z_{1/2}$ , and  $S_2$  intensities with proton fluence. (b) Temperature-dependent Laplace-DLTS measurements of the  $S_1$  peak, demonstrating that  $S_1$  contains contributions from two defect centers, likely  $V_{Si}(h)$  and  $V_{Si}(k)$ . (c) Arrhenius behavior of the two contributions to  $S_1$  revealed by the Laplace-DLTS measurements. The confidence intervals for the activation energies are approximately  $\pm 0.01$  eV for  $E_t(P_1)$  and  $\pm 0.02$  eV for  $E_t(P_2)$ . Source: Reprinted with permission from [59] under the terms of the Creative Commons CC BY license. Copyright 2019, Springer Nature.



**Figure 6.14** (a) Simulation of a Schottky barrier diode using Sentaurus S-device [7], without applied bias and at 100 K and depiction of the different charges states of  $V_{Si}$ . (b) Selective switching of the  $V_{Si}$  luminescence intensity is experimentally demonstrated for the forward- and reverse-biased Schottky barrier diode. The sample has been irradiated with a proton fluence of  $1 \times 10^{12} \text{ cm}^{-2}$ . For each acquisition cycle, the intensity level on the plot represents an averaged value over 201 measurements, resulting in minimal standard deviation (within the marker size). Source: Adapted from [59].

centers for fast switching devices. Other transition metals are interesting for use in spintronic applications, e.g. for formation of diluted magnetic semiconductors. In Tables 6.1–6.3 and Figure 6.15, all unambiguously identified trap levels in SiC are summarized. The experienced reader will notice that the list of impurities and references is limited compared to the data collection presented in [13] and other reviews. We justify this approach by the careful analysis of the available data and publications. All data and references included in this work have been obtained by direct electrical measurements using DLTS, most of them using radiotracer DLTS, allowing an unambiguous assignment of the trap level to the impurity element, i.e. avoiding misinterpretation due to incompletely annealed radiation or any other processing damage. Also, the collection does not contain data from any optical method such as photoluminescence. As discussed above, the comparison between charge transitions as observed in photoluminescence with the capture and emission directly measured using DLTS is not straightforward and may be misleading. Furthermore, we did not include data where the original reference was not retrievable.

It should be pointed out here that this extreme approach does not allow us to provide any information on the following elements, which have been presented elsewhere: molybdenum, manganese, and oxygen. We hope that the reader acknowledges this rigor and that we can provide a truly reliable database for the years to come.

**Table 6.1** Transition metal impurities in SiC–parameters identified by DLTS.

Element	4H				6H				15R				3C			
	E (eV)	$\sigma$ ( $10^{-14}$ cm $^2$ )	Site	References	E (eV)	$\sigma$ ( $10^{-14}$ cm $^2$ )	Site	References	E (eV)	$\sigma$ ( $10^{-14}$ cm $^2$ )	Site	References	E (eV)	$\sigma$ ( $10^{-14}$ cm $^2$ )	Site	References
Cr (−/−)	−0.14	0.1		[1,2]												
	−0.18	0.1		[1,2]												
Cr (−/0)	−0.74	0.2	k/h	[1,2]	−0.53	2	k	[4]	−0.45	1	k	[5]				
					−0.55	2	h	[4]	−0.47	1	h	[5]				
Cr (+/++)	0.54	0.2	h	[3]												
	0.63	1	k	[3]												
V (−/0)	−0.96	1	k	[1,2]	−0.71	0.04	k	[4]	−0.7	0.2	k	[1,2]				
	−0.98	1	h	[1,2]	−0.75	0.1	h	[4]	−0.72	0.2	k	[1,2]				
									−0.74	0.01	k	[1,2]				
									−0.76	0.01	h	[1,2]				
									−0.8	0.01	h	[1,2]				
Ti (0/−)	−0.13	1		[1,2]												
	−0.17	1		[1,2]												

Negative values of  $E_a$  denote values measured from the conduction band edge, positive values of  $E_a$  denote values measured from the valence band edge.  
References: [1–5, 67–71]

**Table 6.2** Transition metal impurities in SiC–parameters identified by DLTS.

Element	4H				6H				15R				3C			
	E (eV)	$\sigma$ ( $10^{-14}$ cm $^2$ )	Site	References	E (eV)	$\sigma$ ( $10^{-14}$ cm $^2$ )	Site	References	E (eV)	$\sigma$ ( $10^{-14}$ cm $^2$ )	Site	References	E (eV)	$\sigma$ ( $10^{-14}$ cm $^2$ )	Site	References
Ta (0/+) -0.66 5 <i>h</i> [1] -0.46 10 <i>h</i> [2,3] -0.42 10 <i>h</i> [2,3]	-0.69 5 <i>k</i> [1] -0.49 10 <i>k</i> [2,3] -0.45 10 <i>k</i> [2,3]															
Ir (-/-) -0.82 7 [4]																
Pt (-/-) -0.81 0.4 [4]																
Pt (-/0) -1.46 0.3 [4]																
Ru (-/0) -0.87 1 [5]																
Pd (-/0) -1.03 0.1 [5]																
W (-/0) -0.17 50 <i>k/h</i> [6]	-1.43 100 <i>k/h</i> [6] -1.16 60 <i>k/h</i> [6] -1.14 60 <i>k/h</i> [6] -0.47 10 [7]															
Fe -0.39 0.2 [8]	1.46 3 [8]															
0.97 0.07 [8]																

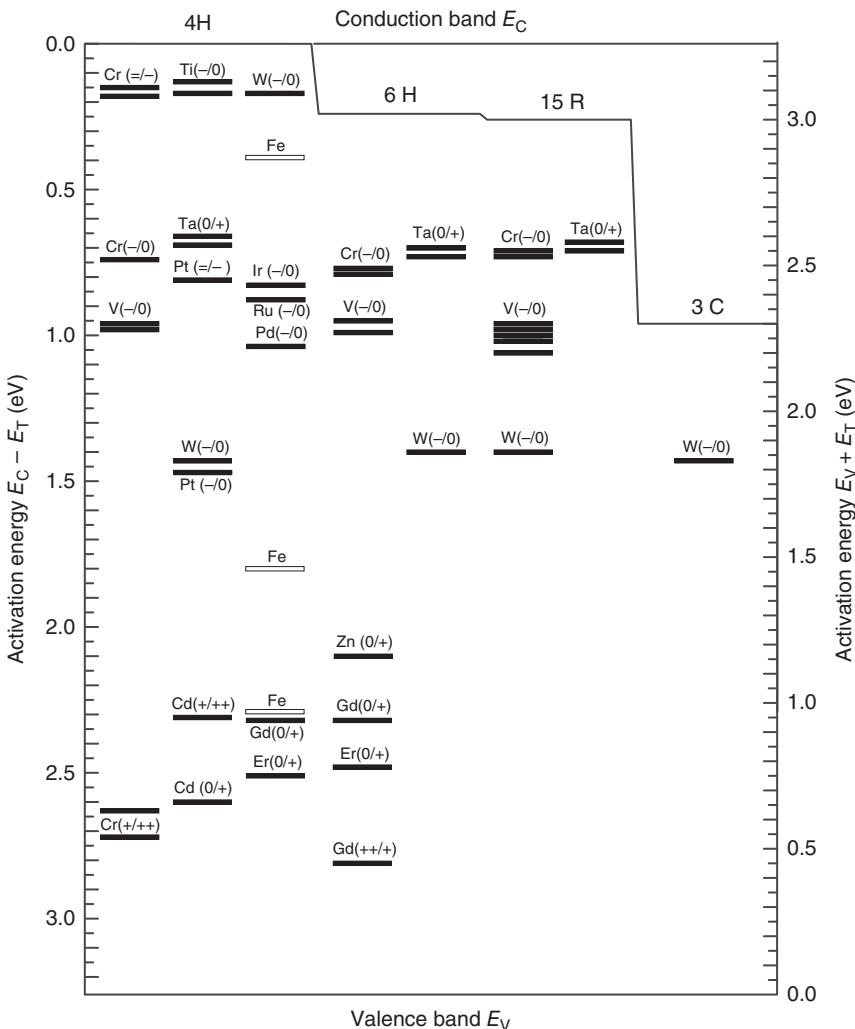
Negative values of  $E_a$  denote values measured from the conduction band edge, and positive values of  $E_a$  denote values measured from the valence band edge.  
References: [1–8, 15, 72–78]

**Table 6.3** Other impurities in SiC—parameters identified by DLTS.

Element	4H				6H				15R				3C			
	E (eV)	$\sigma$ ( $10^{-14}$ cm $^2$ )	Site	References	E (eV)	$\sigma$ ( $10^{-14}$ cm $^2$ )	Site	References	E (eV)	$\sigma$ ( $10^{-14}$ cm $^2$ )	Site	References	E (eV)	$\sigma$ ( $10^{-14}$ cm $^2$ )	Site	References
Be (-/0)	1.06	5	k/h	[1]												
Zn (+/0)					1.16	1.4										
Cd (++/+) 1.19	0.02	k/h	[2]													
Er (+/0) 0.75	2	k/h	[4]	0.78	2	k/h	[4]									
Gd (+/0) 0.94	4		[5]	0.95	4		[5]									
Eu (+/0) 0.86	4...7		[6]	0.88	4...7		[6]									

Negative values of  $E_a$  denote values measured from the conduction band edge, and positive values of  $E_a$  denote values measured from the valence band edge.

References: [1–6, 79–84]



**Figure 6.15** Overview of all, by means of DLTS, directly measured trap levels caused by impurities, which have been unambiguously assigned to the respective element and have been measured in the respective polytype. Detailed data and the corresponding references are listed in Tables 6.1–6.3.

## 6.4 Summary

To conclude this chapter on electrically active defects in SiC, let us briefly summarize our findings first.

For both  $V_C$  and  $V_{Si}$ , the electrical signatures have now been clearly identified. This enables not only a much clearer picture on how these intrinsic defects behave but it also allows the cross pollination toward a variety of very targeted new studies and the development of new and exciting applications.

Furthermore, it is impressive how the combination of methods such as DLTS, LE- $\mu$ SR, photoluminescence spectroscopy, and DFT can deliver insights into the capture and emission processes of charges in these intrinsic defects. A  $\mu^+$  in the vicinity of  $V_{\text{Si}}$  is captured to form an isolated and stable  $\text{Mu}^0$ , which does not interact further with the environment. The capture of  $\mu^+$  at  $V_{\text{C}}$  may also result in the formation of  $\text{Mu}^0$ , but interactions between  $V_{\text{C}}$  and the environment are strong, prompting the capture of a second electron and the formation of delayed  $\text{Mu}^-$ . This is similar to electron localization in  $V_{\text{Si}}^-$ , where weak interactions between  $V_{\text{Si}}$  and the surroundings result in long spin coherence times and a weak outward breathing motion of the neighboring carbon atoms. Conversely, the neighboring atoms surrounding  $V_{\text{C}}$  collapse inward following a symmetry-lowering path, leaving a smaller lattice void for the muon to fill in  $V_{\text{C}}$  compared to  $V_{\text{Si}}$ . The strong electron–phonon coupling of  $V_{\text{C}}$  leads to a prominent Jahn–Teller distortion of the surrounding geometry, which may be indirectly probed via the Mu formation process of the implanted  $\mu^+$ . This interpretation is also supported by DFT calculations, where the geometric relaxation surrounding  $(V_{\text{Si}}\text{-Mu})^-$  is almost identical to that of  $V_{\text{Si}}^-$ , while introducing a muon into  $V_{\text{C}}^0$  and forming  $(V_{\text{C}}\text{-Mu})^+$  yields significant interactions between  $\mu^+$  and the lattice.

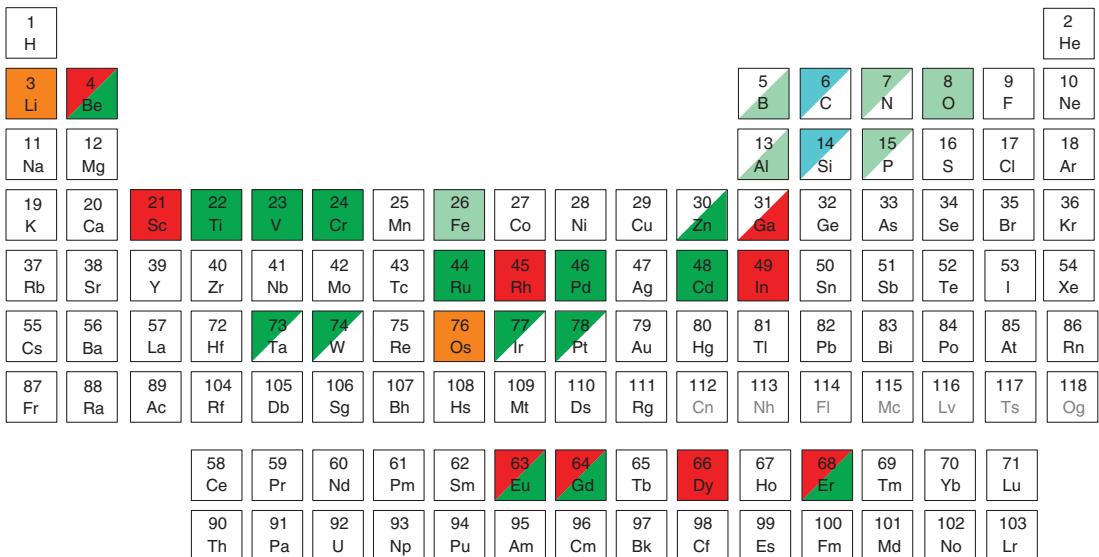
Laplace-DLTS has further revealed the exact activation energies for the different charge states of  $V_{\text{C}}$  and  $V_{\text{Si}}$ , along with small capture cross sections in the range of  $10^{-15} \text{ cm}^2$  to  $10^{-16} \text{ cm}^2$  for  $V_{\text{C}}$  [54] and  $10^{-17} \text{ cm}^2$  to  $10^{-15} \text{ cm}^2$  for  $V_{\text{Si}}$  [65].

This is in contrast to what we often read as a description of “shallow levels” as formed by dopants [20]. Here, higher concentrations are used (see discussion in the very beginning of this chapter) and, therefore, there is a higher probability of overlapping charges. The term “deep levels,” on the other hand, is commonly used for levels with activation energies away from the two band edges, and, more importantly, with localized wave function (and, hence, small capture cross sections). Keeping this strong localization of electrons for both  $V_{\text{C}}$  and  $V_{\text{Si}}$  in mind, let us further assess also the available information on extrinsic electrically active defects.

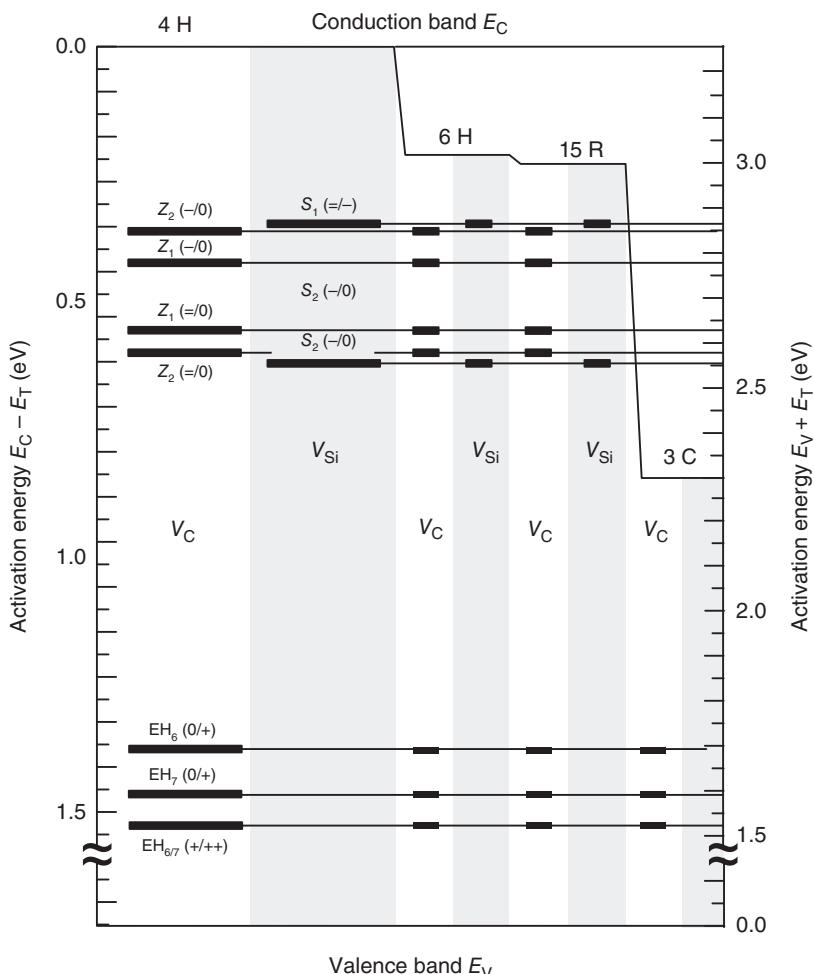
A large variety of elements have been investigated for their impact on SiC and its bandgap. In Figure 6.16, all presently available information is collected in a more graphical manner. In this graph, the information is given for 4H-SiC; the results presented in Figure 6.15 and in the Tables 6.1–6.3, however, represent the collective amount of unambiguously confirmed impurity levels in the respective polytype, as available (4H, 6H, 15R, 3C).

For a very long time now, the alignment of transition-metal-induced traps in the bandgap of SiC has been discussed and is experimentally verified (see also Section 6.3). This alignment has initially been suggested in [85] for transition metals in III–V heterostructures. In addition, the reader shall also be reminded of one of the first theoretical attempts to assess the electronic properties of transition metals in SiC: The site preference for a variety of 3d-transition metals [86].

These early results have shown two aspects: a pronounced difference in the charge configuration of  $V_{\text{C}}$  and  $V_{\text{Si}}$  and, consequentially, a pronounced difference



**Figure 6.16** Depiction of the table of elements: elements marked green have unambiguously been assigned to electrically active defects in 4H-SiC; light green denotes a confirmed assignation using conventional DLTS (POSITIVE), full green an assignation obtained by chemically sensitive radiotracer DLTS (TRUE\_POSITIVE). Marked in full red are the elements that have been investigated, but no trap level has been detected (TRUE\_NEGATIVE). Orange are the elements that have been investigated, but the assignation may be influenced by recoil effects (potentially FALSE\_NEGATIVE). Light blue are the intrinsic defects  $V_c$  and  $V_{Si}$ , which have been unambiguously identified using a combination of different methods (POSITIVE). In any case, upper triangles indicate traps in the upper half of the bandgap, denoting states measurable in n-type SiC; lower triangles indicate traps in the lower part of the bandgap, i.e. in p-type SiC.



**Figure 6.17** Suggested positions for  $V_C$  and  $V_{Si}$  in the 4H, 6H, 15R, and 3C polytype, assuming the validity of the assignment for 4H-SiC and their alignment according to [85].

in bonding of impurity 3d elements: “... the TMs surrounded tetrahedrally by four Si atoms experience a large crystal field splitting while the tetrahedral C environment does not give rise to a significant crystal field splitting at all. It is only in the latter case that high-spin configurations are predicted.” [86].

Let us now put the findings from this early study in context with our current discussion and recapitulate: The Rule of Langer and Heinrich [85] is fully confirmed and accepted for extrinsic defects exhibiting primarily rather small capture cross sections. The identification of the electronic signature for  $V_C$  (i.e. the correct assignment of the levels previously named  $Z_{1/2}$  and  $EH_{6/7}$ ) and  $V_{Si}$  (i.e.  $S_1$  and  $S_2$ , respectively) allowed further characterization and verification of the local charge relaxation behavior and confirmed a similarly small capture cross section as for transition metals.

These considerations now allow us to make a very firm statement toward the alignment of the intrinsic defects, namely,  $V_C$  and  $V_{Si}$ , in different SiC polytypes, similarly to the ones of transition metals. This alignment has been suggested before for the DLTS level EH<sub>6/7</sub> but could not be further confirmed or assigned to either of the vacancy types [87].

Figure 6.17 shows the proposed alignment of the electrically active states of the two intrinsic defects considered in the context of this work.

The collected results are now concluded for their impact in applications. A focus on  $V_C$  concentration for tailoring charge carrier lifetime in power devices is, once more, confirmed to be crucial. For emerging application involving spin control, the focus can be on the  $V_{Si}$ , at least for 4H-SiC and up to temperatures slightly below room temperature. For integration of spintronics on 3C-SiC; however, the use of a transition metal impurity is required. Here, the focus should be on an element substituting for an Si atom (i.e. the site of the  $V_{Si}$ ), as otherwise the formation of a high-spin configuration is unlikely.

And last but not least, for all applications, the position of the Fermi level for the respective operating point should be considered ...

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**7****Dislocations in 4H-SiC Substrates and Epilayers**

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**7.1 Introduction**

Silicon carbide (SiC), chiefly the 4H polytype, is a wide bandgap semiconductor highly suited for electronic and optoelectronic devices operating under high temperature, high power, high frequency, and/or strong radiation conditions, where conventional semiconductor materials such as silicon, GaAs, and InP are considered to have reached their limits [1]. SiC-based devices require the production of high-quality thin films, which in turn require high-quality substrates. Commercial SiC wafers are obtained from bulk crystals predominantly grown by physical vapor transport (PVT, also called seeded modified Lely growth) [2], while homoepitaxial growth of SiC on these substrates is commonly achieved by chemical vapor deposition (CVD) directly from the gas phase [3–6]. The high-temperature chemical vapor deposition (HTCVD) process [7, 8] can also yield thicker films and higher growth rates while halide CVD has also received much attention due to the lower decomposition temperature of halide precursors [9]. Solution growth methods such as the top-seeded solution growth (TSSG) method [10] are also being developed for bulk growth of SiC.

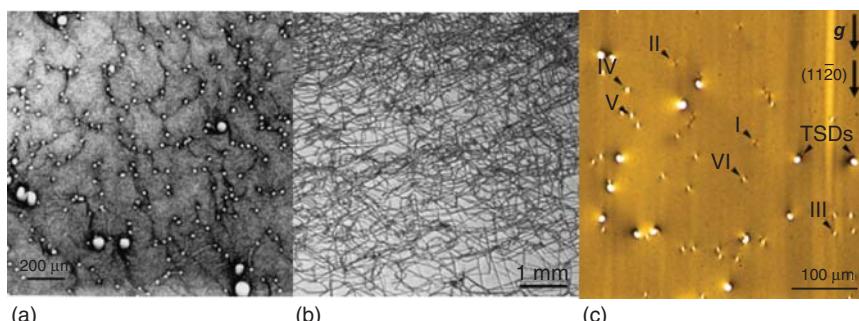
During both bulk and epitaxial growth, management of the various growth parameters including thermal profile of the growth system and resultant thermal gradient stresses within the growing crystal are critical to control the nucleation and propagation of various defects. Crystalline imperfections, such as growth dislocations of screw character with closed-cores and hollow-cores (micropipes [MPs]), deformation-induced basal plane dislocations (BPDs), parasitic polytype inclusions, planar defects (stacking faults, microscopic twins and small angle boundaries), and hexagonal voids, affect the device performance to different extents [11–14], and the lowering of their densities is a primary goal of the SiC crystal growth community. Synchrotron white beam X-ray topography (SWBXT) and synchrotron monochromatic beam X-ray topography (SMBXT) [15] have played a

key role in revealing the detailed configurations of these defects and have been able to shed much light on their origins [16, 17], thereby enabling the development of strategies for their elimination.

## 7.2 Dislocations in Bulk 4H-SiC

### 7.2.1 Micropipes (MPs) and Closed-core Threading Screw Dislocations (TSDs)

Screw dislocations lying along the [0001] axis have Burgers vectors equal to  $nc$  with hollow cores becoming evident with  $n \geq 2$  for 6H and SiC  $n \geq 3$  for 4H SiC [18]. Using back-reflection geometry in SWBXT, both closed- and hollow-core (MPs) screw dislocations (Figure 7.1a) are revealed [19]. Possible mechanism for nucleation of MPs involves the incorporation of inclusions, which could be, for example, graphite particles, silicon droplets or even voids, into the crystal lattice [20–24]. Recent improvements in the growth process have effectively eliminated the nucleation of MPs in 4H-SiC, but Figure 7.1a TSDs are always present. Regarding the nucleation of screw dislocations with predominantly *c*-component Burgers vectors, the highly anisotropic hexagonal structure of 4H (or 6H) SiC may play a critical role. Normally, the relief of external stresses such as those occurring during crystal growth occurs by the process of deformation, i.e. nucleation and motion of dislocations. In 4H-SiC, the basal plane is the predominant deformation plane, and dislocations with Burgers vectors of type  $1/3\langle 11\bar{2}0 \rangle$  are involved to relieve stresses within the basal plane. Prismatic slip on the  $\{1\bar{1}00\}$  planes also involves dislocations with the same Burgers vector type, i.e.  $1/3\langle 11\bar{2}0 \rangle$  and thus displacements are limited to the basal plane. Since no deformation-induced dislocations contribute to relief of stresses outside the basal plane, threading screw dislocations (TSDs) and threading mixed



**Figure 7.1** (a) Back-reflection X-ray topograph images of closed-core (smaller white spots) and hollow-core (large white spots) screw dislocations in a (0001) 6H SiC wafer; (b) transmission X-ray topograph of 4H-SiC substrate showing network of BPDs; (c) monochromatic beam X-ray topograph ( $g = 11\bar{2}8$ ) showing the images of six types of TEDs in 4H-SiC; (I)  $b = 1/3[\bar{1}2\bar{1}0]$ ; (II)  $b = 1/3[\bar{2}110]$ ; (III)  $b = 1/3[1\bar{1}20]$ ; (IV)  $b = 1/3[1\bar{2}10]$ ; (V)  $b = 1/3[\bar{2}110]$ ; (VI)  $b = 1/3[11\bar{2}0]$ .

dislocations (TMDs) that have Burgers vectors perpendicular to or at large angles to the basal plane provide the displacements to accommodate local high stress concentrations. Such stress concentrations while present around inclusions also exist at the seed-crystal interface thereby resulting in nucleation of TSD or TMD pairs.

### 7.2.2 Basal Plane Dislocations (BPDs)

BPDs are glissile dislocations with both line directions and Burgers vectors (i.e.  $1/3\langle 11\bar{2}0 \rangle$ ) in the basal plane (0001) (Figure 7.1b). Detailed Burgers vector analysis of these dislocations can be easily performed using the  $\mathbf{g} \cdot \mathbf{b}$  and  $\mathbf{g} \cdot \mathbf{b} \times \mathbf{l}$  criteria similar to TEM. Observation of the morphologies of the BPD loops clearly indicates that they are deformation induced and appear to have been nucleated both at the crystal edges and at the sites of MPs/screw dislocations [16].

### 7.2.3 Threading Edge Dislocations (TEDs)

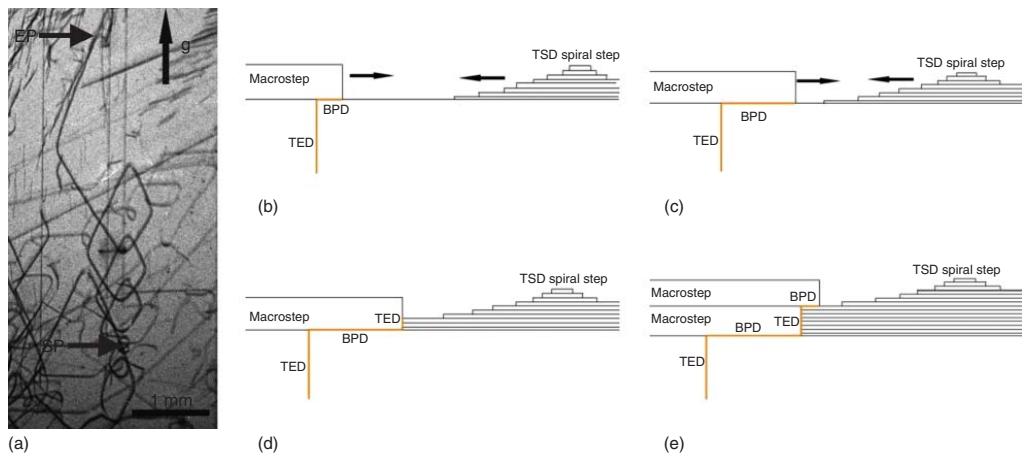
In 4H-SiC, threading edge dislocations (TEDs) are dislocations with line directions roughly parallel to *c*-axis and Burgers vectors in basal plane, i.e  $1/3\langle 11\bar{2}0 \rangle$ . TEDs are one of the major components of low-angle grain boundaries (LAGBs). The six different directions of the TED Burgers vector in 4H-SiC (Figure 7.1c) can be unambiguously identified by comparing their image features to their corresponding ray tracing simulated  $(1128)$  grazing-incidence topograph images [25].

### 7.2.4 Interaction between BPDs and TEDs

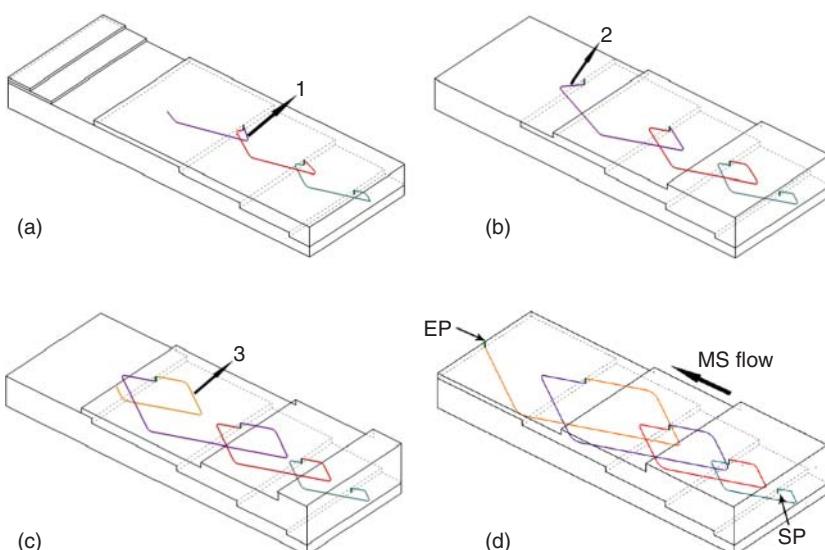
#### 7.2.4.1 Hopping Frank–Read Source of BPDs

Studies of the configurations and behavior of BPDs in wafers cut from PVT-grown SiC boules have enabled identification of the operation of single-ended Frank–Read sources which are interconnected on different basal planes [26]. Figure 7.2 shows an example of a final configuration of a BPD which has developed into a sequence of diamond-shaped loops on different basal planes connected by TED segments sufficiently long enough to reduce their mutual interaction forces. The dislocation has a Burgers vector of  $1/3[11\bar{2}0]$  with the segments comprising the loops along  $\langle 1\bar{1}00 \rangle$  line directions.

A macrostep deflection of the surface outcrop of the TED onto the basal plane creates a segment of BPD (Figure 7.2b). If the BPD segment is in screw orientation, further advancement of the macrostep will replicate the BPD in the direction of step flow (7.2c). If the advancing macrostep encounters a step advancing in the opposite direction, for example, a spiral step from a screw dislocation, the dislocation will be re-deflected into the threading direction as shown in the schematic cross sections in Figure 7.2d. At a later stage of growth, if the outcrop of the re-deflected TED encounters another advancing macrostep, the whole process can be repeated (Figure 7.2e). As soon as the TED is deflected onto the basal plane, a single-ended Frank–Read (marked as no. 1) source will begin to operate (Figure 7.3a). The deflected BPD segments move away from screw orientation and is expected to



**Figure 7.2** SWBXT transmission image ( $g = \overline{11\bar{2}0}$ ) showing a diamond-shaped BPD loop (SP – starting point; EP – ending point). (b)–(e) Schematic cross-sectional view of the deflection of a TED onto the basal plane by a macrostep followed by re-deflection up into threading orientation through the encounter between macrostep and a TED spiral advancing in the opposite direction.

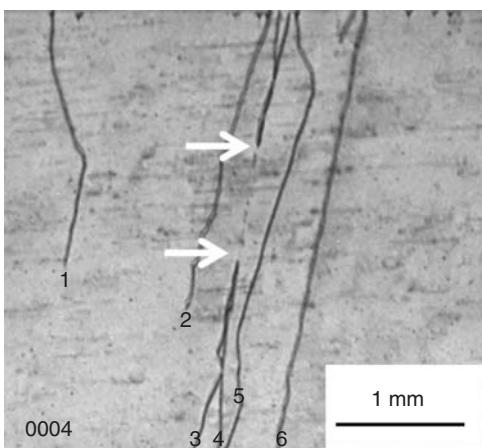


**Figure 7.3** (a)–(c) Schematic of the formation of a single-ended Frank–Read source through the deflection of a TED into a BPD and back again. The TED segments act as pinning points for the BPD glide; (d) the final configuration of the loops produced by the Hopping Frank–Read source. “SP” indicates the starting point, and “EP” end point. Source: Wang et al. (2014). Characterization of Defects in SiC Substrates and Epilayers. ECS Transactions, 64(7), 145–152.

become more susceptible to conversion into a TED segment. When the BPD is re-deflected into threading orientation, a second single-ended source (marked as no. 2) will initiate at that point. As this new TED segment in deflected again onto the basal plane, a third single-ended source (marked as no. 3) will initiate (see Figure 7.3c). For these latter two sources to be able to operate independently the BPD segments on parallel basal planes must be separated by a distance large enough that their mutual repulsive forces can be overcome. If the distance is too small, the gliding BPDs will simply continue to draw out the dislocation dipole which will remain locked in place (Fig 7.3a). On the other hand, if the separation is large enough, the two BPD arms can effectively behave independently of each other as single-ended sources (Figure 7.3b). Thus, the resultant BPD configuration effectively behaves like a series of single-ended Frank–Read sources which “hop” from one slip plane to other parallel slip planes through a process of double deflection involving overgrowth by macrosteps followed by impingement of the overgrowing macrostep on a step moving in the opposite direction. This behavior is termed as a Hopping Frank–Read source mechanism.

### 7.2.5 Threading Mixed Dislocations (TMDs) in 4H-SiC

In addition to MPs and pure screw dislocations where the Burgers vectors are one to several times  $c$ , 4H-SiC crystals also contain threading dislocations with both  $c$  and  $a$  components [27, 28]. Figure 7.4a shows an SWBXT image ( $g = 0004$ ) from



**Figure 7.4** Transmission topograph ( $g = 0004$ ) shows dislocation contrast from 1 to 6.

**Table 7.1**  $\mathbf{g} \cdot \mathbf{b}$  values for dislocations from 1 to 6 in Figure 7.9.

$\mathbf{g} \cdot \mathbf{b} \mathbf{g} \mathbf{b}$	0004	$0\bar{1}10$	$1\bar{2}10$	$01\bar{1}\bar{1}$	$0\bar{1}11$	$10\bar{1}5$
<b>1&amp;6:</b> $1/3[1\bar{2}13]$ , $c+a$	4	1	2	0	2	-5
<b>3:</b> $1/3[\bar{1}\bar{1}23]$ , $c+a$	4	1	1	0	2	-5
<b>4:</b> $1/3[\bar{1}\bar{1}2\bar{3}]$ , $-c+a$	-4	1	1	-2	0	5
<b>2&amp;5:</b> $\langle 0001 \rangle$ , TSD	4	0	0	1	1	-5
<b>Arrow:</b> $2/3[\bar{1}120]$ , $2a$	0	2	2	-2	2	-2

an axial slice where segments of six threading dislocations labeled **1–6** are visible although dislocations **3** and **4** appear to have interacted such that parts of their length have apparently annihilated. By carrying out detailed contrast analysis on multiple reflections (see Table 7.1), the Burgers vectors of these dislocations are estimated.

The exact Burgers vectors are revealed through the interactions between the threading dislocations with  $c$ -component of Burgers vector. Two closed-core threading dislocations with opposite  $c$ -component experience a strong attractive force but the reaction is difficult via slip but can be achieved by interaction with non-equilibrium concentration of vacancies (i.e. climb). These reactions are summarized later.

### 7.2.5.1 Reaction Between Threading Dislocations with Burgers Vectors of $-c+a$ and $c+a$ Wherein the Opposite $c$ -Components Annihilate Leaving Behind the Two $a$ -Components

In Figure 7.4, a segment of dislocation lines **3** and **4**, marked with arrows, appears to have annihilated and shows no contrast. As illustrated in Figure 7.5a, dislocation **3** and **4** have opposite sign  $c$ -components and these  $c$ -components annihilate while the two  $a$ -components are left behind. Figure 7.5b shows a section topograph superimposed onto a  $0004$  projection topograph. From the sense of the mutual shift between the bimodal image components, it can be seen that dislocation **3** and **4** have

right-handed and left-handed screw components, respectively, and thus annihilate when they meet.

#### 7.2.5.2 Reaction Between Threading Dislocations with Burgers Vectors of $-c$ and $c + a$ Leaving Behind the $a$ -Component

Figure 7.5d shows a reaction between  $-c$  and  $c + a$  dislocations. The  $-c$  TSD annihilates with the opposite sign  $c$ -component of the  $c + a$  dislocation leaving a single  $a$ -component behind (Figure 7.5d). TSD dislocation 7 is visible in Figure 7.5e and out of contrast in Figure 7.5f while dislocation 8 is visible in both images, which suggest that it has both  $c$ - and  $a$ -components. The annihilated segment, marked by arrows, is invisible in Figure 7.5e and visible in Figure 7.5f, which indicates that the annihilated segment has only an  $a$ -component of Burgers vector.

#### 7.2.5.3 Reaction Between Opposite-sign Threading Screw Dislocations with Burgers Vectors $c$ and $-c$

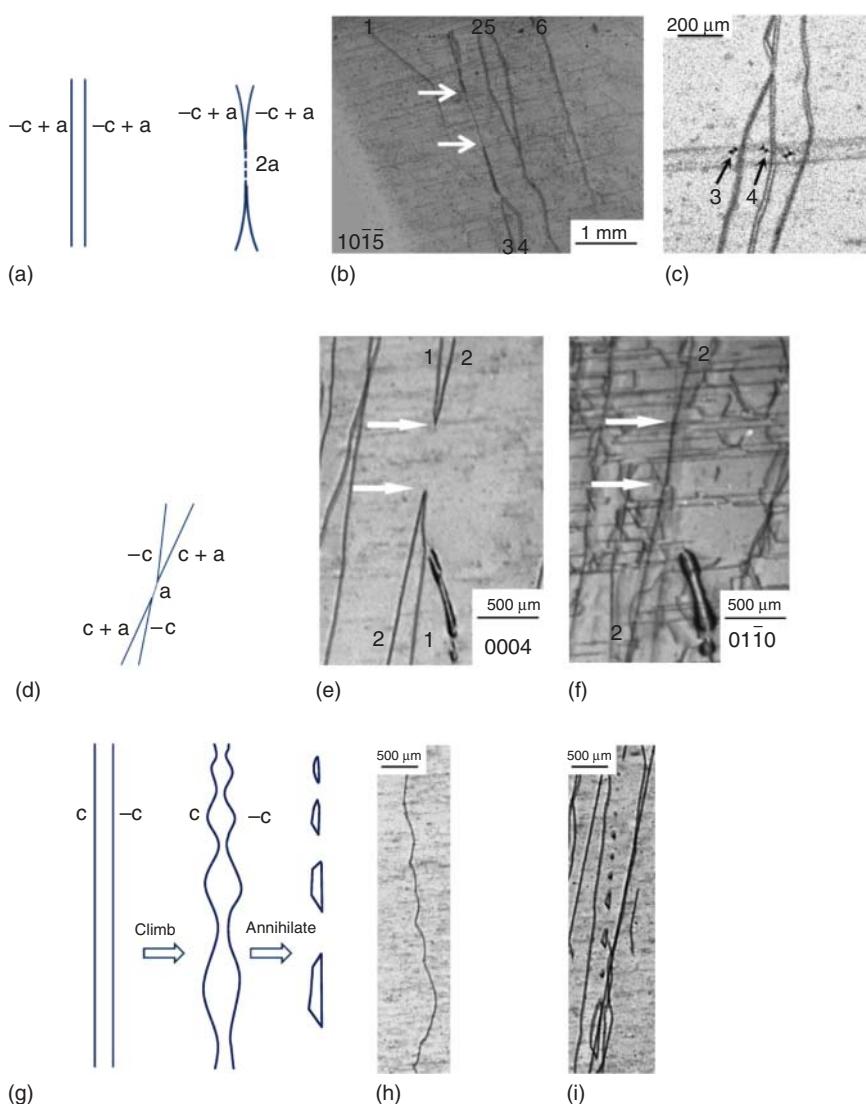
Figure 7.5g shows a typical helical morphology of a TSD and when two dislocations like this are close to each other, the interaction between TSDs with opposite signs of Burgers vectors will occur, as shown in Figure 7.5h where some segments annihilate leaving others in the form of trails of stranded loops comprising closed dislocation dipoles.

#### 7.2.5.4 Nucleation of Opposite Pair of $c + a$ Dislocations and Their Deflection

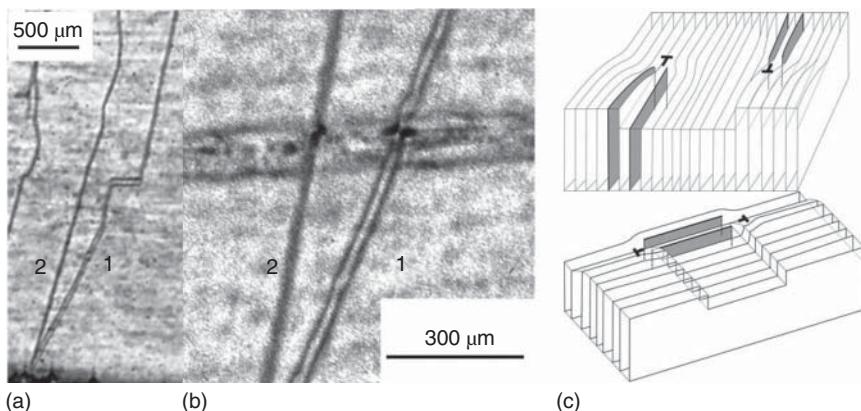
Figure 7.6a shows a pair of  $c + a$  dislocations nucleated from an inclusion. To satisfy Burgers vector conservation, these two dislocations originating from an isolated inclusion inside a perfect crystal region must have opposite sense of Burgers vector. This is evident from Figure 7.5b that shows a section topograph, which shows the sense of the mutual shift between the bimodal image components, it can be seen that dislocation 1 has right-handed screw component while dislocation 2 has left-handed which confirms that dislocations 1 and 2 have opposite  $c$ -components.

Overgrowth of an inclusion during step flow crystal growth creates a closure failure which is accommodated by the nucleation of the opposite sign pair of screw dislocations [29]. Similarly, when an inclusion is overgrown by growth steps on the growth face, dislocations of opposite sense are created to accommodate the misalignment that has magnitude equal to  $c + a$ . Two possible surface configurations at the growth front after the generation of the opposite sign pairs are shown Figure 7.6c. Two extra half-planes are associated with  $a$ -component of  $c + a$  dislocations and the surface outcrop at the dislocation core is associated with  $c$ -component of the dislocations.

Occasionally, partial deflection of  $c + a$  dislocation is observed, in which the  $a$ -component of  $c + a$  dislocation deflects onto basal plane and  $c$ -component continues growing along the growth direction; as a result,  $c + a$  dislocation diverges into a BPD with  $\mathbf{b} = a$  and a TSD with  $\mathbf{b} = c$ , as shown in Figure 7.7. A pair of opposite sign  $c + a$  dislocations described above propagates along growth direction, and later at some level,  $a$ -component of the dislocation on the left is deflected onto the basal plane and the  $c$ -component continues to propagate while the  $c + a$  dislocation on



**Figure 7.5** (a) Illustration of the reaction between  $-c+a$  and  $c+a$  dislocation; (b) overlapping 0004 section topograph on projection topograph shows opposite signs of dislocation 3 and 4, since their screw arrangements are mirror images. (d) Illustration of the reaction between  $-c$  and  $a+c$  dislocation; (e) SWBXT image of 0004 reflection showing the annihilation of  $-c$  and  $c+a$  dislocation, named 7 and 8, respectively; (f) 0110 reflection showing the strong contrast of dislocation 8 as well as "the annihilation segment," and absence of dislocation 7. (g) Illustration of the reaction between  $c$  and  $-c$  dislocation; (h) SWBXT image of 0004 reflection showing curved slightly helical morphology of  $c$  dislocation; (i) 0004 reflection at different regions showing annihilation of  $c$  and  $-c$  dislocation at some segments leaving others in the form of stranded loops comprising closed dislocation dipoles. Source: Wang et al. (2014). Characterization of Defects in SiC Substrates and Epilayers. ECS Transactions, 64(7), 145–152.



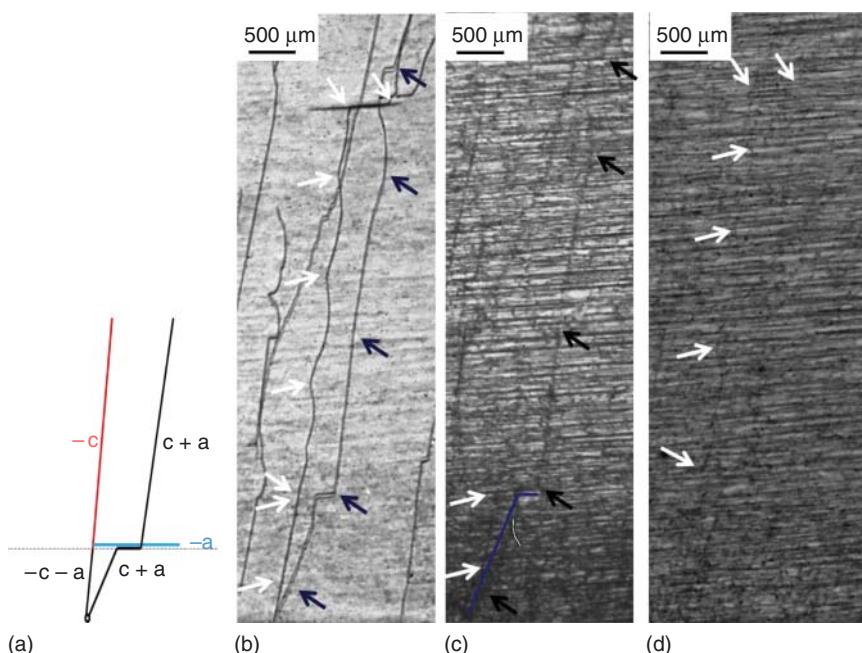
**Figure 7.6** (a) SWBXT transmission image of 0004 reflection; (b) a section topograph superimposed on a projection topograph revealing the sense of the opposite sign dislocation pairs. (c) two possible configuration of the opposite sign  $c + a$  dislocations being nucleated

the right is completely deflected onto the basal plane and later redirected back into the growth direction. The deflection process here is strongly related to the advancement of macrosteps.

#### 7.2.5.5 Deflection of Threading $c + a$ , $c$ and Creation of Stacking Faults

Three types of stacking faults have been observed to date in 4H-SiC: Shockley faults, Frank faults and those which comprise some kind of combination of these two. Such faults can arise from the deflection of  $c$ -axis threading dislocations of Burgers vector  $\mathbf{c}$  and  $\mathbf{c} + \mathbf{a}$  onto the basal plane [30, 31]. If the spiral step risers of such dislocations divide into  $c/4$  and  $3c/4$  increments, overgrowth can be facilitated by the simultaneous dragging of one of the Shockley partials associated with the core structure of the original dislocation by the overgrowing macrostep. This acts like an interfacial Shockley partial and adds the Shockley component to the  $c/4$  Frank component of fault vector. Stacking faults vectors can be determined by X-ray topography by analyzing the contrast from stacking faults on multiple X-ray topographs which arises from the phase shift experienced by the X-ray wavefields as they cross the fault plane [32]. This phase shift has been computed to be equal to  $\delta = (-2\pi g \cdot R)$ , where  $g$  is the active reciprocal lattice vector for the reflection and  $R$  is the fault vector.

Formation of these faults can be understood by considering two processes. First is the overgrowth of TEDs onto the basal plane in the step flow direction and the second involves the overgrowth of dislocations of the type  $c + a$  (i.e. both  $c$  and  $a$  components are anchored at the dislocation outcrop). This result in the deflection of extra half planes associated with “ $a$ ” component to deflect onto basal plane, but in this case, the Shockley partial dislocations are separated by the step height of the “ $c$ ” dislocation. The deflected dislocations under thermal shear stress glides creating large faults, with the leading partial faulting and trailing partial unfaulting the plane in case of TEDs and in case of  $c + a$  dislocations the partials cannot move in tandem as they are separated by step height due to which depending on direction of force

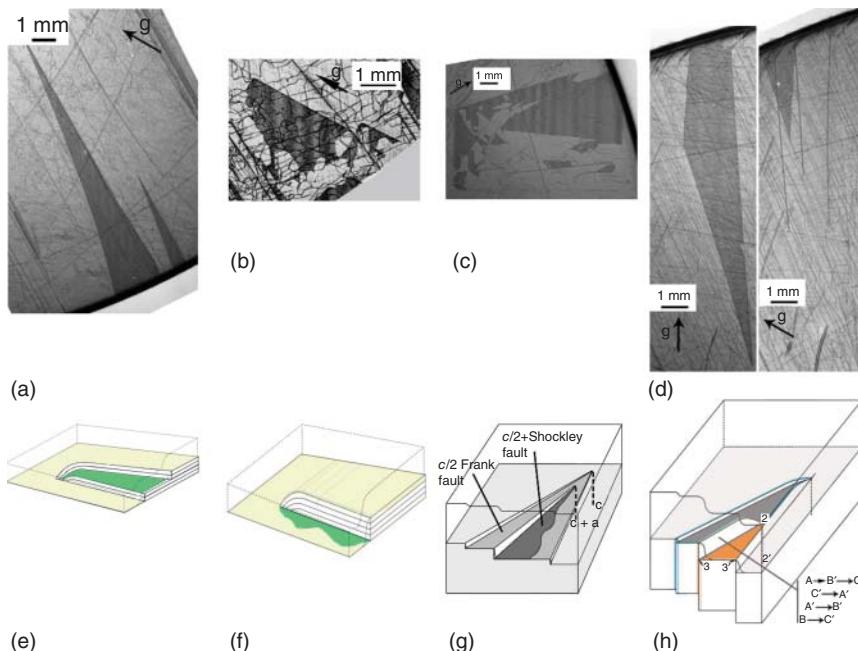


**Figure 7.7** (a) Illustration of partial deflection of threading  $c+a$  dislocations shown in (b)–(d); (b) 0004 reflection shows a pair of opposite-sign threading  $c+a$  dislocations as well as a segment of pure screw dislocation; (c) 0110 reflection shows contrast from the segments of  $-c-a$  dislocation marked by white arrows and  $c+a$  dislocations marked by black arrows; (d) 0111 reflection shows contrast from the segment of pure screw dislocation marked by white arrows.

one partial glides creating faults while the other partial gets locked. Based on these two models, four fault vectors have been determined described as follows:

**Type I: Frank Fault:** Frank faults are “in-grown” stacking faults and result from the overgrowth of  $c$ -axis screw dislocations whose surface growth spiral steps were separated into  $c/2$  increments. Figure 7.8a shows SWBXT image in transmission geometry of such a fault. Detailed analysis of the contrast from different reflections shows the fault vector is  $1/2[0001]$ .

**Type II: Shockley faults:** Figure 7.8c is a SWBXT image recorded from a section of a  $n+$  4H-SiC crystal showing stacking fault configurations which has one straight edge corresponding to the sessile partial and the other being curved corresponding to the glissile partial. In this case the step has an integral number of unit cells high, the resultant expanding fault will be a Shockley fault (since the out-of-plane component is  $nc$ , where  $n$  is an integer). Detailed analysis of the fault contrast revealed the fault vector to be  $1/3[01\bar{1}0]$  which corresponds to a Shockley fault. Figure 7.8d is an illustration showing the integral number of step height, where the glissile partial lying below the step has created faults while the sessile partial at the top gets locked.



**Figure 7.8** Transmission SWBXT images from 4H-SiC crystals showing stacking faults with fault vector: (a)  $R = 1/2[0001]$  (Frank fault); (b)  $R = 1/3[\bar{1}\bar{1}00]$  (Type I Shockley fault); (c)  $R = 1/6[20\bar{2}3]$  vector ( $S + c/2$ ); (d)  $R = 1/12[\bar{4}043]$  (i) and  $R = 1/12[\bar{4}403]$  (ii) (vector  $S + c/4$ ). Illustration of the stacking faults: (e) Frank-type stacking fault resulting from the overgrowth of a  $c$ -axis screw dislocation which has separated into two  $c/2$  step heights. The area between the two demisteps corresponds to the Frank fault; (f) Type I Shockley fault vector showing integral number of step height with the glissile partial lying below the step and the sessile at the top which is locked; (g) Overgrowth of  $c$  dislocation and formation of the  $c/2$  Frank-type fault within which a  $c + a$  dislocation with one sessile Shockley partial and one glissile Shockley partial converts some part of the fault to  $c/2$  plus a Shockley type; (h) overgrowth of  $c + a$  dislocation with a  $c$ -height step converting it into a Frank dislocation plus two Shockleys with one sessile and the other glissile. Overgrowth of  $c + a$  dislocation 11' with  $c/4$  and  $3c/4$ -height steps which has second 22' with  $c$ -height spiral step protruding onto the terrace between these two step risers. Stacking sequences are indicated, the “interfacial Shockley” converts A layer into B', allowing overgrowth by the A' layer at the bottom of the macrostep. Following overgrowth the Shockley associated with the deflected 22' dislocation located at 23 glides under stress until it reaches the edge of the step 23' creating the fault of type A shown in (d). Source: Wang et al. (2014). Characterization of Defects in SiC Substrates and Epilayers. ECS Transactions, 64(7), 145–152.

**Type III:** Combination of Shockley and Frank fault with fault vector  $S + c/2$ :

These faults are a combination of Shockley and Frank faults resulting from the overgrowth of  $c$ -axis screw dislocations whose spiral steps have divided into two  $c/2$ -high demisteps and which has several  $c + a$  dislocations with  $c$ -height spiral step risers protruding onto the terrace between the two demisteps. Figure 7.8e shows a SWBXT image of stacking faults in a 76 mm wafer. Overgrowth of  $c$ -axis screw dislocation and  $c + a$  dislocations which has protruded the terrace created

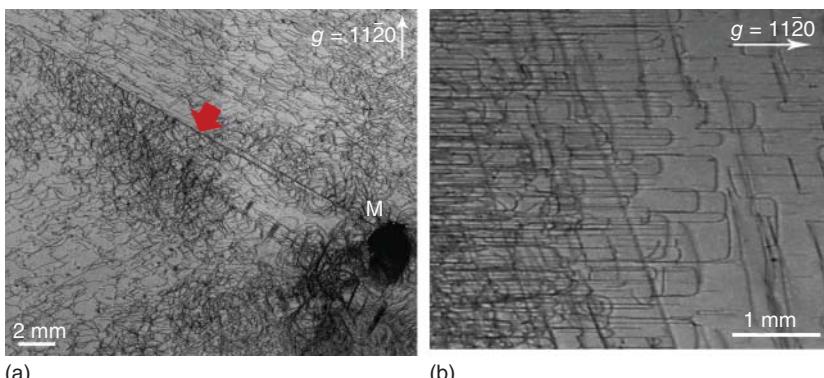
by two demisteps results in both  $c/2$  Frank fault and Shockley fault associated with  $c + a$  to lie on the same basal plane.

**Type IV:** Combination of Shockley plus a Frank fault with Fault vector  $S + c/4$ : Type IV is also a combination of Shockley and a Frank fault but of the type  $S + c/4$ , where the  $c$ -axis screw dislocation has divided itself into  $c/4$  and  $3c/4$  step heights. Such faults can arise from the deflection of  $c$ -axis threading dislocations of Burgers vector  $c + a$  onto the basal plane. If the spiral step risers of such dislocations divide into  $c/4$  and  $3c/4$  increments, overgrowth can be facilitated by the simultaneous dragging of one of the Shockley partials associated with the core structure of the original dislocation by the overgrowing macrostep. This acts like an interfacial Shockley partial and adds the Shockley component to the  $c/4$  Frank component of fault vector. Figure 7.8g shows a SWBXT image taken in transmission geometry showing the area marked C is a fault with  $R = 1/12[4403]$  which is a combination of Shockley and  $c/4$  Frank fault and similarly area marked D in 7.8g corresponds to  $R = 1/12[\bar{4}043]$  which is due to a second  $\mathbf{c} + \mathbf{a}$  dislocation protruding the terrace. Such deflection process generally leads to exit of the threading dislocations through the crystal sidewalls and provide a mechanism by which the density of threading dislocations in the boules can be lowered.

### 7.2.6 Prismatic Slip during PVT growth 4H-SiC Boules

Prismatic dislocations are dislocations with Burgers vector  $1/3\langle 11\bar{2}0 \rangle$ , generated and gliding on the  $\{1010\}$  planes. They are mostly generated from the same sources that BPDs are generated from, such as crystal edge, MPs, etc. Figure 7.9a shows a prismatic slip band (marked with red arrow) nucleated from a MP. In addition, the gliding of TEDs on the prismatic planes can generate prismatic dislocation half loops as well. Examples of TEDs gliding on prismatic planes are shown in Figure 7.9b.

6" 4H-SiC commercial wafers often reveal an inhomogeneous distribution of prismatic slip with only two sets of prismatic slip systems activated in each of the 12 regions around the periphery of the wafer as shown in the enlarged X-ray



**Figure 7.9** SWBXT images recorded from 4H-SiC samples showing (a) a prismatic slip band emanating from a MP in a commercial wafer and (b) the gliding of TEDs on prismatic plane generating a lot of prismatic dislocation half loops (this image is recorded from an axially-cut sample).

topographs in Figure 7.10 [33]. Such non-uniformity clearly indicates that the resolved shear stresses caused by radial temperature gradients that induced the dislocation nucleation in different prismatic slip systems were also distributed non-uniformly. By thermal modeling of the temperature distribution in the boule during PVT growth, the radial temperature gradient and resultant thermal stresses was determined at any location in the crystal boule. The corresponding resolved shear stress on each prismatic plane was calculated and the distribution plotted. The regions where the resolved shear stress exceeds the critical resolved shear stress are determined, and predicted distribution of prismatic dislocations for the three different slip systems is shown in Figure 7.10. Clearly, the predicted distribution is in excellent agreement with the observed distribution on the SWBXT topographs. Clearly, thermal stresses induced by radial temperature difference play a key role in the activation of prismatic slip in 4H-SiC crystals grown by PVT.

### 7.2.7 Relationship Between Local Basal Plane Bending and Basal Plane Dislocations in PVT-grown 4H-SiC Substrate Wafers

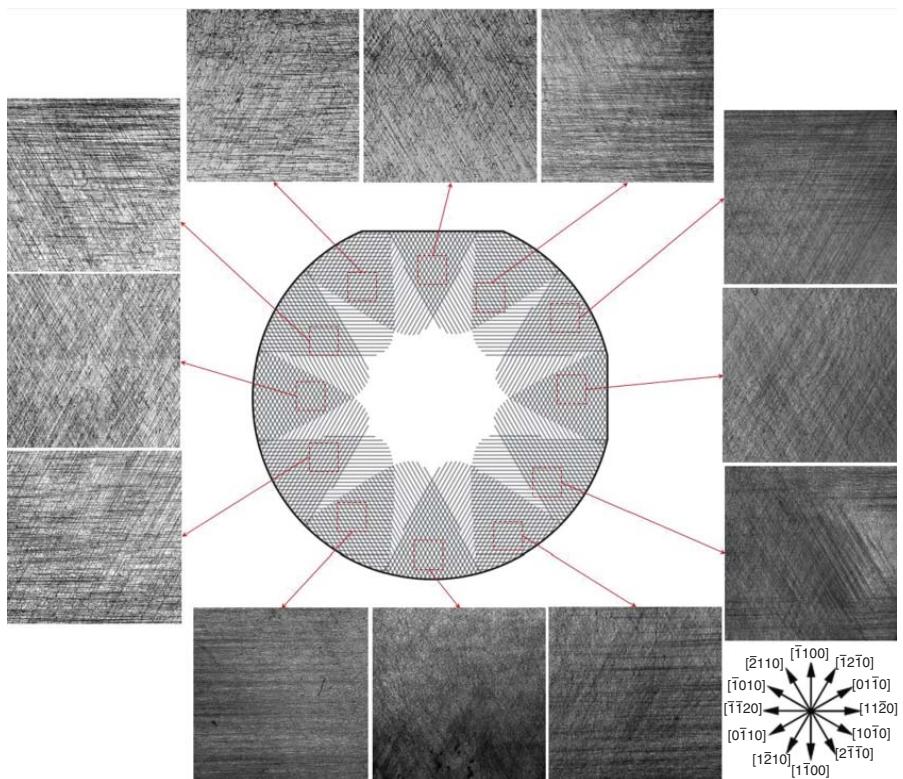
During PVT growth of 4H-SiC boule, internal stresses due to non-uniformity of temperature field results in basal plane bending that is accommodated by the inhomogeneous distribution of BPDs during cool down and persists in wafers sliced from the boule. Nature of basal plane bending measured by high-resolution X-ray diffraction (HRXRD) was compared with net BPD distribution across the whole diameter range of different wafers [34]. On synchrotron monochromatic beam X-ray topographs recorded in grazing incidence geometry, ray tracing principle denotes that black contrast BPD is created when diffracted X-ray beams converge from concave-shaped basal plane (extra half plane of edge dislocation facing way from surface), while white contrast BPD is created when diffracted X-ray beams diverge from a convex-shaped basal plane (extra half plane facing toward the surface). Thus, the net BPD distribution can be indicative of nature of basal plane bending, i.e. if black contrast BPDs are predominant, basal plane is bent in a concave manner, if white contrast BPDs are predominant, basal plane is bent in a convex manner. Figure 7.11b,d shows results of such BPD distribution measurement along the  $[1\bar{1}\bar{2}0]$  and  $[1\bar{1}00]$  for a 6" 4H-SiC wafer, respectively. Comparison of the net BPD variation with the peak shift on HRXRD measurements shows good agreement qualitatively (Figure 7.11a,c). To quantitatively estimate the basal-plane tilt angle, from the dislocation measurement, the following equation can be applied [35]:

$$\frac{\delta\phi}{\delta x} = nb \quad (7.1)$$

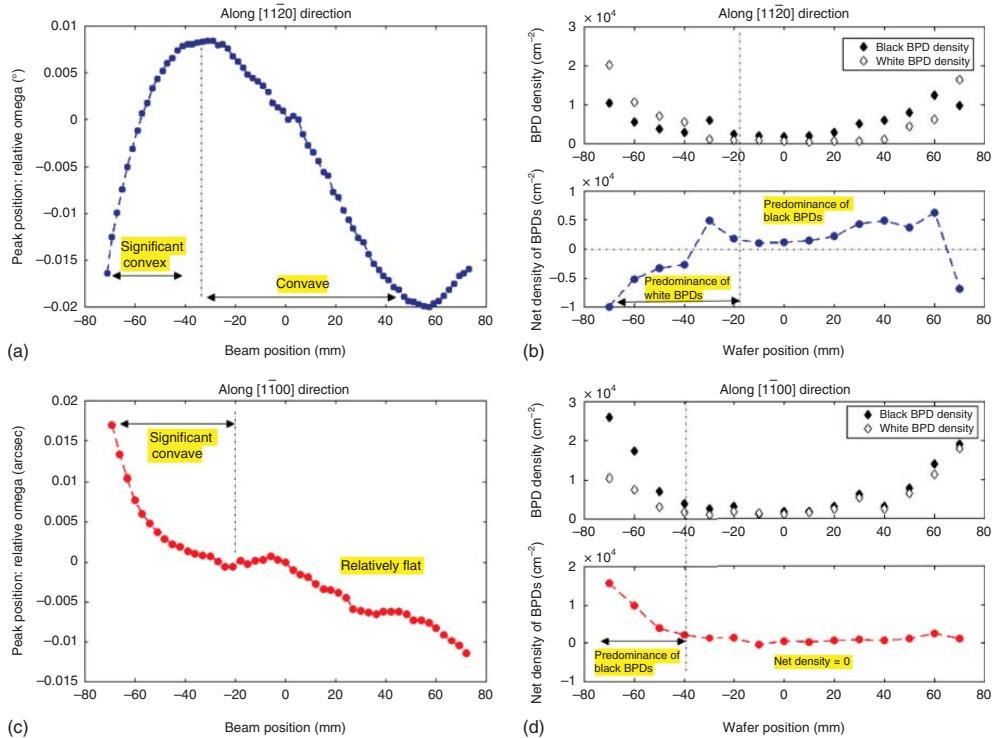
where  $n$  is the net BPD density on the plane perpendicular to the basal plane,  $b$  is the Burgers vector,  $\delta\theta$  is the total peak shift in an interval  $\delta x$ . Calculated values matches well with experimentally determined values from HRXRD [34].

### 7.2.8 Investigation of Dislocation Behavior at the Early Stage of PVT-grown 4H-SiC Crystals

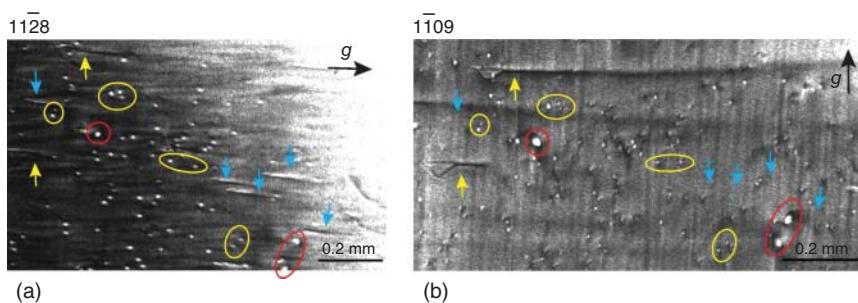
The behavior of defects during the early stages of PVT growth in large diameter (6-in.) 4H-SiC crystals was investigated, especially nucleation and multiplication that form the basis of the overall dislocation distribution during subsequent growth



**Figure 7.10** Correlation of wafer map (middle) showing the predicted distribution of prismatic dislocations for the three different slip systems with SWBXT images from the corresponding areas of the 150 mm 4H-SiC wafer showing excellent agreement. Source: Based on Guo et al. [33].



**Figure 7.11** (a, c) X-ray rocking curve peak position as a function of the beam position across the diameter of 6 in. 4H-SiC crystal (wafer#1). Scan direction is along  $[11\bar{2}0]$  (a) and  $[1\bar{1}00]$  (c), respectively. (b, d) Results from black/white contrast BPD density analysis along  $[11\bar{2}0]$  (b) and  $[1\bar{1}00]$  (d) directions. Source: Based on Guo et al. [33].



**Figure 7.12** Grazing incidence X-ray topographs recorded from the same area of early grown 4H-SiC wafer in different diffraction vectors (a)  $g = 11\bar{2}8$ , (b)  $g = 11\bar{0}9$ . Blue arrows indicate straight BPD segments showing contrast in (a) but out of contrast in (b) proving these are screw-oriented BPDs.

of the full boule [36]. Studies from initial grown seeded layers with thickness of several hundred microns by synchrotron X-ray topography reveals the deflection of TEDs and TMDs with same or opposite sign pairs nucleated from the seed with unique configurations as shown in Figures 7.12–7.14. Configurations observed include the deflection of TEDs into screw-type BPDs (Figures 7.12), deflection of pairs of TEDs with same or opposite sign of Burgers vector by macrosteps followed by glide of resultant BPDs (Figure 7.13) and the deflection of TMDs followed by separation of the  $\mathbf{a}$  component (Figure 7.14).

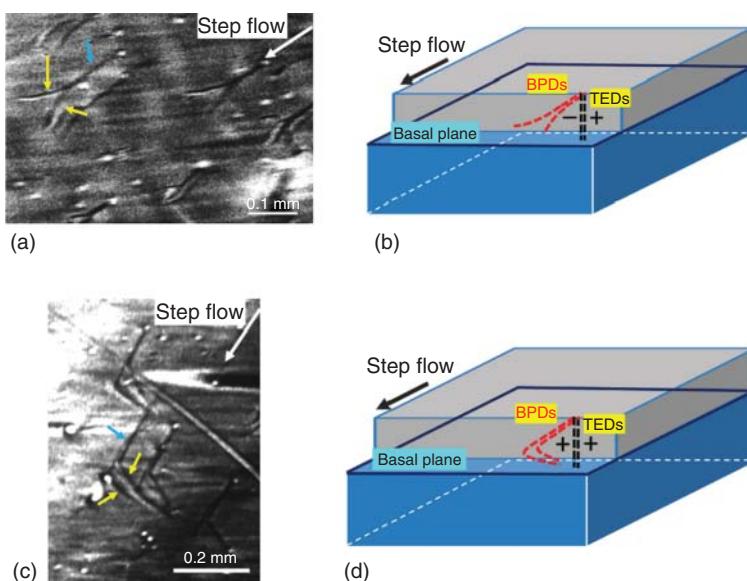
### 7.3 Dislocations in Homoepitaxial 4H-SiC

#### 7.3.1 Conversion of BPDs into TEDs

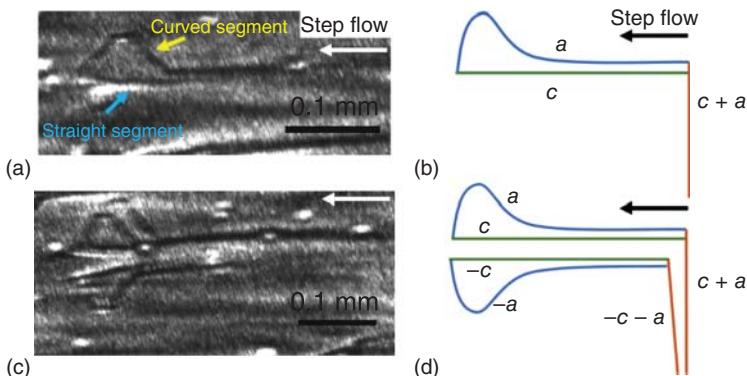
During homoepitaxial growth on 4H-SiC substrates, BPDs intersecting the surface are replicated into the epilayer and are susceptible to recombination enhanced dislocation glide (REDG) during device operation (see Section 7.3.2). However, by conversion of BPDs to TEDs, this can be prevented. One way to facilitate this is by engineering the substrate surface prior to CVD growth, i.e. defect preferential etching. Etch pits produced at BPD outcrops can facilitate lateral growth over step flow growth within the pits resulting in TED conversion [37]. See Figure 7.15 for schematic of this conversion and Figure 7.16 for examples of this observed in 4H-SiC crystals by monochromatic X-ray topography.

#### 7.3.2 Susceptibility of Basal Plane Dislocations to the Recombination-Enhanced Dislocation Glide in 4H Silicon Carbide

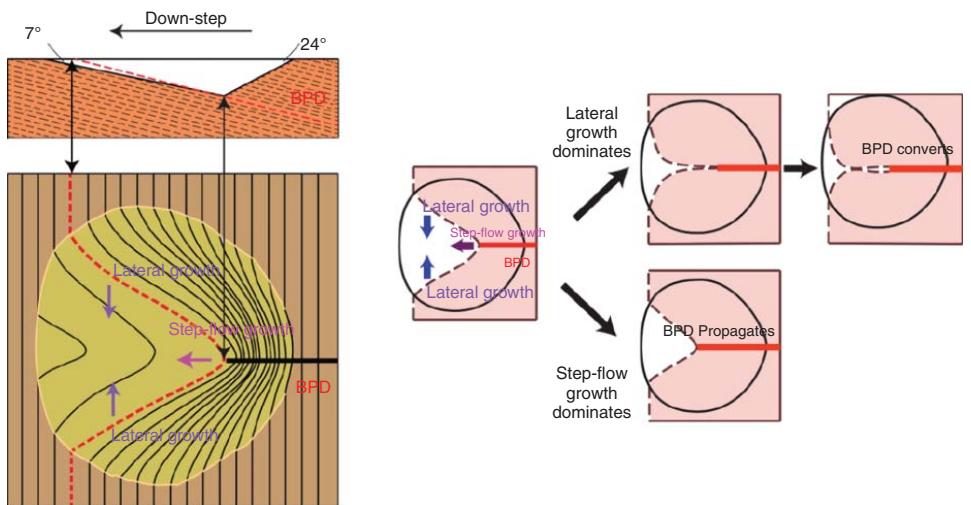
Dissociation of BPDs into mobile silicon-core (Si-core) partial dislocations and subsequent expansion of Shockley stacking faults (SFs) associated with advancement of these partial dislocations under forward bias causes forward voltage drop



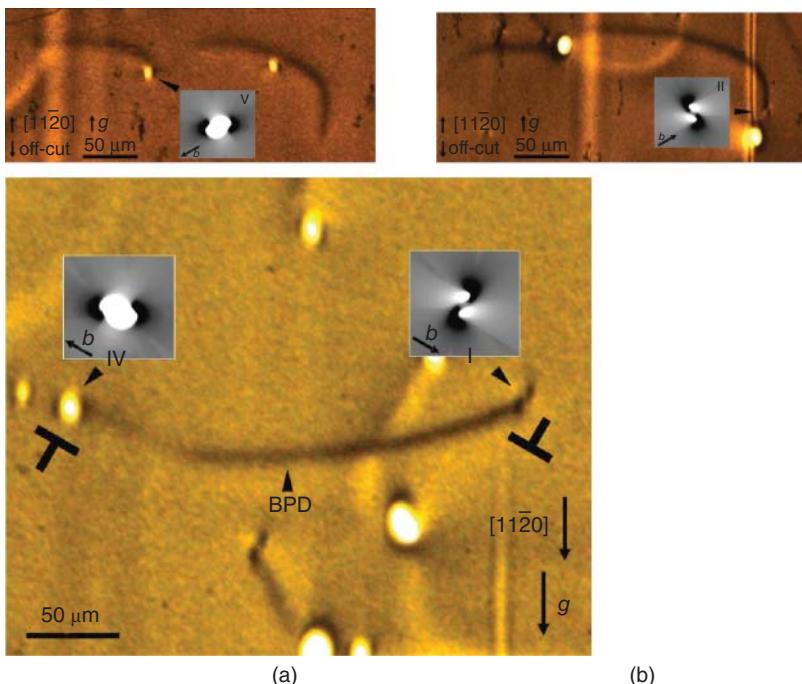
**Figure 7.13** Dislocations with unique shapes are observed in grazing incidence X-ray topograph ( $g = 11\bar{2}8$ ). (a, c) Stationary segments of the dislocation marked with blue arrows are along the step flow direction. Dislocation segments marked with yellow arrows refer to two gliding segments, which are separated parts of opposite sign deflected TEDs gliding toward opposite directions in (a), while two segments in (c) are associated with two deflected TED segments with same sign of Burgers vector. Formation mechanism is illustrated in (b) and (d), respectively. Source: Based on Guo et al. [33].



**Figure 7.14** (a, c) Grazing incidence X-ray topographs of one or a pair of deflected TMDs with Burgers vector of  $c + a$  in  $11\bar{2}8$  reflection. Straight segment corresponds to  $c$  component while gliding segment corresponds to  $a$  component. (a) Deflection of one single TMD. (c) Deflection of a pair of TMDs with opposite sign Burgers vectors. (b, d) Illustration showing the deflection process for single or opposite sign pair of TMDs. Source: Based on Guo et al. [33].



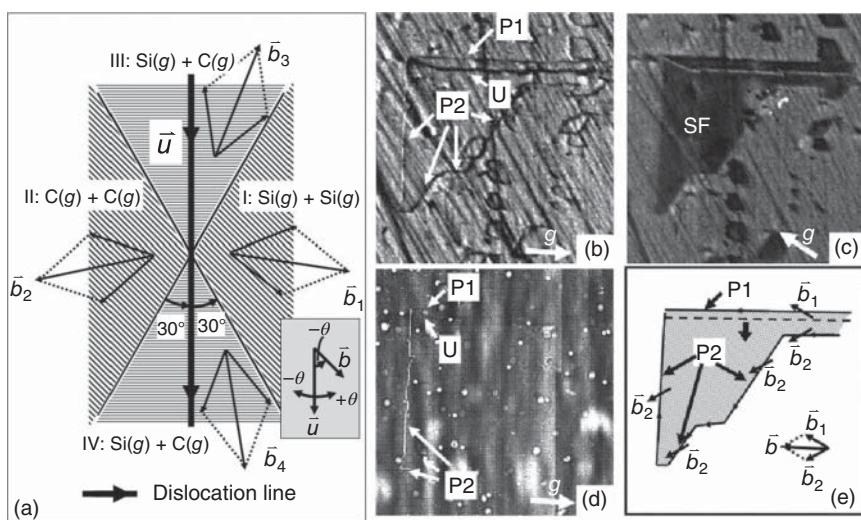
**Figure 7.15** (a) Cross section of the BPD etch pit along the line bisecting the sector-shaped plane. The parallel dotted lines illustrate the basal planes. Schematic of steps in and around the pit; (b) schematics of the basal plane in which the BPD lies; evolution of the basal plane during epitaxy if lateral growth dominates, and evolution of the basal plane during epitaxy if step-flow growth dominates. Source: Based on Zhang and Sudarshan [37].



**Figure 7.16** SMBXT images showing the conversion of BPDs to TEDs. Burgers vectors of TEDs are determined by comparison to simulated contrast from ray tracing simulations.

and reduced lifetime of silicon carbide (SiC) based bipolar devices [14]. Such expansion of basal SFs is activated by the electron-hole REDG process [38–40]. Through detailed X-ray topography analysis of a dislocation configuration formed after stacking fault expansion under forward bias, the susceptibility of BPDs to REDG is shown to be determined by the counterclockwise angle  $\theta$  from the line direction to its Burgers vector (*Figure 7.11a*). Figures 7.11b–f shows the X-ray topographs and schematic configuration (*g*) after the advancement of the mobile partial. During the advancement of the partial, it interacted with a few TSDs, and the final configuration obtained is shown in *Figure 7.11g*. The Burgers vector *b* of the original BPD is determined to be  $1/3(\bar{1}\bar{1}20)$ . Thus, the original BPD is screw oriented ( $\theta = 0^\circ$ ), and it is dissociated into a C-core and a Si-core partials. The BPDs with  $30^\circ < \theta < 150^\circ$  are most BPDs detrimental, as both partials will advance under forward bias. If  $-30^\circ < \theta < 30^\circ$  or  $150^\circ < \theta < 210^\circ$ , only one partial advances. Both partials are immobile if  $210^\circ < \theta < 330^\circ$  [41] (*Figure 7.17*).

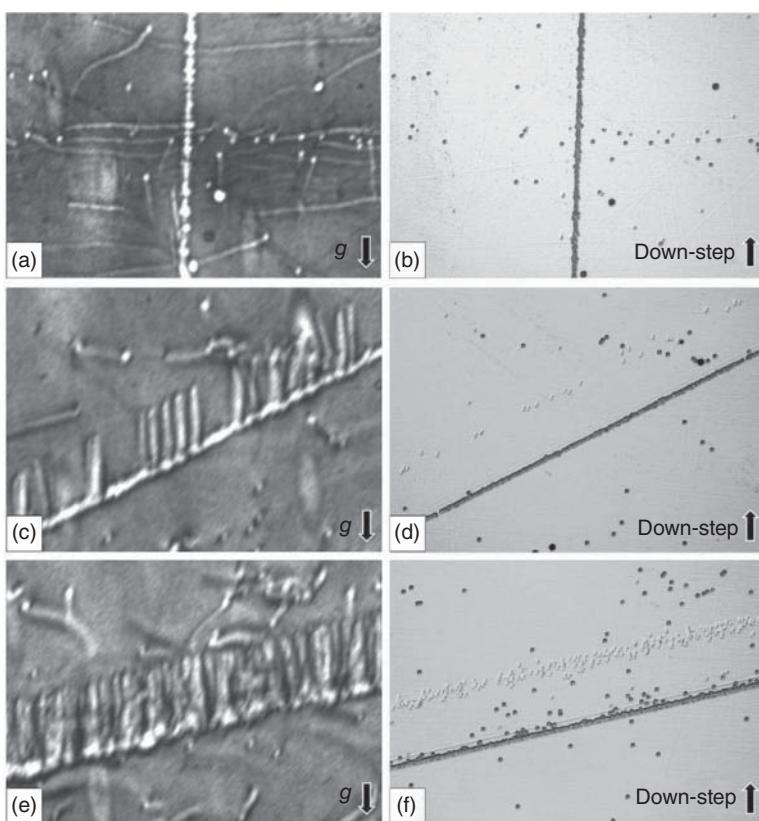
In summary, the susceptibility of the BPDs to REDG process is determined by the counterclockwise angle  $\theta$  from the line direction to its Burgers vector. The BPDs with  $30^\circ < \theta < 150^\circ$  are most detrimental, as both partials will advance under forward bias. If  $-30^\circ < \theta < 30^\circ$  or  $150^\circ < \theta < 210^\circ$ , only one partial advances. Both partials are immobile if  $210^\circ < \theta < 330^\circ$ .



**Figure 7.17** Schematics showing Shockley partial dislocations of different core structures dissociated from a perfect BPD. Four regions are defined, according to the direction of Burgers vector with respect to the line direction of the dislocation, assuming Si-face is facing up; Region I:  $30^\circ < \theta < 150^\circ$ , the BPD is dissociated into two Si-core partials; Region II:  $210^\circ < \theta < 330^\circ$ , the BPD is dissociated into two C-core partials; Region III:  $150^\circ < \theta < 210^\circ$ , one Si-core and one C-core. Region IV:  $-30^\circ < \theta < 30^\circ$ , one Si-core and one C-core;  $\theta$  is defined in the inset of (a). REDG activated SF after forward bias from a screw-oriented BPD. (a)  $(11\bar{2}0)$  transmission topograph showing the partials (P1 and P2) bounding the SF. The SF area is out of contrast since  $\mathbf{g} \cdot \mathbf{R}$  is equal to an integer. Source: Zhang et al. [43]; (b)  $(\bar{1}010)$  transmission topograph showing the SF; (c) P2 is out of contrast in  $(21\bar{1}0)$  transmission topograph, indicating its Burgers vector of  $1/3(01\bar{1}0)$ ; (d) P1 is out of contrast in  $(\bar{1}210)$  transmission topograph, indicating its Burgers vector of  $1/3(\bar{1}010)$ ; (e)  $(0008)$  back-reflection topograph. The sign of P1 and P2 can be determined; (f) schematics showing the SF configuration. The SF is obtained via expansion of Si-core partial toward the bottom edge of the view (see the dashed line) and interaction with TSDs. The Burgers vector of each partial segment is labeled; the Burgers vector  $\mathbf{b}$  of the original BPD can be obtained and it is screw-oriented. Source: Modified from Chen et al. [41].

### 7.3.3 Nucleation of TEDs, BPDs, and TSDs at Substrate Surface Damage

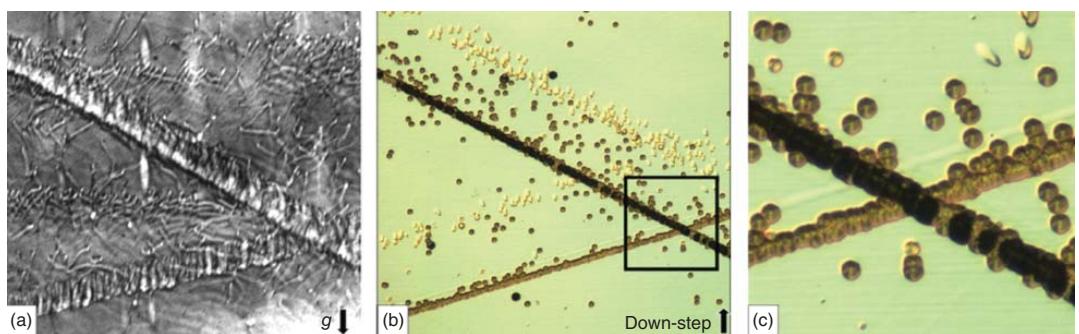
Subsurface damage associated with surface scratches on the substrate, residual from polishing act as dislocation nucleation sites during epitaxial growth. X-ray topography and chemical etching studies suggest that the scratches on the substrate surface act as dislocation nucleation centers during the growth. TED-TED pairs, TED-BPD pairs, TSD-TSD pairs, and Carrot defects are generated at scratches [42]. It is observed that the orientation of the scratch with respect to the off-cut direction exerts influence over the nucleation process. When scratches are parallel to the off-cut direction (Figure 7.18a,b), they manifested themselves as a single, dense row of TEDs. For scratches inclined to the off-cut direction (see Figure 7.18c-f), in addition to a single, dense row of TEDs, linear features verified as BPDs are



**Figure 7.18** Synchrotron X-ray topographs ((a), (c), and (e)) and corresponding etch pit patterns ((b), (d) and (f)) recorded from epilayers grown on a scratched substrate surface. Panels (a) and (b) show a scratch parallel to the off-cut direction while panels (c)–(f) show scratches inclined to the off-cut direction.

observed. The density of the BPDs associated with the scratch increases with the angle between the scratch direction and off-cut direction.

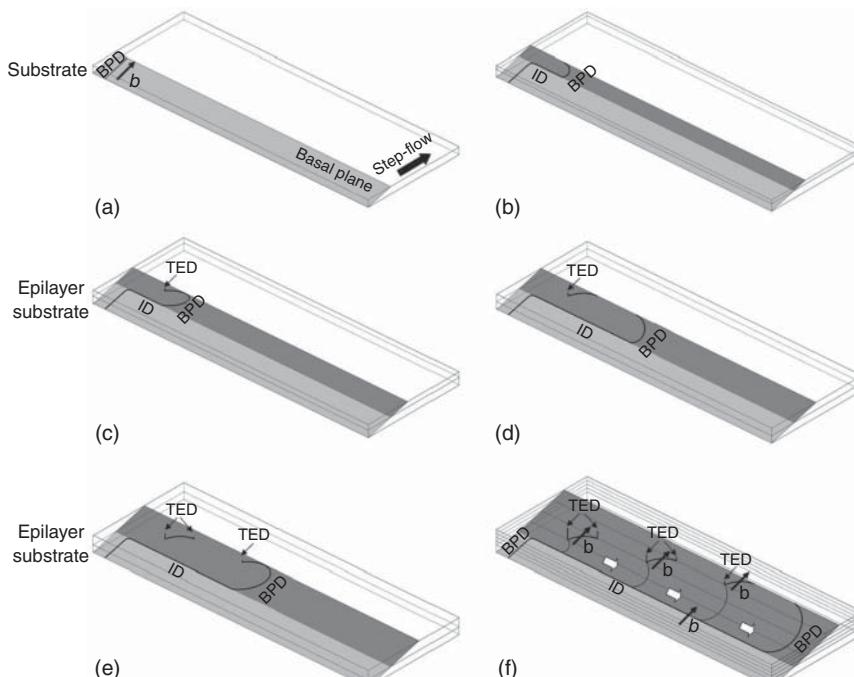
TSDs can also be nucleated along substrate surface scratches as seen in the case of two scratches shown in Figure 7.19a,b. On the topographs, both scratches have linear features attached to them which project along the off-cut direction. X-ray topography reveals the lower one as a single white band similar to the cases discussed above. Compared with the etch pit pattern, it is clear that only TEDs and BPDs nucleated along it. But the upper one manifested itself on the topographs as a single but wider white band of contrast. The corresponding etch pit pattern confirmed that some other dislocations whose pits are bigger and deeper than TED etch pits were also nucleated along the scratch. Figure 7.19c shows an enlarged area, and it is observed that these dislocations appear as large hexagonal pits which correspond to elementary TSDs.



**Figure 7.19** (a) SMBXT image recorded from an epilayer grown showing defects nucleated at two residual scratches on the substrate surface; (b) corresponding etch pit pattern; (c) enlargement of the framed region in (b).

### 7.3.4 Nucleation Mechanism of Dislocation Half-Loop Arrays in 4H-SiC Homo-Epitaxial Layers

BPDs in the 4H-SiC homepitaxial layers largely result from the replication, during growth, of BPDs which intersect the surface of the off-cut SiC substrates. BPDs which intersect the surface in screw orientation are observed to nucleate half loop arrays. By recording the behavior of a half-loop array (HLA) from a Si-face epilayer using ultra violet photoluminescence (UVPL) imaging, a model has been developed to explain the formation of HLAs [43]. Figure 7.20a shows a screw-type BPD with Burgers vector  $1/3[1\bar{1}\bar{2}0]$  intersecting the surface of the substrate which is expected to be replicated during epitaxy in contrast to those with significant edge components which are likely to be converted into TEDs. As soon as the epilayer exceeds critical thickness, as per the predictions of Matthews and Blakeslee [44], the threading segment of the screw-oriented BPD will be forced to glide sideways leaving a trailing interfacial segment in its wake at or near the substrate/epilayer interface. During this glide process, the mobile threading segment adopts more edge character near the growth surface (see Figure 7.20b) rendering it susceptible to conversion to a TED during continued growth. The sessile TED segment pins the surface intersection of the mobile BPD segment. During further growth, the TED segment is replicated while the mobile



**Figure 7.20** Schematic diagram showing the formation mechanism of a HLA. (a)–(e) sequential stages in the process; (f) summary of process. The lighter shaded planes in (a)–(f) indicate the basal plane on which the BPD lies in the substrate, while the darker one lies in the epilayer. See text for details of mechanism. Source: Zhang et al. [43].

basal segment of dislocation pivots about the pinning point as shown in Figure 7.20c. At this juncture, part of the mobile BPD segment can escape through the epilayer surface (creating a surface step of magnitude equal to the Burgers vector), as shown in Figure 7.20d leaving two further BPD surface intersections which, since they are not in screw orientation, are susceptible to conversion to TEDs. Upon conversion, one of these TEDs is connected via a short BPD segment to the TED segment created in Figure 7.20b, thus creating a half loop comprising two TEDs and a connecting BPD. The other TED again acts as a pinning point for the still mobile segment of threading BPD, as shown in Figure 7.20e, as the process repeats during continued growth as the TED segments further replicate and the threading BPD segment continues to glide. The net result of this process is an array of half loops with short, large edge component BPD segments, all deposited on the exact same basal plane. The direction of the array is nearly perpendicular to the off-cut direction as summarized in Figure 7.20f. The value of this angle depends on the competition between the growth rate and the rate of sideways glide of the threading BPD segment.

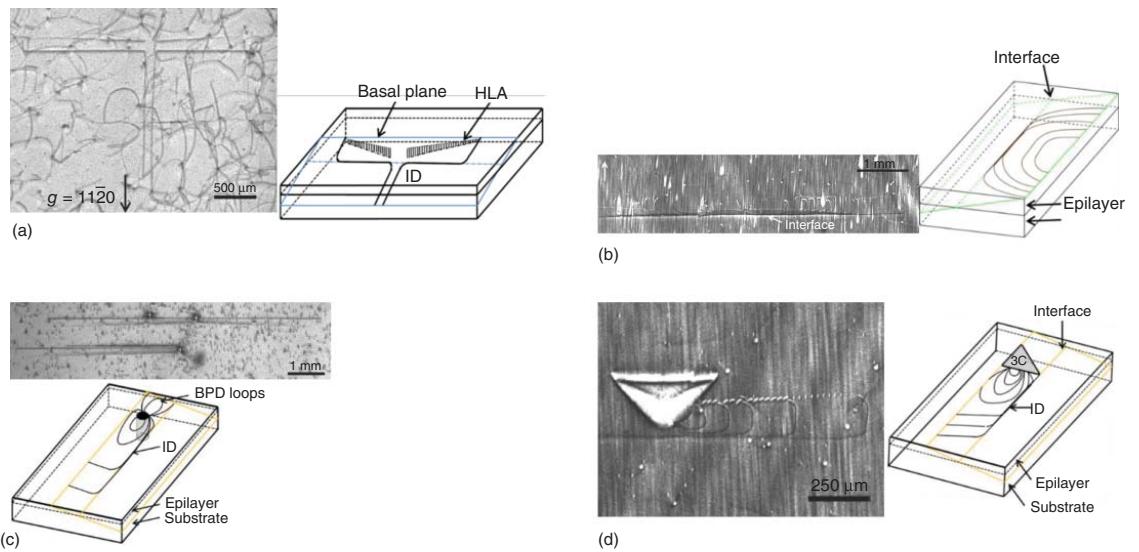
In addition to the above mechanism, HLAs are also observed to be generated from epilayer surface-nucleated half-loops of BPD, BPD half-loops generated from 3C inclusions in the epilayer, and from BPD half loops emanating from substrate/epilayer interface scratches as shown in Figure 7.21 [45].

### 7.3.5 V- and Y-shaped Frank-type Stacking Faults

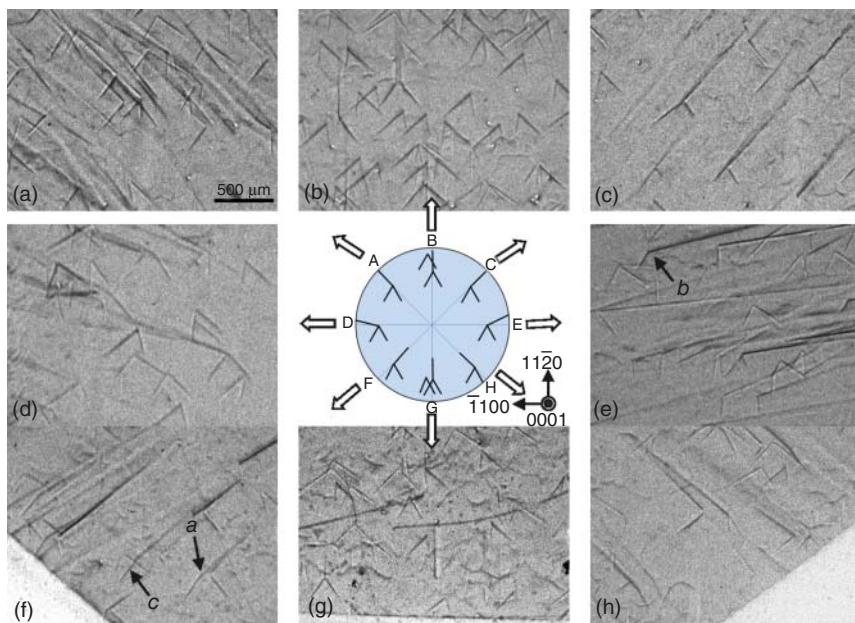
Grazing incidence synchrotron white beam X-ray topographs showing V- and Y-shaped features (Figure 7.22) are revealed to be  $\frac{1}{4}[0001]$  Frank-type stacking faults [46]. Geometric analysis of the size and shape of these faults indicates that they are fully contained within the epilayer and nucleated at the substrate/epilayer interface. Detailed analysis shows that the positions of the V shape stacking faults match with the positions of c-axis threading dislocations with Burgers vectors of  $c$  or  $c + a$  in the substrate and thus appear to result from the deflection of these dislocations during epilayer growth. Similarly, the Y-shaped defects match well with the substrate surface intersections of c-axis threading dislocations with Burgers vectors of  $c$  or  $c + a$  in the substrate which were deflected onto the basal plane during substrate growth. For the V-shaped defects, this is based on the overgrowth of the surface spiral steps associated with the surface intersections of the threading dislocations (Figure 7.23a–c). For the Y-shaped defects, this is based on overgrowth of the special configurations of steps at the surface intersections of the threading dislocations that were deflected onto the basal plane during substrate growth (Figure 7.23d–f).

## 7.4 Summary

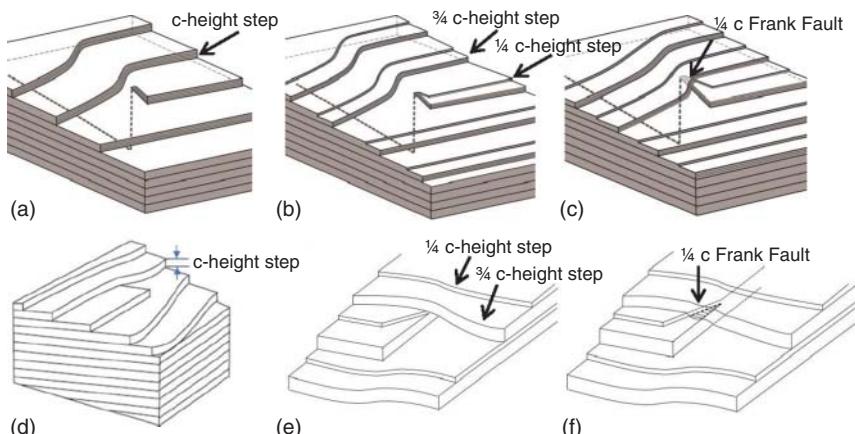
By applying synchrotron X-ray topography techniques in conjunction with complementary characterization techniques, information on different dislocation types in bulk and thin film SiC materials has been obtained. Analysis of the behavior of these dislocations and their interactions during crystal growth has provided valuable information to either eliminate defects or engineer their structures to minimize their impact.



**Figure 7.21** X-ray topographs and corresponding schematics of formation of interfacial dislocations and associated HLAs during (a) epilayer growth, (b) on epilayer surface, (c) micropipes and (d) 3C polytype inclusions. Source: Wang et al. [45].



**Figure 7.22** Grazing incidence X-ray topographs of V and Y shape defects around the periphery of the 4H-SiC wafer. Schematic in the middle shows how the V and Y shape defects distribute around the periphery of the wafer. Source: Wang et al. [46].



**Figure 7.23** (a, c) The formation mechanism of V shape stacking fault during epitaxial growth; (d-f) the formation mechanism of Y shape stacking fault during epitaxial growth. Source: Wang et al. [46].

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# 8

## Novel Theoretical Approaches for Understanding and Predicting Dislocation Evolution and Propagation

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### 8.1 Introduction

Dislocations in semiconductors have been studied extensively for Si and GaAs, both of which have a face-centered cubic crystal structure. Such crystal boules are grown from the melt using the Czochralski and floating zone method in the case of Si and liquid-encapsulated Czochralski and vertical gradient freeze method in the case of GaAs. The application of the so-called Dash necking technique [1] allows the reduction of the dislocation density in Si during the initial seeding growth stage down to a zero dislocation density value and then to retain this state throughout the complete growth process. Si ingots of up to 450 mm in diameter and wafers cut from those with a dislocation density of  $0 \text{ cm}^{-2}$  nowadays can be considered state of the art. GaAs as compared to Si has different thermoelastic properties and exhibits a greater brittleness, which is why the growth of “zero dislocation” GaAs succeeded only up to a crystal diameter of roughly 70 mm [2]. GaAs crystal boules with a diameter  $>100 \text{ mm}$  exhibit dislocation densities of approximately  $100\text{--}3000 \text{ cm}^{-2}$ . There, dislocations often cluster or form dislocation networks, sometimes termed *dislocation patterns*, that consist in an inhomogeneous dislocation distribution with regions of very low density bounded by strongly localized regions of very high densities. Due to the performance killing impact of dislocations on electronic devices, their propagation, multiplication, and annihilation have been studied in many aspects. Usually, the study of dislocation behavior during bulk growth is related to thermoelastic strain in the growing crystal. For a recent overview, please refer to the “Handbook of crystal growth – bulk growth” edited by P. Rudolph [3] and to the recent work [4, 5] which particularly considers the formation of cellular dislocation networks also in SiC. Besides high dislocation densities and small-angle grain boundaries, also micro-pipes and super-screw dislocations with Burgers vectors larger than the c-lattice parameter are an important issue in SiC growth [6]. Last but not least stacking faults together with the occurring partial dislocations of different

core structures form extended defects, especially in non-cubic semiconductors such as nitrides and SiC [6]. This makes SiC a particularly interesting model system for defects in non-cubic semiconductor crystals.

In the following, we first introduce the state of the art in terms of modeling and simulation approaches. After that we concentrate on continuum modeling approaches for dislocation emphasis on two specific model classes, the Alexander-Haasen model and continuum dislocation dynamics (CDDs) models. This is followed by numerical examples that demonstrate different features of evolving dislocation structures: the first example shows that the ability to represent the flow of dislocations is important; the second example deals with dislocation motion between dislocation veins which act as strong obstacles for the motion of dislocations. We then summarize our work and put it into the perspective of ongoing research.

## 8.2 General Modeling and Simulation Approaches

There are many modeling and simulation approaches for defect-related phenomena on (sub) nanometer length scales. e.g. in the context of defects in semiconductors, Łażewski et al. [7] used density function theory for investigating the electrostatic barrier near the core of a pair of edge dislocations, and a number of authors, among them Rao et al. [8], Oren et al. [9], Zhou et al. [10], Chen et al. [11] applied molecular dynamics simulation for simulating dislocation in various materials such as, e.g. B3-GaN. However, such simulations are – for reasons of computational cost – not appropriate for simulating the structure–property relation of specimens on a macroscopic length scale. Discrete dislocation dynamics (DDD) simulations [12–17] have been used only in rare cases with simulation codes from the metal plasticity community [18] and also suffer from a large computational cost. Nonetheless, they are able to simulate larger volumes/numbers of interacting dislocations than atomistic simulations. In the field of metal plasticity, phase field methods for dislocation dynamics gained some popularity [19, 20]. They do not resolve individual atoms but are still able to represent the dislocation core energy in some physical detail – unlike the DDD methods most of which are based on linear elasticity approaches. So far, there have been no applications to the domain of semiconductors.

Most of the (commercially) available software for macroscopic modeling on the device scale of semiconductors usually is only able to compute thermal stress during the growth process and, based on this, to roughly estimates the dislocation density based on a resolved shear stress; neither strain hardening nor details of the nucleation process or the flow of dislocations can be considered. Among the most commonly used phenomenological model is the Alexander-Haasen (AH) model [21], which is utilized in a range of different formulations to semi-quantitatively describe dislocation structures. Yonenaga and Sumino [22, 23] developed an elastic-viscoplastic type of constitutive equation for predicting the quantity of dislocation density. Ide et al. [24] analyzed the influence of oxygen diffusion on dislocation density during crystal growth and during the cooling processes. State-of-the art

simulation methods furthermore embed the AH model into a crystal plasticity finite element model [25–27] and thereby also consider the influence of the crystallographic orientations and slip systems on the resolved shear stress.

A novel type of continuum models is motivated by work that, so far, has been undertaken only within the small-scale metal plasticity field. The so-called Continuum Dislocation Dynamics (CDD) theory [28–32] is a strongly enhanced continuum crystal plasticity formulations in terms of additional microstructural information (i.e. detailed geometrical information of dislocation) and their nonlocal evolution equations (describing dislocation flow). The result is a continuum theory that is almost as detailed as a DDDs model but that does not suffer from the same computational restriction [33]: the computational time in DDD simulations scales almost quadratically with the number of interacting line segments, while for the CDD theory the number of dislocations has no influence, which allows for computational models that can eventually reach length and time scales comparable to experimental ones. As opposed to other continuum approaches, CDD can naturally differentiate and convert between straight and curved dislocations, as well as between “geometrically necessary dislocations (GNDs) and “statistically stored dislocations (SSDs) [29, 31].

## 8.3 Continuum Dislocation Modeling Approaches

Continuum models for predicting the evolution of dislocations have been used for more than half a century. The popularity is a result of the fact that continuous representations do not resolve each individual dislocation but rather operate with continuous density fields. The benefit is that the computational cost can be strongly reduced due to the fact that a density, i.e. the *dislocation line length per volume* is just a single number regardless how many dislocations are present. Thus, the computational cost does not scale with the number of interacting dislocations or atoms. The drawback is that a density value is not able to represent all details of the potentially complex dislocation microstructure [34–36]. In the following, we will introduce the theoretical background of two different models, the Alexander–Haasen model and the CDDs theory.

### 8.3.1 Alexander–Haasen Model

The Alexander–Haasen (AH) model [21] is based on the standard assumption of additive decomposition of the total strain rate  $\dot{\epsilon}$  into an elastic part  $\dot{\epsilon}^{\text{el}}$ , a thermal part  $\dot{\epsilon}^{\text{th}}$ , and a plastic contribution  $\dot{\epsilon}^{\text{pl}}$  as,  $\dot{\epsilon} = \dot{\epsilon}^{\text{el}} + \dot{\epsilon}^{\text{th}} + \dot{\epsilon}^{\text{pl}}$ . Thermal loading causes thermal eigenstrains  $\dot{\epsilon}^{\text{th}}$ , while the mechanical loading gives rise to elastic strains  $\dot{\epsilon}^{\text{el}}$ , and additionally, the presence of dislocations causes eigenstrains  $\dot{\epsilon}^{\text{pl}}$ . Explicitly solving the (anisotropic) elastic boundary value problem yields stresses  $\sigma$ . Projecting those by application of the symmetric projection tensor  $\mathbf{M}_s = \mathbf{n} \otimes \mathbf{s}$ , with the slip plane normal vector  $\mathbf{n}$  and the slip direction  $\mathbf{s}$  gives resolved shear stresses  $\tau_{\text{res}}$  in the local coordinate system of the respective slip systems  $s$ . The plastic

shear strain contribution to  $\dot{\varepsilon}^{\text{pl}}$  in the slip coordinate system is obtained from the Orowan equation,  $\dot{\varepsilon}^{\text{pl}} = \rho_m b v$ , with the modulus of the Burgers vector  $b$ , the density of mobile dislocations  $\rho_m$ , and the velocity of mobile dislocations  $v$ . The latter is phenomenologically given as a function of temperature and local effective stress

$$v = v_0 \left( \frac{\tau_{\text{eff}}}{\tau_0} \right)^m \exp \left( -\frac{Q}{k_B T} \right) \text{sign}(\tau_{\text{res}}) \quad (8.1)$$

where  $k_B$  is the Boltzmann constant,  $Q$  is the activation enthalpy,  $T$  is the temperature, and  $m$  is a fitting parameter. Furthermore, the effective shear stress is

$$\tau_{\text{eff}} = \langle |\tau_{\text{res}}| - \tau_y \rangle \quad \text{with} \quad \langle \cdot \rangle = \begin{cases} \langle \cdot \rangle \text{ for } \langle \cdot \rangle > 0 \\ 0 \text{ for } \langle \cdot \rangle \leq 0 \end{cases}. \quad (8.2)$$

Therein, the yield stress  $\tau_y$  governs dislocation interactions and is given by the so-called Taylor relation [37],  $\tau_y = a G b \sqrt{\rho_m}$ , with a constant  $a$  typically in the range of 0.2–0.5 and the shear modulus  $G$ . The yield stress acts like a friction stress which has to be overcome for plastic activity to take place. The set of equations is completed by a constitutive rate expression for the dislocation density of the form

$$\dot{\rho}_m = K \left( \frac{\tau_{\text{eff}}}{\tau_0} \right)^\lambda \rho_m |v|, \quad (8.3)$$

with parameters  $\lambda$  and  $\tau_0$ . Model extensions may separately consider evolution equations for mobile and immobile dislocations but are not able to convert the former into the latter quantity, or vice versa (cf. [38] for a discussion of the shortcomings of these models).

This macroscopic constitutive model might be used for obtaining a rough estimate of the order of magnitude of dislocation density in situations where homogeneous plasticity can be assumed. However, it is generally not possible to decide a priori whether homogeneous plasticity can be assumed or not. The AH model fails to predict fluxes of dislocations since it is a local model, given as an ordinary differential equation. It therefore also cannot represent, e.g. loss of dislocations through surfaces, as has been investigated in more details in [39]. Another consequence is that it fails to predict the peculiarities of occurring heterogeneous dislocation microstructures as, e.g. during dislocation cell structure formation. Thus, the AH model has only a limited range of applicability.

### 8.3.2 Continuum Dislocation Dynamics Models

Any version of a CDDs model is a nonlocal model which was obtained by coarse graining the geometrical properties and the motion of discrete dislocations (the so-called *kinematics* of dislocations). As such, it is based on a set of continuous variables and describes at least the *flux* of dislocation density by a set of transport equations. These models have been developed for and so far mainly used in the domain of metal plasticity [29, 31, 40–43].

### 8.3.2.1 The Simplest Model: Straight Parallel Dislocation with the Same Line Direction

In the particular case of straight dislocations of the same line direction, running along the  $y$  direction of a Cartesian coordinate system and that move in a slip system with  $\mathbf{n} = \mathbf{e}_z$ , the continuum dislocation kinematics is described by a scalar evolution equation of dislocation density  $\rho$

$$\partial_t \rho = -\partial_x (\rho v), \quad (8.4)$$

where  $\partial_i(\cdot) \equiv \partial(\cdot)/\partial i$ . For a constant dislocation velocity  $v$ , this would be a pure convection equation. It is accompanied by the Orowan equation

$$\partial_t \gamma = \rho v b \quad (8.5)$$

where  $b$  is the magnitude of the Burgers vector and  $\gamma$  is the plastic shear strain in the respective slip system.  $\gamma$ , as an eigenstrain, serves as the connection to the elasticity theory, similar as in the AH model. The resulting stresses reflect in the velocity function  $v$  as detailed below.

### 8.3.2.2 The “Groma” Model: Straight Parallel Dislocations with Two Line Directions

Among those who established a more general continuum model in the dislocation community were [44] as well as I. Groma et al. [28, 45] who additionally investigated how the interaction of dislocations can be described in terms of continuum variables. The evolution equation Eq. (8.4) is then replaced by a set of evolution equations for the total and signed GND densities as,

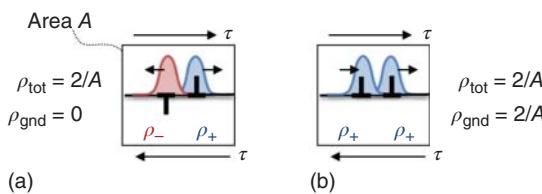
$$\begin{aligned} \partial_t \rho_{\text{tot}} &= -\partial_x (\rho_{\text{gnd}} v) \\ \partial_t \rho_{\text{gnd}} &= -\partial_x (\rho_{\text{tot}} v). \end{aligned} \quad (8.6)$$

Dislocation densities still describe only straight (edge) dislocation, but this model allows for two different line orientations. The positive and negative dislocation densities,  $\rho_+$  and  $\rho_-$ , are then defined as the number of dislocations with positive or negative line direction per averaging area. Thus, the total and GND density can be alternatively expressed as

$$\rho_{\text{tot}} = \rho_+ + \rho_- \quad (8.7)$$

$$\rho_{\text{gnd}} = \rho_+ - \rho_- . \quad (8.8)$$

Figure 8.1 shows a sketch of two different dislocation configurations highlighting the need for *two* different density variables. In the Groma model, it is possible to represent a so-called SSD content inside an averaging volume, e.g. the volume contains both an edge dislocation with positive line orientation and an edge dislocation with negative line orientation. As a consequence, positive and negative densities can move past each other without being annihilated, i.e. as if on different slip planes inside the averaging volume.



**Figure 8.1** (a) An averaging area containing two edge dislocations with opposite line directions. (b) Same averaging area containing two edge dislocations with the same line direction. Both systems have the same total density but differ in the net GND content.  $\tau$  is the applied shear stress under which action a positive edge dislocation moves in positive  $x$  direction (here: to the right), a negative edge moves toward the left, as indicated by the small arrows.

### 8.3.2.3 The Kröner–Nye Model for Geometrically Necessary Dislocations

A different approach is based on the Kröner–Nye tensor [46] which is defined as

$$\alpha = \text{curl } \beta_{\text{pl}}, \quad (8.9)$$

where  $\beta_{\text{pl}}$  is the plastic distortion. This representation is only valid if all dislocations in an averaging volume share the same line direction  $\mathbf{l}$ , which is why there is an alternative formulation based on the GND density,

$$\alpha = \rho_{\text{gnd}} \mathbf{l} \otimes \mathbf{b}. \quad (8.10)$$

If the coordinate system is aligned with the Burgers vector direction and the edge orientation, the individual coefficients of the Kröner–Nye tensor contain the edge and screw GND contributions. One of the main differences to the above introduced two models is that here dislocations can also be curved. A serious drawback of this quantity is that once the assumption of GND content is violated, e.g. an averaging volume contains dislocations of opposite line orientation, the dislocation content would be “annihilated.” This is nonphysical in particular in situations where averaging volumes are larger than the annihilation distance which for metals has a typical order of magnitude of a few Burgers vectors. Combining the advantage of the Groma model to handle SSD densities with opposite line orientations with the ability of the Kröner–Nye model to handle arbitrarily curved lines leads to extended CDDs models that can also work in truly three-dimensional situations.

### 8.3.2.4 Three-dimensional Continuum Dislocation Dynamics (CDD)

Representing dislocation microstructures as only straight edge dislocations in 2D or as GND structures has many limitations and is therefore not suitable to be used as basis for 3D models:

- (i) Curved dislocations may bow out and thereby increase the line length contained in the system, while straight dislocations can only translate [40]. However, the resulting densities and the plastic slip are very different.
- (ii) While only GNDs give rise to internal stresses [32, 45], *all* dislocations need to be considered because due to the motion of dislocations they can change their “character,” e.g. a GND configuration may become a dipole configuration with a zero net GND content.

- (iii) Real dislocation microstructures are intrinsically three dimensional and may include many complex phenomena such as junctions or locks that can only be represented in truly three-dimensional models. A detailed comparison of CDD models of varying complexity can be found in [38].

To alleviate the above shortcomings, a more advanced CDDs model was introduced by Hochrainer et al. [29], which also can be generalized to three-dimensional systems. Similar to the above models, the dislocation velocity drives the evolution of the dislocation microstructure in each slip system, which in the case of Hochrainer's CDD is represented by four field variables: the total density  $\rho_t$  (which upon volume integration gives the total line length inside the volume), a vector of “geometrically necessary dislocation density  $\varrho = [\varrho_s, \varrho_e]$ , e.g. of screw ( $\varrho_s$ ) and edge ( $\varrho_e$ ) dislocations, a curvature density  $q_t$  (which upon volume integration gives the number of closed dislocation loops as multiple of  $2\pi$ ) and the plastic strain  $\gamma$ . The temporal change is governed by evolution equations in the form of partial differential equations (PDEs) which have the character of transport equations

$$\begin{aligned}\partial_t \rho_t &= -\nabla \cdot (\nu \varrho^\perp) + \nu q_t \\ \partial_t \varrho &= -\nabla \cdot (\nu \rho_t) \\ \partial_t q_t &= -\nabla \cdot (-\nu Q^{(1)} + \mathbf{A}^{(2)} \cdot \nabla \nu)\end{aligned}\quad (8.11)$$

and which are, for each slip system, completed by the Orowan equation for the rate of plastic strain  $\dot{\gamma} = \rho_t b \nu$ . Therein, a dot denotes the scalar product,  $\varrho^\perp = [\varrho_e, -\varrho_s]$  is the  $90^\circ$  rotated GND density vector. As stated in [36], we assume that,

$$Q^{(1)} = -\varrho^\perp q_t / \rho_t \quad (8.12)$$

$$\mathbf{A}^{(2)} = \frac{\rho_t}{2} [(1 + \Psi) \mathbf{l}_\varrho \otimes \mathbf{l}_\varrho + (1 - \Psi) \mathbf{l}_{\varrho^\perp} \otimes \mathbf{l}_{\varrho^\perp}] \quad (8.13)$$

where  $\mathbf{l}_{\varrho^\perp}$  is the unit vector perpendicular to  $\mathbf{l}_\varrho$  and  $\mathbf{l}_\varrho = \varrho / |\varrho|$  is the average line direction, and  $\Psi$  is approximated as

$$\Psi \approx \frac{(|\varrho|/\rho_t)^2 \left(1 + (|\varrho|/\rho_t)^4\right)}{2} \quad (8.14)$$

[29] showed that it is possible to construct CDD formulations that additionally include higher-order equations, which was analyzed for a number of formulations by Monavari et al. [38]. However, [47] showed that already the above set of equations is well able to represent many important features of DDD simulations.

The velocity  $\nu$  in the above equations needs to be specified in terms of a constitutive equation through which elastic interactions enter the model,

$$\nu = \begin{cases} \frac{b}{B} (|\tau_0| - \tau_y) & \text{for } |\tau_0| > \tau_y \\ 0 & \text{otherwise} \end{cases} \quad (8.15)$$

where  $\tau_0 = \tau_{\text{ext}} + \tau_{\text{int}}$  is the summation of the external shear stress ( $\tau_{\text{ext}}$ ) and the long-range (or “internal”) interaction stresses ( $\tau_{\text{int}}$ ) which have to be obtained from the additional solution of a dislocation eigenstrain problem [32, 48, 49].  $\tau_y$  is as above the Taylor-type yield stress.

## 8.4 Example 1: Comparison of the Alexander–Haasen and the Groma Model

### 8.4.1 Governing Equations

In the following, we only want to study the difference due to the transport character of the evolution equations. To make the two models comparable, we will use the same phenomenological source term for dislocation multiplication of the AH model for the Groma model. By adding the right-hand side of Eq. (8.3) into the transport equations Eq. (8.6) with the assumption that  $\rho_{\text{tot}} \equiv \rho_m$ , the evolution equations Eq. (8.6) then simply become

$$\begin{aligned}\partial_t \rho_{\text{tot}} &= -\partial_x (\rho_{\text{gnd}} v) + S \\ \partial_t \rho_{\text{gnd}} &= -\partial_x (\rho_{\text{tot}} v)\end{aligned}\quad (8.16)$$

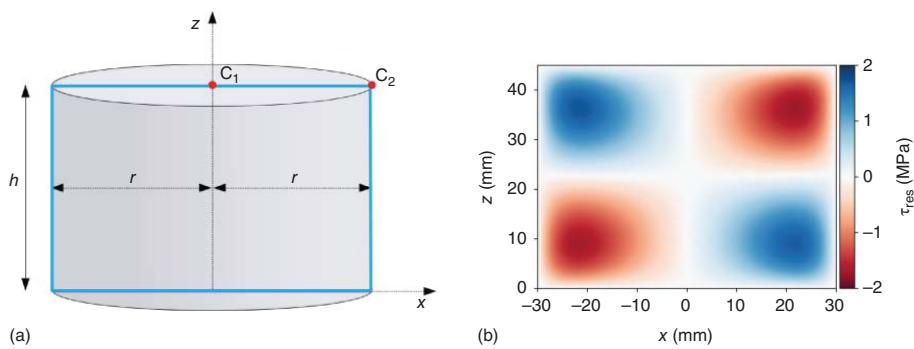
with

$$S = K \left( \frac{\tau_{\text{eff}}}{\tau_0} \right)^\lambda \rho_{\text{tot}} |v| \quad (8.17)$$

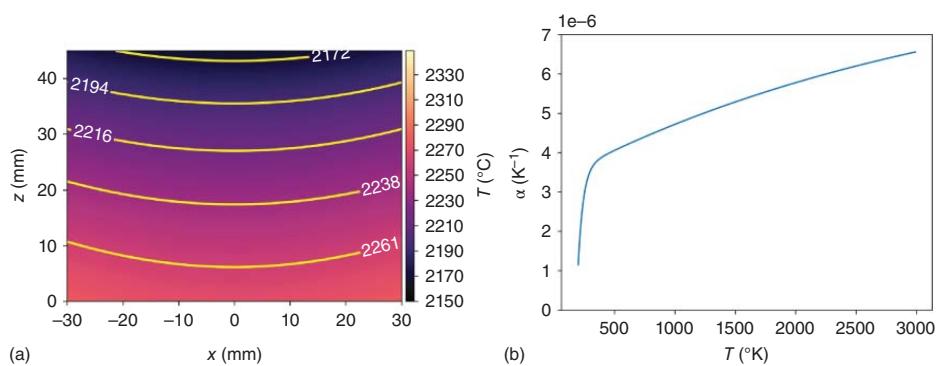
where  $v$  is again given by Eq. (8.1). The subscript “m” in the AH model indicates that only mobile and no sessile dislocations are considered; the Groma model does not have to differentiate between the two “types” of dislocations. However, since in our model no, e.g. junction formation can take place, all dislocations could be considered as mobile.

### 8.4.2 Physical System and Model Setup

The considered physical system is a hexagonal 4H-SiC crystal as, e.g. grown by the physical vapor transport (PVT) technique. The crystal is assumed to have  $h = 45$  mm and the radius  $r = 30$  mm, as shown by the gray-shaded region in Figure 8.2a. As a simplification, we only consider a two-dimensional cross-section as indicated by the blue rectangle in the same figure. There, the basal plane that is characterized by a normal pointing into the  $z$  direction is the only active slip system. As mechanical boundary conditions the crystal is fixed in the  $x$  and  $z$  directions at point  $C_1$  and only in  $z$  direction at point  $C_2$ . For simplicity, we do not consider cooling, heating, or heat fluxes, only a time-independent symmetrical temperature field is prescribed during simulation. The resulting resolved shear stress distribution is shown in Figure 8.2. The same geometry setup is used for the AH model and the Groma model. The simulations are based on the following material parameters and constants:  $b = 3.073 \times 10^{-10}$  m,  $v_0 = 8.5 \times 10^{-15}$  m/s,  $K = 2.0 \times 10^{-5}$  m $^{-1}$ ,  $Q = 3.3$  eV,  $\lambda = 1.1$ ,  $m = 2.8$ ,  $a = 0.425$ , and the Boltzmann constants is  $k_B = 8.617 \times 10^{-5}$  eV/K. For the mechanical problem, the thermal expansion coefficient is temperature dependent [50] as shown in Figure 8.3; also the components of the stiffness tensor



**Figure 8.2** (a) 2D crystal geometry and (b) initial distribution of the resolved shear stress  $\tau_{\text{res}}$  at  $t = 0$  seconds in the plane indicated by the blue lines in (a).



**Figure 8.3** (a) Prescribed temperature field, (b) Thermal expansion coefficient.

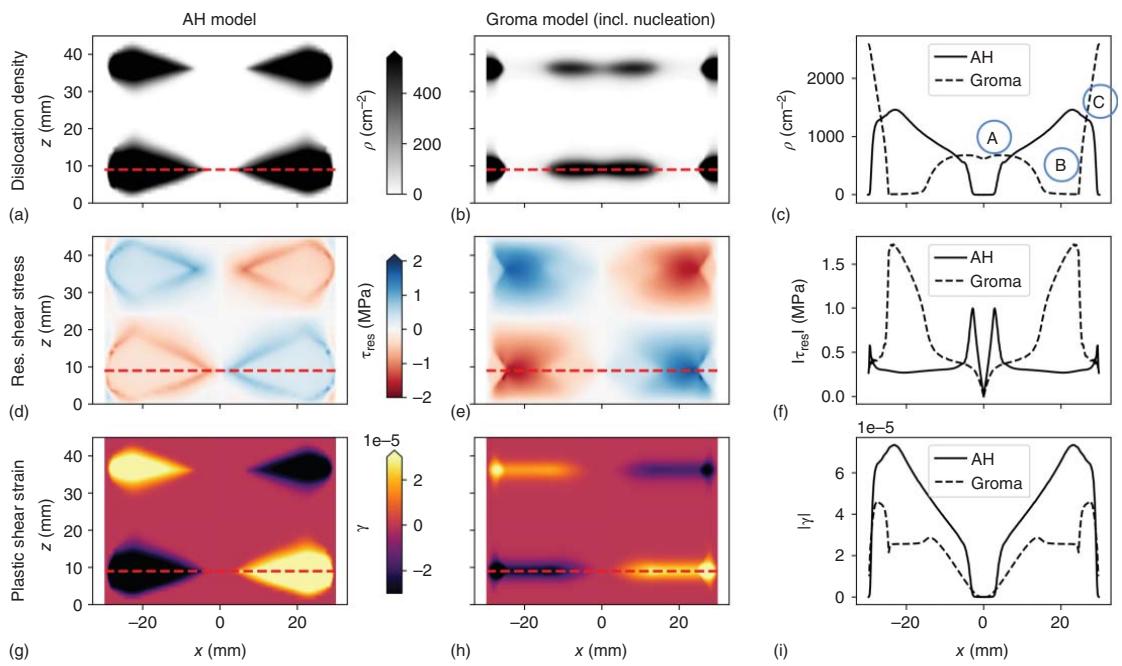
are temperature dependent [51]. In Voigt notation, they read for hexagonal SiC: The temperature-dependent shear modulus is taken as the elastic constant  $C_{44}$ .

$$\begin{bmatrix} C_{11} \\ C_{12} \\ C_{13} \\ C_{33} \\ C_{44} \end{bmatrix} = T \times \begin{bmatrix} -0.025 \\ -0.011 \\ -0.011 \\ -0.025 \\ -0.007 \end{bmatrix} \frac{\text{GPa}}{\text{K}} + \begin{bmatrix} 486.6 \\ 101.3 \\ 59.02 \\ 528.9 \\ 150.3 \end{bmatrix} \text{GPa} \quad (8.18)$$

For the numerical solution of this time-dependent, multiphysics problem which consists of a mechanical part, a thermal part and the dislocations part, the finite element method is used. For the numerical discretization, triangular elements with quadratic shape functions were used for both the elastic and thermal problem; for the CDD dislocation problem, we used cubic shape functions so that all derivatives are approximated properly.

### 8.4.3 Results and Discussion

The simulation results of the AH model and the Groma model are shown in Figure 8.4 and include dislocation density, resolved shear stress, and plastic shear strain at a total time of  $t = 3000$  seconds. There, the plots in the left column display the result from the AH model, the middle column shows the results from the Groma model, and the last column are the corresponding results along the red, dashed line. The difference between these two model is then easily observable with both the magnitude of dislocation density (Figure 8.4a,b) and the qualitative shape of the plots themselves (see Figure 8.4c). The AH model shows a growing patch of increasing dislocation density (see Figure 8.4a) where the resolved shear stress is highest while the Groma model exhibits smaller patches of dislocation density (see Figure 8.4b) at the surface ( $x \approx 30$  mm, label C) and around the crystal axis ( $x = 0$  mm, label A). The maximum dislocation density values of the Groma model are observed to be close to the surface with values of roughly  $2500 \text{ cm}^{-2}$  and a value of  $600 \text{ cm}^{-2}$  around the axis, while the AH model has a maximum value of approximately  $1500 \text{ cm}^{-2}$ . In a way, the two models behave opposite to each other. The difference between the two models is also obvious in the results of the resolved shear stress. Figure 8.4d,e shows the resolved shear stress  $\tau_{\text{res}}$  field for the basal slip system with respect to the dislocation density distribution in Figure 8.4a,b. In the AH model,  $\rho_m$  will initially increase at the four stress hot spot (see Figure 8.2b) and then decrease as a consequence of plastic relaxation which can be observed in the shape change (compared Figure 8.2 and Figure 8.4d); it reaches the state shown in Figure 8.4d. As a result of this “stress transfer,” a substantial increase in dislocation density by nucleation of new dislocations takes place in regions where originally the initial stress was low. As opposed to that, in the Groma model, dislocation accumulations occur close to the surface and close to the crystal axis. The reason for this behavior is that dislocations are nucleated where the stress is highest, but then move away, driven by shear stresses. They accumulated where the shear stress is low (see Figure 8.4e,f) and form quasi-stationary pile-up structures. It ultimately



**Figure 8.4** Comparison between AH model and Groma model including a source term: the top row shows the density, the middle row the resolved shear stress, and the bottom row depicts the plastic strain. The left column are results for both models plotted along the red, dashed lines.

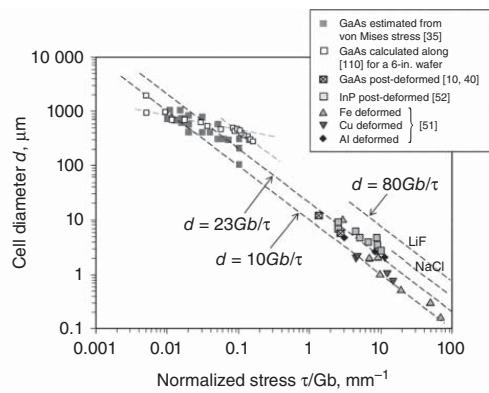
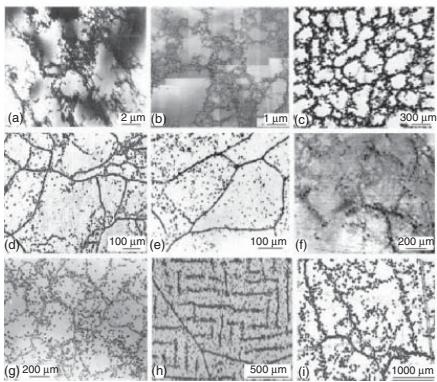
leads to a depleted zone where in the AH model the density is highest (see label B in Figure 8.4c).

Is this consistent with the results for the plastic shear? For the AH model, plastic strain co-evolves with the nucleation of dislocation density, and therefore, as expected, has roughly the same shape as the dislocation density (see Figure 8.4g,i). The Groma model behaves quite differently as the AH model. In the Groma model, the plastic strain is caused by dislocation *motion* and is high in the regions which were swept by dislocation (see Figure 8.4h,i). These are, for this example, exactly the regions where no dislocations are present any more. This is the expected behavior which is consistent with basic dislocation dynamics. Thus, the comparison of the two different simulations revealed that the flow of dislocation in the crystal during growth cannot be neglected, as it is done in the AH model. The dislocation motions controls the distribution of dislocation inside the crystal and makes it possible that dislocations can move even to places where originally the stress was low, such as the surfaces or the central region. However, the Groma model has some limitation, as already above stated: e.g. the source term is just an approximation which cannot capture the whole mechanisms of dislocation nucleation; furthermore, dislocations are only assumed to be straight lines. And last but not least, the simulation only considers basal plane dislocation while there are many more types of dislocations in reality that also need to be taken into account.

## 8.5 Example 2: Dislocation Flow Between Veins

### 8.5.1 A Brief Introduction to Dislocation Patterning and the Similitude Principle

Under certain conditions, it is observed that dislocations tend to form heterogeneous but regular structures, some of which are termed “dislocations patterns.” They are observed both in metals as well as in semiconductors. The micrographs in Figure 8.5 show examples of such structures. These dislocation patterns can occur, e.g. as approximately periodic dislocation agglomerations or sharply distinguishable cell (e.g. Figure 8.5c) or “labyrinth” structures (Figure 8.5h). The common feature is that all of these structures are characterized by clusters of very high dislocation density alternating with regions of very low (or zero) density. These dislocation formations are usually “metastable structures which mostly persist upon unloading. One of the remarkable features is that the cell sizes  $\Lambda$  – regardless material, loading condition or temperature – are always related to the applied stress  $\tau_{\text{ext}}$  through the “law of similitude [52, 53] by  $\Lambda = DaGb/\tau_{\text{ext}}$ , where usually the constant  $D = 10\text{--}20$  and  $G$  is the shear modulus, and  $a \approx 0.3$  is the nondimensional coefficient relating flow stress and dislocation density  $\rho$  in the Taylor relationship  $\tau = aGb\sqrt{\rho}$ . This has been known for plastically deformed metals for about half a century [54] but is also observed in semiconductors as pointed out more recently by Rudolph [4, 5]: e.g. in GaAs dislocations arrange themselves in experimentally observable cellular structures of diameter in between 100 and 1000  $\mu\text{m}$ . Although



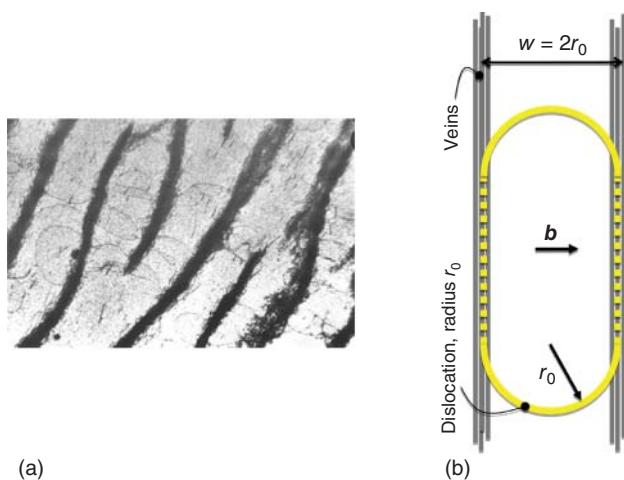
**Figure 8.5** Dislocation organizes themselves into patterns as, e.g. cell structure, independent of the material or loading condition (A). The cell size is related to the applied stress through the “similitude relation (B). Images taken with permission from [4].

the regular (sometimes fractal) appearance is visually interesting, these dislocation structures deteriorate the electronic and mechanical properties of semiconductors, and their formation needs to be prevented as far as possible. Hence, understanding the mechanisms leading to the occurrence of patterns is crucial for being able to prevent such structures. Rudolph [4] suggested to relate the origin of this phenomenon to the same mechanisms as in the case of metals (where cells form roughly in the  $1\text{--}10\ \mu\text{m}$  size range, see Figure 8.5A). The different cell size regimes, i.e. mm-range for semiconductors and  $\mu\text{m}$ -range for metals, is related to the very different dislocation densities at saturation which result in different stresses due to the Taylor relationship (8.5B). In the case of SiC dislocation, cell structures have also been reported in the past for materials exhibiting dislocation densities in the mid  $10^4\ \text{cm}^{-2}$  to low  $10^5\ \text{cm}^{-2}$  range; however, basically no attention has been paid to describe the dislocation microstructure in terms of such networks or cells. At lower dislocation densities in the mid  $1\times 10^3\ \text{cm}^{-2}$  range as it is typical for best commercial SiC wafer materials, the cell structure is difficult to visualize and mainly occurs in defective areas where dislocation bundles occur. So far, no detailed theoretical concept or computational model of dislocation cell formation in semiconductor materials exists. There is, however, a great need to explain and therefore to be able to take countermeasures against the formation of dislocation entanglements, which also has been recognized in the literature: for instance, the 2014 edition of the book *Extended Defects in Semiconductors* by Holt and Yacobi [55] strongly emphasizes within the last sentence of the section *Major Persisting Issues* "... The need for a theoretical framework for this phenomenon [cellular dislocation structures]....". Encouraged by this general viewpoint, we take it as an worthwhile task to transfer modeling of dislocation patterning from metals to the semiconductor case.

### 8.5.2 Physical System and Model Setup

Approaches that are able to predict dislocations patterning are – even in the modeling community for dislocation mediated metal plasticity simulation – very scarce: even discrete simulation methods are due to the computational cost generally not able to predict the evolution of dislocation patterns. This is why in the following a CDD model will be used to demonstrate some of the most important mechanisms involved during formation of dislocation patterns. The first stage, i.e. the formation of such stable dislocation agglomerations has already been investigated in [34] and for a different formulation also in [56] where it was shown that the above CDD model is indeed able to simulate this.

As a model system, we now assume that already a stable wall-like structure (e.g. a cell wall or the wall of a persistent slip band, PSB) exists. A dislocation dynamics model must then be able to represent the motion of dislocations between these constraining walls, similar to the situation investigated in [38]. The experimental results from [57] shown in Figure 8.6a illustrate the walls structure in a so-called persistent slip band (PSB) which consist of dipolar edge dislocation configurations. The dislocations gliding in the channels between the walls have mainly



**Figure 8.6** (a) TEM micrograph showing walls of PSBs (dark) [57] and gliding of screw segments between walls; (b) schematic of dislocation vein structure made up of extended edge dipoles and glide screw dislocation of radius  $r_0$ . The channel width is  $w = L_x$ . Source: Hael Mughrabi. Cyclic slip irreversibilities and the evolution of fatigue damage. Metallurgical and Materials Transactions B, 40(4):431–453, 2009. Source: Hael Mughrabi. Cyclic slip irreversibilities and the evolution of fatigue damage. Metallurgical and Materials Transactions B, 40(4):431–453, 2009.

screw orientation. In cell structures, the cell walls may have a different dislocation content; however, the ability to represent bowing out of dislocations and glide in between the walls is equally important. In what follows we will now demonstrate that the CDD model is able to represent the bowing-out/gliding mechanism, which is a prerequisite for predicting the formation for cell or wall structures.

### 8.5.3 Geometry and Initial Values

The geometry is chosen to be rectangular with the channel width  $L_x$  and the channel length  $L_y$  (see Table 8.1 for all numerical values and used material parameters). The system is periodic in  $y$  direction, i.e. dislocations exiting the system at the top will flow back in at the bottom. In horizontal direction, the boundaries are

**Table 8.1** Parameters for dislocation flow between veins.

Parameter	Value
System size $L_x$	$1 \times 10^{-5}$ m
System height $L_y$	$2 \times 10^{-5}$ m
Loops radius $r_0$	$2 \times 10^{-6}$ m
Standard deviation $s$	$7 \times 10^{-6}$ m
Burgers vector modulus $b$	$0.256 \times 10^{-9}$ m
Drag coefficient $B$	$5 \times 10^{-8}$ Pa s
Shear modulus $G$	$128 \times 10^9$ Pa

impenetrable for dislocations, which are modeled by a horizontal velocity profile that is zero directly at the boundaries, constant inside the channel with a value of  $v_0$ , and has a smooth transition in between:

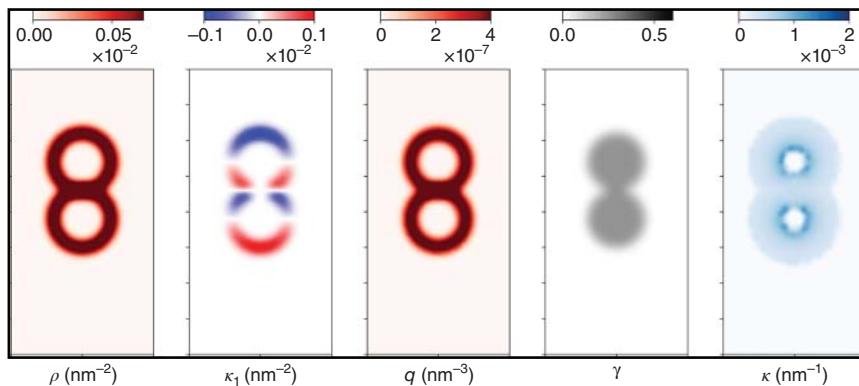
$$v = v_0 \left( \frac{2}{1 + e^{-(x+L_x/2)\beta}} - 1 \right) \left( \frac{2}{1 + e^{-(L_x/2-x)\beta}} - 1 \right) \quad (8.19)$$

with  $v_0 = 0.4 \text{ ms}^{-1}$ ,  $\beta = 0.004$ . Within the present work, we ignore all dislocation interactions and concentrate exclusively on the “kinematics” that is, how curved and connected lines move and evolve in space and time without interactions.

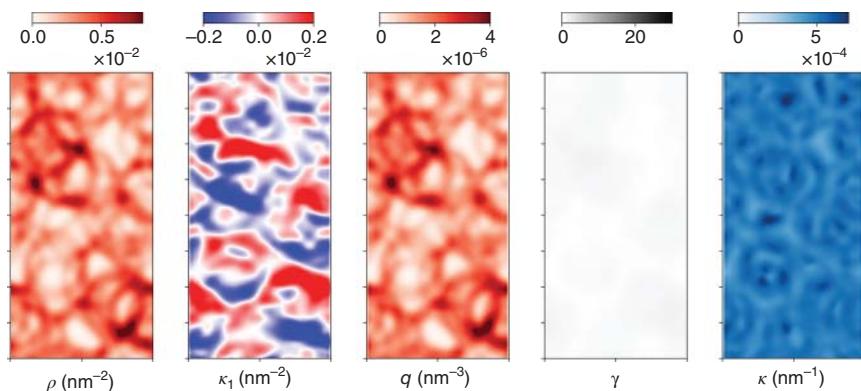
In order to consistently representing a system of curved and connected lines in a coarse-grained continuum manner, we obtain dislocation density distributions (such as  $\rho_t$ ) by first defining a distribution of a number of mathematical dislocation loops. This is followed by convolution along the loops’ lines with a Gaussian normal distribution function  $(s\sqrt{2\pi})^{-1} \exp(-\xi^2/2s^2)$ , where  $s$  is the width of the distribution and  $\xi$  is the distance perpendicular to the loop. This effectively “smears out” the line perpendicular to it. By multiplication of the dislocation density with the normalized radial unit vector or division by its radius,  $r$ , we can determine the dislocation density vector  $\varphi$  or the curvature density  $q_t = \rho_t/r$ , respectively. CDD initial values are obtained by summing up the individual fields. Initial values with two dislocation loops and 50 dislocation loops for our simulation are shown in Figures 8.7 and 8.8. The curvature, i.e. 1/radius of a line is obtained in a postprocessing step from  $k = q/\rho$ ; it is not defined in regions where the density is zero (compare the right most plot in Figure 8.7). More details on the process of creating consistent initial values can be found in [33, 34].

#### 8.5.4 Results and Discussion

Because of the zero velocity in the walls and the smooth transition from  $v = 0$  to a constant velocity  $v_0$  further away from the wall, the velocity field acts such that dislocations are first slowed down on their way toward the walls and eventually freeze



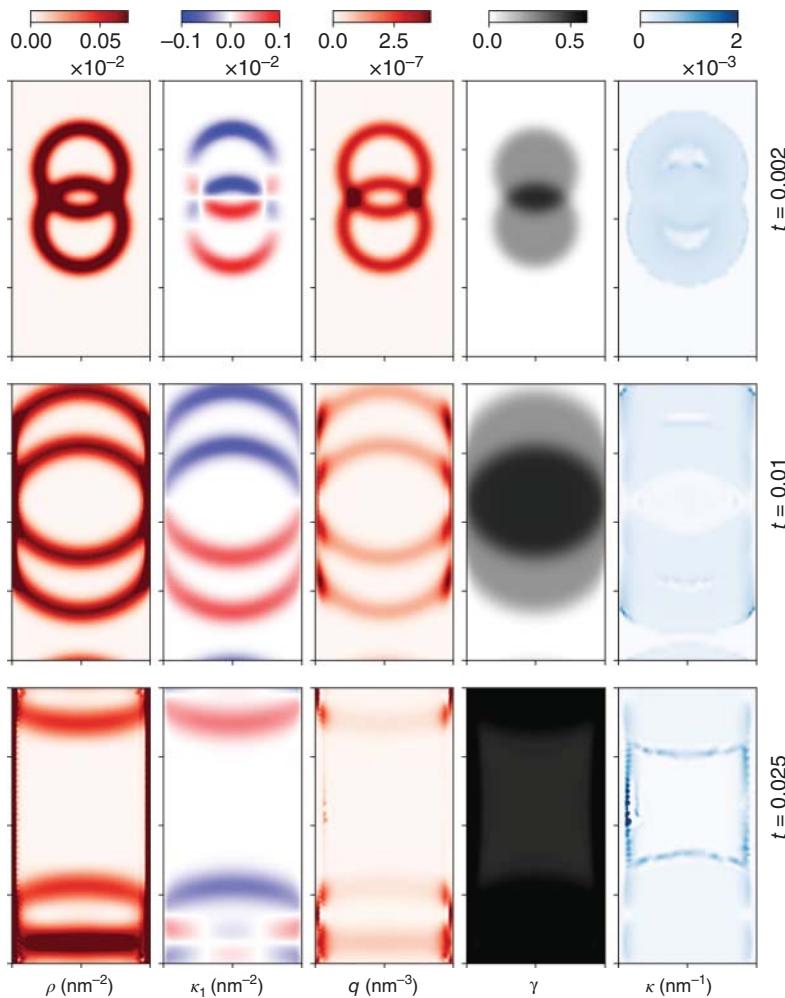
**Figure 8.7** Initial CDD field values for two quasi-discrete dislocation loops. From left to right: total density  $\rho$ , edge GND density component  $\kappa_1$ , curvature density  $q$ , plastic slip, curvature.



**Figure 8.8** Initial CDD field values for a distribution of 50 dislocation loops. From left to right: total density, edge GND density component, curvature density, plastic slip, curvature.

in their motion so that they cannot enter the walls. Figures 8.9 and 8.10 present the relations among the four CDD variables during dislocation evolution. The two-loop system is not fundamentally different from the 50-loop system but makes it easier to understand the meaning of the different fields. Initially, one can observe free loop expansion inside the domain because of the constant velocity. Since we neglect interaction between dislocations and assume that they are on different but near-by slip planes in their respective averaging volumes, they will pass through each other during expansion. Later, at time  $t = 0.01$ , we can observe that dislocation will reach the left and right boundaries and begin to a pile-up at these walls while they still expand in the vertical direction (see Figures 8.9 and 8.10). An interesting feature is the formation of pile-ups of bent lines at walls: when expanding dislocation loops touch the left and right boundaries, they bend and adjust to the shape of the walls. Because of that, the values of curvature density  $q$  at these areas are larger than inside area. Line pile-ups of dislocation density can be seen in the left and right boundaries and even clearer as a banded structure at time  $t = 0.025$ . The dislocation density  $\rho$  has a high value in the vicinity of the walls because of the density from piled-up dislocations. The threading edge segments, i.e. density with approximately horizontal orientation, are segments from expanding loops. Therefore, they become more straight, which also shows in their reduced curvature (last column of Figures 8.9 and 8.10). Investigating the curvature  $k = q/\rho$ , because of the impenetrable walls we observe that the screw segments are straight with the curvature value  $k = 0$  at walls and we find a nonzero curvature shortly before the surface where dislocations need to bend strongly.

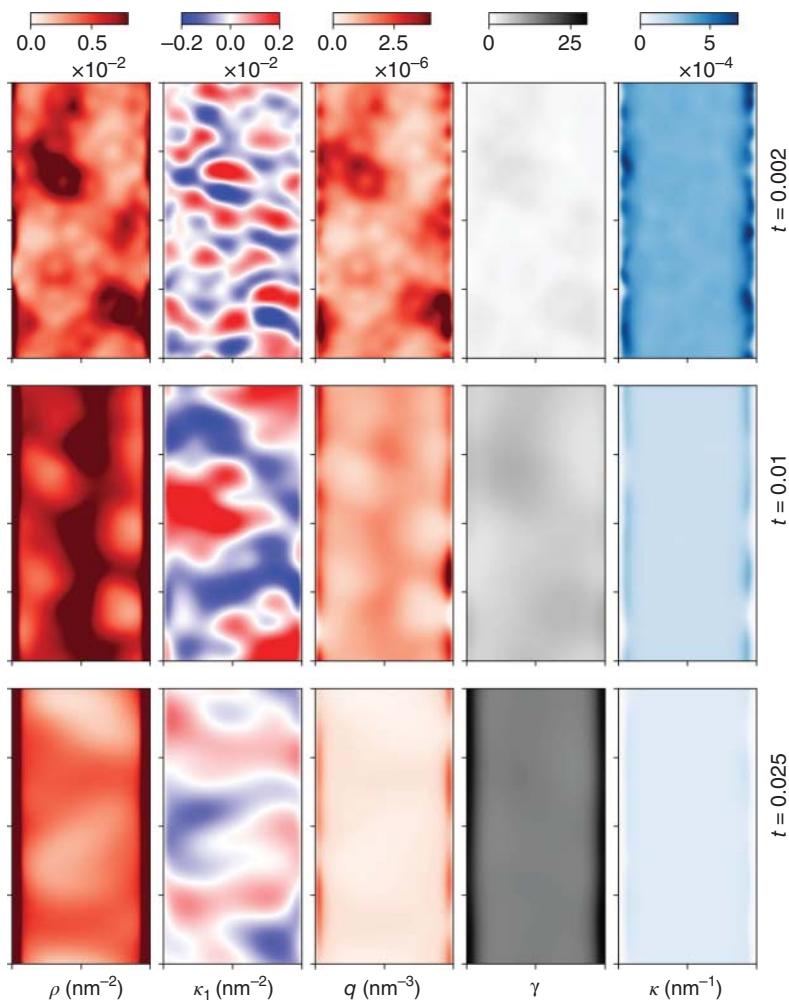
The plastic slip  $\gamma$  – which is the pendant of the plastic strain on the level of the individual slip plane – shows clearly that it is proportional to the slipped area. Where two loops overlap, the value of  $\gamma$  is doubled. The system with 50 loops, on the other hand, shows nearly homogeneous plasticity in the inside of the channel and a larger accumulation of plastic slip directly at the boundaries. This is due to the fact that the high curvature density scales is responsible for additional line length production.



**Figure 8.9** Two mobile dislocation loops expansion in the channel.

How do these microscopic field variables relate to average quantities on the macroscopic system scale? Figure 8.11 shows the total dislocation line length  $l = \int_A \rho dA$  versus time. To validate our model results, we construct two extreme cases:

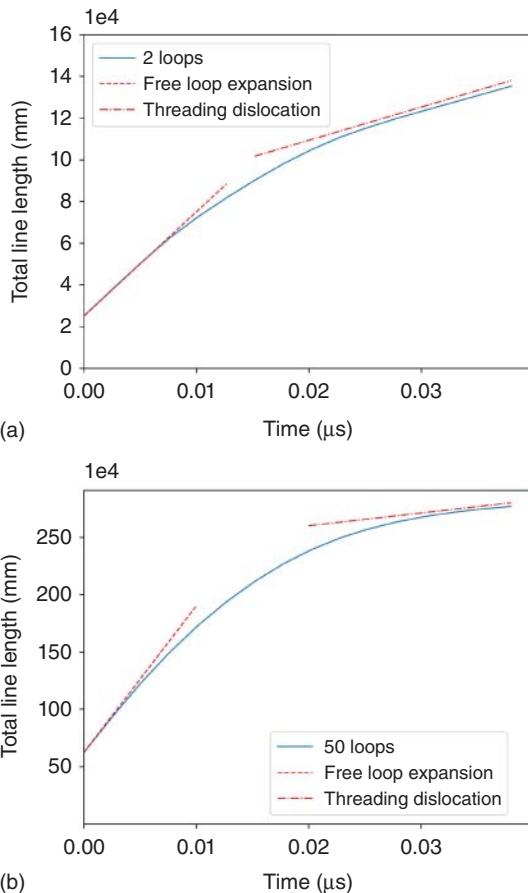
- (i) There is only free loops expansion as if no boundaries and interactions are present. This results in a linear line length increase  $L = N_d 2\pi (r_0 + vt)$  (with  $N_d$  the number of loops and  $v$  the velocity) and is shown as the tangent in Figure 8.11a.
- (ii) Loops have a very large radius such that the threading edge segments can be considered as straight. Then these segments move and at the same time deposit straight screw segments at the boundaries, as if it were a rectangular loop. This yields a line length of  $L = N_d (\pi w + 4vt + 2w)$  with  $w$  the width of the channel. This is shown as the tangent in Figure 8.11b.



**Figure 8.10** Fifty mobile dislocation loops expansion in the channel.

One can observe that the simulation reproduces the correct rate of line length at the beginning of the simulation and toward the end, in between is a larger transition region. This clearly demonstrates that the complex interplay between dislocation loop expansion, dislocation motion, line bending, and deposition at a boundary can all be predicted by this CDD model. Additionally, without dislocation interactions, the system is just a superposition of individual loops, even in cases where the individual loops can no longer be distinguished. Using just the Groma model could not work because the line length production due to the threading edge dislocations cannot be represented and the total line length in the system would stay constant. How would the AH model have performed? A direct comparison is difficult because the CDD model can operate even without stresses and just by prescribing a velocity. Assuming a constant shear stress, the AH model would not be able

**Figure 8.11** Total line length vs. time. The two tangents denote the line length assuming (i) only free loop expansion without any boundaries and (ii) only straight edge segments that are connected by straight screw segments as in a rectangular loop.



to represent the deposition of density at the boundary, similar to what was shown in Figure 8.4. Furthermore, it would not be possible to interpret the resulting density or plastic strain configuration in terms of geometrical properties of dislocations lines. Since dislocations are the carrier of plastic deformation, we see the lag of interpretability as one of the big drawbacks of any purely phenomenological continuum model – irrespective of the quality of the overall predictions.

## 8.6 Summary and Conclusion

An overview over current state of the art modeling techniques for predicting defects in semiconductors has been presented. Putting a focus on systems of dislocations, it was discussed that it might be very lucrative to apply simulations methods from the metal plasticity domain to the domain of semiconductors. In this context, a number of state-of-the art methods for predicting the dislocation dynamics in a continuum frame work were introduced and critically discussed. In particular, the comparison with one of the most established simulation model used in the

semiconductor domain, the Alexander–Haasen model demonstrated that it is very important to be aware of the limitations and the range of applicability of a model: the Alexander–Haasen model is not able to predict fluxes of dislocations, which in many applications might be a strong limitation.

Discussing modeling approaches in the context of dislocation pattern formation, we demonstrated that the introduced CDD model is able to represent many important dislocation features that also can be clearly interpreted in terms of geometrical features of curved lines. Nonetheless, the current CDD theory still has not been applied to general system in three dimensions. This will require detailed work on extracting data from DDD and MD simulations that can then be used as input for dislocation interaction formulations. Nonetheless, a continuum model that operates on length and time scales comparable to experimental ones also might be very well able to act as a link between theory, modeling, and experiment. In particular, experimental data is, of course, the ultimate benchmark for any model. Therefore, one might be tempted to say that a good simulation model need not exactly reproduce experimental results; rather, a good simulation model is a model that can be easily interpreted as well as parameterized and directly validated by experiments, both on the microscopic and macroscopic scale.

## References

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# 9

## Gate Dielectrics for 4H-SiC Power Switches: Understanding the Structure and Effects of Electrically Active Point Defects at the 4H-SiC/SiO<sub>2</sub> Interface

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### 9.1 Introduction

At the heart of every metal oxide semiconductor field effect transistor (MOSFET) is the interface between the oxide and the semiconductor. The field effect may create a conducting channel between the source and the drain of the transistor [1] which makes up an electronic switch. Especially in the field of power transistors, designed to block source-drain voltage above 600 V, silicon carbide (SiC) has become an important semiconductor in recent years. However, there was a 10-year delay between the introduction of the first SiC diode and the first SiC MOSFET [2]. This delay can partially be attributed to SiC specific manufacturing challenges for MOSFETs. Among them, it was crucial to be able to control the detrimental impact of electrically active point defects at the four layer hexagonal SiC (4H-SiC)/silicon dioxide (SiO<sub>2</sub>) interface which impacted the performance and reliability of SiC MOSFETs.

Here, we summarize previous research on a few SiC specific electrical effects of interface traps on the performance and reliability of SiC MOSFETs. In Section 9.2, we describe the electrical characteristics and how they are efficiently characterized with electrical measurements. In Section 9.3, we discuss possible microscopic origins for the individual electrical effects.

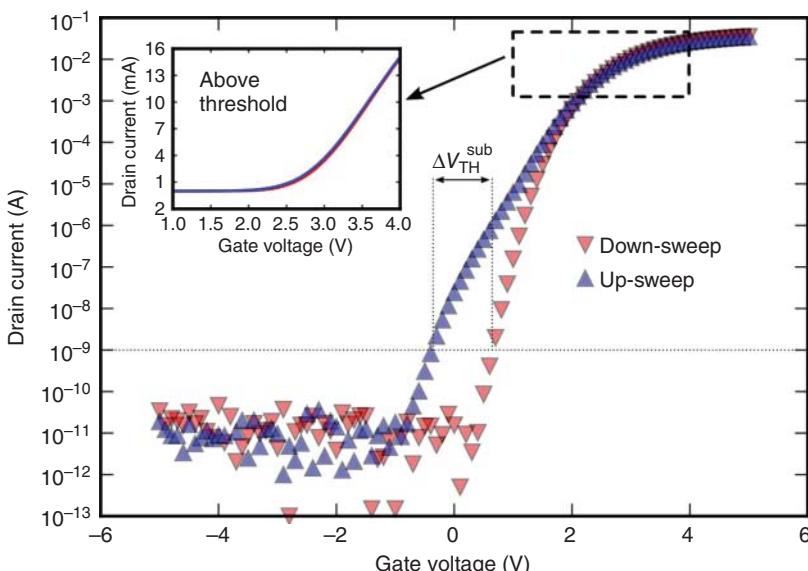
### 9.2 Electrical Impact of Traps on MOSFET Characteristics

It is rather obvious that point defects at or near the SiC/SiO<sub>2</sub> interface have a potentially detrimental impact on the performance and reliability of SiC MOSFETs. However, it is difficult to draw a connection between a group of electrically active point defects to a certain electrical effect in state-of-the-art MOSFETs. Here, we list a handful of electrical effects which can be described independently and can be assigned to a group of electrically active point defects.

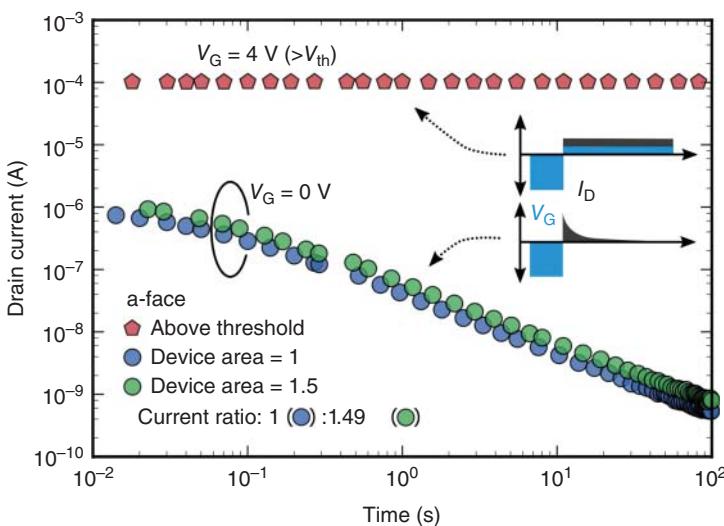
### 9.2.1 Sub threshold Sweep Hysteresis

The subthreshold sweep hysteresis has been found in 2016 by comparing the transfer characteristic (drain current–gate voltage ( $I_D V_G$ )) of trench SiC MOSFETs measured with upward vs. downward gate voltage sweep direction [3], see Figure 9.1. It occurs only if the upward sweep starting gate voltage is a few volts negative and thus at the onset of the accumulation of holes at the interface. When the gate bias is then swept into the positive direction to turn on the transistor, a small drain current starts to flow already at negative gate biases. This also leads to a small but measurable drain current at zero volts gate bias [2]. However, when staying at zero gate bias after a previously negative gate bias phase, the drain current slowly decreases and eventually vanishes completely, as can be seen in Figure 9.2. When continuing the gate bias sweep to more positive voltages, the difference between up- and downward sweep vanishes nearly completely. The remaining few mV hysteresis at positive gate biases can be attributed to the charging/discharging of oxide defects, similar to what has been measured two decades ago on SiC metal oxide semiconductor capacitors (MOSCAPs) [4].

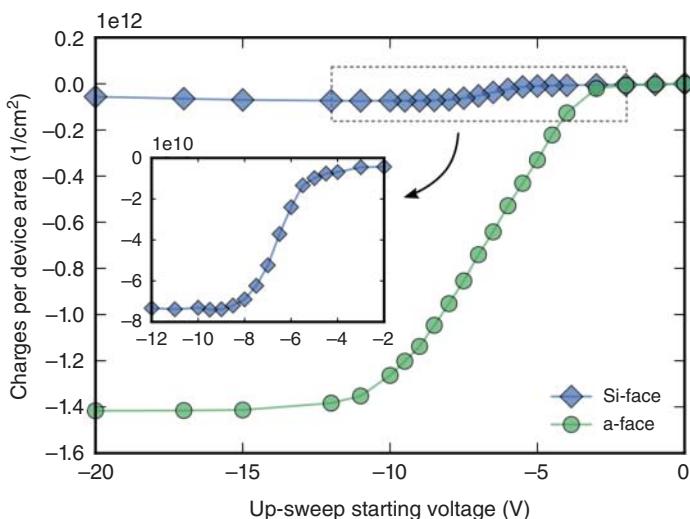
The amount of SH depends strongly on the sweep starting voltage, as depicted in Figure 9.3. The larger the negative sweep starting bias, the larger the hysteresis, until a saturation level below approximately  $-15$  V. When defining a small drain current level for a  $V_{TH}^{\text{sub}}$ , one can use the oxide capacitance to calculate a number of charges at the 4H-SiC/SiO<sub>2</sub> interface as  $N = C_{\text{ox}} \Delta V_{TH}^{\text{sub}} / q$ , where  $q$  is the elementary charge. It is found that the number of charges leading to the few volts of SH is in the range of  $10^{12} \text{ cm}^{-2}$ . The same effect occurs on Si-face (planar) and a-face (trench)



**Figure 9.1** Example for the sub-threshold sweep hysteresis (SH) for a sweep starting gate voltage of  $-5$  V. The inset shows that above the  $V_{TH}$  the hysteresis is negligibly small [3].



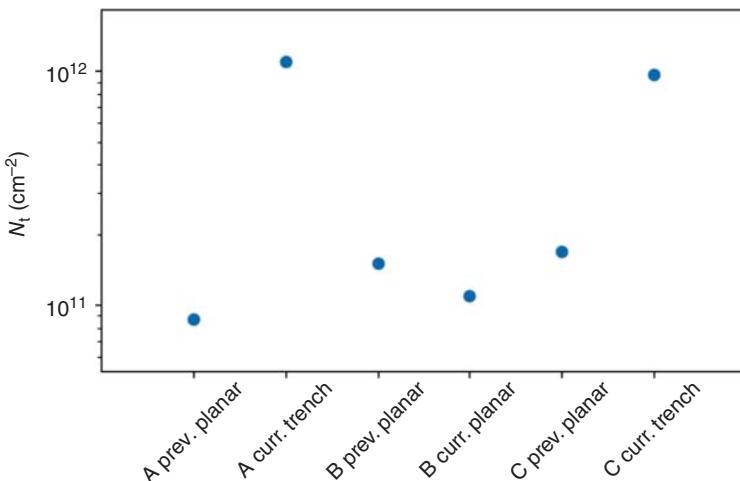
**Figure 9.2** At the  $V_{TH}$ , the drain current shows negligibly tiny transient variations. At 0 V, after a negative gate bias pulse, the drain current decreases slowly over time. The current scales with the device area, indicating a uniform distribution of the drain current on the whole device area [3].



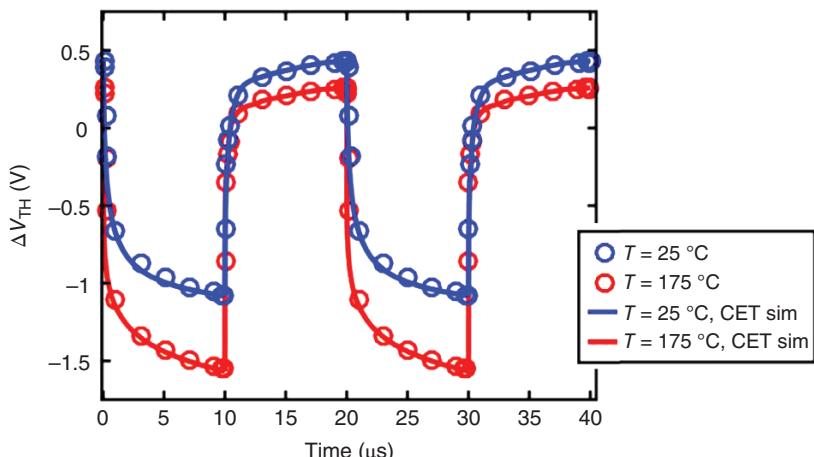
**Figure 9.3** Dependence of the amount of SH on the upward-sweep starting voltage for silicon (Si)-face (planar) and a-face (trench) MOSFET devices [3].

MOSFET devices but is about ten times larger on trench MOSFETs. This finding is fairly independent of the manufacturer and its particular technology, as depicted in Figure 9.4.

SiC MOSFETs are often used in half-bridge configuration where the gates of the two transistors are switched with e.g. 50kHz. When the low level of the gate signal

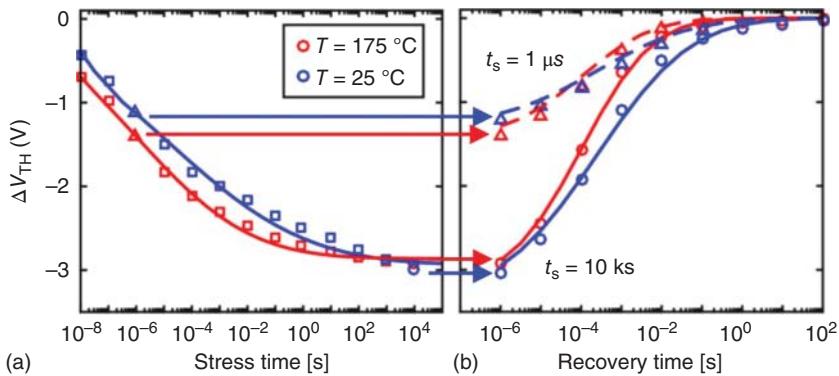


**Figure 9.4** Comparison of the amount of SH for different manufacturers (A, B, and C), their current (curr.) and previous (prev.) generation, and whether the device technology is planar (Si-face) or trench (a-face) [5].



**Figure 9.5** Evolution of the  $\Delta V_{TH}$  during the application of a bipolar alternating current (AC) signal on the gate between  $-5$  and  $25$  V [6]. Symbols are measurements, lines are calculations from the corresponding capture-emission time (CET) map.

to drive the transistor in off-state is negative, the actual  $V_{TH}$  of the device varies a few volt in these small time frames [6], see Figure 9.5. In order to measure this effect, a dedicated setup which switches from the applied gate voltage to a quick  $V_{TH}$  measurement and back within less than  $1\ \mu\text{s}$  is needed [6]. Then, the charging and discharging of the traps within  $\mu\text{s}$  and  $\text{ms}$  can be seen. Figure 9.6 shows the change of  $V_{TH}$  during a negative gate bias application as well as right after this period at a positive gate voltage close to the  $V_{TH}$ . Independent of the duration of the negative



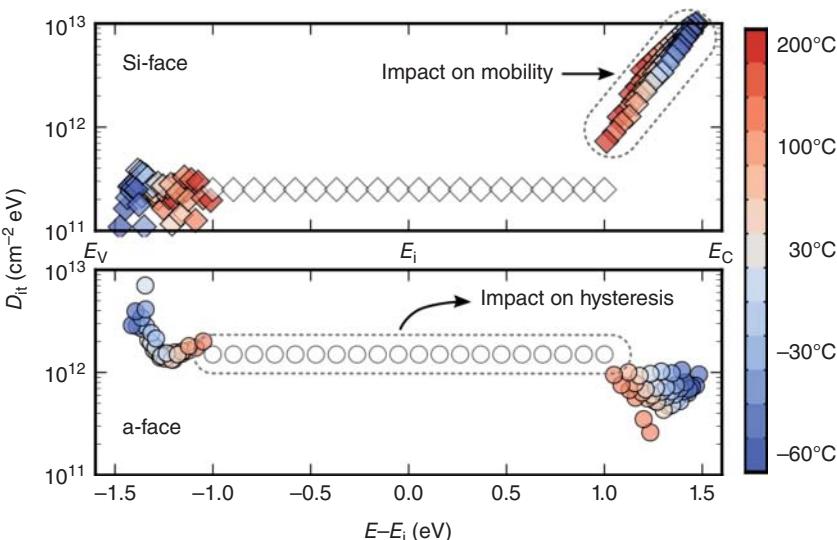
**Figure 9.6** (a) Decrease of the  $V_{TH}$  by the application of a negative gate bias of  $-5\text{V}$ . (b) Recovery of the  $V_{TH}$  shift by the application of the  $V_{TH}$  voltage at the gate. No matter if the negative bias has been applied  $1 \mu\text{s}$  or  $10 \text{ ks}$ , the  $V_{TH}$  variation vanishes after about  $100 \text{ ms}$  [6].

bias applied to the gate ( $1 \mu\text{s}$  or  $10 \text{ ks}$  in Figure 9.6), the negative  $V_{TH}$  shift vanishes after about  $100 \text{ ms}$  at the  $V_{TH}$ .

The time and voltage dependence of this charging and discharging processes can fully be modeled and calculated employing the concept of capture-emission time (CET) maps [6, 7]. A large number of traps all having the same electron capture time constant  $\tau_c$  would cause a drain current transient of the form

$$I_D(t) = I_{D,0} \exp\left(-\frac{t}{\tau_c}\right) \quad (9.1)$$

thus giving a single exponential transient which would span over about two to three decades in time. The experimentally observed transient (as depicted in Figure 9.6b) spans over about four to six decades. Therefore, it cannot be due to a single capture time constant but has to have a wider distribution of capture time constants. This distribution of time constants can be obtained by performing an multi exponential analysis (MEA) on the drain current transient data (see also Section 9.2.3). The resulting density function of the number of traps with a certain capture time constant can be displayed vs. the density of the emission time constants from the inverted process. The resulting contour map is thus a different way to display the transient behavior of a SiC MOSFET at negative gate voltage and is called a CET map. It essentially gives the number of charges with a certain capture and emission time constant. A particular measurement procedure compiles to a certain occupation of the CET map [8]. The easiest example being a finite stress duration at negative gate bias and subsequent readout at the  $V_{TH}$  is a rectangular integration of the CET map of the lower right corner [7]. The perfect agreement between experiment and CET map-based simulation in Figures 9.5 and 9.6 (circles are experimental values and lines are the corresponding calculation/simulation) is nearly obvious, indicating solely the correct derivation of the CET map from previous measurements. However, having obtained the correct CET map, any arbitrary gate bias evolution can be input and the resulting change of the  $V_{TH}$  be calculated. This allows to calculate



**Figure 9.7** Density of interface traps for similar planar (top) and trench (bottom) SiC MOSFETs [3].

and model the fast transient behavior of the  $V_{\text{TH}}$  for various application scenarios and the actual  $V_{\text{TH}}$  value can be determined at every time instance [9].

To understand the reason for the observed SH and fast  $V_{\text{TH}}$  transient, further physical analysis have been performed. The ten times larger SH effect on a-face devices compared to Si-face devices has been investigated by employing charge pumping (CP) measurements [3]. Figure 9.7 shows the density of interface traps  $D_{\text{IT}}$  for the two device types obtained by spectroscopic CP at temperatures ranging from  $-60$  to  $205$  °C. Si-face devices have a small  $D_{\text{IT}}$  near the valence band edge  $E_V$  and around mid-gap and a large increase toward the conduction band edge  $E_C$ . a-face devices do not show the increase toward  $E_C$  but have an increased density around mid-gap. This larger mid-gap density is attributed to the occurrence of SH. By applying negative biases to the gate, the Fermi level gets close to  $E_V$  which can charge these interface traps positively, resulting in shift of the  $V_{\text{TH}}$  toward negative infinity. The large increase of the  $D_{\text{IT}}$  toward  $E_C$  for the Si-face device can explain the reduced apparent channel mobility of these devices compared to a-face devices (see Section 9.2.4 for details).

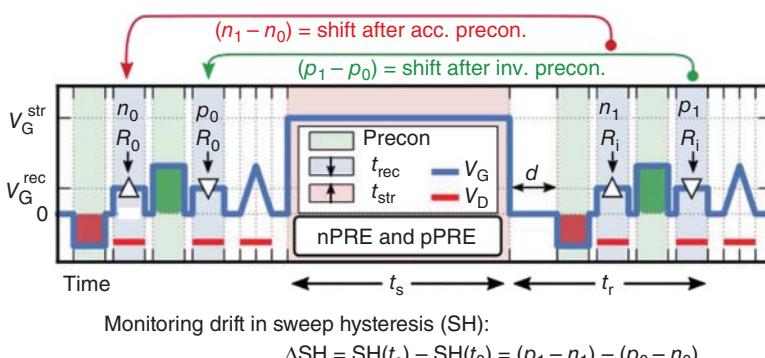
Further investigation of the SH revealed even more interesting physical details to the charging/discharging effect [10]. By analyzing the decrease of the drain current over seven decades in time, it could be proved that electron capture into interface traps obeying the Shockley–Read–Hall (SRH) theory is the physical reason for this effect. The maximum amount of chargeable interface traps could be determined to be  $4.2(1) \times 10^{12} \text{ cm}^{-2}$ . The distribution of time constants spans over 3.7 decades in time and has a capture cross section of  $2.5(3) \times 10^{-19} \text{ cm}^{-2}$ . The extraction of these parameters allows for consistent inclusion of this dynamic trapping process into device simulations.

### 9.2.2 Preconditioning Measurement

Having understood the electrical effects due to continuous charging and discharging of interface traps from the Section 9.2.1, the need for adapted measurement procedures, different from those developed for Si technology, becomes evident for the throughout characterization of 4H-SiC MOSFETs. While measurement procedures for Si-based MOSFETs had been standardized by a few organizations several decades ago, new standards for SiC-based devices are under development e.g. in the JEDEC Solid State Technology Association (see [www.jedec.org](http://www.jedec.org)).

A very promising approach to differentiate between recurring charging/discharging processes of interface traps and the creation of new traps has been proposed recently [11]. The heart of the approach is a specific evolution of the bias applied to the gate as depicted in Figure 9.8, together with instructions concerning the voltage applied to the drain and rough timing specifications. The first pulse to negative gate voltages (marked red in Figure 9.8) drives the MOSFET into accumulation, and thus, charges interface traps positively. The measurement of the threshold voltage directly after ( $n_0$ ) measures thus a very small or even negative  $V_{TH}$ . Afterwards, a positive preconditioning pulse, larger than the  $V_{TH}$ , is applied to invert the SiC in the channel region and bring the interface traps back to a neutral charge state.  $p_0$  gives a  $V_{TH}$  value close to the real  $V_{TH}$  of the device because the interface traps are neutral during normal operation around the  $V_{TH}$ . This positive preconditioning pulse is a minimum requirement for a reproducible  $V_{TH}$  measurement and has to be done prior to every  $V_{TH}$  measurement. Before the stress phase, a sweep of the gate voltage may be performed to obtain the full transfer characteristic of the device. After the stress, the same measurement procedure is applied again, leading to the two threshold voltage values  $n_1$  and  $p_1$ .

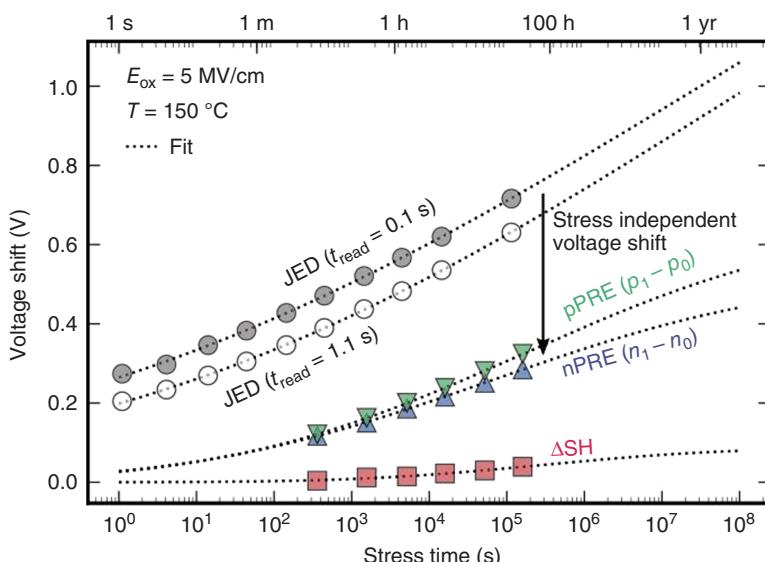
The impact of the stress phase can now be separated between a change of the  $V_{TH}$  and a change of the SH. For the change of the  $V_{TH}$ , one best uses the shift



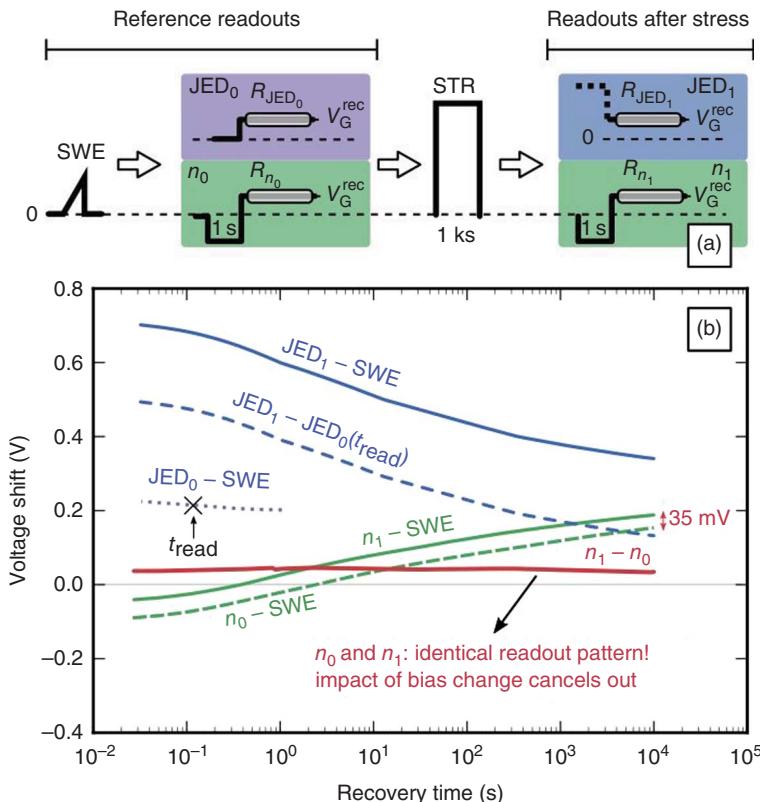
**Figure 9.8** Evolution of the voltage applied to the gate ( $V_G$ ) and drain ( $V_D$ ) with respect to the source for a preconditioning measurement [11].  $V_G^{rec}$  and  $V_G^{str}$  are the gate voltages for recovery and stress phases, respectively. With this approach, the impact of the stress phase can be measured with preconditioning after an accumulation phase (acc. precon., negative gate bias) or after an inversion phase (inv. precon., positive gate bias).

after positive preconditioning ( $p_1 - p_0$ ), since  $p_0$  and  $p_1$  are very independent on the timing of the measurement. These values are easier to measure and easier reproducible than  $n_0$  or  $n_1$ . The amount of SH can be obtained before ( $p_0 - n_0$ ) and after the stress ( $p_1 - n_1$ ). The difference between these values ( $\Delta SH$ ) indicates a change of the amount of interface traps due to the stress phase. An example result of constant gate bias stress of 5 MV/cm is compared to conventional JEDEC Solid State Technology Association (JEDEC)-like measurements (similar to what is defined in the JEDEC JESD241 document) in Figure 9.9. The comparison reveals that JEDEC-like measurements, as they had been developed for Si-based MOSFETs, do not properly account for the charge state of interface traps and overestimate the amount of threshold voltage shift for 4H-SiC MOSFETs. Using the preconditioning measurement approach, it is revealed that a large fraction of the shift which is observed in the standard JEDEC test is a recurring charging/discharging process of interface traps which cannot be accounted as degradation of the device.

Another key benefit of the method is that arbitrary delays between the end of the stress and the readout of the  $V_{TH}$  shift (time duration  $d$  in Figure 9.8) become irrelevant. This is especially beneficial in an industrial environment, where delay times between e.g. a minute and the duration of a weekend may occur. Figure 9.10 displays the dependence of the threshold voltage shift on the recovery time for different measurement approaches. JEDEC-like measurements show a large dependence on the recovery time (cf. lines with JED in Figure 9.10). The  $V_{TH}$  measurements after a negative preconditioning pulse do have a time dependence (green lines in Figure 9.10) but it cancels out when the time delay is the same before and after stress



**Figure 9.9** Voltage shift of a SiC-MOSFET due to constant gate bias stress [11].



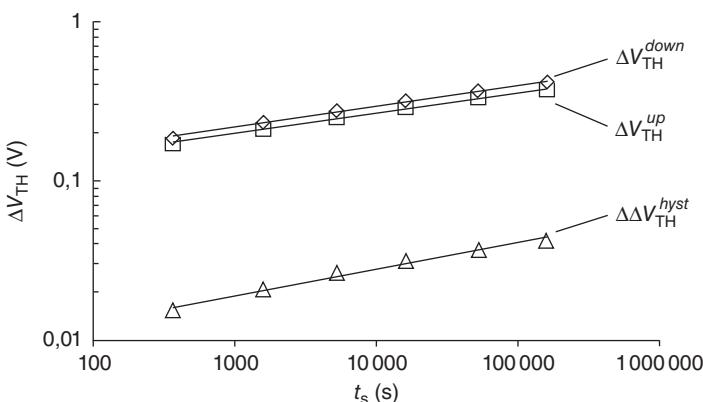
**Figure 9.10** (a) Measurement procedures and (b) their corresponding dependence of the threshold voltage shift on the recovery time [11].

(red line in Figure 9.10). As such, ensuring always the same time delay (it may also be as large as e.g.  $10 \text{ ks} \approx 3 \text{ h}$ ) is sufficient to obtain reproducible voltage shift results.

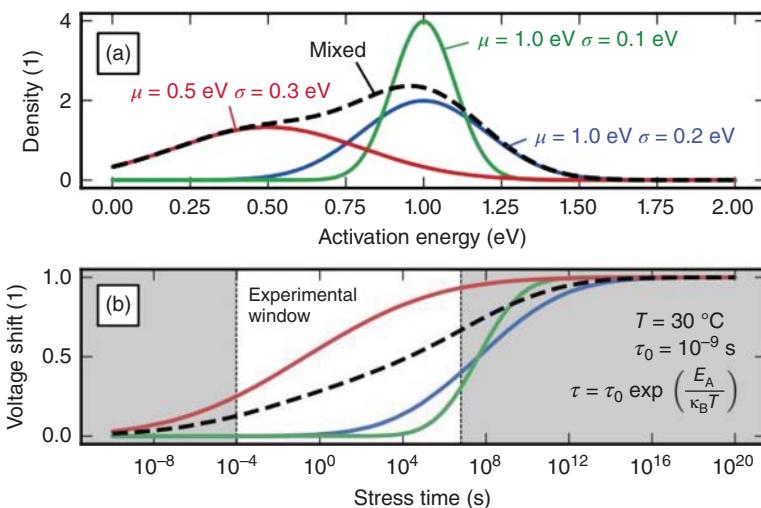
### 9.2.3 Bias Temperature Instability

With the aforementioned preconditioning measurement procedure, the drift of the threshold voltage under positive bias temperature stress (PBTS) or negative bias temperature stress (NBTS) can be cautiously characterized. The positive and negative preconditioning pulses are therefore applied before and after a bias temperature stress (BTS) phase of a certain duration and temperature and give the impact on the  $V_{\text{TH}}$  as well as a possible change of the SH. Figure 9.11 depicts an exemplary drift as a function of stress time. The change of the  $V_{\text{TH}}$  depends approximately logarithmically on the stress time for the given durations and is nearly independent of the preconditioning pulse polarity. The change of the SH is about an order of magnitude smaller.

The apparent logarithmic dependence of the  $\Delta V_{\text{TH}}$  on the stress time is a result of the broad distribution of activation energies of point defect



**Figure 9.11** Drift of the threshold voltage over BTS time.  $\Delta V_{\text{TH}}^{\text{down}}$  denotes the change of  $V_{\text{TH}}$  after a positive preconditioning pulse and  $\Delta V_{\text{TH}}^{\text{up}}$  after a negative one.  $\Delta\Delta V_{\text{TH}}^{\text{hyst}}$  is the change of the SH [2].



**Figure 9.12** (a) Calculated probability density function over activation energy. Green, red, and blue are hypothetical normal distributions which sum up to the black dashed line. (b) The resulting time dependence of the  $V_{\text{TH}}$  shift for the different distributions. Highlighted is the typical experimental window for electrical measurements.

charging/discharging/creation processes in the dielectric at or near the interface to SiC. Figure 9.12 depicts an assumption of the distribution of activation energies and the resulting time dependence of the  $V_{\text{TH}}$  shift. The resulting  $\Delta V_{\text{TH}}$  transients appear logarithmically dependent on the stress time within narrow experimental windows.

To calculate the result of charging processes of individual point defects, a number of physical models are needed. The most basic idea is that a point defect can be in two charge states: either neutral or charged. A defect whose charged state is

positive is called donor-like defect, one with a negative charge state acceptor-like. The second important assumption is that the state of the defect is only dependent on its current state and not any previous states (Markov chain of first order). These two simple assumptions result in an exponential function of the time dependence of the probability of having the defect in one charge state as  $p(t) \propto \exp(-t/\tau)$  [12]. The characteristic time constant  $\tau$  for a Markov process is calculated from the transition rates (probability per unit time) from one charge state to the other. For physical or chemical processes, the time constant  $\tau$  is inversely proportional to the reaction rate constant which quantifies the rate of a given chemical reaction. In our case, the chemical reaction is the possible rearrangement of the amorphous network of Si and oxygen (O) (or potentially other elements) surrounding the point defect in  $\text{SiO}_2$ . Exactly, this rate constant obeys Arrhenius' law and thus the time constant is temperature activated as

$$\tau = \tau_0 e^{\frac{E_A}{k_B T}} \quad (9.2)$$

The measured  $\Delta V_{\text{TH}}$  transient is the result of a superposition of a large number of single exponential functions and the superposition can be easily calculated by summing the individual components. The inverse problem, the identification of the underlying distribution of time constants from the resulting transient is called multi exponential analysis (MEA) and is an important and challenging problem for many different scientific fields [13]. This inverse problem has a unique solution only in the case of zero noise, id est (latin, read as *that is to say*) (i.e.) for real-world measured transient data there is no unique solution [14]. Some parameters of the distribution of time constants have to be assumed and still only an approximation of the distribution can be derived. Important methods to perform MEA can be found in these references [13–18].

The identification of the point defect in the  $\text{SiO}_2$  which causes the bias temperature instability (BTI) cannot be easily performed from  $\Delta V_{\text{TH}}$  transient data alone. Due to the broad distribution of time constants, it is difficult to study the temperature dependence of an individual time constant which would allow an Arrhenius analysis and thus the identification of the activation energy. To identify single defects, the active area of the MOSFET has to be around  $100 \text{ nm} \times 100 \text{ nm}$  such that the impact of a single charge on the drain current is sufficiently large [19]. Such small devices exist for Si technology where the charging/discharging processes have been extensively studied employing time-dependent defect spectroscopy [20, 21]. For SiC, such small devices do not exist yet. But without the basic information of the barrier energy for the defect charging process, it becomes nearly impossible to compare with ab initio calculations of defects in  $\text{SiO}_2$ . For the time being, one has to assume that similar defects are responsible for BTI in both Si- and SiC-based MOSFETs. Further discussion on this topic can be found in Section 9.3.3.

#### 9.2.4 Reduced Channel Electron Mobility

The mobility  $\mu$  of electrons in a semiconductor is the proportionality factor between the electric field and the electron drift velocity. For bulk 4H-SiC, the mobility may

have values between  $10^2$  to  $10^4 \text{ cm}^2/\text{V s}$ , depending on the doping level and the temperature [22]. For all semiconductors, the mobility decreases with increasing impurity concentration (because of increased scattering probabilities [1]) and with increasing temperatures (increased phonon scattering [1]). A typical value for the bulk mobility of 4H-SiC (at room temperature and for a typical doping level of  $10^{17} \text{ cm}^{-3}$ ) is around  $700 \text{ cm}^2/\text{V s}$  [22], measured by employing the Hall effect.

For MOSFETs, the channel electron mobility is usually calculated by fitting the output characteristic of the MOSFET in the linear regime (small  $V_D$ ) employing

$$I_D = \frac{W}{L} \mu_{\text{FET}} C_{\text{ox}} (V_G - V_{\text{TH}}) V_D \quad (9.3)$$

where  $I_D$  is the drain current,  $W$  and  $L$  are the MOSFET channel width and length, respectively,  $\mu_{\text{FET}}$  is the MOSFET channel electron mobility,  $C_{\text{ox}}$  is the oxide capacitance,  $V_G$  is the voltage at the gate,  $V_{\text{TH}}$  is the threshold voltage, and  $V_D$  is the drain voltage. A peculiarity of SiC is a heavily reduced electron mobility in the MOSFET channel, down to values as low as  $10^{-3} \text{ cm}^2/\text{V s}$  [23]. With such low  $\mu_{\text{FET}}$  values, it would be unreasonable to build a power MOSFET because the resulting  $R_{\text{DS,}on}$  would not be competitive with available Si-based transistors (especially insulated gate bipolar transistors [IGBTs]).

The apparent strong reduction of  $\mu_{\text{FET}}$  is only to a tiny part due to a reduction of the actual electron mobility itself [24–26]. In fact, the free electron density  $n_{\text{free}}$  decreases through trapped electrons, which reduces the drain current of the transistor. Since the free electron density is not considered in (9.3) the reduction is caught by  $\mu_{\text{FET}}$  as a fitting parameter. To separate between MOSFET channel mobility and free carrier density, Hall effect measurements are most useful. But also the fitting of the transfer characteristic of the MOSFET under the assumption of a particular energetic distribution of the interface trap density allows to obtain  $n_{\text{free}}$  and  $\mu$  independently [24, 27].

By using an POA after the oxidation (or deposition) of  $\text{SiO}_2$  in nitrogen (N) containing atmospheres, the MOSFET mobility is increased to values ranging from  $10^1$  to  $10^2 \text{ cm}^2/\text{V s}$ . Typical gases for the POA are nitric oxide (NO), nitrous oxide ( $\text{N}_2\text{O}$ ), and ammonia ( $\text{NH}_3$ ), usually mixed with dinitrogen ( $\text{N}_2$ ).  $\text{N}_2$  alone normally does not lead to significant improvements in the MOSFET mobility. Most efficient is usually the annealing in NO at temperatures around  $1150^\circ\text{C}$  [28].

The particular reasons for the remaining reduction of the channel electron mobility beside the effect of the  $n_{\text{free}}$  reduction are still under debate [29]. The decreased mobility values in Hall measurements could be due to a natural reduction of the interaction of channel electrons with acoustic phonons, ionized impurities, and other known physical effects [1]. However, the impact of the mobility change is very small compared to the impact of the  $n_{\text{free}}$  reduction and is thus not of utmost importance. The overall topic of an increased  $R_{\text{DS,}on}$  because of the two effects remains, however, of very high importance, because the channel resistance is the part of the MOSFET where most improvement is possible. Solving this issue would allow to build competitive SiC MOSFETs for the voltage class below approximately 1.2 kV [30].

## 9.3 Microscopic Nature of Electrically Active Traps Near the Interface

The electrical effects mentioned in Section 9.2 all occur due to charging/discharging/creation processes of point defects near the SiC/SiO<sub>2</sub> interface. Here, we give an overview about the research toward the identification of the microscopic composition and nature of these defects. In the following, we will formulate hypotheses for likely defect candidates for each aforementioned electrical effect.

### 9.3.1 The P<sub>bc</sub> Defect and the Subthreshold Sweep Hysteresis

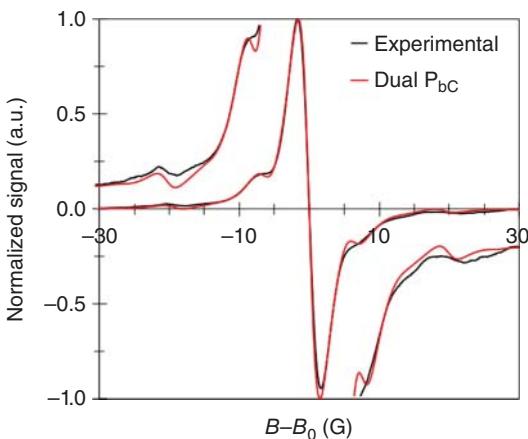
The SH effect in SiC MOSFETs has been summarized in Section 9.2.1. In order to identify the microscopic defect responsible for the SH effect, electron paramagnetic resonance (EPR) experiments have been combined with ab initio density functional theory (DFT) calculations [23, 31].

EPR employs the Zeeman effect: the energy level of an unpaired electron splits in a magnetic field into two levels. If the energy difference between these two levels is exactly matched by electromagnetic radiation, a resonance condition occurs. Because the local magnetic field at a nucleus is also impacted by neighboring nuclei, one can draw conclusions on the structure of the surroundings of the electron (hyperfine interaction). Conventional EPR experiments give information of all paramagnetic centers within a sample. This is naturally a weakness of the method for the investigation of defects in MOSFETs because the SiC/SiO<sub>2</sub> interface region is only a few nm thick compared to the several orders of magnitude larger sample thickness. Furthermore, the method cannot easily be applied to fully fabricated MOSFETs because the metal layers lower the quality factor of the standing electromagnetic wave in the resonator cavity.

Employing electrically detected magnetic resonance (EDMR) instead of EPR can circumvent these problems. Using EDMR, the current through the transistor changes due to the resonance condition and gives a similar defect fingerprint as in an conventional EPR experiment. The signal is, however, only due to carrier recombination centers at the SiC/SiO<sub>2</sub> interface and is insensitive to centers energetically close to the valence or conduction band edges. The method thus gives information on defects responsible for the SH but not those which limit the MOSFET mobility.

As already stated in Section 9.2.1 (and depicted in Figure 9.7), the larger SH effect in trench MOSFET devices compared to planar devices can be attributed to a larger density of interface traps around mid-gap for a-face compared to Si-face. Consistently, also the EDMR signal was generally larger for trench MOSFET devices compared to standard planar devices. This supports the argument that interface traps energetically close to the center of the band gap cause the SH effect.

For full identification of the defect causing the SH effect, a significant increase of the signal-to-noise ratio for EDMR experiments was important to allow for reasonable resolution of the hyperfine side peaks. This could be reached by employing the



**Figure 9.13** Example normalized EDMR spectrum with zoomed in lines for better visibility of the hyperfine side peaks at about  $\pm 7\text{G}$  and  $\pm 20\text{G}$ . The red line is a simulated spectrum for dual-P<sub>bc</sub> [31].

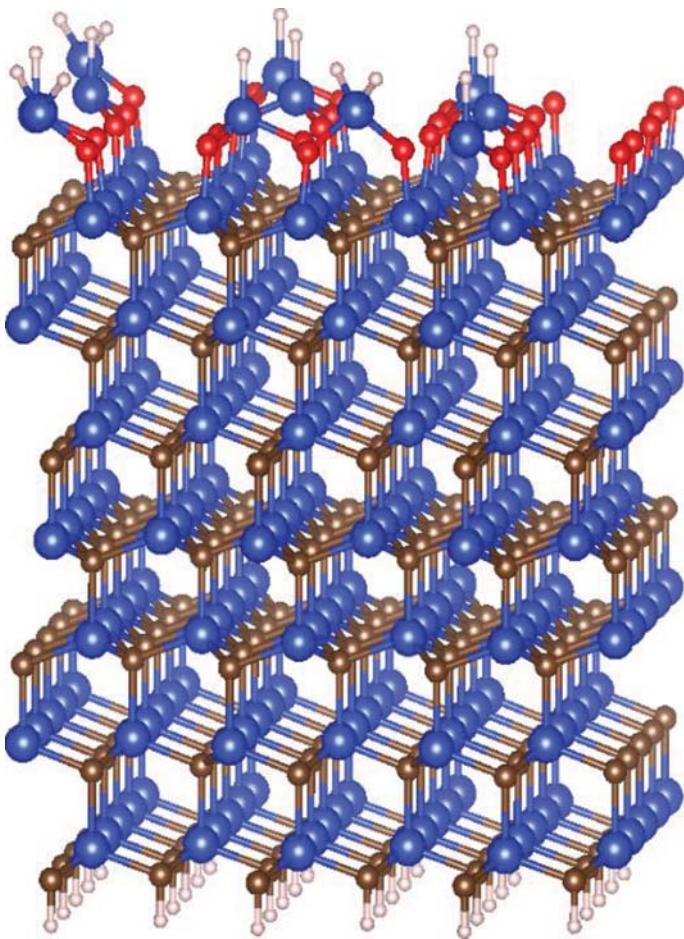
bipolar amplification effect (BAE) [32]. Figure 9.13 gives an example EDMR spectrum of SiC MOSFET with the resolved hyperfine peaks.

The hyperfine peaks are of particular importance because they allow for a direct comparison with DFT calculations. For the identification, several steps were needed. First, a defect-free interface model was designed, as depicted in Figure 9.14. This is possible because in the case of the Si-face of 4H-SiC, there exists a connection scheme for an ideal interface to SiO<sub>2</sub> [33]. Into this model, all possible point defects near the SiC/SiO<sub>2</sub> interface were introduced, including all sorts of vacancies, interstitials, anti-site pairs in SiC, and their variants with neighboring nitrogen atoms. From all these possible defect candidates, a short list was created by removing all defects with unreasonably large formation energy. These remaining defects were investigated in more detail and their average hyperfine splitting was calculated. By calculating the relative intensity of the peaks based on the isotopic abundance of the spin active nuclei, the EDMR spectrum can be calculated and compared to the experimental observation (red vs. black line in Figure 9.13).

The occurrence of the hyperfine side peaks at the same magnetic field value is a very strong indication that the P<sub>bc</sub> defect family [23, 31, 34, 35] is responsible for a recombination current in SiC MOSFETs. However, there is an indication that the type of interface defect visible in EDMR is process dependent, because variants of the defect have been identified, namely the silicon vacancy near the interface [36] and the carbon P<sub>b</sub> center [37]. However, this does not exclude even more defects or other defect types to cause recombination processes at the SiC/SiO<sub>2</sub> interface, since they could be not paramagnetic and thus simply not visible in the EPR experiment.

### 9.3.2 The Intrinsic Electron Trap and the Reduced MOSFET Mobility

A summary about the smaller MOSFET mobility compared to the bulk electron mobility has been given in Section 9.2.4. The majority of the apparent reduction of the MOSFET mobility is a misinterpretation because of the reduced free electron density in the MOSFET channel. Here, we summarize the hypothesis that the microscopic defect causing the large number of trapped electrons close to the channel is

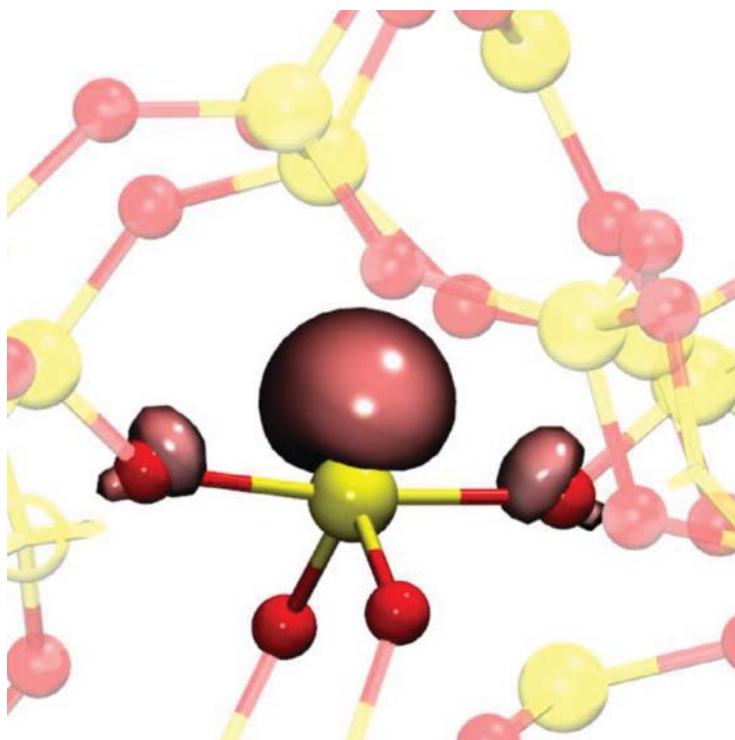


**Figure 9.14** Atomistic model of 4H-SiC with one layer of  $\text{SiO}_2$  on top.

the intrinsic electron trap in amorphous  $\text{SiO}_2$  [38], favored against other defects as e.g. the  $\text{Si}_2\text{C}-\text{O}$  structure [39].

Ab initio calculations of amorphous silica  $\text{SiO}_2$  revealed trapping of an electron in preexisting structural precursors. The precursor sites are characterized by wide (greater than  $130^\circ$ ) O–Si–O angles. These sites can occur randomly distributed in the  $\text{SiO}_2$  network because of distributions of bond angles and lengths in the amorphous crystal, resulting in a density of approximately  $5 \times 10^{19} \text{ cm}^{-3}$ . The calculated energetic trap level is approximately 3.2 eV below the bottom of the conduction band of  $\text{SiO}_2$  [38]. Figure 9.15 shows an example for the spin density upon charge capture of an intrinsic electron trap.

The intrinsic electron trap can be correlated especially with experimental findings which had utilized photon stimulated electron tunneling [40]. Therefore, the energy difference between the trap level and the  $\text{SiO}_2$  conduction band edge was determined by optical excitation of the trapped electrons under an applied electric field. The



**Figure 9.15** Charged intrinsic electron trap with the spin density of the trapped electron (Si atoms yellow, O atoms red).

value for the trap energy level was determined as 2.8 eV. Specifically, the energy level is independent of the underlying semiconductor material (4H-SiC, 6H-SiC, or even Si). This is a strong argument for the intrinsic electron trap, since other defect candidates, like e.g. the Si<sub>2</sub>-C-O structure, involve carbon and are thus very unlikely to occur in Si-SiO<sub>2</sub> structures.

The experimental trap energy level is 2.8 eV and thus smaller than the theoretically suggested value of 3.2 eV. However, calculations also show that the trap energy is significantly smaller for crystalline  $\alpha$ -quartz (2.5 eV). As such, the strained environment for this defect in SiO<sub>2</sub> close to the interface a semiconductor may cause a different energy trap level, besides a possibly increased density [41]. Mind that the conduction band edge of 4H-SiC is 2.7 eV below the conduction band edge of SiO<sub>2</sub> and thus populating the intrinsic electron trap works most efficient for 4H-SiC compared to other SiC poly types or other semiconductors.

### 9.3.3 Point Defect Candidates for BTI

Research concerning bias temperature instability (BTI) in SiC MOSFETs benefits from the research previously performed for Si-based MOSFETs. However, also for Si-based MOSFETs the exact microscopic point defect causing BTI has not yet been

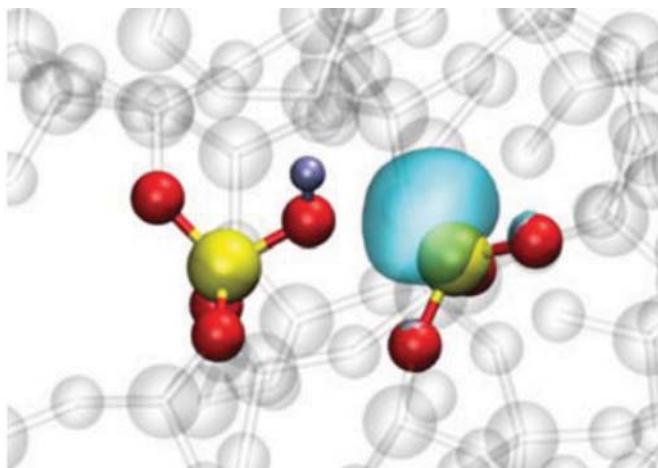
unambiguously identified, but many candidates exist. In Si MOSFETs, the only defect type which is unambiguously created during BTS is the dangling bond on a Si atom at the Si–SiO<sub>2</sub> interface ( $P_b$  center) [42–46]. It becomes most probably created through dissociation of a neutral hydrogen atom passivated dangling bond on a silicon atom at the silicon-silicon dioxide interface ( $P_b$ H complex). The identification was done by performing EDMR measurements before and after BTS.

However, for SiC MOSFETs, the similar defect type  $P_{bc}$  is not changed in its density through NBTS [47]. Even more, the EDMR signal did not change at all despite a very large change of the  $V_{TH}$ , thus indicating that the defects charged or created during NBTS in SiC MOSFETs are not spin dependent. This is again similar to Si MOSFETs where EDMR after NBTS shows only the increase of the  $P_b$  signal, but no other additional defect has been unambiguously identified. Few reports claim signatures of a dangling bond on a silicon atom bonded to three oxygen atoms within the silicon dioxide (E' center) after NBTS [42].

As no direct evidence of the defects created through NBTS appears possible as they could be diamagnetic, alternative approaches have to be employed. For Si MOSFETs, a very promising approach has evolved in recent years by studying the charge state of individual defects. In nanometer-sized devices, the change of the  $V_{TH}$  due to BTS occurs in discrete steps of several millivolt [48]. The step height is a fingerprint of a particular defect in the device because of the lateral distribution of the current through the transistor and the individual impact of a single defect charge state on the overall current [49]. Because of this possibility to identify the response of a single defect on temperature, time, and bias, the time dependent defect spectroscopy (TDDS) can give physical properties of the defects contributing to BTI. These properties, such as the barrier energy for charging/discharging or its charge transition level with respect to the valence and conduction band edges, may then be compared to the results of ab initio calculations employing DFT.

One important property which has been found for defects contributing to BTI in Si MOSFETs is the bistability in every one of the two charge states. This means that there have to exist at least two configurations in e.g. the neutral charge state, where only one of the two configurations allows a transition to the say positive charge state [50]. This property of a defect leads to effects like temporarily activated random telegraph noise (RTN) during the recovery after BTS or the volatility of defects in repeated stress/recovery BTI experiments [51]. Since the bistability of the charge states has been observed consistently in Si-based MOSFETs, possible defect candidates have been screened to have more than two states (as well as a charge transition level close to the center of the SiO<sub>2</sub> band gap) [50]. The remaining candidates are the oxygen vacancy, the hydrogen bridge, and the hydroxyl E'-center [50, 52], where the latter is currently most promising. An example of the defect is given in Figure 9.16.

Considering the dynamics and overall behavior, BTI in SiC MOSFETs is similar to BTI in Si MOSFETs [53]. However, there are a few peculiarities and differences which have to be considered. The bistability criterion does not necessarily need to be important for SiC MOSFETs. This could render the list of possible defects for BTI in SiC MOSFETs much longer compared to Si MOSFETs. As such, it is important to



**Figure 9.16** Example configuration of the hydroxyl E' center in the neutral charge state [52]. Hydrogen, silicon, and oxygen atoms are silver, yellow, and red, respectively.

obtain physical properties of the defects contributing to BTI in SiC MOSFETs additionally to the information given from Si MOSFETs. Nanometer-sized devices are not yet possible with SiC technology, so the response of an ensemble of defects on BTS has to be analyzed (see also Section 9.2.3). The obtained BTI measurement data have to be modeled in a compact framework where the physical defect parameters are calculated individually but the computational effort is kept low by calculating the semiconductor/insulator system macroscopically. Such a simulator has been written and released [54] and has been applied to SiC MOSFETs [9]. The result reveals two electron and one hole trap band close to the conduction and valence band edges of 4H-SiC, respectively. The shallow electron trap band has thereby similar parameters as for Si MOSFETs, suggesting the existence of an electron trap intrinsic to  $\text{SiO}_2$ , just as previously submitted by DFT calculations alone (as described in Section 9.3.2). Given the complexity of deriving physical parameters of an ensemble of defects contributing to BTI, additional research is necessary to identify and eventually remove the defect responsible for  $V_{\text{TH}}$  shifts following BTS.

## 9.4 Conclusions and Outlook

It is obvious that the natural mismatch of the crystal structure between SiC and  $\text{SiO}_2$  will naturally cause many different point defects near the interface of these two materials. Through improved high temperature processes, many of these defects have been completely removed or rendered electrically inactive, because their charge transition levels have been shifted outside the SiC band gap. It is, however, not obvious how these remaining electrically active defects impact the performance and reliability of MOSFET devices which employ the SiC/ $\text{SiO}_2$  interface as the central element for electronic switches.

We think the effect of a hysteresis between the upward- and downward transfer characteristic sweep with negative start gate voltages is due to interface traps, energetically located close to the center of the band gap. A possible defect candidate for this effect is the P<sub>bC</sub>, a dangling bond at a carbon atom directly at the interface. In order to have these interface traps in a defined charge state whenever the transistor is characterized by measuring the threshold voltage, the preconditioning measurement method should be used. Therefore, a preconditioning gate voltage pulse to deep accumulation or inversion is used to have most interface traps either charged positively or neutral, respectively. This allows to be able to study the impact of e.g. BTS with reliable and reproducible measurements. Investigating the instability of SiC MOSFETs due to BTS by using this measurement method reveals a very broad distribution of capture time constants, presumably due to a broad distribution of charging barrier energies of the individual defects. Several point defects may cause BTI in SiC or Si MOSFETs, but recently mostly discussed for Si is the hydroxyl E'-center.

The smaller MOSFET mobility compared to the bulk mobility value of SiC is due to a misinterpretation of the strongly reduced free electron density in the MOSFET channel. The majority of electrons are trapped and thus immobile and do not contribute to the drain current in unpassivated devices. A possible candidate for this effect is the intrinsic electron trap in SiO<sub>2</sub>, wide angle O–Si–O bonds occurring naturally in the amorphous SiO<sub>2</sub> and eventually more frequent near the SiC/SiO<sub>2</sub> interface because of localized strain.

The summary gives only a few candidate point defects for different electrical effects in SiC MOSFETs. It cannot be a definitive answer on the nature of interface traps, as e.g. other recombination centers could be more prominent but are simply not paramagnetic. Also, even though BTI is comparable between Si and SiC MOSFETs, the defects responsible for BTI in SiC-based MOSFETs could be different from those in Si devices because of possibly carbon-related defects. As such, further research is needed to fully clarify the role of point defects near the SiC/SiO<sub>2</sub> interface for the operation of SiC-based MOSFETs.

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# 10

## Epitaxial Graphene on Silicon Carbide as a Tailorable Metal–Semiconductor Interface

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### 10.1 Introduction

The discovery of monolayer graphene growth on silicon carbide (SiC) [1–4] provides a unique opportunity to rediscover the very fundamental concept of a metal–semiconductor interface [5, 6] providing an accurately defined structure with atomic precision. This chapter summarizes recent experiments and technological concepts that benefit from this exceptional monolithic material system. We start with a review of the formation of the graphene layer and its tailorabile interface, and we continue by discussing the basic electronic functionality, which can immediately be used to define diodes, transistors, and electronic circuits. These devices open up opportunities to study the very fundamentals of semiconductor textbook physics in a new context, in particular, with unprecedented access to the high-frequency limit of electronic information processing. Key to these experiments is the optical transparency of graphene electrodes. This can further be exploited for solid-state quantum technology with SiC.

### 10.2 Epitaxial Graphene as a Metal

Graphene is an atomically thin material [7], the single layer version of the well-known material graphite. After its discovery, graphene attracted a lot of attention (including the Nobel prize 2010 in physics) because of its unusual quantum mechanical structure that roots in the honeycomb  $sp^2$  lattice and its symmetry. Its electronic bands merge conically in six points at the edge of the Brillouin zone (Dirac cones) and, hence, graphene has no electronic bandgap, but is a (semi-) metal. A figure of merit in semiconductor technology, the charge-carrier mobility reached unprecedented values up to  $10^6 \text{ cm}^2/\text{Vs}$  in graphene flakes, which raised wishful fantasies with regard to this novel electronic material [8, 9].

For this manuscript, the special properties of the Dirac electrons (“relativistic electrons”) and the high mobility are unimportant, but we focus instead on the

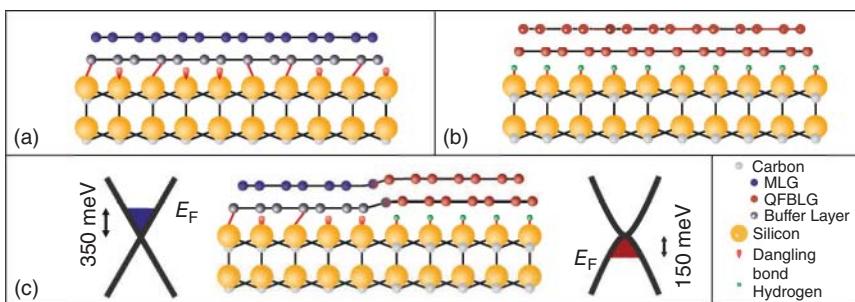
simple fact that graphene is an atomically thin metal. Different to standard 3D metals, which are charge neutral in the bulk and can have excess charge only at their surfaces, graphene, being a surface-only material, can be entirely electron charged (n-type) or hole charged (p-type), but remains metallic.

## 10.3 Fabrication and Structuring of Epitaxial Graphene

### 10.3.1 Epitaxial Growth by Thermal Decomposition

It is known since the early days of SiC material research that heating SiC leads to a decomposition of the surface and the formation of graphitic structures [10, 11], which means  $sp^2$  hybridized carbon. With the advent of graphene as an interesting atomically thin and truly two-dimensional material that is uniquely formed of  $sp^2$  carbon [7, 12], an interest was raised to fabricate graphene on SiC single crystal wafers, both on their carbon face (C-face) [13, 14] and on their silicon face (Si-face) [3, 15]. While the results on the C-face are highly interesting, but did not result in a controlled monolayer growth, it turned out that the Si-face is perfectly suited for this purpose. A recent review is given in Norimatsu et al. [4]. When SiC(0001) is heated up to approximately 1100 °C under ultrahigh vacuum conditions, a decent local graphene monolayer growth can be observed, however, with rather rough surfaces that contain graphene islands, multilayer graphitic areas, voids, and structural defects [15, 16]. The problem under these conditions is that the silicon loss is fast and kinetically driven, but the remaining material remains far from annealing conditions and cannot reconfigure structurally. For the latter, higher annealing temperatures are required, but the silicon loss has to be balanced. The solution turned out to be the use of inert gas at ambient pressure during annealing, in particular argon (Ar). Under these conditions, the thermal decomposition of the SiC surface is slowed down kinetically and can be performed at approximately 1700 °C, which meets nicely the annealing conditions of SiC. The result is a nearly intact SiC bulk crystal with a sharp and atomically flat interface to a monolayer (or few layers) material that consists entirely of carbon on macroscopic or even wafer scales [3, 17]. The first grown layer is an atomically thin carbon layer that looks in top view like the honeycomb lattice of graphene.

A closer look, however, reveals that it has still out-of-plane bonds to the underlying Si atoms of the SiC crystal (among those Si atoms, there are numerous sites that are not saturated with carbon and provide dangling bonds, cf. Figure 10.1a). The carbon atoms of this so-called buffer layer have, hence, both  $sp^2$  and  $sp^3$  contributions [19]. As a consequence, the  $\pi$  electronic band typical for graphene is missing and this layer is therefore electronically insulating [15]. On top of this buffer layer, under appropriate conditions, a second layer is formed which is the desired pure  $sp^2$  graphene layer. Its electronic band structure has been determined by angular-resolved photo electron spectroscopy (ARPES) [15]. Note that this graphene layer is not charge neutral; because of the electron-donating interface it is charged with a typical charge density of  $10^{13} \text{ cm}^{-2}$ , which corresponds to a Fermi energy of  $\Delta E_F \approx 350 \text{ meV}$  above the



**Figure 10.1** Scheme of epitaxial graphene on SiC. (a) Epitaxial graphene on SiC as obtained from thermal decomposition. The graphene layer (blue) is formed on top of an insulating carbon buffer layer (black). This material is negatively charged (n-type) and is termed monolayer graphene (MLG). (b) By high-temperature hydrogen treatment, the buffer layer is converted into a graphene layer, such that quasi-freestanding bilayer graphene (QFBLG) resides on the substrate. This material is positively charged (p-type). (c) Employing milder intercalation conditions, it is possible to fabricate both materials side by side in a closed sheet. This junction links n-type MLG with p-type QFBLG without interruption of the carbon layers. Values for  $E_F$  are deduced from Hall measurements under ambient conditions.

Dirac point (see Figure 10.1c left). The charge carrier mobility at room temperature is typically limited to  $\mu_e = 1000 \text{ cm}^2/\text{V s}$ . The mobility rises toward low temperatures to about  $2000 \text{ cm}^2/\text{V s}$ , which corresponds to mean free paths of approximately 50 nm [3]. This limitation can be traced back to line defects in the graphene plane, more precisely stacking faults with respect to the underlying buffer layer [20, 21]. The temperature dependence of the mobility stems from electron–phonon interaction with particularly strong influence of the buffer layer phonons [22]. Significantly higher values of the mobility can be achieved when the open surface of graphene is chemically doped such that the charge carrier density approaches zero [23]. The described monolayer graphene (MLG) is atomically flat on atomically flat substrate terraces, which may be up to 3  $\mu\text{m}$  wide and >100  $\mu\text{m}$  long on nominally on-axis substrates. They are interrupted by substrate steps. There, interestingly, the graphene grows uninterruptedly like a carpet over the steps, with an additional graphene layer in vicinity of the step such that there, effectively, bilayers or even multilayers are observed [3]. Fabricating MLG means, therefore, creating a continuous layer of large area epitaxial graphene, which includes bilayer contributions of about 20%.

This fabrication is predominantly temperature controlled. The temperature can be chosen such that (nearly) exclusively buffer layer is produced. At somewhat higher temperatures, MLG is formed, and at even higher temperatures, bilayer graphene (BLG) can be fabricated. It should be mentioned, however, that the MLG process is most reliable; buffer layer growth is more critically dependent on a subtle choice of growth parameters and initial surface morphology.

### 10.3.2 Intercalation

Starting from MLG, the application of hydrogen at temperatures around 900 °C provides an interesting tool to modify the material. Initially applied to terminate the

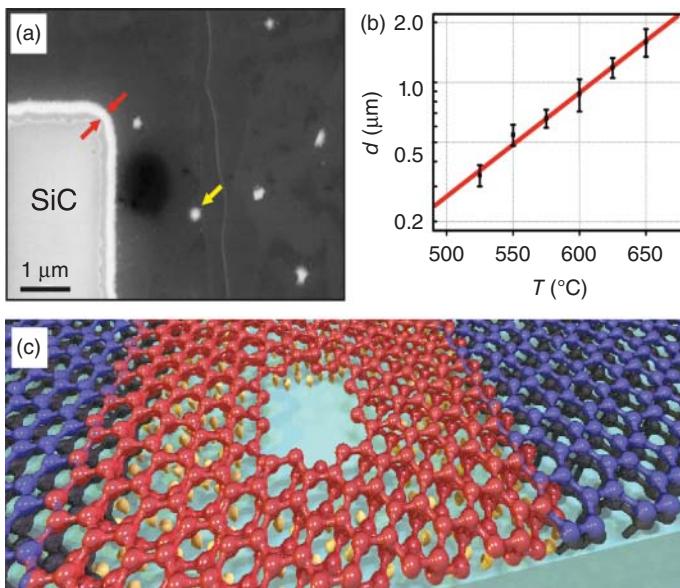
dangling bonds, it turned out that hydrogen also cuts the covalent bonds between SiC and the buffer layer [24, 25]. The result is the conversion of the electrically inactive buffer layer into a truly  $sp^2$  graphene layer, while additional graphene layers remain unchanged (see Figure 10.1b). This leads to the following conversion scheme: buffer layer only is converted to quasi-freestanding monolayer graphene (QFMLG), MLG is converted to quasi-freestanding bilayer graphene (QFBLG), and so on. The terminology of *quasi-freestanding* indicates that the interaction with the substrate is substantially released. In particular, the charge carrier mobility of the quasi-freestanding material is independent of the temperature; the electron–phonon scattering is suppressed [25]. Also, the negative charge induced by the buffer layer is removed; however, another mechanism becomes dominant. The static electric dipole moment of the hexagonal SiC crystal (absence of inversion symmetry) requires a positive termination of the surface and, therefore, charges quasi-freestanding graphene species with a hole density in the range of  $(10^{12}\text{--}10^{13})\text{ cm}^{-2}$  [26], a typical value for the Fermi energy under ambient conditions is  $\Delta E_F \approx -150\text{ meV}$  below the charge-neutrality point (cf. Figure 10.1c right). Note that intercalation of this interface has turned out to be a rich research area in itself (see e.g. [27, 28]). Recently, even 2D metallic sheets have been stabilized as an interface layer [29, 30]. In the course of this paper, we consider only the “simplest” hydrogen intercalation, with which, however, striking effects can be demonstrated.

### 10.3.3 Structuring of Epitaxial Graphene Layers and Partial Intercalation

Starting with a continuous large-area graphene layer, device fabrication requires lateral structuring. An obvious strategy is to cover graphene with resists, in particular polymethyl methacrylate (PMMA) or photo resists, which is then patterned by electron beam or optical lithography. Unwanted graphene areas are subsequently removed by oxygen plasma etching at mild conditions. This technique has previously been applied to exfoliated graphene [31, 32] and epitaxial graphene on the C-face of SiC [14] and leaves the charge carrier mobility mainly unaffected. The resist materials can be nearly completely removed. However, even little resist residues can be problematic for specific applications if the graphene surface is key to functionality (e.g. sensors). Strategies to remove contaminations are described by Algara-Siller et al. [33] and Yager et al. [34].

While the lateral patterning of the graphene sheet is common to all graphene materials (e.g. exfoliated graphene, chemical vapor deposition [CVD] graphene [35]), a specialty of epitaxial graphene is the opportunity to tailor the epitaxial interface by intercalation. This intercalation can even be performed locally such that the electronic properties of a continuous graphene layer can laterally be varied (see Figure 10.1c). Conceptually, the intercalation process, which on the wafer scale was thermodynamically driven, must be controlled kinetically.

For this purpose, edges or voids are defined by lithography techniques [18, 36]. Under relatively mild conditions (approximately  $500^\circ\text{C}$ ), hydrogen cannot diffuse through the closed layer, but creeps underneath graphene from the predefined



**Figure 10.2** Partial intercalation of epitaxial graphene. (a) Scanning electron micrograph of a graphene edge exposed to hydrogen ( $530\text{ }^{\circ}\text{C}$  for 30 min). The bright strip along the edge (indicated by red arrows) corresponds to locally intercalated graphene. The spots in the closed graphene areas (yellow arrow) indicate unintended conversion at pinholes. (b) Measurement of the intercalation width  $d$  as a function of temperature  $T$  for 90 minutes exposure time. An exponential dependence is observed indicating a temperature-activated process. (c) Artist's view of alternating n-type and p-type graphene stripes: the red layer indicates p-type QFBLG (hydrogen termination of the substrate in yellow). The blue layer represents n-type MLG with the buffer layer (black) underneath. Source: Reprinted with minor adaptions from Sorger et al. 2015 [18], license: CC BY 3.0.

edges (see Figure 10.2a). The intercalation depth is then temperature controlled; application time is less critical (see Figure 10.2b). This technique allows for side-by-side fabrication of MLG and QFBLG on the very same chip and even within one continuous graphene sheet. Note that this offers the opportunity of graphene p-n junctions (p-type QFBLG and n-type MLG; sketched in Figures 10.2c and 10.1c), which differ, however, from semiconductor p-n junctions because graphene provides no electronic bandgap. Thus, graphene p-n junctions are essentially metallic with linear  $I$ - $V$  characteristics.

## 10.4 Epitaxial Graphene as Tailorable Metal/Semiconductor Contact

In general, a metal/semiconductor contact forms a space-charge region, which originates from the different work functions of the metal and the semiconductor. As a consequence, a Schottky barrier is formed [6] providing nonlinear current–voltage characteristics through the interface. In the case of an n-type semiconductor, the Schottky barrier vanishes only if the metal's work function is smaller than that of the

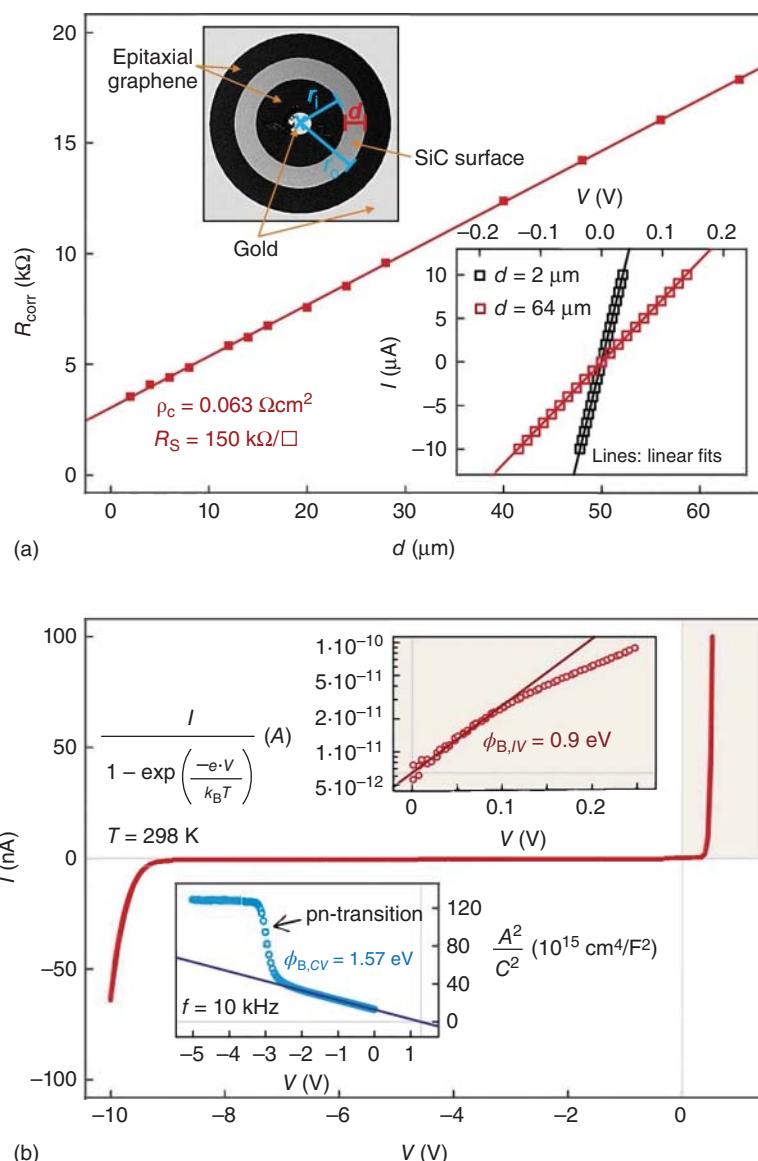
semiconductor. This is the textbook case of a flat-band ohmic contact with linear  $I$ – $V$  characteristics. The typical work function of SiC, which consists of the electron affinity ( $\chi_{\text{4H-SiC}} = (3.4\text{--}3.6)\text{ eV}$  or  $\chi_{\text{6H-SiC}} = (3.85\text{--}4.0)\text{ eV}$  [37–39]) and the Fermi energy  $\Delta E_F = E_C - E_F$  (typical values  $\approx 0.1\text{ eV}$ ), is small. As a consequence, no flat-band ohmic metal/SiC contact is known (Schottky barrier heights of typical metal/SiC contacts range between 1.0 and 1.8 eV [40]).

As outlined earlier, graphene essentially behaves like a metal due to the absence of a bandgap. It turns out that epitaxial graphene being the combination of graphene, SiC and their common interface behaves very similarly to the metal/semiconductor textbook case. The fact that the metal is only atomically thin does not provide a conceptual change. The interaction between graphene and SiC is now controlled by the interface layer that has been described above as buffer layer plus dangling bonds (as illustrated in Figure 10.1a). It turns out that its properties determine the band alignment through Fermi level pinning and can be purposefully controlled by intercalation.

#### 10.4.1 Ohmic Contacts

As-grown epitaxial graphene on n-type 6H-SiC(0001), i.e. MLG, provides an excellent ohmic contact. This is an astonishing observation that is depicted in Figure 10.3a. Even when comparing it with technologically relevant ohmic contacts [41, 42], MLG outperforms those. Whereas the use of bulk metals for ohmic contacts always requires high contact doping of the semiconductor and sophisticated recipes including annealing, the ohmic contact with MLG is close to the flatband case. This becomes particularly evident at low semiconductor doping concentrations, where nickel (Ni) or other metals always result in rectifying Schottky contacts, whereas MLG/SiC remains nicely ohmic (see Figure 10.3a). This remarkable fact is determined by the atomically thin interface layer between graphene and SiC (see Figure 10.1a). The buffer layer and the dangling bonds jointly provide a rich density of electronic interface states, which results in the well-known effect of Fermi-level pinning [6] with three consequences: (i) Strong electron doping of the MLG layer [3]. (ii) Consequently, a reduced work function for MLG. (iii) Screening of MLG from vertical electric fields originating in the semiconductor [43]. An important consequence of this situation is that the charge density in MLG sticks to  $n = 10^{13}\text{ cm}^{-2}$  as mentioned previously, independent of temperature, doping of the semiconductor, electric fields in the semiconductor, etc. The second important consequence is the robust ohmic behavior on n-type 6H-SiC. A closer look by photoelectron spectroscopy reveals a small Schottky barrier height of  $\Phi_B = 0.3\text{ eV}$  of the MLG/6H-SiC contact [44], which does not influence the electrical characteristics.

For the technologically more relevant polytype 4H-SiC with its larger bandgap and thus smaller electron affinity, the band alignment is less pronounced resulting in a slightly higher Schottky barrier height of  $\Phi_B = 0.6\text{ eV}$  [44]. This leads to deviations from perfect ohmic characteristics at low doping levels. In turn, little contact doping is sufficient to recover the ohmic MLG/4H-SiC characteristics. The described properties have been studied in depth using the transfer length method (TLM) [45].



**Figure 10.3** Epitaxial graphene as ohmic and Schottky contacts to SiC. (a) MLG ohmic contact: transfer length method (TLM) measurement using a circular contact geometry (see scanning electron micrograph). MLG has been covered with gold to reduce series resistances. Despite a very low doping concentration of the SiC ( $[N] = 1 \times 10^{15} \text{ cm}^{-3}$ ), the  $I$ - $V$  characteristics of the MLG contacts are perfectly ohmic (see inset). (b) QFBLG Schottky contact:  $I$ - $V$  characteristics of a QFBLG/SiC junction, which clearly displays rectification. A Schottky barrier height  $\Phi_{B,V} = 0.9 \text{ eV}$  is extracted from the forward characteristics (shaded area, same data shown in upper inset).  $\Phi_{B,CV} = 1.57 \text{ eV}$  is extracted from  $C$ - $V$  data (lower inset) on the same device. Source: Reprinted from Hertel et al. 2012 [36], license: CC BY-NC-SA 3.0.

**Table 10.1** Comparison of specific contact resistances  $\rho_c$ : MLG ohmic contacts vs. conventional metal ohmic contacts.

Polytype	Doping ( $\text{cm}^{-3}$ )	Contacts	$\rho_c (\Omega \text{ cm}^2)$	References
6H-SiC	$1.0 \times 10^{15}$	MLG	$6.3 \times 10^{-2}$	[45]
	$1.0 \times 10^{15}$	Ni	Not ohmic	[45]
	$4.5 \times 10^{17}$	Ni	$1.7 \times 10^{-4}$	[46]
	$7.4 \times 10^{18}$	Ni	$3.6 \times 10^{-5}$	[42]
	$(7\text{--}9) \times 10^{18}$	Ni	$5.0 \times 10^{-6}$	[47]
	$1.0 \times 10^{19}$	MLG	$5.9 \times 10^{-6}$	[45]
	$4.5 \times 10^{20}$	Ni	$1.0 \times 10^{-6}$	[48]
4H-SiC	$4.2 \times 10^{18}$	Ni	$6.4 \times 10^{-5}$	[49]
	$7 \times 10^{18}$	Ni	$4.8 \times 10^{-5}$	[50]
	$1.6 \times 10^{19}$	MLG	$5.6 \times 10^{-5}$	[45]
	$1.6 \times 10^{19}$	Ni	$4.1 \times 10^{-4}$	[45]
	$1 \times 10^{20}$	Ni	$5.3 \times 10^{-4}$	[51]

The results are summarized in Table 10.1 and underscore the advantageous properties of MLG in terms of ohmic contact performance.

#### 10.4.2 Schottky Contacts

It was already mentioned that the modification of the interface via intercalation has significant impact on the charging of the graphene sheet. In particular, hydrogen intercalation leads to a positive charge density in the graphene layer, cf. Figure 10.1c. This indicates that the band alignment between graphene and SiC strongly changes after intercalation [52]. A measurement of the Schottky barrier height can be performed by photoelectron spectroscopy, leading to a value of at least 1.5 eV [18]. Electrical measurements on large-scale QFBLG/SiC contacts indeed prove the rectifying diode behavior (Figure 10.3b) [36]. However, a closer analysis (inset in Figure 10.3b) rather indicates a smaller Schottky barrier height of 0.9 eV, which is substantially lower than the X-ray photoelectron spectroscopy (XPS) result. To resolve this discrepancy, it is instructive to determine the Schottky barrier height via capacitance–voltage ( $C$ – $V$ ) measurements on the very same junction, from which  $\Phi_B \approx 1.5$  eV is obtained again [36]. The difference originates from the fact that both  $C$ – $V$  and XPS techniques probe the area-averaged barrier height, whereas the  $I$ – $V$  analysis is sensitive to the lowest barrier height in the contact region, even if it is only in a small spot (pin hole).

The origin of these pinholes can be investigated more systematically by using nanocharacterization techniques. At first, QFBLG/SiC Schottky contacts were fabricated with a large span of contact diameters from 200  $\mu\text{m}$  down to 0.5  $\mu\text{m}$ , the smallest being electrically contacted using the tip of a conductive atomic force

microscope (C-AFM). It was observed that the Schottky barrier height increases with decreasing contact diameter and finally saturates at  $\Phi_B \approx 1.5$  eV for the smallest contacts. This can be better understood by C-AFM current maps and their immediate comparison with the topology. It turns out that the Schottky barrier height lowering occurs at the step edges of the SiC substrate terraces. Hence, these line defects provide the pinholes. When they are avoided, the Schottky diodes display the Schottky barrier height of 1.5 eV even in  $I-V$  analyses [53]. Note that the terrace widths strongly depend on the off-cut angle of the SiC substrate [53] and the step-bunching effect, which occurs under certain annealing conditions [54].

## 10.5 Monolithic Epitaxial Graphene Electronic Devices and Circuits

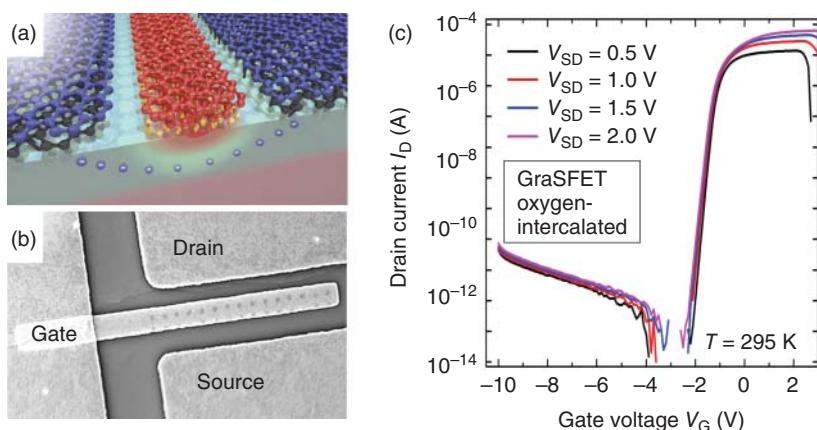
### 10.5.1 Discrete Epitaxial Graphene Devices

Provided with graphene ohmic and Schottky contacts, and further with recipes for their side-by-side fabrication on the very same wafer, resistors, diodes, as well as transistors are feasible.

We focus here on the transistors, which are of the metal-semiconductor field-effect transistor (MESFET) type. The metal is fully substituted by epitaxial graphene; we term this transistor, therefore, epitaxial graphene-silicon carbide field-effect transistor (GraSFET) [36, 55]. Notably, all metallic contacts can be established by epitaxial graphene; the gate contact being of the Schottky type (QFBLG/SiC) and the source and drain contacts being of the ohmic type (MLG/SiC). As all components are carved out of a single root SiC material, we termed the overall devices *monolithic*.

The situation is graphically sketched in Figure 10.4a. Blue graphene layers indicate MLG with the underlying (black) buffer layer; the red double layer corresponds to QFBLG with hydrogen atoms (yellow) saturating SiC's dangling bonds. The SiC consists of a layer structure: the top layer (light blue) is n-type and conductive, whereas the underlying layer is either semi-insulating or p-type to suppress unwanted current pathways through the substrate. Current can flow from the source contact (left MLG contact) via the n-type SiC layer to the drain contact (right MLG contact). The current flow can be controlled by the gate contact (QFBLG contact in the middle) with its underlying space-charge region. The depth/width of the latter is enlarged by driving the Schottky contact in reverse direction (negative voltage applied to the gate). When the n-type SiC channel is fully depleted, i.e. all current paths are squeezed off, the transistor is fully switched off. In turn, when releasing the negative voltage, the channel is opened allowing for an electrical current from source to drain.

Figure 10.4b displays a scanning electron microscopy (SEM) image of an actual implementation of a GraSFET. We now describe the manufacturing processes. It starts with high-purity semi-insulating on-axis 4H-SiC into which nitrogen is implanted to define the conductive transistor channel volume (n-type well). Subsequently, MLG is grown, a step that includes the post-implantation annealing. In the next step, partial intercalation of the gate contact is prepared by defining voids in the



**Figure 10.4** Monolithic epitaxial graphene/SiC transistor (GraSFET). (a) An artist's view of a monolithic epitaxial graphene transistor. Current can flow from MLG (blue hexagonal grid with underlying bufferlayer in black; source electrode) through the n-doped SiC (light blue) to a second MLG electrode (drain). The current path is confined by a non-conducting layer underneath (purple). The voltage applied to the Schottky gate provided by QFBLG (red) opens or closes the channel. (b) Scanning electron micrograph of an improved GraSFET implementation. The conductive transistor channel is defined by nitrogen implantation between source and drain contacts. To reduce series resistances, contact areas have received an additional contact implant and MLG is covered by Ti/Au. Note that the graphene gate finger has intentionally been placed onto a single substrate terrace, which reduces gate leakage currents. (c) Transfer characteristics of a normally-on oxygen-intercalated GraSFET with improved device design. A large on/off ratio of  $10^8$  with a subthreshold swing of  $110\text{ mV/dec}$  is achieved. Source: (a) Reprinted from Hertel et al. 2014 [56], with the permission of WILEY-VCH, ©2014 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. (b) Reprinted with minor adaptions from S Hertel 2016 dissertation, urn:nbn:de:bvb:29-opus4-72024, license: CC BY-SA 3.0.

appropriate graphene area using electron beam lithography and subsequent oxygen plasma etching. When exposing the sample to hydrogen under mild conditions, partial intercalation takes place only in the predefined area around the voids. The residue of this void pattern can be seen in Figure 10.4b (gate finger). Subsequently, source, drain, and gate contacts are defined by electron beam lithography and metal deposition of gold (Au) or titanium/gold (Ti/Au) (cf. also [57]). The metal layer serves as an etch mask for the final oxygen plasma etch. This ensures that the graphene electrodes to SiC are carved out congruently with the metal layer. Hence, in contrast to the artist's view, all graphene areas with their rather high series resistances are additionally covered with metal. This reduces the sheet resistances of the leads from  $\text{k}\Omega/\square$  down to below  $\Omega/\square$  and, thus, improves the transistor performance.

Further improvement can be achieved when substituting the hydrogen intercalation by oxygen intercalation in water vapor [58], which again allows partial

intercalation when using mild conditions. The oxygen intercalation is more stable. Moreover, recent long-term experiments with hydrogen-intercalated QFBLG have revealed that hydrogen atoms are replaced by oxygen when storing the sample in ambient air for several months [58].

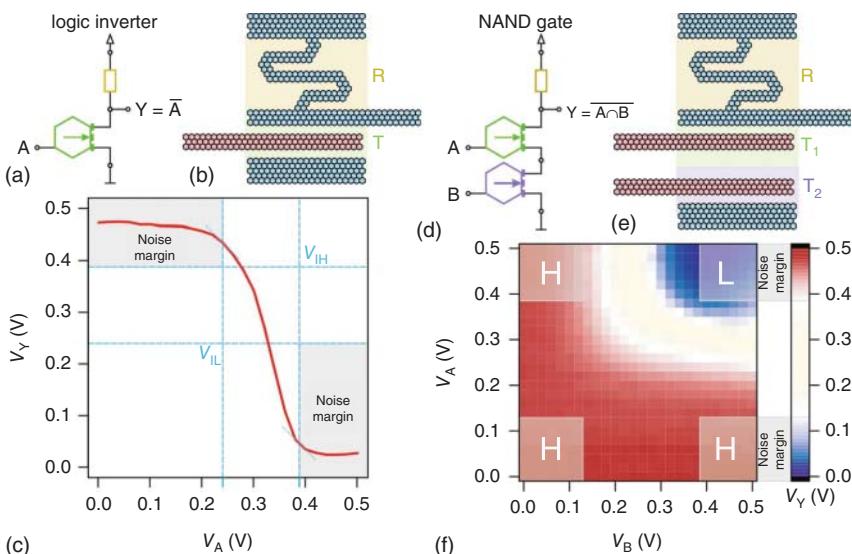
The transfer characteristics obtained with such a device for various source-drain voltages  $V_{SD}$  at room temperature are shown in Figure 10.4c. They display a remarkable on-off ratio up to  $10^8$  with a subthreshold swing of 110 mV/dec. The threshold voltage can be engineered: the implantation depth of the n-type well defines the zero-gate voltage channel thickness, which may be chosen normally-on or normally-off. Here we display a normally-on case with a threshold voltage of  $\approx -1$  V. The on-state current obtained for this small test device is in the order of 100  $\mu$ A; it can be extended by adjusting geometry and channel doping. GraSFET devices are able to operate at high temperatures [58]; the temperature limit is rather determined by the increase of leakage current than by material instabilities. QFBLG (including the intercalation) is stable at least up to 800 °C; this is particularly valid for oxygen-intercalated QFBLG [58].

### 10.5.2 Monolithic Integrated Circuits

Having resistors, diodes, transistors, and interconnects at hand, integrated analog and digital circuits with monolithic epitaxial graphene devices become feasible. Here we demonstrate two very elementary logic components in the simplest realization (resistor-transistor-logic).

Figure 10.5a displays the circuit of a simple logic inverter; the chip layout is sketched in Figure 10.5b. All components are monolithically made of epitaxial graphene (partially hydrogen intercalated). The channel of the GraSFET is chosen to be normally-off with a threshold voltage around 0.25 V. The circuit was operated with a supply voltage of 0.5 V. The logic input is denoted as A and the logic output as Y. Figure 10.5c presents the logic signal transfer characteristics of this device, which shows nicely the inverter operation. The output voltage lies perfectly within the noise margin ensuring stable operation of subsequent logic components.

Another important device is the NAND gate. With a NAND gate at hand, a full logic becomes possible according to de Morgan's theorem [59]. A demonstrator of a NAND gate can easily be achieved by extending the described inverter circuit with a second gate contact in the GraSFET (see Figure 10.5d,e). Figure 10.5f displays the corresponding measurement obtained on such a device. The input voltages  $V_A$  and  $V_B$  are plotted on the vertical and horizontal axes, respectively, while the output voltage  $V_Y$  is color coded. The NAND logic can immediately be seen: the output becomes low only if both inputs are high at the same time. The noise margins are indicated as rectangles in the plot; again, the output voltages lie perfectly within the noise margins ensuring stable logic operation. These findings on a single inverter and NAND gate demonstrate that the GraSFET architecture is suited to build up any logic circuit.



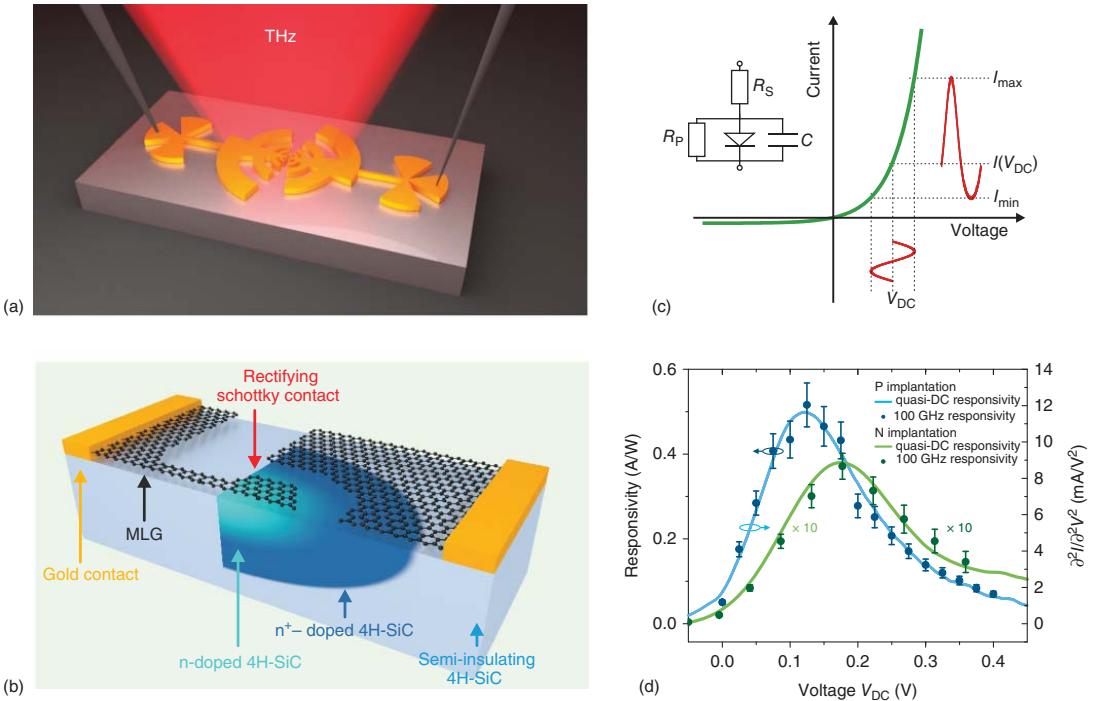
**Figure 10.5** Monolithic integrated logic circuits. Logic inverter: circuit (a) and schematic implementation (b) of an inverter built in transistor-resistor logic by a monolithic epitaxial graphene transistor together with a graphene resistor (blue hexagons indicate MLG, red hexagons indicate QFBLG). (c) Voltage transfer characteristics of the inverter showing output voltages clearly within the noise margins. NAND gate: circuit (d) and schematic implementation (e) of a NAND gate; the circuit is similar to the logic inverter, but the GraSFET is equipped with a double gate connected to the NAND inputs A and B. (f) Color-coded output voltage as a function of the two input voltages. NAND function is visible with output voltages well within the noise margins. Source: Reprinted from Hertel et al. 2014 [56], with the permission of WILEY-VCH, ©2014 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

## 10.6 Novel Experiments on Light–Matter Interaction Enabled by Epitaxial Graphene

### 10.6.1 High-Frequency Operation and Ultimate Speed Limits of Schottky Diodes

We now guide our attention to an elementary process in electronics that is rectification by a diode. Common wisdom tells that the speed of Schottky diodes is governed by  $RC$  limitations of their parasitic environment. Little, however, is known about intrinsic limitations of Schottky diodes for timescales faster than the  $RC$  limit. It turns out that epitaxial graphene Schottky diodes are an interesting prototype for the investigation of such very fundamental speed limits of Schottky rectification [60].

Notably, the metallic (graphene) layer is only one atom thick. We start the description with experiments in the THz spectral range ( $\gtrsim 100$  GHz). THz radiation is coupled via logarithmic periodic antennae (Figure 10.6a) to a Schottky diode, which is fabricated similar to the abovementioned procedures and schematically displayed in Figure 10.6b. Here, Schottky and ohmic contacts are defined side by side both using MLG on 4H-SiC(0001) with its rather low Schottky barrier height; the ohmic



**Figure 10.6** Detection of THz radiation with epitaxial graphene/SiC Schottky diodes. (a) The Schottky diode is connected in the center of a logarithmic periodic antenna. The THz radiation is transformed by the antenna into a THz voltage  $V_{AC}$ , which is rectified by the device. The resulting time-averaged current  $\langle I(t) \rangle$  is proportional to the square of the field amplitude of the THz radiation. (b) Close-up of the Schottky diode. MLG forms the metal of the Schottky contact, the semiconductor is n-doped SiC. By increasing the doping level, an ohmic contact between the two materials is achieved. (c) Schematic of rectification in a Schottky diode and its equivalent circuit: an incident voltage  $V_{AC}$  superimposed on bias voltage  $V_{DC}$  translates via the curvature into an asymmetric AC current response that increases the time-averaged (DC) current. (d) Responsivities calculated from quasi-static  $I-V$  characteristics (solid lines) and THz responsivities (at 100 GHz, symbols) as a function of the bias voltage obtained on two Schottky diodes with phosphorous (P) or nitrogen (N) doping, respectively. Remarkably, the quasi-DC responsivity and the THz responsivity are barely distinguishable. Source: Reprinted with minor adaptions from Schlecht et al. 2019 [60], license: CC BY 4.0.

contact differs only by a significant contact implantation. We first present a DC electrical characterization (Figure 10.6c), which corresponds to a typical textbook  $I$ – $V$  characteristic of a diode with a non-vanishing serial resistance. The equivalent circuit is depicted in the inset. Now, THz radiation is applied to the diode from a homebuilt cw-THz source based on n-i-pn-i-p superlattice photomixers [61] via the antennae. As the resulting oscillating voltage  $V_{\text{AC}}$  is rather small, it provides an oscillation around the operating point  $V_{\text{DC}}$ . In forward direction with its strongly nonlinear characteristics, an oscillation in  $V_{\text{AC}}$  results in an oscillating current  $I_{\text{AC}}$  that is non-sinusoidal. Hence, a Taylor expansion immediately results in higher-order corrections. In particular, the time-averaged signal of  $I(t)$  deviates from  $I_{\text{DC}}$  such that

$$\langle I(t) \rangle = I_{\text{DC}} + \frac{1}{2} \frac{\text{d}^2 I}{\text{d}V^2} \hat{V}_{\text{AC}}^2 + \dots$$

As a consequence, the response to the THz radiation (quantified by its power) can simply be measured as DC current with a proportionality constant that is termed responsivity. Figure 10.6d shows the central result of this setup for n-type SiC which is doped by either phosphorous (P) or nitrogen (N). With increasing bias voltage  $V_{\text{DC}}$ , the responsivity increases first exponentially (due to the curvature of the exponential increase of  $I(V)$ ). It has a maximum at a few hundred millielectronvolt and is then reduced because the series resistance suppresses the curvature. While the responsivity of the device is competitive with state-of-the-art Schottky diode detectors, the more interesting aspect is the comparison of the quasi-DC responsivity (i.e. the second derivative of the static  $I$ – $V$  characteristics) and 100 GHz responsivity: their shape is barely distinguishable. From this observation, we conclude that the epitaxial graphene Schottky diode behaves nearly identically on extremely different time scales: between 1 Hz for the quasi-DC characterization and the 100 GHz, the physics apparently does not change despite 11 orders of magnitude differing frequencies. In this setup, however, the  $RC$  limitation is still important: the cutoff frequency is at 580 GHz.

To access even faster time scales, different strategies must be chosen that entirely avoid  $RC$  limitations. We chose a femtosecond excitation with a laser. Photoelectrons are charge-neutral excitations within graphene that rapidly establish non-equilibrium to the diode without  $RC$  delays in electrical leads. Again, epitaxial graphene Schottky diodes turn out to be the ideal choice for such experiments. Not only they withstand highest laser intensities because of the outstanding robustness of both graphene and SiC but also SiC is entirely transparent while graphene absorbs about 2.3% of the incoming light pulse [62].

For the experiment a photodiode with a Schottky barrier height of 0.8 eV is chosen (cf. Figure 10.6b). It is operated in reverse bias conditions and illuminated with ultrashort pulses (5.5 fs) perpendicular to the graphene plane. Via internal photoemission, which is considered to be prompt, high-energy electrons are generated, which have now two options: either they tunnel through the barrier (prompt internal photoemission, PIPE) or they exchange energy with other photoelectrons, which leads to an increased electronic temperature after the pulse. As a consequence of the latter, there are electrons at even higher energies that can travel over the barrier

(photothermionic current, PTI). The measured quantity is the overall photocurrent, which consists of both PIPE and PTI electrons. When the laser power is enhanced, the ratio of PIPE and PTI rates with their characteristic power dependencies can be identified.

As it turns out, an even more meaningful quantity is the saturation absorption. When the laser power is increasing, the photocurrent increases as well, but only up to the point where optical saturation is reached. At this point, there are so many excited electrons filling the limited electronic graphene density of states that additional photons cannot excite further electrons (Pauli blocking). This is a remarkable regime that can only be reached because of the extreme robustness of epitaxial graphene and is indeed detected in our experiments. It turns out experimentally that the saturation absorption of the photocurrent depends on the bias applied to the junction. This guides the attention to a counteracting mechanism: subsequent to photoexcitation, there is a time scale after which a hot electron is extracted from the graphene plane toward SiC, the charge transfer time  $\tau_{ct}$ . The shorter  $\tau_{ct}$ , the more laser power is required to saturate the electronic excitation. Hence, the bias voltage controls via  $\tau_{ct}$  the saturation absorption process. From a detailed numerical analysis of the photocurrent as a function of laser power and bias voltage across the diode (including PIPE, PTI and saturation absorption) meaningful timescales for  $\tau_{ct}$  can be extracted. It yields  $\tau_{ct} \approx (300 \pm 200)$  as (attoseconds), which is the fastest time ever observed for electrons that are transferred from one material to another. Hence, with ultrafast optical excitations, a Schottky diode can resolve timescales faster than femtoseconds, i.e. Petahertz [63].

### 10.6.2 Transparent Electrical Access to SiC for Novel Quantum Technology Applications

In recent years, SiC has been identified as a promising material for quantum technology applications such as quantum sensors and single photon sources required for quantum communication and quantum cryptography [64–67]. Key elements are optically excitable and luminescent point defects that are often termed color centers. They are similar to single atoms regarding their quantum mechanical properties, but they are contained in a well manageable solid host material. Most experiments in this novel field, which brings together quantum optics, solid-state physics, and material sciences, have been performed on the NV center in diamond (see e.g. [68–70]). Compared to diamond with its technological shortcomings, SiC has significant advantages like a mature process technology and large-scale wafer availability. Most importantly, various luminescent point defects in SiC have been identified with excellent properties for quantum applications, and recipes have been developed for their fabrication [71–75].

Since point defects in a solid host material are subject to interactions with the crystal environment, the detailed properties of individual defects vary even though they are nominally of the same type. On the other hand, precise spectral matching is required when two or more color centers shall be coupled for quantum communication [76]. As a consequence, a handle is needed for fine-tuning the spectral

properties of individual color centers into resonance. Stark tuning is a promising strategy because electrical fields can be generated locally using electrodes in the vicinity of the defects, which need to be spectrally fine-tuned [77].

Here, SiC inherently brings along epitaxial graphene with the unprecedentedly useful properties of being an atomically flat and one-atom thick transparent metal [62] in epitaxial registry to the SiC surface. These properties are of great importance because luminescent defects are typically read out by optical means, i.e. they should be located surface-near and not be obscured by other materials like metal electrodes or surface contamination. We recently demonstrated the use of epitaxial graphene electrodes for Stark tuning spectral lines of the silicon vacancy defect  $V_{Si}$  in 4H-SiC, which were created between and underneath the electrodes [78]. Employing the transparent properties of epitaxial graphene contacts, it was possible to observe spectral fine-tuning or line splitting in symmetry-conserving axial electric fields or symmetry-breaking basal electric fields, respectively. This allows for both Stark effect analysis of defect symmetries [79] and spectral matching of several remote single-photon sources paving the way for integrated quantum technology.

## 10.7 Conclusion

Graphene that grows out of SiC(0001) provides an unprecedented material system. Graphene in many aspects behaves like a standard metal but is atomically thin, ultrarobust, and optically nearly fully transparent. Different to bulk metals, the full graphene sheet can be charged either with electrons or holes not only by gating (which is not considered here) but also even more interestingly by defining via intercalation the epitaxial interface to SiC with atomistic control. In turn, this interface influences the electronic properties of the underlying SiC as well. Epitaxial graphene and SiC thus provide a monolithic metal/semiconductor system with atomic precision. This is not only very elegant but also extremely powerful: epitaxial graphene/SiC Schottky contacts and ohmic contacts can be prepared side by side and functionality up to the level of logic inverters and NAND gates is demonstrated. Epitaxial graphene/SiC Schottky diodes show unchanged operation even at 100 GHz. Hence, we see SiC as an upcoming material for applications in the THz spectral range. Further, relying on the extreme robustness of the combined material system, experiments under extreme conditions can be carried out. For example, extreme ultrashort laser pulses can be used to explore charge transfer in a diode on the (sub-) femtosecond time scale. Finally, SiC provides opportunities as a quantum technology platform. Here, epitaxial graphene electrodes can solve the problem of compensating even finest spectral differences of luminescent point-like quantum objects.

We foresee a bright future for SiC and epitaxial graphene. This unique material system paves the way for many future applications well beyond pure electronic functionality.

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# 11

## Device Processing Chain and Processing SiC in a Foundry Environment

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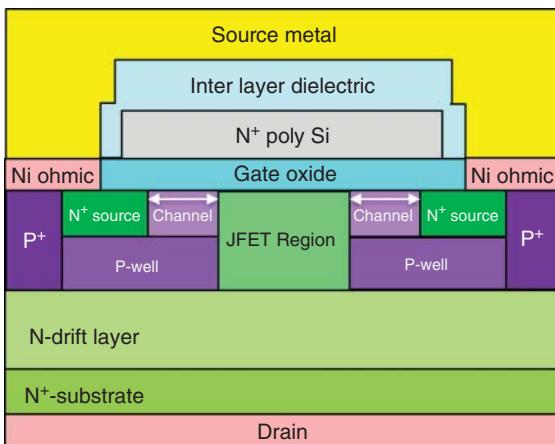
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### 11.1 Introduction

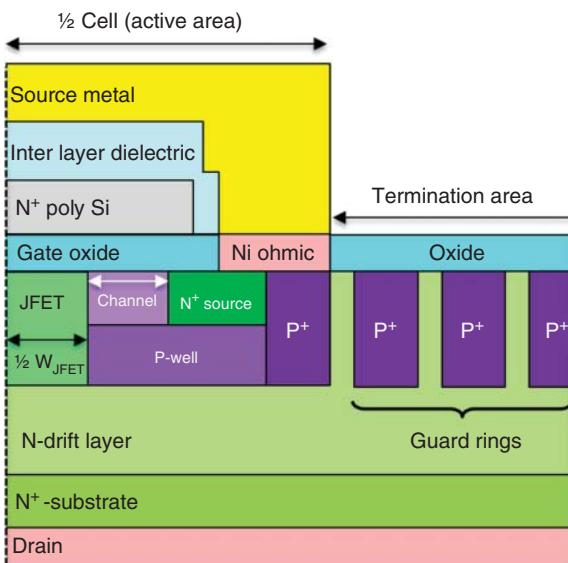
Silicon carbide (SiC) metal–oxide semiconductor field-effect transistors (MOSFETs) became commercially available in January 2011 to satisfy the demand of a higher voltage, lower on-resistance, and faster device. Since then, the availability of larger substrates, lower epitaxial defect density, mature process technology, higher demand by the electric vehicle, renewable market and the growth of commercial foundries have helped to put the SiC technology on a rapid growth curve. This chapter describes the fabrication process for a SiC vertical power DMOSFET. The process flow is meant to provide a starting point for existing 150–200 mm Si foundries which are rapidly becoming obsolete and wish to add another 10–15 years to their productive life. The cost of SiC power MOSFETs will reduce in time due to increase in volume by commercial foundries and reduction of prices for substrate and epitaxial layers. This will create a healthy growth curve for SiC technology for the next 20–30 years.

### 11.2 DMOSFET Structure

Silicon carbide DMOSFET is used as a vehicle to describe the process integration in SiC technology. Other devices such as Schottky diode will use a sub-set of these steps. A cross-sectional view of a vertical power DMOSFET is shown in Figure 11.1. This name comes from the Si technology where both P-well and N<sup>+</sup> source are formed by diffusing p-type and n-type impurities through the open areas in the mask (diffused MOSFET). Although SiC technology uses double implantation instead of diffusion process as discussed later, this name is still used for the technology. DMOSFETs include two main areas: active and termination, as shown in Figure 11.2.



**Figure 11.1** Cross-sectional view of a vertical power DMOSFET cell.



**Figure 11.2** A cross-sectional view of a vertical power DMOSFET including active and termination areas.

The operation of an n-channel DMOSFET is based on applying a positive voltage to the gate. This results in formation of an inversion layer (n-type) in the P-well close to the SiO<sub>2</sub>/SiC interface. By applying a positive voltage to the drain, the electrons can move from the source through this channel, passing through the junction gate field-effect transistor (JFET) region (sandwiched between two P-wells), the N-drift layer and collected by the drain.

In the active area, all DMOSFET cells are in parallel and connected to each other by overlayer metallization. It should be noted that different cell geometries can be utilized for the DMOSFETs such as linear, square, hexagonal, and orthogonal [1, 2]. Figure 11.3 shows a top view and cross-sectional view of three linear cells in the active area.



**Figure 11.3** (a) Top-view and (b) cross-sectional view of three linear cells in the active area.

Different types of terminations such as guard rings (GRs) or junction termination extensions (JTEs) or combinations of these can be utilized for these devices. The GRs have an advantage over the JTEs with respect to reduced number of ion implantation steps. The GRs can be formed along with the P<sup>+</sup> formation with the same mask and implantation.

## 11.3 Process Integration of SiC MOSFETs

SiC DMOSFET processing includes several main steps such as dry etching, ion implantation, implant activation anneal, thermal oxidation, surface passivation, poly-Si deposition, metallization, and polyimide coating. In this section, we first provide an overview of the process integration of SiC DMOSFET. This section is adapted from [3]. Then, all the unit steps are discussed further in Sections 11.3.1–11.3.9.

Figure 11.4 shows a cross-sectional view of a nominal 1.7 kV SiC vertical DMOSFET. All the doping concentrations and thicknesses of this structure have been carefully simulated utilizing 2D simulator Silvaco Atlas at the Ohio State University. The last P<sup>+</sup> region at the periphery of the device is needed to be wider in order to provide enough space for gate runner. The gate runner is connected to the gate pad not shown in Figure 11.4.

Figure 11.5 shows a mask layout of a 1.7 kV 4H-SiC DMOSFET, including 46 GRs for termination of the device, which gradually reduce the electric field for a stable breakdown voltage. Each GR has a width of 2 μm, and a gap between each GR is 0.8 μm. The source and gate pads are used for wire bonding in the packaging step. The channel stop ring is made by N<sup>+</sup> implantation and forms along with the N<sup>+</sup> source with the same mask. This ring is used to terminate any shallow depletion layers formed near the surface and thus to eliminate leakage paths. It stops the electric field from extending up to the edge of the chip. The source and gate pads are used

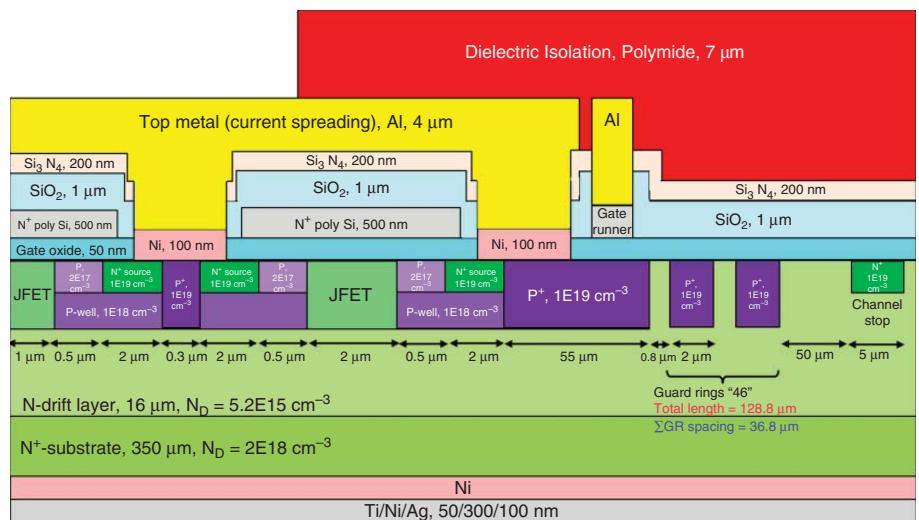
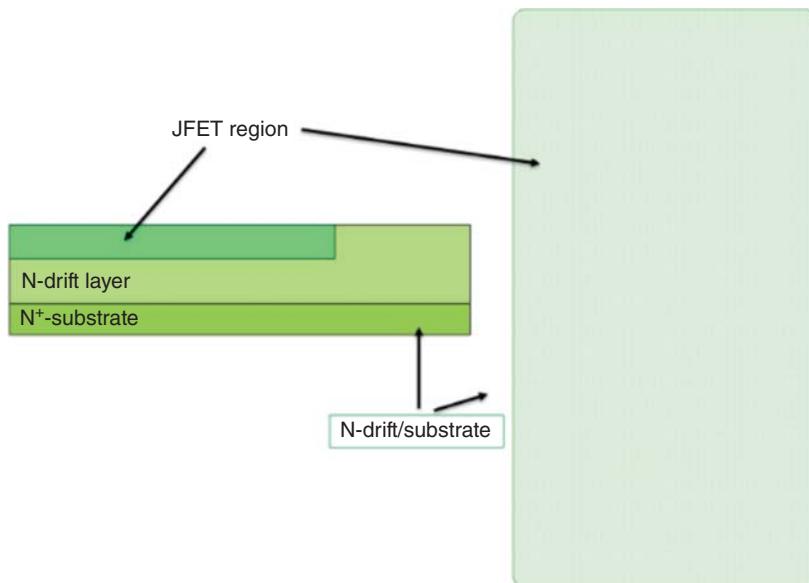
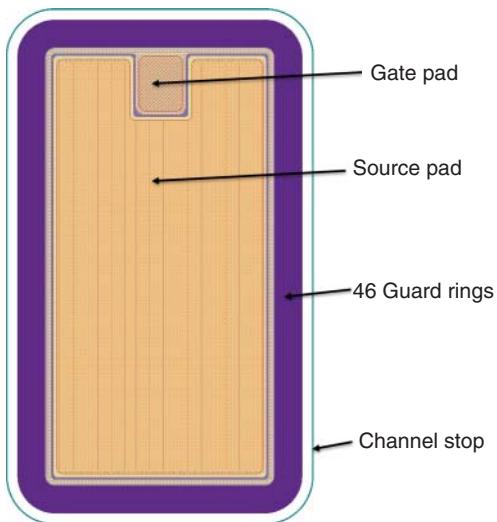


Figure 11.4 A cross-sectional view of 1.7 kV SiC vertical power DMOSFET.

**Figure 11.5** A top-view of a vertical power DMOSFET.

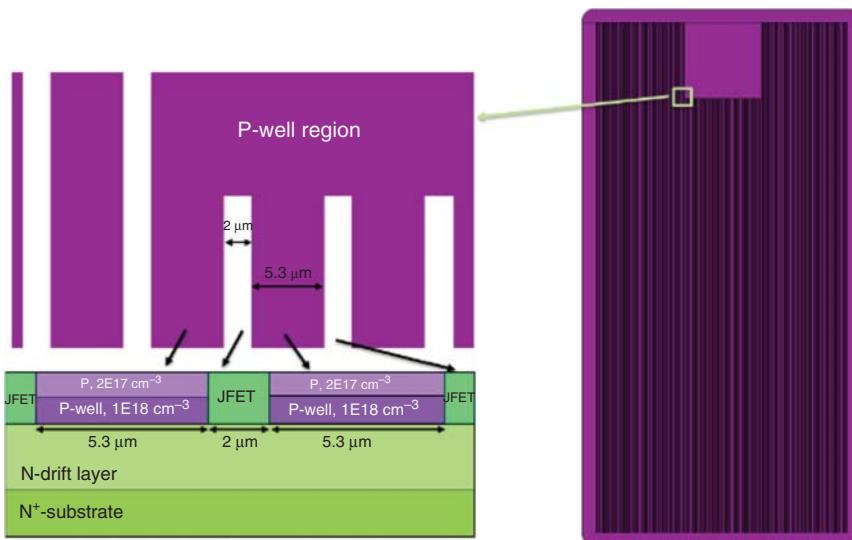


**Figure 11.6** (Right) Mask #2: JFET mask and (left) a cross-sectional view of the wafer including the JFET region within the drift layer.

for wire bonding in the packaging step. Ten masks are needed for the fabrication of this MOSFET.

The first mask step is to create alignment marks by dry etching. Different structures are designed for these marks based on the lithography tool utilized in the clean room.

Figure 11.6 shows Mask #2 for forming an n-type JFET region within the drift layer. Nitrogen (N) implantation with several energies is performed at room

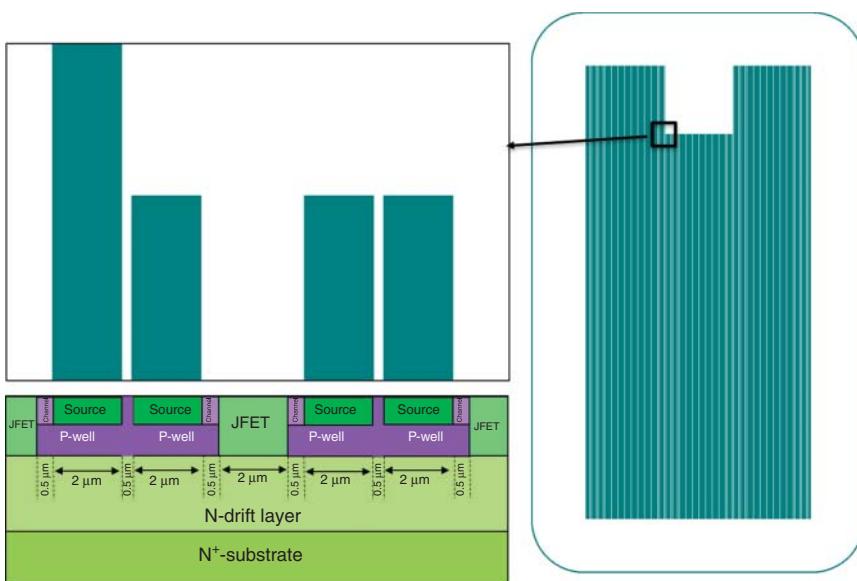


**Figure 11.7** Mask #3: P-well mask along with a cross-sectional view of the wafer (bottom left).

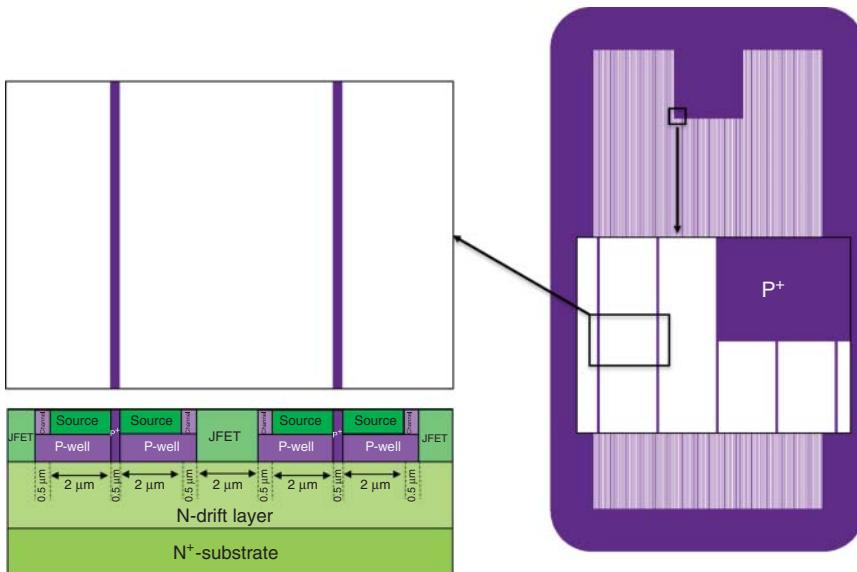
temperature (since the dose is below  $10^{15} \text{ cm}^{-2}$ ) with a photoresist masking layer (see Section 11.3.3). Aluminum (Al) implantation with several energies at high temperature ( $\sim 600^\circ\text{C}$ ) with an oxide mask is utilized for forming the P-well (Mask #3) as shown in Figure 11.7. Woongje Sung et al. reported how two different channels (accumulation vs. inversion modes) can be formed by the P-well implants, which result in different channel mobilities as well as threshold voltages [4].

Similarly, N and Al series implants at high temperature ( $\sim 600^\circ\text{C}$ ) are used for forming the N<sup>+</sup> source (Mask #4) and P<sup>+</sup> (Mask #5), respectively (see Figures 11.8 and 11.9). It should be noted that the channel stop and all the GRs are also made at the same time with Mask #4 and Mask #5, respectively. To prevent electric field crowding at the corners, all corners at the periphery of a high-voltage device are rounded. As a rule of thumb (confirmed by simulations), the radius of the first corner is set to be three times the thickness of the drift layer (see Figure 11.10). Figure 11.11 shows all the masks together for making JFET, P-well, N<sup>+</sup> source, and P<sup>+</sup> in the drift layer. However, a high-temperature annealing process is required to electrically activate all implanted dopants. A capping layer is generally used to reduce surface roughness during the activation annealing. A graphite-cap layer on the surface can be formed by coating the wafer by a suitable photoresist followed by high-temperature bake as shown in Figure 11.12. Then, activation annealing is done in Ar ambient at temperatures around 1600–1700 °C for 10–30 minutes. After the activation anneal process, the capping layer is removed by ashing in O<sub>2</sub> plasma.

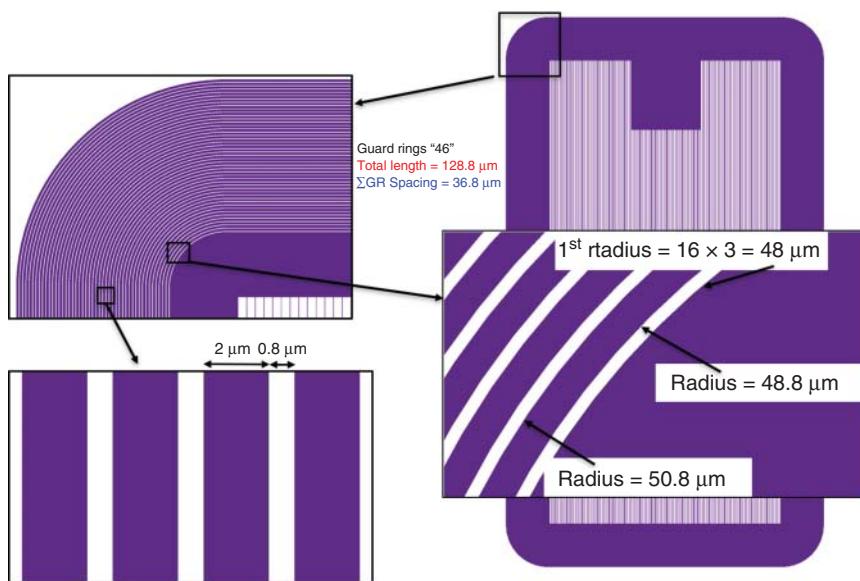
To clean the surface after ion implantation followed by high-temperature annealing, sacrificial oxidation is performed by a thermally grown oxide layer followed by removal with HF acid. Growth of a high-quality SiO<sub>2</sub> gate oxide layer (40–50 nm) followed by post-oxide annealing (POA) with Ar and NO to reduce fixed oxide



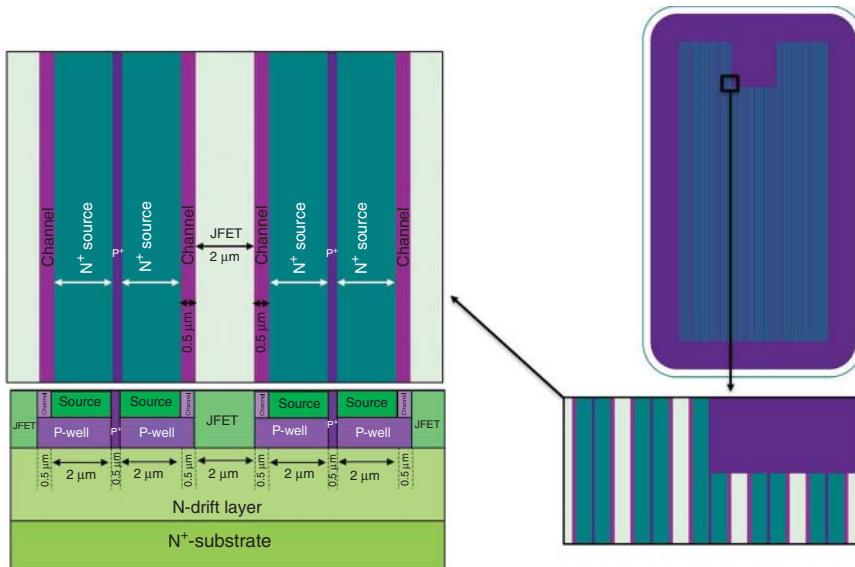
**Figure 11.8** Mask #4:  $N^+$  source mask along with a cross-sectional view of the wafer (bottom left).



**Figure 11.9** Mask #5:  $P^+$  mask along with a cross-sectional view of the wafer (bottom left).



**Figure 11.10** Guard rings in the Mask #5.



**Figure 11.11** All masks #2 to #5 together for forming JFET, P-well, N<sup>+</sup> source, and P<sup>+</sup> in the drift layer by ion implantation.

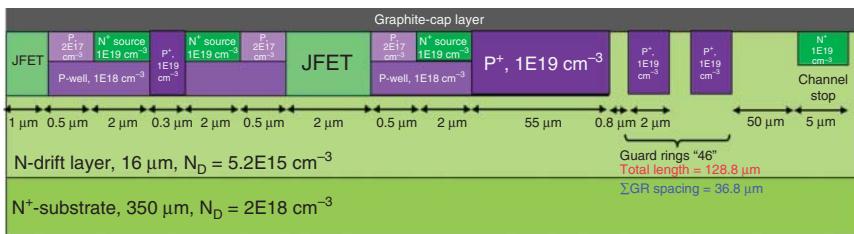


Figure 11.12 Formation of a graphite-cap layer used for activation anneal.

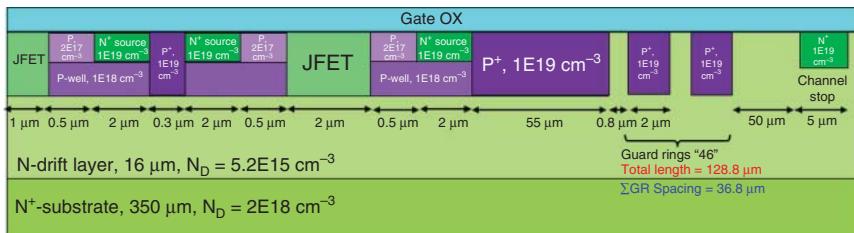


Figure 11.13 Gate oxide growing on the surface.

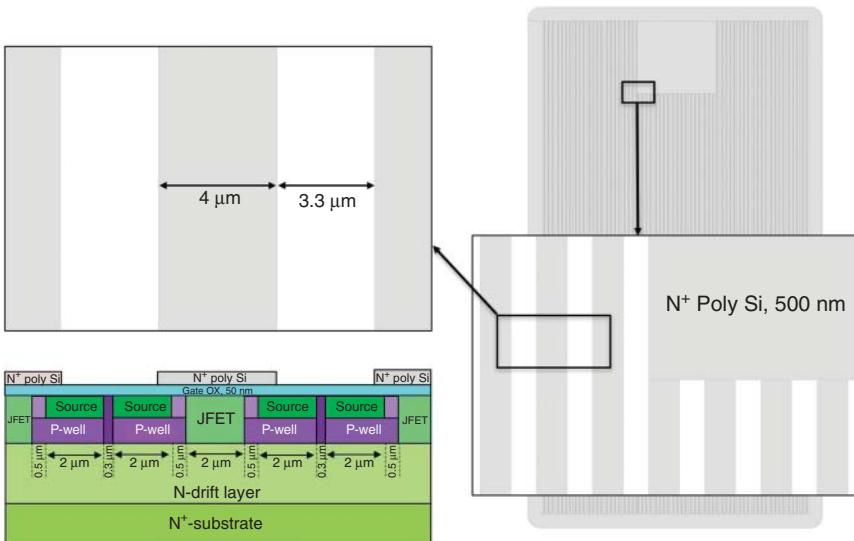
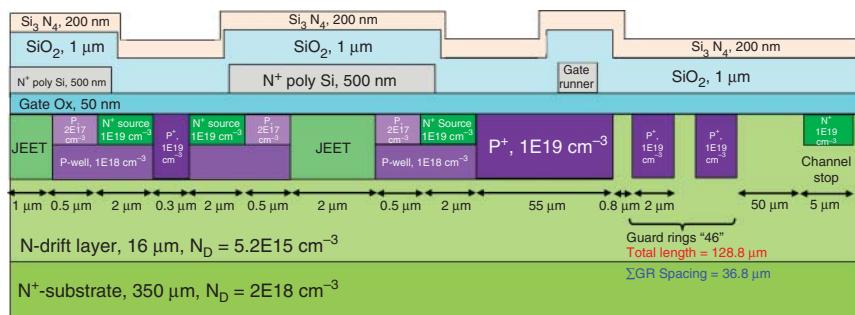


Figure 11.14 Mask #6: gate poly for forming the polysilicon on the gate oxide.

charges and interface state density are critical steps to achieving high channel mobility (see Figure 11.13).

A polysilicon layer ( $\sim 500 \text{ nm}$ ) is deposited by low-pressure chemical vapor deposition (LPCVD). It is doped by phosphorus to obtain n-type polysilicon over the gate oxide. Then, Mask #6 Gate Poly is used to dry etch the polysilicon as shown in Figure 11.14.



**Figure 11.15** Stack of oxide and nitride layer deposition.

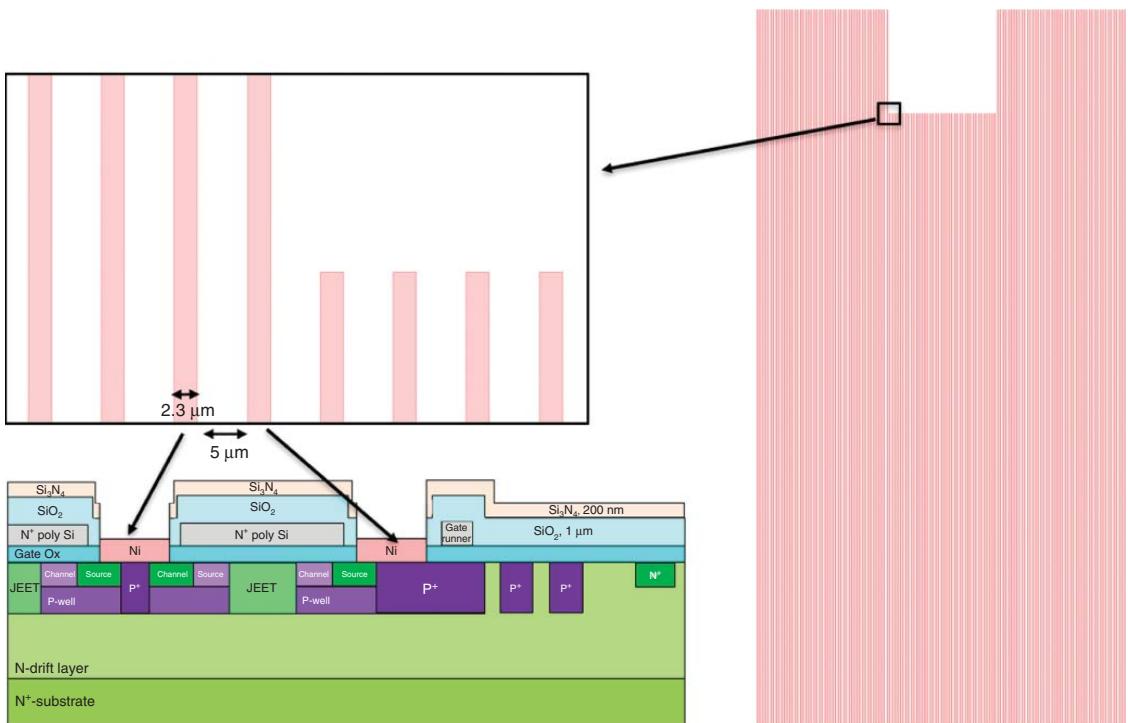
Stacked layers of  $\text{SiO}_2/\text{Si}_3\text{N}_4$  are then deposited as passivation and moisture barriers (see Figure 11.15). The deposited  $\text{SiO}_2$  layer is generally porous and should be densified by wet oxidation. Then, Mask #7 (Ohmic metal) is utilized to open windows over the  $\text{N}^+$  source and  $\text{P}^+$  by dry etching the passivation stack (see Figure 11.16). A 100-nm Ni deposition followed by first step anneal at a temperature of about  $600^\circ\text{C}$  is performed in a rapid thermal anneal (RTA) equipment to make at least one phase of nickel silicide  $\text{Ni}_x\text{Si}_y$  [5]. The unreacted Ni over the oxide is then easily removed by wet etching with the Piranha solvent. Then, the second step RTA anneal at  $>950^\circ\text{C}$  for  $>1$  minute in  $\text{N}_2$  ambient is performed to form the low-resistivity ohmic contacts.

Figure 11.17 shows both Masks #6 and 7 Gate Poly and Ohmic Metal, respectively. It shows an overlap of the gate poly over the source determined by the photolithography resolution. The overlap is necessary to ensure that the gate poly can entirely cover the channel length. There is also a gap of 0.5  $\mu\text{m}$  between gate poly and ohmic contact to  $\text{N}^+$  source and  $\text{P}^+$  body contact which ensures that there is no short between the gate and the source.

An ohmic metal is needed on the backside of the wafer for having a low resistivity contact to the drain. It can be done by Ni deposition on the backside. However, the native oxide on the backside should be removed by wet-dry etching before Ni deposition. Ni is deposited on the backside of the wafer followed by high-temperature annealing at  $950^\circ\text{C}$  for one minutes in  $\text{N}_2$  ambient to form the low-resistivity ohmic contact (see Figure 11.18).

Figure 11.19 shows Mask #8 Gate Runner used for oxide opening (via) by dry etching for the gate pad area and over the gate poly on the periphery of the device as shown in Figure 11.20. The gate runner at the periphery is made in order to have a uniform gate voltage distribution (a precondition for minimum switching losses) in the entire device. An overlayer metal is needed to connect the sources together and also provide a low resistance path on the gate runner. A thick layer (typically 3–5  $\mu\text{m}$ ) Al is sputtered on the wafer. Then, the overlayer metal over the source pad, gate pad, and the gate runner is formed by Al etching with Mask #9 as shown in Figure 11.21.

A thick layer (typically 5–10  $\mu\text{m}$ ) of polyimide is coated and formed utilizing Mask #10 on the wafer to provide insulation for high voltage areas for packaging as shown



**Figure 11.16** Mask #7: Ohmic Metal for forming the metal on the source.

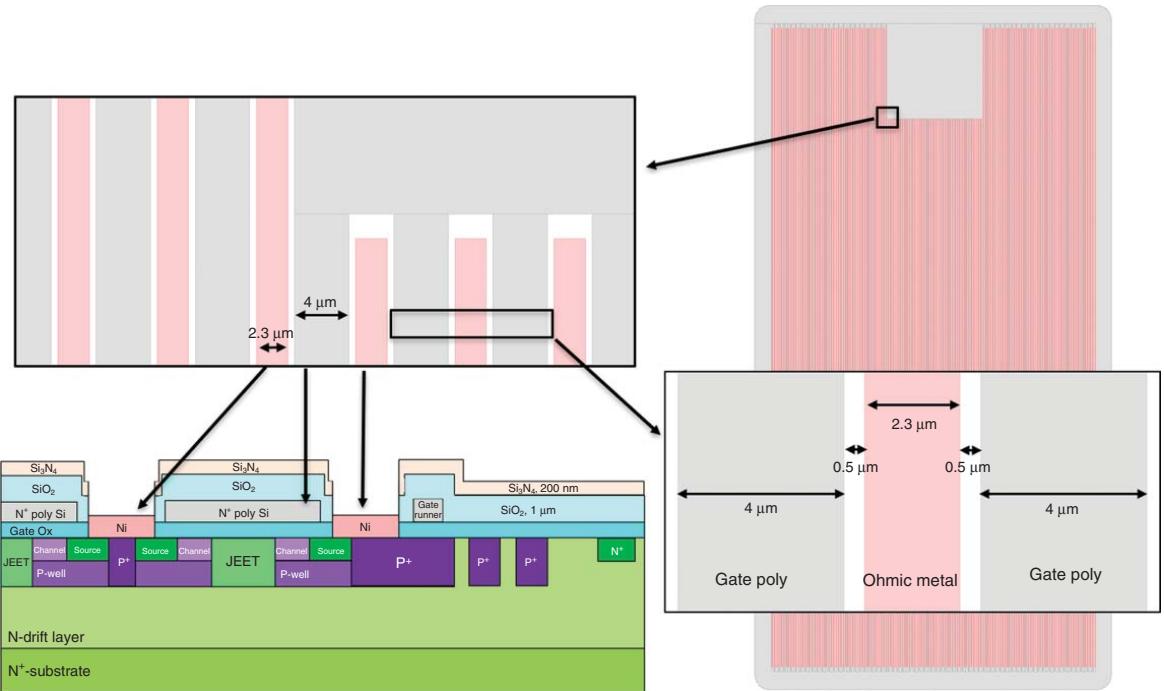
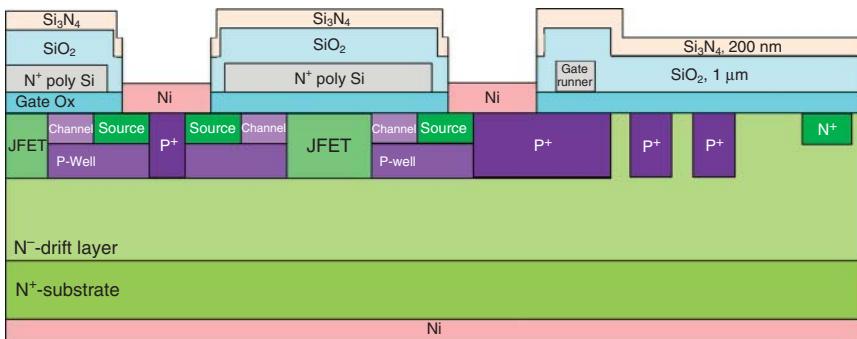


Figure 11.17 Mask #6 (Gate Poly) and #7 (Ohmic Metal).



**Figure 11.18** Backside ohmic metal deposition.

in Figure 11.22. Therefore, two vias are made over the source and gate pads while the rest of the die is covered by polyimide. It should be noted that the Al on the gate runner is connected to the gate pad not seen in Figure 11.22.

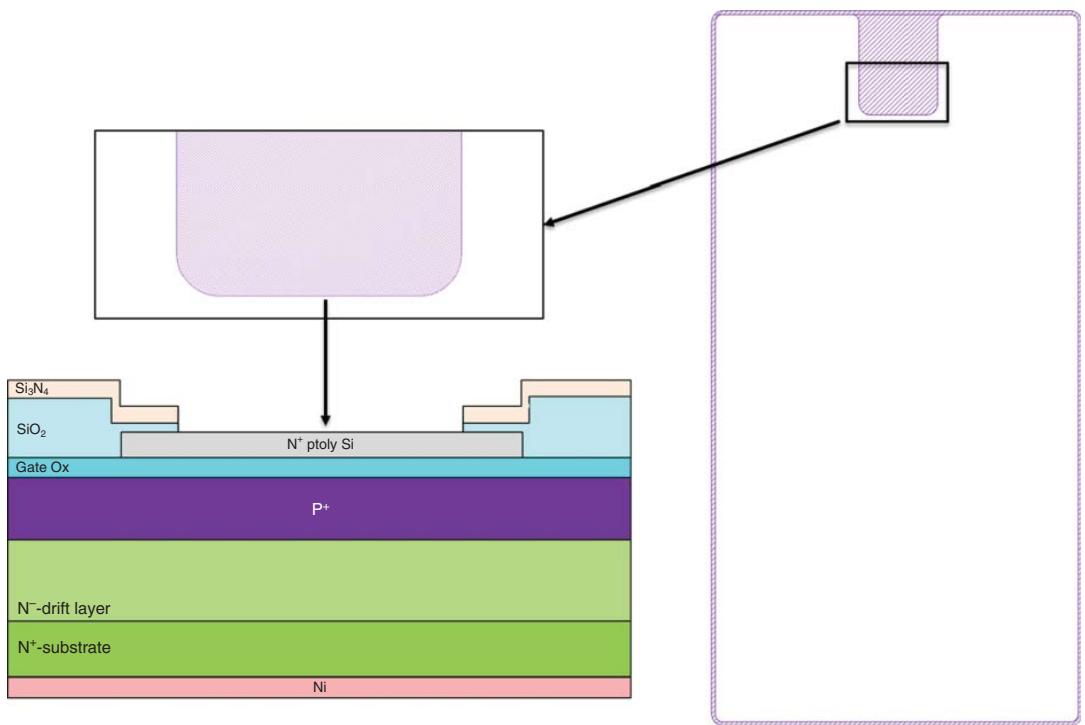
Finally, a stacked layer of metal is deposited on the backside (drain) of the wafer in order to have a better current distribution (see Figure 11.4) and solderability.

### 11.3.1 Lithography

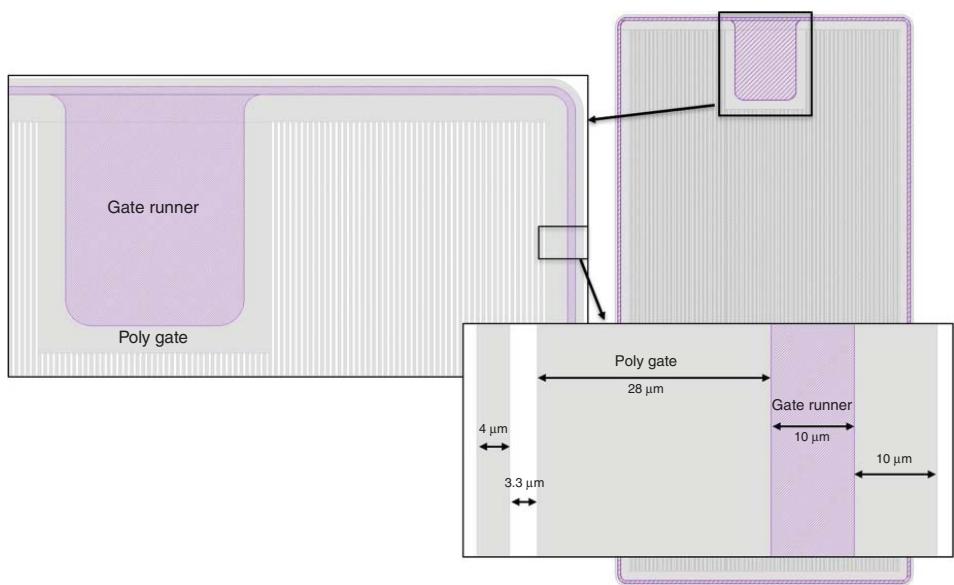
Lithography is the cornerstone of fabrication process technology. G- or I-line steppers along with a suitable mask are normally utilized for fabricating power devices like DMOSFETs as shown in Figure 11.1. A minimum of 10 steps of lithography are needed to make this structure, i.e. Alignment marks, JFET implantation, P-well implantation, N<sup>+</sup> source implantation, P<sup>+</sup> implantation, Polysilicon gate, Ohmic metal, Gate Runner, Overlay metallization, and Pad via. For example, to form the JFET region within the N<sup>-</sup> drift layer by ion implantation, an oxide layer is utilized as a mask. However, this oxide layer needs to be formed by a lithography step following oxide dry etching. This lithography includes photoresist coating and exposing by ultra violet (UV) light through a mask. Generally, I-line lithography is used for SiC fabrication in existing 150–200 mm commercial foundries. The minimum line width and spacing are about 0.6–0.8 μm which are also process dependent and vary somewhat between various photolithography steppers. The typical alignment tolerance is 0.2 μm. Given these, the minimum pitch of a planar MOSFET cell is around 3.5–4 μm. Smaller pitch leads to better on-resistance since more width of MOSFET channel can be accommodated in a given active area of the chip.

### 11.3.2 SiC Etching

SiC etching can be done by wet or dry etching processes. SiC is an extremely inert material against chemical solvents, so the wet etch process is very difficult. Although SiC wet etching by molten KOH, NaOH, or Na<sub>2</sub>O<sub>2</sub> at 450–600 °C and its mechanism has been reported [6], it results in some defects such as dislocation pits



**Figure 11.19** Mask #8: Gate Runner.



**Figure 11.20** Mask #7 (Gate Poly) and #8 (Gate Runner) together.

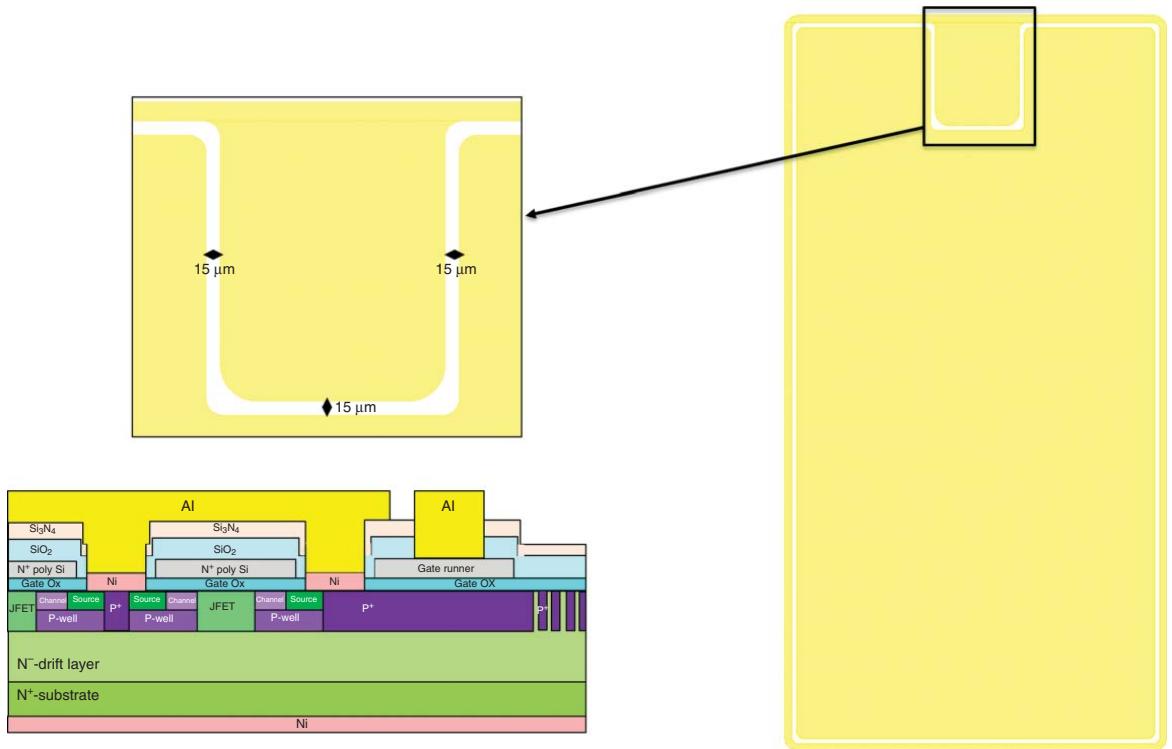


Figure 11.21 Mask #9: Overlayer Metal.

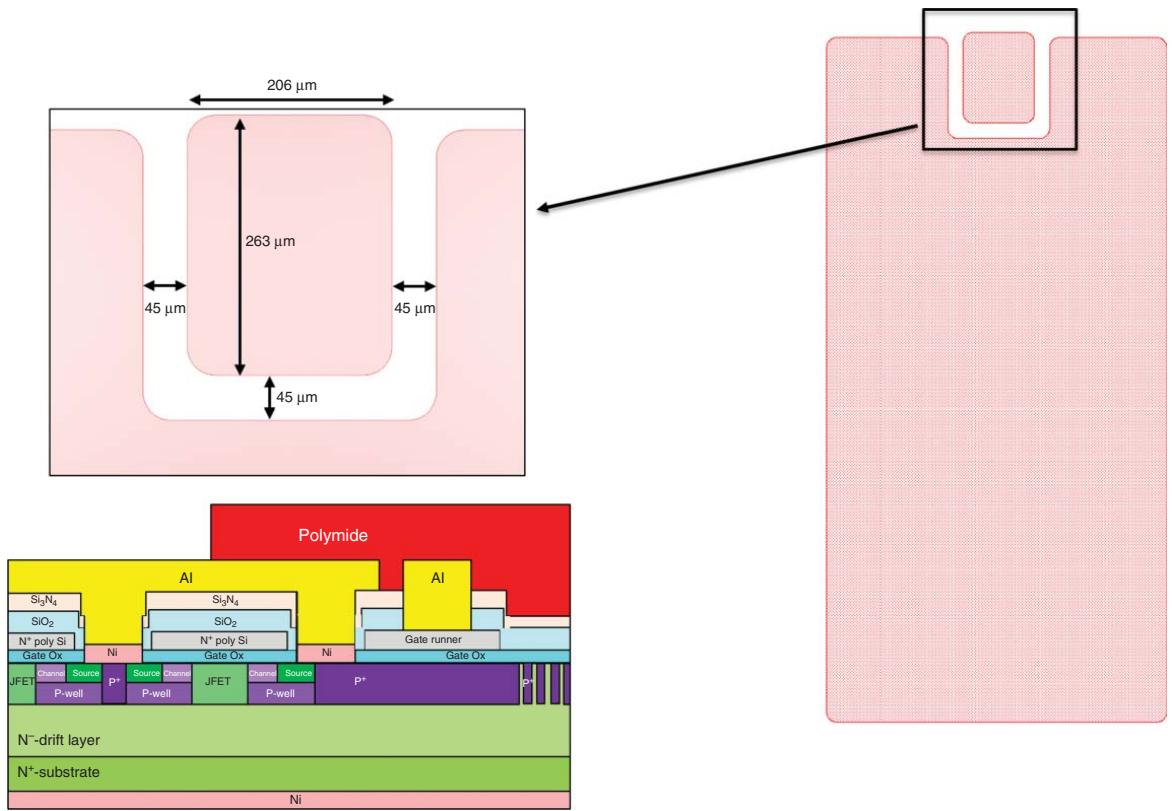


Figure 11.22 Mask #10 (Polyimide).

or hillocks on the surface [7]. Therefore, a dry etch process is generally utilized for SiC Technology [1–40].

The main difference between Si and SiC dry etching is how carbon is removed from SiC. In this process, generating positive ions and active radicals on plasma are accelerated toward the sample and induce physical and chemical etching, respectively. Three main etching gas systems are generally utilized for etching the SiC samples: fluorine-based ( $\text{SF}_6$ ,  $\text{CF}_4$ ,  $\text{NF}_3$ ,  $\text{BF}_3$ ,  $\text{CHF}_3$ ), chlorine-based ( $\text{Cl}_2$ ,  $\text{SiCl}_4$ ,  $\text{BCl}_3$ ), and bromine-based ( $\text{Br}_2$ ,  $\text{IBr}$ ) [7, 34]. Among these different gases, the fluorine-based ones make more volatile products thus resulting in higher etch rates. In order to increase the active species and enhance the etch rate one can add  $\text{O}_2$  and  $\text{Ar}$  [13, 31]. In contrast, adding  $\text{H}_2$  results in a lower etch rate [7] but may reduce micro-masking.

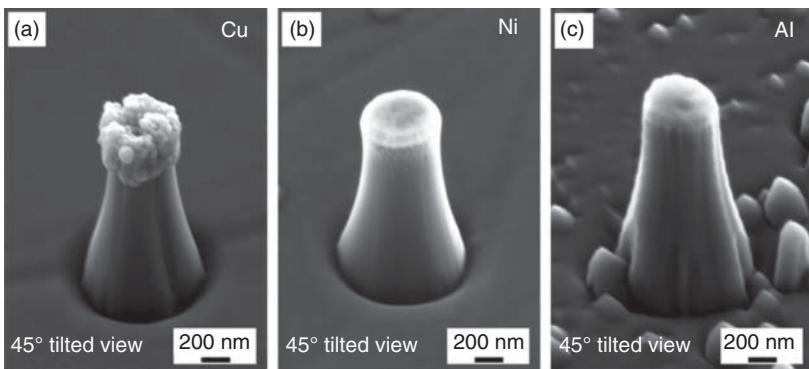
Inductively coupled plasma (ICP) and reactive ion etching (RIE) are widely employed for Si and SiC dry etching. RIE with a photoresist mask results in a faster process than ICP with a  $\text{SiO}_2$  or metal mask. In an RIE, one can enhance the etch rates by increasing the direct current (DC) self-bias and plasma density. However, increasing the DC self-bias results in an increase of energy of ions which causes more surface damage. In addition, increasing the plasma density raises isotropic etching and can jeopardize the vertical sidewalls. Koutarou et al. reported that deep levels are also induced by the RIE process in both n- and p-type 4H-SiC [41]. Therefore, an ICP processing is preferred for SiC dry etching.

In ICP dry etching, by utilizing an radio-frequency (RF) power to an inductive coil, one can produce a high plasma density at low pressure with low ion energies. It results in a lower ion bombardment damage than the RIE [36]. It should also be noted that employing a mask oxide instead of metal in ICP prevents the trenching effect [37]. In order to improve the surface damage after dry etching, a sacrificial oxidation process needs to be utilized [35, 38].

An important challenge in dry etching is the selectivity when both sample and mask are etched at the same time. For example, when a photoresist is used as a mask, it shows a low selectivity and cannot be used for forming a deep mesa. It is a good candidate for a shallow etch. For etching in a medium-range, oxide films like  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$  are utilized. A deep etching process utilizes a metal mask such as Ni, Al, and Cu. However, their nonvolatile by-products named micromasks are formed on the surface. These micromasks act as tiny masks and result in nanopillars on the surface during dry etching. This leads to a considerably rough surface (see Figure 11.23). Adding  $\text{H}_2$  results in a lower etch rate [7] but may reduce micro-masking.

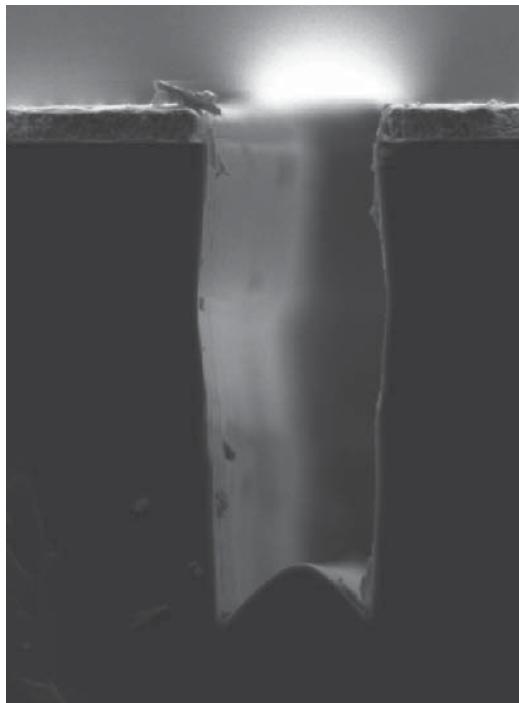
Micro-trenches or the trenching effect in which the area close to the sidewalls has a deeper depth than the bottom of the trench is another issue in the dry etching process (see Figure 11.24). This effect is strongly related to the DC self-bias. Utilizing a high DC-self bias increases the ion bombardment at the base of the sidewalls due to the deflection of ions impinging on the sidewall at low angles [12]. Therefore, all parameters such as DC-self bias, RF power, pressure, and gases flow should be comprehensively optimized in order to achieve an acceptable dry etch result.

Recently, Yu et al. reported an SiC deep dry etching of 184  $\mu\text{m}$  utilizing a stacked layer of Ti/indium Ti oxide (ITO) with a ratio of 20 nm/2  $\mu\text{m}$  as a hard mask to form a waffle structure on a SiC substrate (see Figure 11.25) [24]. ITO does not react with

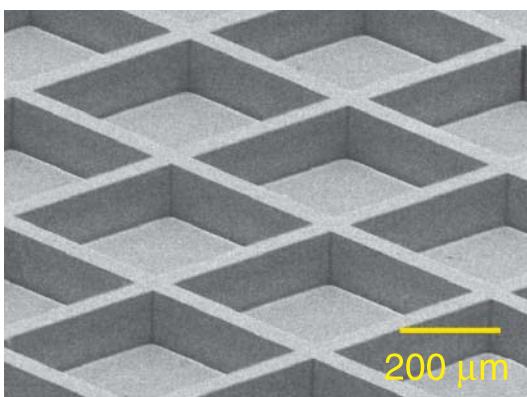


**Figure 11.23** SEM images of nanopillars with (a) Cu, (b) Ni, and (c) Al metal mask (45° tilted view). Source: Choi et al. [13].

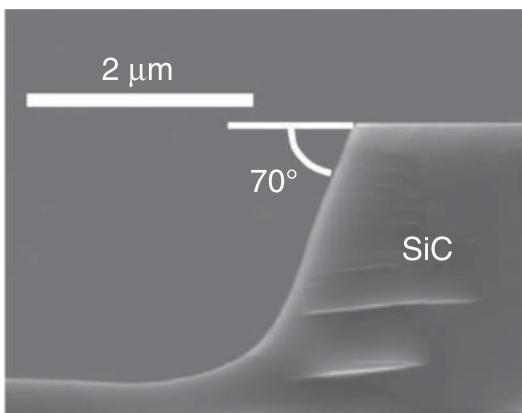
**Figure 11.24** Micro-trenching side effect in a 4H-SiC dry etching. Source: Luna et al. [31].



fluorine ions and is stable under high energies. They reported a vertical sidewall with no micro-mask and micro-trenching in this work. Thinning a 4H-SiC substrate by chemical mechanical polishing (CMP) followed by forming a waffle structure could be used for lowering the on-resistance of the devices (up to 1200 V) by reducing the resistance of the substrate [39]. For a device with a voltage  $\geq 1200$  V, the main resistance component comes from the drift layer. Therefore, it is not worth performing this process on the substrate which raises the cost.



**Figure 11.25** A waffle structure on a 4H-SiC substrate formed by dry etching. Source: Yu et al. [24].



**Figure 11.26** Improved bevel mesa formed with the optimized RIE condition. Source: Hiyoshi et al. [40].

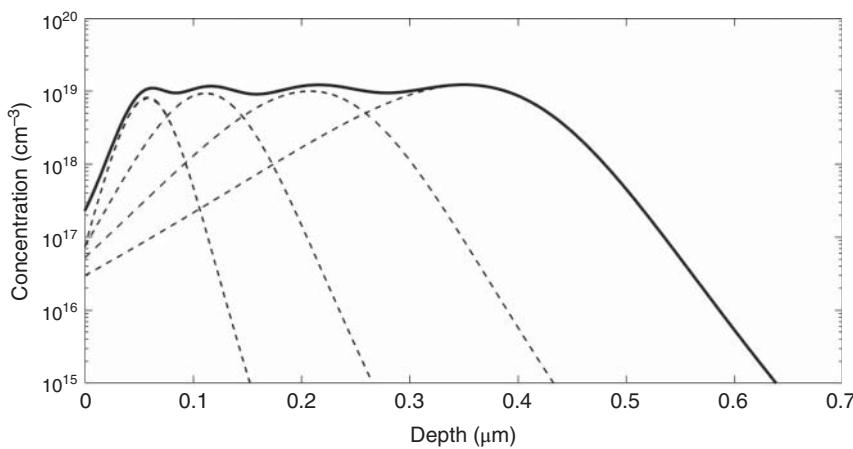
When a rounded bottom is needed in a device (edge termination area as an example), one can form it by wet etching the  $\text{SiO}_2$  mask followed by SiC dry etching (see Figure 11.26) [40].

Metal masks are generally avoided to reduce the contamination throughout the processing. A  $\text{SiO}_2$  layer deposited by chemical vapor deposition (CVD) is a good candidate for a mask. By optimizing all etch parameters and adding  $\text{O}_2$ , one can increase the selectivity and form the trenches with a proposed angle.

One can conclude that, although the SiC dry etching has been developed in recent years, there are some issues such as vertical sidewalls, micro-trenching, micro-masking, and surface roughness that have not been fully optimized and need a comprehensive investigation. The process optimization of dry etching is very useful for trench MOSFETs.

### 11.3.3 Ion Implantation and Activation Annealing

Three different technologies generally can be utilized for the doping process in the semiconductor technology: diffusion processing, in situ doping during crystal and epitaxial growth, and ion implantation. Since SiC has wide bandgap energy and



**Figure 11.27** Simulation profile of N implantation for forming N<sup>+</sup> in 4H-SiC according to [42].

small interatomic distances, the main dopants have negligible diffusion coefficients even at high temperatures (>2000 °C). Diffusion processing in SiC is only available for small atoms such as H, He, Li, B, and Br [7, 34]. To predict the implant profiles by implanting various ions into different targets, Monte Carlo simulations, like SRIM (stopping and range of ions in the matter), are utilized.

Shielded DMOSFET results in a lower electric field peak in the JFET region and low saturation drain current at high drain voltages without compromising device on-resistance making this structure a preferred design to have a better short circuit capability [1]. This structure needs four ion implantation steps for forming the JFET region, P well, and P<sup>+</sup> shield under the P well (with one mask and process step), N<sup>+</sup> source, and P<sup>+</sup> into the N<sup>-</sup> drift layer. In general, N and phosphorus are utilized for forming n-type regions, whereas Al and B are used for forming p-type regions. Figure 11.27 shows a simulation result of a nitrogen profile for forming an N<sup>+</sup> source with a doping concentration of 10<sup>19</sup> cm<sup>-3</sup> according to [42]. It consists of four implantation steps at room temperature with the energies of 35, 70, 140, and 260 keV and doses of  $3.5 \times 10^{13}$ ,  $7 \times 10^{13}$ ,  $1.2 \times 10^{14}$ , and  $2 \times 10^{14}$  cm<sup>-2</sup>, respectively.

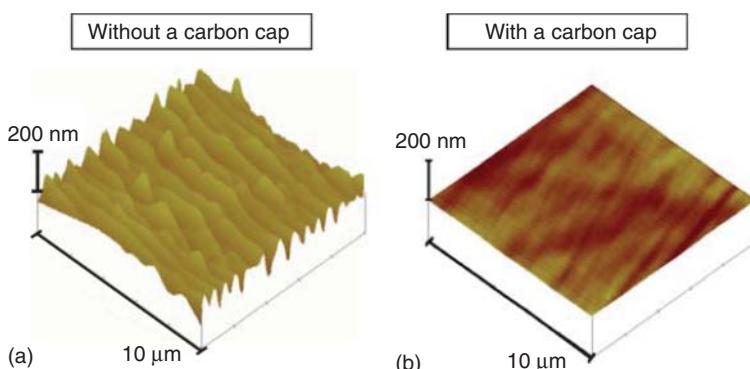
It should be noted for forming N<sup>+</sup> regions with a doping concentration greater than 10<sup>19</sup> cm<sup>-3</sup> (required for low ohmic contacts), phosphorous implantation results in a lower sheet resistance than an N implantation owing to its higher solid solubility limit [43, 44]. Therefore, P implantation at high temperatures is preferred for such a heavily doped N<sup>+</sup> region. Likewise, Al implantation results in lower sheet resistance than boron (B) implantation for forming P<sup>+</sup> regions with a doping concentration greater than 10<sup>19</sup> cm<sup>-3</sup>; thus, Al is preferred for heavily doped P<sup>+</sup> regions [7].

In recent years, there has been considerable interest in ion implantation study in SiC technology utilizing several ions [42–77]. Most of these works have studied the effect of ion implantation and its post-activation annealing in the SiC. The implantation energy needed to achieve a given depth in SiC is higher than Si due to the higher atomic density of SiC [7].

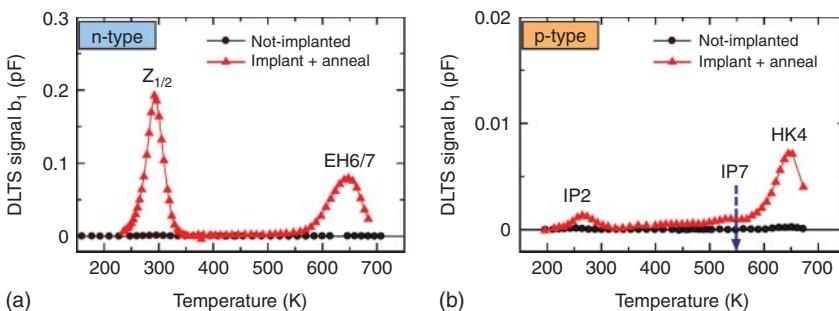
A valuable advantage of the ion implantation process is doping in the selected area by utilizing a mask and avoiding the wet or dry etching for forming the lateral structure. The type and thickness of the mask are related to the dose and energy of the ions. Photoresists,  $\text{SiO}_2$ , and some metals are utilized as a mask. It should be thick enough and robust at high temperature to stop the ions in the masked areas.

It should be noted that to prevent a highly damaged lattice in SiC, the implantation process should be done at elevated temperatures ( $300\text{--}800\text{ }^\circ\text{C}$ ), especially when the dose is higher than  $10^{15}\text{ cm}^{-2}$ . Otherwise, it results in an amorphous structure at the surface, and there is no guarantee to recover the lattice and obtain the original polytype of SiC with any high-temperature annealing [7]. However, room temperature implantation could be performed for lower doses ( $<10^{15}\text{ cm}^{-2}$ ) [75]. Ion implantation generally causes some damages to the crystal lattice in which the ions can kick out the Si and C atoms from their lattice positions thus leaving vacant lattice sites [76]. It is worth noting that the C displacement rate is higher than the Si displacement. Thus, the implanted ions can occupy the interstitial lattice sites. They should be steered to substitutional lattice sites to be electrically active. Therefore, a post-high-temperature activation annealing ( $>1600\text{ }^\circ\text{C}$  for SiC) is necessary to activate the dopants (>95%) even if the implantation has been done at elevated temperature [7]. In this process, the interstitial ions compete with interstitial Si and C atoms to take the vacancies in the crystal lattice and be electrically active. During the activation annealing, a capping layer like  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ , AlN, or graphite (carbon) should be deposited on the SiC surface to suppress the migration of surface atoms and Si desorption [7]. Negoro et al. reported that utilizing a carbon cap layer in an Ar ambient provides the most successful results [43]. Figure 11.28 shows atomic force microscopy (AFM) images of  $\text{Al}^+$ -implanted (with a total dose of  $10^{16}\text{ cm}^{-2}$ ) off-axis 4H-SiC (0001) annealed at  $1800\text{ }^\circ\text{C}$  for five minutes with and without a carbon cap layer [7]. It shows utilizing a carbon cap layer results in better surface roughness.

As discussed above, the implanted ions make Si and C vacancies in the lattice. These vacancies become mobile during high-temperature annealing forming some



**Figure 11.28** Atomic force microscopy (AFM) images of  $\text{Al}^+$ -implanted (with a total dose of  $10^{16}\text{ cm}^{-2}$ ) off-axis 4H-SiC (0001) annealed at  $1800\text{ }^\circ\text{C}$  for five minutes with and without a carbon cap layer. Source: Kimoto and Cooper [7].



**Figure 11.29** The DLTS spectra obtained from  $\text{Al}^+$ - room temperature implanted followed by annealing at  $1700^\circ\text{C}$  for 20 minutes in (a) n-type and (b) p-type 4H-SiC epitaxial layers. Source: Based on Kawahara et al. [80].

defects such as vacancy clusters, interstitial clusters, and anti-site vacancy pairs [7]. These defects act as localized shallow- or deep levels in the bandgap thus affecting the on-state and off-state characteristics. For example,  $Z_{1/2}$  ( $E_C - 0.63\text{ eV}$ ) [77], EH<sub>6/7</sub> center ( $E_C - 1.55\text{ eV}$ ) [78], and HK4 center ( $E_V + 1.45\text{ eV}$ ) [79] are three major deep levels generated during this processing.  $Z_{1/2}$  centers caused by C vacancies are one of the most important defects in SiC known as carrier lifetime killer which causes higher on-resistance, lower reversed recovery charges, and faster switching in pn junctions. Figure 11.29 shows the deep level transient spectroscopy (DLTS) spectra obtained from  $\text{Al}^+$ -room temperature implanting followed by annealing at  $1700^\circ\text{C}$  for 20 minutes in (a) n-type and (b) p-type 4H-SiC epitaxial layers [80]. It shows how this process results in an increase of these defects.

Additionally, the ion implantation followed by high-temperature annealing can form basal plane dislocations (BPDs). This effect may be strongly dependent on the implant temperature, annealing temperature, the quality of the graphite cap, etc. This high-temperature processing results in stress within the SiC thus causing movement of pre-existing dislocations and even making new dislocations. The BPDs are reported to act as a source of expanding stacking faults (SFs) formation during the bipolar injection. These SFs induce energy levels in the SiC bandgap which act as recombination centers, decreasing the minority carrier lifetime in the drift layer. This may result in an increased forward voltage drop during the on-state mode, i.e. bipolar degradation [36, 81].

Today, there are various companies providing ion implantation for SiC technology processing with different doses, energies, temperature, and sources. Table 11.1 summarizes these companies available around the world.

#### 11.3.4 Oxidation and Oxide

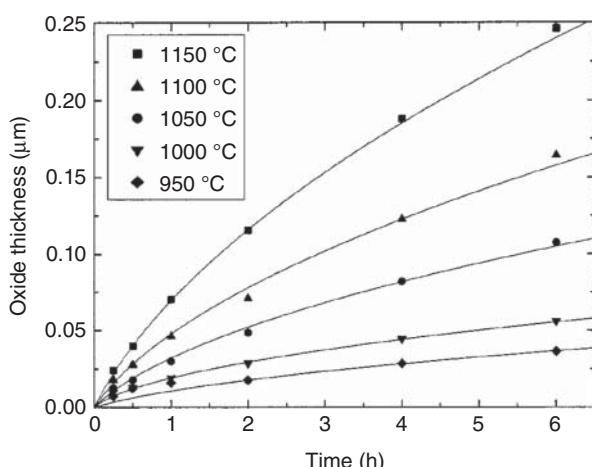
Both Si as an elemental semiconductor and SiC as the only compound semiconductor have a unique advantage over the other semiconductor materials of thermally grown  $\text{SiO}_2$  on their surfaces. It is worth noting that  $\text{Si}_3\text{N}_4$  is generally utilized as a moisture barrier in the Si and SiC technology. The  $\text{SiO}_2$  layer can be employed

as a gate dielectric in MOSFETs. The main difference in the thermally grown  $\text{SiO}_2$  layer on Si and SiC surfaces is the presence of C atoms in the SiC. The quality of the grown  $\text{SiO}_2$  layer plays an important role in device reliability and on-state and off-state characteristics. This quality is related to the oxidation condition, surface roughness before deposition, semiconductor material, the device area, post-annealing condition, etc. The channel mobility is a good example showing how poor quality of the  $\text{SiO}_2$  layer at the  $\text{SiO}_2/\text{SiC}$  interface lowers the mobility by an order of magnitude. Although the bulk electron mobility in an n-type 4H-SiC may reach to about  $1000 \text{ cm}^2/\text{V}\cdot\text{s}$ , it degrades to about  $10\text{--}30 \text{ cm}^2/\text{V}\cdot\text{s}$  in an n-channel of a MOSFET. This is due to the presence of a high-density interface states at the  $\text{SiO}_2/\text{SiC}$  interface especially close to the conduction band [82]. Dangling bonds at the  $\text{SiO}_2/\text{SiC}$  interface also contribute to the interface state density.

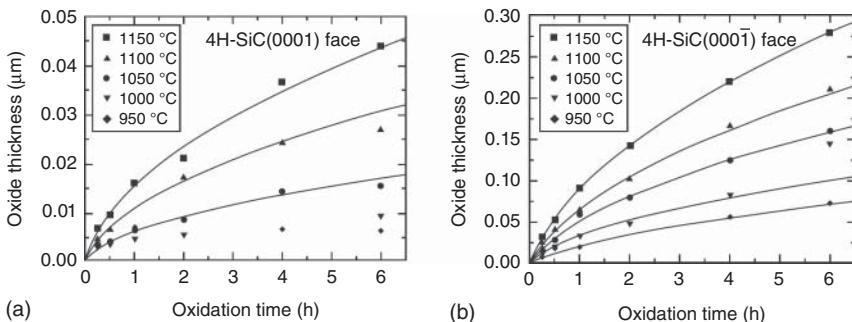
Moreover, the presence of the fixed charges in the gate oxide affects the threshold voltage and its stability. In addition,  $\text{SiO}_2/\text{SiC}$  has a lower barrier height than the  $\text{SiO}_2/\text{Si}$  interface. This results in higher tunneling current at the higher electric field and elevated temperature and affects the oxide reliability. As a result, the growth of gate oxide film, improving its quality, and its effects on device performance have been considerably studied in the last few years [82–120].

The thermal growth of  $\text{SiO}_2$  on Si and SiC is performed by oxidation in dry ( $\text{O}_2$ ) or wet ( $\text{H}_2\text{O}$ ) oxidation in an oxidation furnace. The wet oxidation is faster than dry oxidation in SiC [34]. To enhance the oxidation growth rate of SiC, an elevated temperature ( $>1000^\circ\text{C}$ ) is utilized. Figure 11.30 shows how oxide thickness is increased at elevated temperatures in dry thermal oxidation of the a-face of 4H-SiC [83].

In the oxidation process of SiC, the free C atoms escape from the surface through the formation of CO gas or remain at the surface and form C clusters at or near the  $\text{SiO}_2/\text{SiC}$  interface. These C clusters affect the electrical properties at the interface [34] such as channel mobility in the SiC MOSFETs. Although one can decrease



**Figure 11.30** Oxide thickness as a function of time and temperature for dry thermal oxidation of the a-face of 4H-SiC. Source: Song et al. [83]. © 2004, AIP Publishing.



**Figure 11.31** Oxide thickness of 4H-SiC for (a) Si-face and (b) C-face as a function of oxidation time at different temperatures. Source: Kimoto and Cooper [7]. John Wiley & Sons. © 2014, John Wiley & Sons.

these C clusters at the interface by depositing  $\text{SiO}_2$  instead of the thermal growth process, the quality of the deposited layer is still under investigation [34].

The thermal oxidation growth rate of SiC is much lower than Si. The thermal oxidation of C face is about three to ten times faster than Si face in SiC [34]. The rate is related to the temperature of the oxidation process. Figure 11.31 shows the oxide thickness of 4H-SiC for Si-face and C-face as a function of oxidation time at different temperatures. Other faces like a-face and m-face have thermal oxidation rates between the Si- and C-faces (see Figures 11.30 and 11.31). This processing becomes important in trench shape structures like trench MOSFETs in which the side walls oxidize more than three times faster than the bottom of the trenches. It is also worth noting that the oxidation rates are increased for the implanted regions and decreased for the dry-etched regions [34].

Despite a lot of optimization and enhancement of the thermally grown oxide quality in SiC processing, the  $\text{SiC}/\text{SiO}_2$  interface has a high density of interface state defects. It is about two orders of magnitude higher than for the  $\text{Si}/\text{SiO}_2$  interface which affects the reliability and performance of the SiC power devices [117]. This topic is discussed in detail in the chapter written by Thomas Aichinger and Gregor Pobegen in this book.

Most of the interface states in the lower half of the SiC bandgap (near the valence band) are donor like [7]. They capture the holes in and do not release them at room temperature [118]. These holes act as positive fixed charges. It has been reported that wet oxidation results in better quality than the dry oxidation and lowers the density of these donors like states at the  $\text{SiC}/\text{SiO}_2$  interface [118].

Likewise, most of the interface states in the upper half of the SiC bandgap (near the conduction band) are acceptor like. They capture electrons and do not release them at room temperature. These electrons act as negative fixed charges at the interface. It is worth noting that in an n-channel MOSFET, when an inversion layer is formed by a positive gate voltage, many electrons may be captured in these states. The captured electrons become immobile and act as Coulomb scattering centers thus lowering the effective n-channel mobility ( $5\text{--}8 \text{ cm}^2/\text{V s}$  with no POA [7]). Most recent work at the time of proof reading this chapter was reported by Kobayashi et al. This work was

able to reduce the interface states in the upper half of the band gap to very low numbers equivalent to what is generally found in Si MOS structures by using hydrogen etching, oxidized silicon at 700 °C and POA with Nitrogen gas at >1400 °C. [Applied Physics Express 13, 091003 (2020)].

Afanas'ev et al. reported that the source of the donor-like interface states is carbon clusters, whereas the source of the acceptor-like interface states is near interface states [119, 120]. These states are located inside  $\text{SiO}_2$  close to the interface and act as a trap for electrons.

### 11.3.5 Post Oxidation Annealing

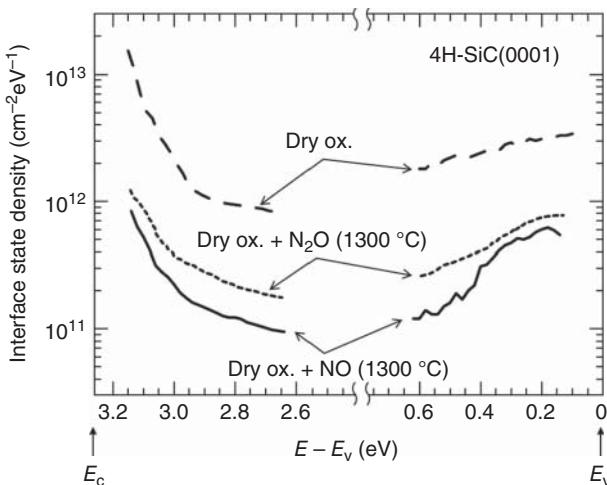
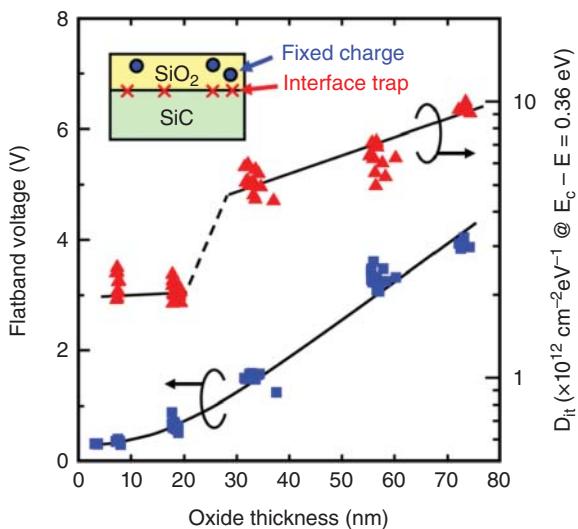
POA is a good method to passivate dangling bonds at the interface and reduce fixed positive charge in the gate oxide films. In Si technology, a hydrogen-containing gas, like an  $\text{H}_2\text{-N}_2$  mixture, at 400–500 °C is utilized to lower the interface state density ( $D_{it}$ ) to about  $10^9 \text{ eV}^{-1} \text{ cm}^{-2}$  [121]. Fukuda et al. reported that in SiC technology, hydrogen POA needs to be done at elevated temperatures (about 1000 °C) to reduce the  $D_{it}$  to about  $10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$  [122].

A popular way for reducing the fixed oxide charge and  $D_{it}$  in SiC processing is a POA in an inert gas such as Ar and  $\text{N}_2$  at the same temperature of the oxidation (1100–1200 °C) [7]. In addition, it was reported that Ar POA results in an improvement in the dielectric properties and reliability of oxides [99]. Kato et al. reported that an Ar POA at high temperature (1300–1350 °C) after thermal oxidation followed by  $\text{N}_2\text{O}$  annealing results in diffusion of accumulated carbon atoms at the  $\text{SiO}_2/\text{SiC}$  interface. This process results in an improvement of the peak value of field-effect mobility from 19 to 33  $\text{cm}^2/\text{V}\cdot\text{s}$  [123].

As discussed in the previous section, wet oxidation generally has better quality than dry oxidation. It shows a significantly lower  $D_{it}$  near the valance band and slightly lower  $D_{it}$  near the conduction band. Therefore, it results in better hole mobility in a p-channel device. However, for improving the electron channel mobility in an n-channel device, one can utilize dry oxidation at a high temperature of about 1250–1300 °C. This can reduce the  $D_{it}$  near the conduction band [7]. However, when the oxide thickness exceeds 20 nm, the  $D_{it}$  is increased as shown in Figure 11.32 [124]. These results show the  $D_{it}$  and  $V_{fb}$  values as a function of oxide thickness with no POA process after dry oxidation. The positive flat band voltage ( $V_{fb}$ ) shift shows an increase of the negative fixed charges in the oxide by increasing the oxide thickness.

In recent years, there has been a considerable interest to lower the  $D_{it}$  by post-oxidation nitridation in a nitrogen-containing gas such as nitric oxide (NO) [105, 110, 111, 125–135], nitrous oxide ( $\text{N}_2\text{O}$ ) [136, 137], ammonia ( $\text{NH}_3$ ) [138, 139], and in the presence of nitrogen radicals [140]. Figure 11.33 clearly shows how  $\text{N}_2\text{O}$  and NO POA results in a lower  $D_{it}$  over the entire range of energies within the bandgap [7]. This causes the dangling bonds to passivate and remove the interstitial carbon and carbon clusters left in the oxidation process [111]. It should be noted that two mechanisms compete during POA in NO or  $\text{N}_2\text{O}$  ambient, i.e. nitridation and oxidation. Figure 11.33 illustrates how NO POA results in lower  $D_{it}$  than  $\text{N}_2\text{O}$  POA.

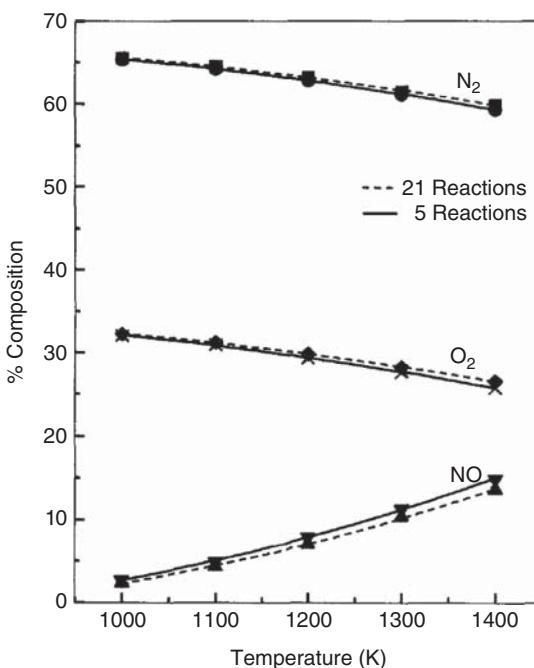
**Figure 11.32**  $D_{it}$  and  $V_{fb}$  values as a function of oxide thickness with no POA process after dry oxidation [124].



**Figure 11.33** Reduction of the  $D_{it}$  over the entire range of energies within the SiC bandgap in 4H-SiC (0001) MOS capacitors utilizing N<sub>2</sub>O and NO POA. Source: Kimoto and Cooper [7]. © 2014, John Wiley & Sons.

Decomposition of N<sub>2</sub>O results in N<sub>2</sub>, O<sub>2</sub>, and NO. Figure 11.34 shows the percentage of NO is increased by increasing temperature. One can conclude that N<sub>2</sub>O POA should be done at higher temperatures than the NO POA to increase the nitridation and decrease the oxidation.

Figure 11.35 shows the positive/negative bias threshold voltage instability (PBTI/NBTI) tests for five different commercially available 1200 V 4H-SiC MOSFETs. Due to the existence of these traps, when a positive DC bias is applied to the gate over a long period of time, the threshold value shifts in the positive direction due to the tunneling and capture of electrons by near interface traps. Conversely,

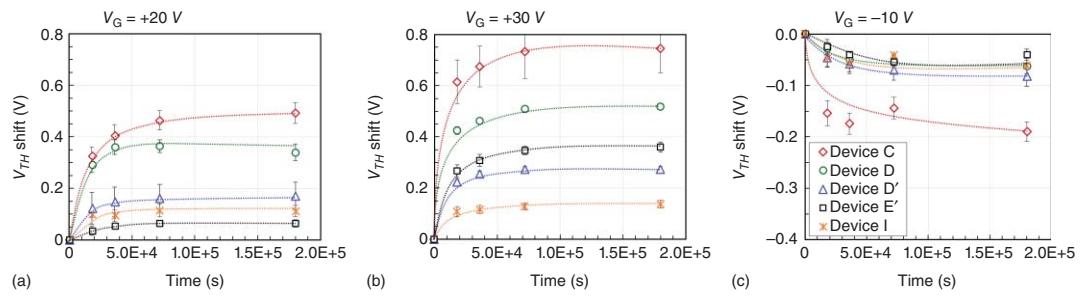


**Figure 11.34** Gas composition in the decomposition of  $\text{N}_2\text{O}$  at various temperatures. Source: Gupta et al. [141]. © 1998, Elsevier.

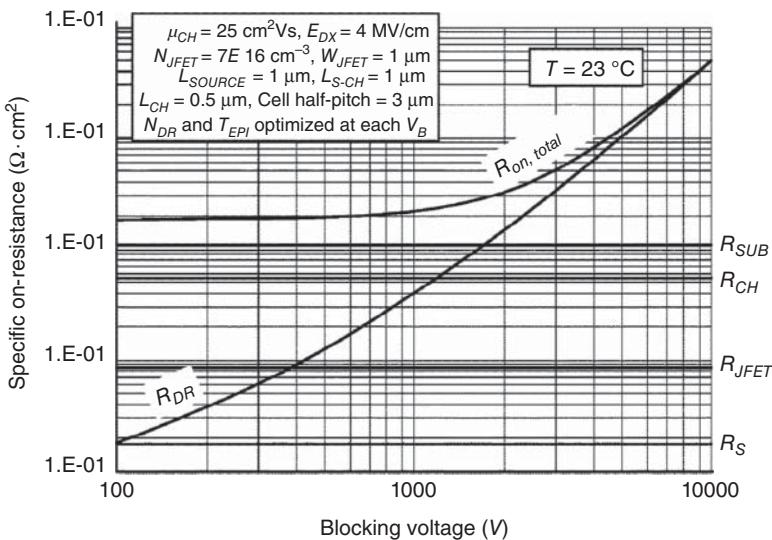
when a negative bias is applied to the gate over a long period of time, the threshold voltage shifts in the negative direction resulting in a significant increase in leakage current in the off-state. Furthermore, a negative shift of threshold voltage can cause devices to turn on unexpectedly and lead to failures. We investigate this particular trap-induced device degradation on commercially available devices by applying positive voltage stress on the gate over a long period of time, with source and drain grounded. At the end of each stress, transfer characteristics ( $I_D-V_G$ ) were measured to determine the threshold voltage shifts. The considerable variance between devices from different vendors was observed implying that while some vendors have been able to significantly reduce the near-interface traps in the gate oxide, the others may still need some development.

### 11.3.6 Poly-Si Deposition

Polysilicon is normally utilized as gate electrode material in metal-oxide-semiconductor (MOS) devices as shown in Figure 11.1. LPCVD is normally utilized for polysilicon deposition [143–150]. It can be undoped or doped with some elements such as N or P. The dopants can be incorporated in situ during the deposition or later by diffusion or ion implantation. Phosphorus doping of polysilicon is very popular in the Si industry as the phosphorus helps to getter the impurities in the gate oxide films during the soak at 800 °C. A higher final doping of the poly Si allows lower internal gate resistance and therefore more homogenous switching of the device in case of fast gate voltage transients.



**Figure 11.35** Time-dependent threshold voltage shifts for (a) positive bias-stress of +20 V, (b) +30 V, and (c) negative bias-stress of -10 V for 50 hours for different commercial available 1200 V 4H-SiC MOSFETs. Source and drain were grounded at room temperature. Source: Yu et al. [142]. © 2020, IEEE.



**Figure 11.36** The internal resistance components state-of-the-arts SiC power MOSFETs as a function of blocking voltage. Source: Cooper [39].

### 11.3.7 Backside Thinning and Waffle Substrates

Specific on-resistance ( $R_{on,sp}$ ) of a power DMOSFET has several internal resistance components such as source resistance, channel resistance, JFET resistance, drift resistance, and substrate resistance [39].  $R_{on,sp}$  plays a key role in power devices because the cost of a power DMOSFET scales as the square root of  $R_{on,sp}$  at a given on- and off-state performance [39]. For example, if  $R_{on,sp}$  decreases four times, the total cost might lower to about two times. Figure 11.36 shows the 4H-SiC substrate resistance is a dominant resistance below about 1700 V. This component is even more important for diodes since they do not have contributions from MOSFET channel. Therefore, lowering this component in the SiC devices below 1700 V could be considered for lowering the total cost. To date, two techniques have been reported for lowering the substrate resistance, i.e. wafer thinning and waffle structure.

Backside wafer thinning was reported by Rupp et al. [151]. This process includes wafer grinding at the last steps of the fabrication in which the substrate thickness is lowered from about 350 to  $<150 \mu\text{m}$ . This process results in better electrical and thermal behavior of the SiC devices. It is worth noting that one cannot reduce the thickness more than this range due to an increase in the probability of the wafer bowing and breaking. Cooper reported a technique named waffle substrates for thinning the substrate up to  $50 \mu\text{m}$  [39]. In this technique, the substrate thickness is firstly lowered by backside wafer thinning as above. Then, the waffle structure is made by SiC dry etching utilizing a metal mask (see Figure 11.25). Finally, a suitable metal is deposited on the backside. It should be noted that since both of the above techniques are done at the last steps of the processing, one cannot utilize regular post metal annealing for creating a proper ohmic contact. However, a laser annealing

with a suitable spot area and energy could be utilized after the metallization on the backside of the wafer.

### 11.3.8 Ohmic Contacts and Metallization

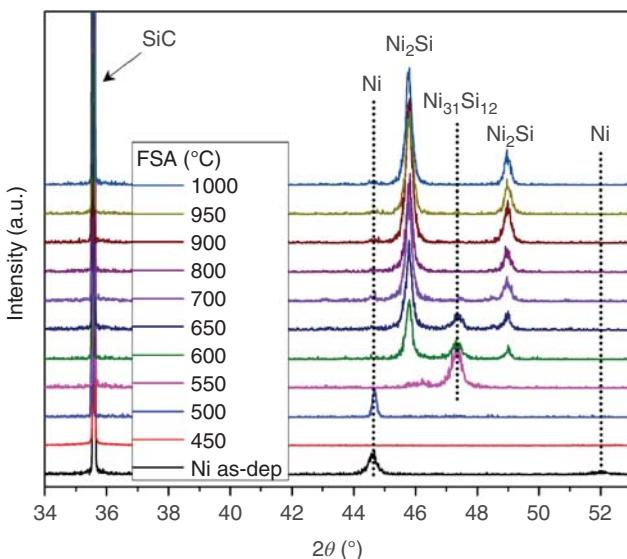
Although some devices such as metal–semiconductor field-effect transistors (MESFETs) and Schottky diodes utilize a Schottky contact, a proper metallization with a good ohmic contact is needed for other devices because a large voltage drop in a poor ohmic contact leads to power loss. A sacrificial oxidation process after ion implantation and dry etching is often used before the metallization to remove damage in SiC.

Three different methods can be used for metal deposition on Si or SiC samples: evaporation, sputtering, and CVD. Evaporation should be performed in an ultra-clean vacuum system to achieve higher rates of deposition. However, poor adhesion of the metal to the sample can be a problem in this method. Sputtering is considered a fast and economical method with good adhesion; however, it might be problematic for lift-off patterning. Although Ni is mostly used as metal for n-type 4H-SiC, different compounds such as Ti [152], Al/Ti [153], Ti/Al [153, 154], Ni/Al [155, 156], Ni/Ti/Al [156, 157], and Ti/Ni/Al [157] have been reported for p-type 4H-SiC metallization.

A key factor for forming good ohmic contacts is post-metal annealing (PMA) in an oxygen-free ambient. It is worth noting that very high-temperature annealing may result in a rough contact surface morphology [156] and might be problematic for adhesion of over-layer metal, poor alignment accuracy in the photolithography process, and reliability of the contacts. Therefore, optimizing the annealing temperature is necessary to have good ohmic contact for all structures at lower temperatures. As Ni atoms can be mobile at about 450 °C, a temperature of 700 °C might be high enough to form the *Nickel-Silicide* for n-type ohmic contacts [36]. However, to achieve good ohmic contact with a high intensity of NiSi and NiSi<sub>2</sub> contacts, a temperature of about 960 °C is needed [158–160]. To have good ohmic contact for p-type 4H-SiC, a lower temperature (750–850 °C) is required [157]. It has been reported that among different intermetallic phases, Ti<sub>3</sub>SiC and NiSi<sub>2</sub> show a significant effect in the formation of p-type ohmic contacts [161].

Although the self-aligned silicide process (Salicide) has been used in Si technology for many years, it has been recently reported in SiC technology [5, 162]. In this process, first, a SiO<sub>2</sub> layer is deposited and patterned on the SiC surface. Then a metal like Ni is deposited and first step annealing (FSA) is performed at lower temperatures (700–800 °C) as shown in Figure 11.37. This forms one phase of Ni silicide in the contact openings (VIAs). There is no reaction between Ni and SiO<sub>2</sub> and unreacted Ni can be easily removed by Piranha clean. One can increase the intensity of the Ni silicide by performing the second step annealing (SSA) at higher temperatures.

A *Nickel-Silicide* is also used for the backside metallization of the wafer for having a low resistivity contact for the 4H-SiC processing technology [36, 38, 163, 164]. It should be noted that the native oxide on the backside should be removed by wet-dry etching before Ni deposition as shown in Figure 11.18.



**Figure 11.37** The X-ray diffraction (XRD) spectra of the Ni contact layer after the first step annealing (FSA) at different temperatures and removal of unreacted Ni. Source: Elahipanah et al. [5]. Licensed under CC BY 4.0.

An overlayer metal on the topside is utilized to connect the source cells together and also provide a low resistance path on the gate runner. A thick layer (typically 3–5  $\mu\text{m}$ ) Al is sputtered on the wafer. It also provides an appropriate surface for wire bonding in packaging. Similarly, an overlayer metal on the backside is needed to achieve a desired current distribution. A stacked-layer metal of Ni/Ti/Ag or Ni/Ti/Au is popular for the backside overlayer metal. It worth noting that the processed wafers need to be shipped in vacuum in the case of using Ag to prevent oxidation of silver.

### 11.3.9 Polyimide Deposition

The last step to process before dicing and wire bonding is a deposition of suitable passivation layer to achieve the electrical insulation of the components in high-voltage devices [145, 149]. Polyimide (PI) materials are considered as suitable candidates due to their excellent intrinsic properties such as high dielectric breakdown fields ( $E_{\text{BR}} > 2 \text{ MV/cm}$ ), thermal stability (weight losses <1% at 500 °C), relatively low losses, and thermomechanical matching with components [148, 150]. Commercial polyimides for microelectronic applications may be prepared as polyamic acid (PAA) solution [148]. This solution is typically spun onto the wafer. Then, a thermal curing process at high temperature (>300 °C) in N<sub>2</sub> ambient for an hour [165] is utilized to drive off the solvent and initiate polyimide ring closure which produces the insoluble polyimide [143]. An alternative deposition method is CVD which results in a better uniformity in thickness [143, 147].

## 11.4 Commercial Foundries for Si and SiC Devices

Although SiC devices have become commercially available in the market, they are still more expensive than the Si devices. Moreover, there are additional equipment and/or unit process steps needed for SiC technology when implemented in a commercial Si Foundry. SiC substrates are available in 150 mm diameter with 200 mm on the horizon. Most Si foundries are at 200 mm or higher and therefore compatibility with 150 mm SiC substrates at the present time is not ideal. There are a few 150 mm Si foundries in the world which may take advantage of the SiC technology to add a few more years to their useful life. Cost model and new equipment and processing requirements are discussed in this section.

### 11.4.1 Cost Model

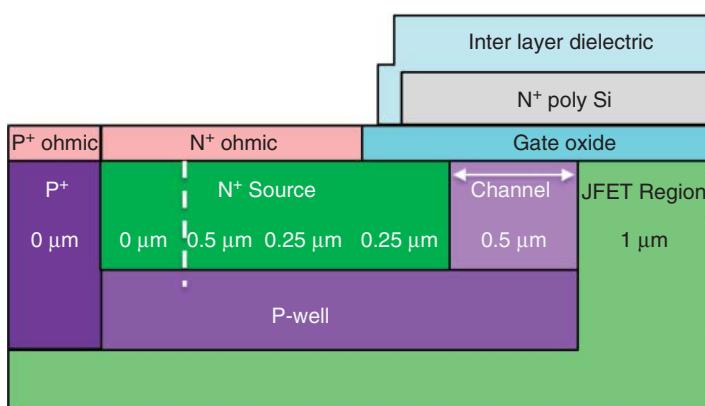
#### 11.4.1.1 Cost Roadmap for WBG Devices

A cost reduction roadmap based on cost models and the Fabless Foundry concept has been developed by Woongje Sung and shows the feasibility of achieving *Power-America* Institute's wide-bandgap (WBG) price goals in three to five years [166].

Referring to Figure 11.38, a DMOSFET structure with a pitch of 5  $\mu\text{m}$  has been modeled by Woongje Sung. It has  $\text{p}^+$  contact regions placed orthogonally to the  $\text{n}^+$  contacts. The structure was modeled for various voltage ranges.

The doping and drift layer thickness values are shown in Table 11.1 along with modeled values for specific on resistances. The average inversion layer mobility was assumed to be  $20 \text{ cm}^2/\text{Vs}$  and the substrate thickness  $180 \mu\text{m}$ . The chip size was calculated for a maximum current rating of  $20 \text{ A}$  (junction temperature of  $150^\circ\text{C}$ ) assuming a gate pad size of  $0.4 \text{ mm}^2$ , dicing lane of  $50 \mu\text{m}$ , and edge termination width of five times the drift-layer thickness.

Assuming the price of a 150 mm SiC substrate and epilayer, as shown in Table 11.1 (these costs are based on basic calculations using SiC powder cost, capital cost



**Figure 11.38** Cross-section of the MOSFET structure modeled.

of furnaces, and other equipment such as wafering and polish, manpower, and utility bills and adding in 25% profit margin by the supplier), a processing cost of \$800/wafer (this can be reduced to \$500/wafer in high volume), production in a commercial silicon foundry, and adding a gross margin of 50% (price =  $2 \times$  the cost), the projected price of SiC chips is shown in Table 11.1. The overall yield is assumed to combine testing and manufacturing (breakage, miss-processing, etc.) yields. The price for a 1.2 kV, 20 A SiC chip is calculated to be 4.7 cents/A, significantly below the *PowerAmerica*'s target of 10 cents/A. The 15 kV SiC chip should be priced at \$3/A assuming a yield of 50% and \$3000 for the 150 mm substrate + epilayer.

If the industry can approach these numbers in three to five years (this seems to be very feasible given the demands of the automotive segment), then the device demand will grow exponentially across multiple applications. Furthermore, 200 mm SiC substrates, expected by 2020–2021, will further reduce the cost of SiC MOSFETs. Additionally, other devices such as JFETs are expected to cost significantly less due to their superior specific on-resistance.

This model applies to a fabless company manufacturing SiC power MOSFETs in a mixed Si/SiC foundry which buys 150 mm SiC substrates and epitaxial layers from vendors who have their own profit margins included in the price of the material. The sawing and testing cost is included in the foundry cost. What is not included is packaging yield (typically 95%) and packaging cost (typically 1–2 cent in large-volume packaging facility in TO-247 or equivalent package). High-voltage devices will require more sophisticated packages and modules which will cost much more.

**Table 11.1** Calculation of potential price/Amp for 20 A max rated SiC chips at different voltages in a high volume commercial 150 mm mixed Si/SiC Foundry.

	1.2 kV	1.7 kV	3.3 kV	4.5 kV	6.5 kV	10 kV	15 kV
Drift layer doping ( $\text{cm}^{-3}$ )	$1 \times 10^{16}$	$7 \times 10^{15}$	$3 \times 10^{15}$	$2 \times 10^{15}$	$1.2 \times 10^{15}$	$8 \times 10^{14}$	$4 \times 10^{14}$
Drift layer thickness ( $\mu\text{m}$ )	10	15	30	40	60	95	145
$R_{\text{on,sp}}$ ( $\text{m}\Omega\cdot\text{cm}^2$ )	1.7	2.5	7.8	14.5	34.0	77.8	237.8
Chip area ( $\text{mm}^2$ )	3.7	4.5	8.0	11.0	17.3	28.0	50.9
Overall yield (%)	85	84	82	80	75	67	50
Packing factor	0.945	0.939	0.925	0.914	0.902	0.890	0.846
Price for 150 mm SiC + epilayer (\$)	800	881	1126	1289	1615	2185	3000
<i>Price per Amp (\$/A) (50% Gross margin assumed)</i>							
Price (\$/A) for 20 A maximum	0.047	0.062	0.133	0.205	0.402	0.910	2.91

### 11.4.2 New Equipment and Processing Requirements

The requirements for additional equipment and/or unit process steps needed for SiC technology when implemented in a commercial Si Foundry are listed below:

1. *Dry etch*: Since SiC is relatively inert, it is not possible to use wet etching. Therefore, dry RIE equipment is needed to etch SiC such as alignment marks, backside etching of vias or thinning with a high etch rate, and trench etch for JFETs or trench MOSFETs. ICP etch systems are popular for etching SiC.
2. *Ion-implantation and post implantation anneal*: As mentioned earlier in this chapter, ion implantation above the amorphization dose of  $10^{15} \text{ cm}^{-2}$  is carried out at high temperature ( $350\text{--}650^\circ\text{C}$ ). This requires implanters especially equipped with a hot wafer stage. Also, since annealing is carried out at approximately  $1700^\circ\text{C}$  with a graphite cap layer, a special anneal equipment is needed for batch processing. The most important considerations are temperature ramp rates and temperature uniformity within the chamber across the substrate and from substrate to substrate in a stack of typically 10–24 substrates.
3. *Gate oxide furnace*: Gate oxidation is critical for SiC MOS devices. Presently, the high density of interface traps at the 4H-SiC/SiO<sub>2</sub> interface limits the effective inversion layer mobility in the 4H-SiC MOSFETs to typically  $15\text{--}20 \text{ cm}^2/\text{Vs}$ . Even this low value is achieved by POA in NO gas at high temperatures. Therefore, specialized oxidation furnace (Quartz or poly SiC tubes), with dry oxidation capability, equipped with NO gas fittings and associated safety measures is required.
4. *Frontside ohmic contact rapid thermal anneal (RTA) furnace*: Typically, SiC ohmic contacts to the frontside are made with Ni (for n<sup>++</sup> ohmics) and Ti/Al (for p<sup>++</sup> ohmics) by evaporating 10–20 nm of metals and annealing them between 800 and  $1050^\circ\text{C}$  for a few minutes. Separate RTA furnaces are recommended for SiC processing in a Si process line to avoid cross contamination.
5. *Backside ohmic contact and thinning systems*: It is important to thin the substrate to 100–150  $\mu\text{m}$  from a standard thickness of 350  $\mu\text{m}$  to reduce the substrate resistance from approximately 0.7 to 0.2–0.3  $\text{m}\Omega \text{ cm}^2$ . This is important in devices rated at 1200 V or below. This is completed as a last step in the process sequence by mounting the frontside of the processed wafer down on a lapping fixture and grinding the backside to the desired thickness. After this, the backside is cleaned while keeping the wafer mounted and a thin metal Ni layer is evaporated on the backside. The Ni is annealed by a raster scan of a laser beam. The wavelength of the laser beam is selected such that it is completely absorbed in a small depth of the SiC and the heat does not reach the frontside of the processed wafer. After this, suitable overlayer is sputtered on the backside and the substrate is released from the lapping plate. The suitable backside lapping and laser anneal systems are needed for this purpose. If the target device voltages are 1700 V or greater, then this step can be skipped.
6. *Transparent wafers*: SiC wafers are transparent to visible light. This may complicate photolithography as the focal plane is determined with the use of an optical microscope. Other tools may be needed (software/gain/hardware adjustments to

move to wavelengths where SiC is opaque) to process SiC wafers through steppers in a Si Fab.

7. *Steppers with long objective length:* Relative lack of flatness in SiC wafers can complicate photolithography and other processing particularly of high-voltage devices (thick drift epitaxial layers). High-temperature processes can further impact wafer flatness. For SiC power devices, “I-line” (365 nm) steppers are usually sufficient which can create 350 nm wide lines. Lense with a long objective length can help with focussing on warped wafers.

## 11.5 Dedicated Foundries vs. Commercial Foundries

SiC devices used to be fabricated in dedicated SiC foundries where the foundry is owned by one user. A good example is General Electric’s 100 mm fab facility in Niskayuna, NY, and 150 mm fab at The New York Power Electronics Manufacturing Consortium (PEMC), led by SUNY Poly in Albany, NY. This model slowed down the development as many researchers and companies were left out since they could not afford to have their own Fabs. Building a dedicated Fab costs \$100–200 M USD and takes a long time to become profitable because the fab has to be fully loaded. It should be noted that PEMC has closed its doors and is looking for industrial partners to be viable at the time of writing this chapter. However, the advantage of this approach is that the dedicated user has the full flexibility of changing the process as needed to improve the performance of SiC devices. This indeed has been proven since the GE devices have demonstrated the best performance and reliability.

*PowerAmerica*, in 2015, introduced the idea of a commercial Si Fab (XFAB in Lubbock, Texas) that can be equipped to handle a small volume of 150 mm SiC wafers along with a high volume of silicon wafers. This was accomplished by a small investment of less than \$20 M shared equally by *PowerAmerica* and XFAB. These funds were used to buy SiC-specific equipment listed in the previous section. This enabled a lot of small companies to be fabless and yet utilize a well-functioning production facility with high yields where the major cost of running the fab is borne by high Si volume. This proved to be a highly successful model, and as a result, SiC design innovations and production increased rapidly by 25+ users, each with moderate volume. More players mean more innovations in the technology. A secondary benefit of this approach was that it provided a concept of adding 10–15 years to an otherwise obsolete Si foundry. This approach is now being used worldwide. However, XFAB evolved and grew with each user bringing its own process to the foundry. As a result, XFAB is having to manage many different process flows with minor differences between them. This makes it difficult to ramp up volume. Furthermore, small researchers and many small companies were left out of using XFAB as they did not bring enough volume to the fab. A big advantage of this approach has been to reduce the cost of SiC components very rapidly as the fab cost is lower by leveraging Si processes and equipment which are fully depreciated. The major cost of SiC fabrication is in starting material (substrates + epilayer) as seen in the discussion of cost earlier in this chapter. By combining volumes by many users, the foundry can get huge discounts on starting material.

The best approach would be to convert an existing commercial Si Fab to a mixed Si/SiC Fab, which can offer its own process flow and SiC-specific unit processes such that almost all users (small and moderately big) can use almost the same process with minor differences. This setup will allow users to bring their innovative design ideas to the market with a relatively small expense. The volume can be rapidly ramped up across 100+ users and cost can be further reduced. Having the same process means several projects can be combined on a single mask set so that the individual cost to each project can be further reduced along the lines of highly successful Si program called “MOSIS”. Reducing the cost of innovation will prove to be a game changer in the future. As mentioned before, this can be done by investing \$15–20 M USD by simply purchasing SiC-specific equipment listed in the previous section.

Another concept would be to build a fab dedicated to SiC manufacturing but run it as a prototyping or commercial foundry with one process flow and design rules. The number of users can again be ramped up easily. However, the initial capital cost of building an SiC-dedicated fab and ramping up the process over two to three years with small number of initial users may be a drawback of this approach. Clas-SiC foundry in Scotland has been fashioned after this model. As of writing this chapter, it has successfully developed the Schottky diode process and is engaged in developing a planar SiC MOSFET process. Once they are ready to offer the process and design kit to the users, it is expected that business will ramp up very quickly. Just getting there requires an investment of approximately 100 M USD. It may take five years to be profitable and fully load the foundry capacity.

As the volume goes up to 50–100 000 SiC wafers per month in the future, enabled by Electric Vehicles, and the 200 mm SiC substrates become the norm, many of the abovementioned foundry models will exist and will serve various needs of customers. It is absolutely certain that the fabless approach will bring about many innovations in this area.

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## 12

### Unipolar Device in SiC: Diodes and MOSFETs

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#### 12.1 Introduction

Power devices in 4H-silicon carbide (4H-SiC) show great performance advantages as compared to those made with other semiconductors. Compared to silicon, 4H-SiC has one order of magnitude higher breakdown electric field ( $2\text{--}4 \times 10^6 \text{ V/cm}$ ), while bulk electron mobility is only about 20% lower than that of silicon. The drift layer of a 4H-SiC power device may have one-tenth the thickness and one hundred times the doping concentration of the drift layer of a silicon power device with the same blocking capability, resulting in about a factor of 800 reduction in drift layer resistance for 4H-SiC power devices. Because of this advantage, high-voltage ( $>600 \text{ V}$ ) 4H-SiC power devices have significantly smaller die size compared to those of silicon power devices with comparable on-state resistance and blocking voltage.

The thinner and higher doped drift layers in 4H-SiC devices result in approximately a factor of 10 larger drift layer capacitances per unit area, which translates into 10 $\times$  greater stored energy, often represented as  $\frac{1}{2}CV^2$ , per unit area, compared to silicon devices with the same blocking voltage. However, due to the much smaller device area of 4H-SiC devices for the same on-state resistance, total device capacitance and stored energy in 4H-SiC are expected to be up to a factor of 80 smaller than silicon devices with comparable blocking voltage and on-resistance. Because of the lower drift layer capacitance and stored energy, 4H-SiC power devices can offer operation at significantly higher switching frequencies, theoretically up to 80 times faster than what silicon devices can offer, while providing equal or better system efficiency.

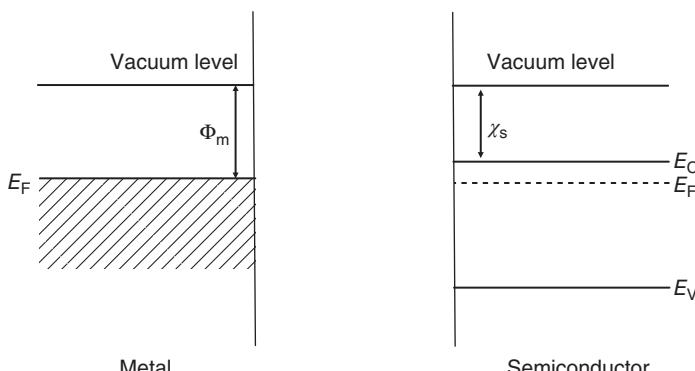
4H-SiC is not the only wide bandgap semiconductor material available. However, 4H-SiC stands out because of the availability of high-quality commercial substrates, and it can be thermally oxidized to form high-quality gate oxide layers for metal-oxide-semiconductor (MOS) devices. In addition, fabrication processes for selective doping, for both p- and n-type, are well established in silicon carbide, which enables realization of most power devices structures, including Schottky and PiN diodes, bipolar junction transistors (BJTs), gate turn off (GTO) thyristors, metal oxide semiconductor field-effect transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs).

In this chapter, basic physics of device operations for the unipolar diodes and power MOSFETs will be discussed. Recent experimental demonstrations and developments will be reviewed and presented.

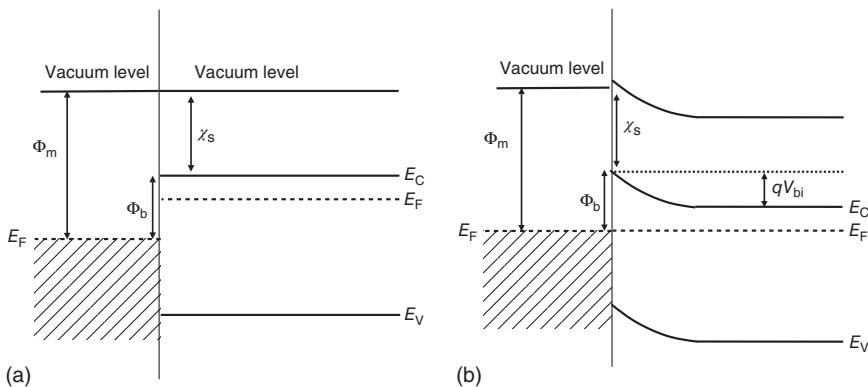
## 12.2 Unipolar Diodes – 4H-SiC JBS Diodes

The band structure for the metal and the semiconductor, when they are electrically and physically isolated from each other, is shown in Figure 12.1. For simplicity, only n-type semiconductor material with Fermi level positioned above that of the metal is shown, which is the case for most of the n-type 4H-SiC and metal combinations in use today. The work function of the metal ( $\Phi_m$ ) is defined as the energy required to move an electron from the Fermi level ( $E_F$ ) position in metal to a state at rest outside the surface of metal, which is called the vacuum level. The work function can also be defined similarly in semiconductors as the energy required to move an electron from the Fermi level in the semiconductor to a state at rest outside the surface of the semiconductor. It should be noted that the Fermi level in semiconductor is placed within the bandgap, where electrons cannot reside in equilibrium. Instead of work function, electron affinity ( $\chi_s$ ), defined as the energy required to move an electron from the bottom of the conduction band to the vacuum level, is more commonly used in semiconductors.

Figure 12.2 shows the energy band diagram when an intimate connection is made between the metal and the semiconductor. The vacuum level must be continuous across the interface between the metal and the semiconductor as shown. This forces formation of a barrier between the metal and the conduction band of the semiconductor, referred to as the Schottky barrier, with a barrier height ( $\Phi_b$ ) determined by the difference between the metal work function and semiconductor electron affinity. When the metal and the semiconductor are electrically connected, through power supplies or characterization systems, electrons are transferred from the semiconductor to the metal to establish thermal equilibrium. The energy band diagram after thermal equilibrium, where Fermi levels for both sides line up, is



**Figure 12.1** Energy band diagrams for a metal and a semiconductor.



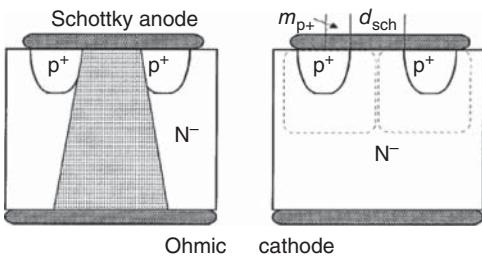
**Figure 12.2** Energy band diagrams for a metal–semiconductor system. (a) After an intimate contact and (b) after thermal equilibrium.

shown in Figure 12.2. The transfer of electrons provides negative charge on the metal side, which is equal in magnitude to the positive charge in the depletion region at the surface of the semiconductor. The voltage formed across the depletion region at thermal equilibrium is referred to as the built-in voltage ( $V_{bi}$ ).

When a negative bias is applied to the semiconductor side with respect to the metal side (forward bias), the height of barrier electrons in the semiconductor side that has to jump over to flow into the metal side reduces and electrons with sufficient energy can transport over the potential barrier into the metal. The current formed by this phenomenon is called thermionic emission current, which increases exponentially with the applied bias. For high-voltage ( $>600$  V) power switching diodes in 4H-SiC, the structure is built with using an n-type semiconductor layer with relatively low doping concentration, typically  $5 \times 10^{16} \text{ cm}^{-3}$  or lower, with a thickness of several microns ( $\mu\text{m}$ ), which results in a series drift resistance. When a forward bias of greater than  $V_{bi}$  is applied, the current through the structure increases linearly with applied bias, with the slope defined by the series drift resistance.

When a positive bias is applied to the semiconductor side with respect to the metal side (reverse bias), the depletion region extends into the semiconductor and supports the voltage. The leakage current of the Schottky barrier diode (SBD) is dominated by the thermionic emission from the metal, which depends exponentially on the Schottky barrier height. It should be noted that the Schottky barrier height reduces with increasing E-field in reverse bias due to image force barrier lowering. Combination of those two effects results in reverse leakage current that increases with temperature and bias.

Junction barrier Schottky (JBS) diode structure [1–3], also referred to as merged PiN Schottky (MPS) diode structure [4], minimizes the impact of image force barrier lowering. Cross sections of a 4H-SiC JBS rectifier operating in the forward and reverse bias are shown in Figure 12.3. A JBS diode consists of interdigitated Schottky and p<sup>+</sup> areas, which are mostly formed by ion implantations in 4H-SiC. In forward bias, only the Schottky regions of the diode conduct provided that the voltage drop across the pn junction, formed at the p<sup>+</sup> region and the n<sup>–</sup> drift layer,

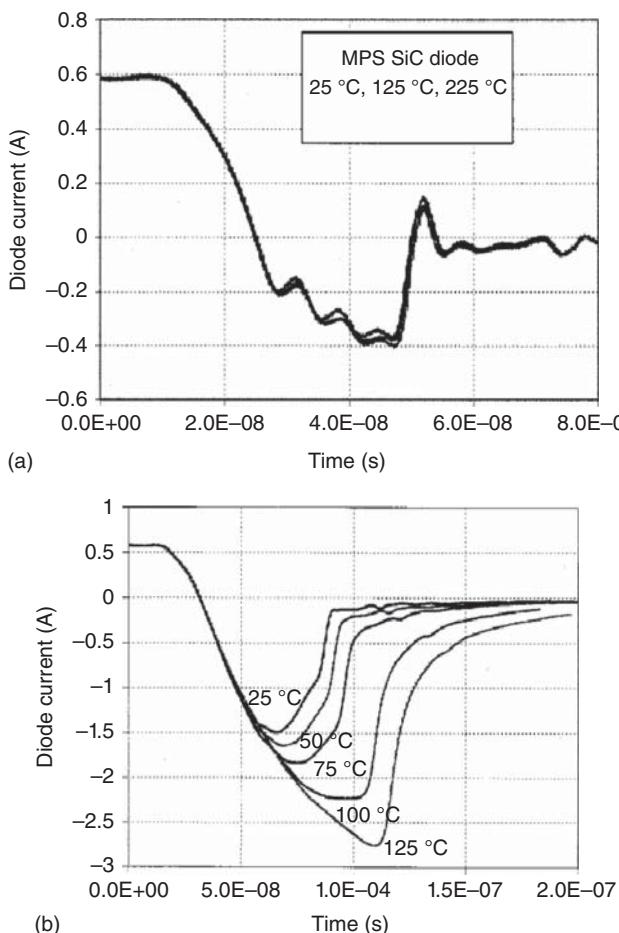


**Figure 12.3** Junction barrier Schottky diode structures [4]. On-state current flows through the Schottky anode, while reverse leakage is limited by depletion from adjacent grids in a JBS diode. Source: Hefner et al. [4]. © 2001, IEEE.

is less than 3 V. In reverse bias, the  $p^+$  areas provide shielding to the Schottky barrier formed at the metal– $n^-$  SiC interface. As the reverse bias increases, the depletion regions from adjacent  $p^+$  regions pinch-off the leakage current from the Schottky contacts of the device. The presence of the  $p^+$  regions reduces the  $E$ -field at the metal– $n^-$  SiC barrier because of two-dimensional charge sharing, where  $E$ -field lines originating from positively charged donors in the drift layer terminate in the negatively charged acceptors in the  $p^+$  regions. This is a very important feature for devices in 4H-SiC, with very high breakdown  $E$ -field and high power density resulting in high junction temperatures. Most, if not all, of the commercially available 4H-SiC Schottky diodes are utilizing the JBS structure for superior blocking performances at elevated temperatures.

The biggest benefit of 4H-SiC JBS diodes is in the reverse recovery characteristics. Figure 12.4 compares the reverse recovery characteristics of a 1500 V 4H-SiC JBS diode and a 1000 V ultrafast silicon PiN diode [4]. The recovery of the 4H-SiC JBS diode is mostly capacitive in nature, and the amount of reverse recovery charge represents depletion capacitance of the drift layer. Hence, the reverse recovery waveforms show virtually no temperature dependence throughout the temperature range used for the measurements, as shown in Figure 12.4. On the other hand, silicon diode reverse recovery waveforms showed much larger amount of reverse recovery charge and time, which increased significantly with the temperature, as shown in Figure 12.4. This indicates that the excess charge storage is far greater than the junction depletion charge and can seriously impact the switching performance of the diode. A factor of 2 increase in reverse recovery time (50 ns at 25 °C, to 100 ns at 100 °C) and a factor of 4 increase in reverse in reverse recovery charge were measured, leading to an unfavorable positive feedback between switching losses and further temperature increase.

The benefits of reduced reverse recovery charge show up in the turn-on losses in the switches. Figure 12.5 shows the schematics of a constant current mode (CCM) active power factor correction (PFC) booster converter [5]. One of the most common applications for the 4H-SiC JBS diode is the use as a boost diode in the PFC circuit. Figure 12.6 shows the reverse recovery waveforms, both voltage and current, of a 4H-SiC JBS diode and a silicon PiN diode. It should be noted that voltage rise is almost immediately observed for the 4H-SiC JBS diode, but the voltage rise is delayed for the silicon PiN diode structure until the peak reverse recovery current has been reached [4]. This means the switch, shown as the MOSFET in Figure 12.5, experiences full load supply voltage at full current (load current plus the reverse recovery

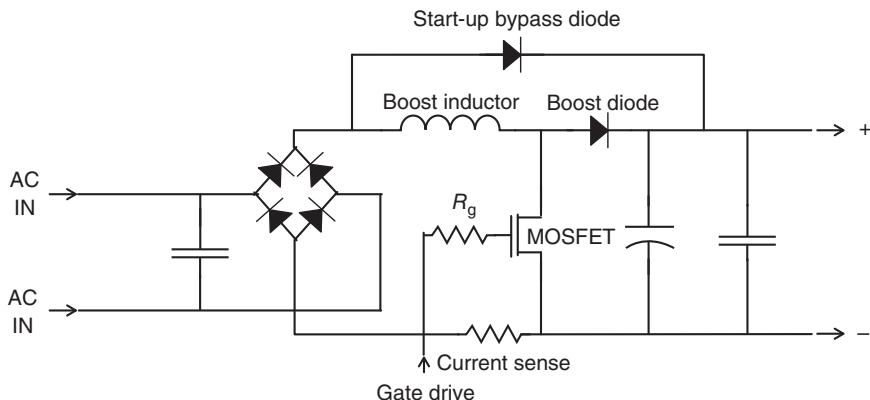


**Figure 12.4** Measured temperature dependence of the reverse recovery characteristics for (a) a 1500 V, 0.5 A 4H-SiC MPS (JBS) diode [4], and (b) a 1000 V, 1 A ultrafast Si PiN diode (MUR1100). Source: Hefner et al. [4]. © 2001, IEEE.

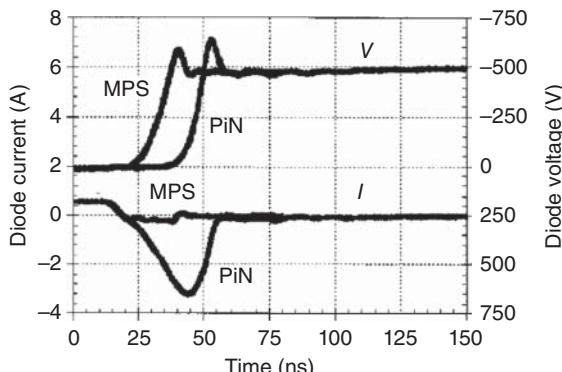
current of the diode) during the turn-on transients until a peak reverse recovery current is reached, resulting in very high turn-on losses. The use of 4H-SiC JBS diode, instead of the silicon PiN diode, significantly reduces the stress on the switch due to reduced current requirement, as well as voltage stress since the switch voltage starts decreasing without delay. This feature allows system designers to use MOSFETs with significantly reduced current ratings, resulting in substantial cost savings, as well as clear improvements in system efficiency [5].

### 12.2.1 Optimization of 4H-SiC JBS Diodes

Commercial availability of high-performance 4H-SiC JBS diodes revolutionized the power industry. However, the adoption of 4H-SiC JBS diodes was limited to high-end switching power applications. The cost of silicon carbide devices was still very high.



**Figure 12.5** Active power factor correction boost converter. Source: Wolfspeed [5]. © 2012 Cree, Inc.



**Figure 12.6** Comparison of the reverse recovery characteristics of the 4H-SiC MPS (JBS) and silicon PiN diode (MUR1100) at a  $dI/dt$  of  $100 \text{ A}/\mu\text{s}$ . Source: Hefner et al. [4]. © 2001, IEEE.

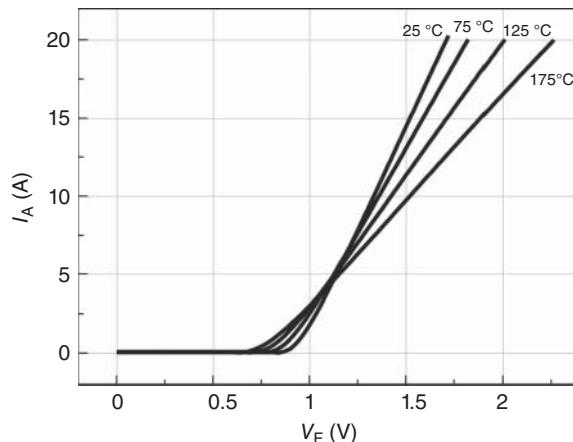
To win wider acceptance in a wide range of applications, further optimization of the 4H-SiC JBS diode structure was necessary. The following improvements were made to the 4H-SiC JBS diode structure to answer these challenges.

- Improvements in surge current capability.
- Further reduction in forward voltage drop.
- Increase in current conduction capability.

### 12.2.1.1 Injection from the $p^+$ Regions for Surge Operation

4H-SiC JBS diodes show typical characteristics of majority carrier devices. The forward resistance depends on the resistivity of the drift layer, which is determined by doping concentration and electron mobility in the layer. The electron mobility reduces with temperature due to lattice scattering, which results in an increase of drift resistance and the forward voltage drop ( $V_F$ ) of the diode; hence, the positive temperature coefficient of  $V_F$  is achieved as shown in Figure 12.7, while a negative temperature coefficient of  $V_F$  is observed for silicon bipolar diodes. This is a great feature when paralleling multiple discrete power devices, when a suitably rated single device is not available. Paralleling can also help to simplify thermal management

**Figure 12.7** Forward bias curves of a 600 V 4H-SiC Schottky diode as a function of temperature.

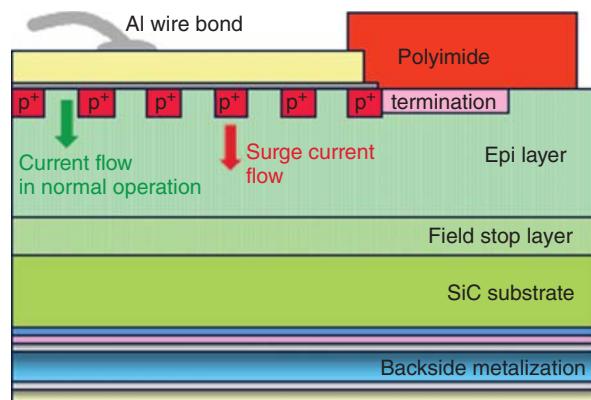


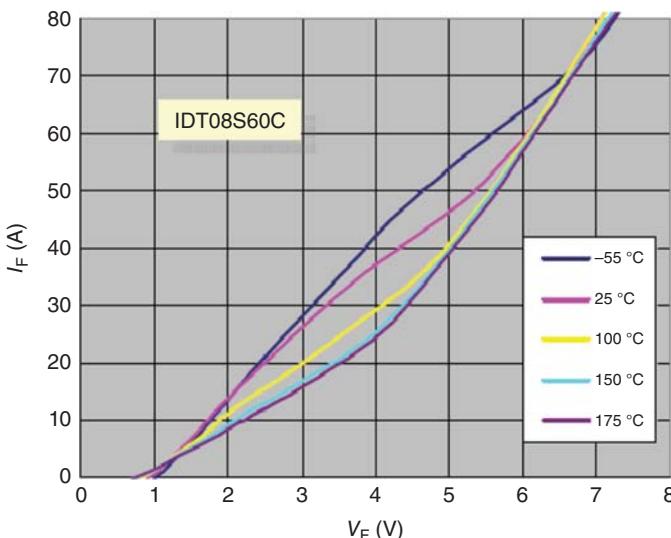
by distributing power losses evenly to a larger area in a module [6]. The positive temperature coefficient of  $V_F$  helps to balance currents among paralleled devices. The device carrying more initial current experiences higher power dissipation and heats a little more than its neighbors. This results in an increase of  $V_F$ , which causes the current to decrease. A stable operating point is reached where currents through all the devices are balanced, though junction temperature of each device may be slightly different.

However, the positive temperature coefficient of  $V_F$  can cause a thermal runaway when the device is exposed to surge current stress [7]. One example of the surge current situation is start-up conditions, where output capacitance charges up to a steady state value, for which a silicon bipolar diode can be used as the start-up bypass diode, as shown in Figure 12.5 [5].

This weakness was addressed by optimizing p regions within the JBS diode with respect to emitter efficiency and conductivity, which can eliminate the needs for an additional surge current bypass diode [6, 7], as shown in Figure 12.8. During normal forward operation at typical operating currents, only the unipolar structure of the device is active with fast turn-off characteristics. However, under transient

**Figure 12.8** SiC diode with merged p-doped islands (MPS structure). Source: Rupp et al. [7]. © 2006, IEEE.





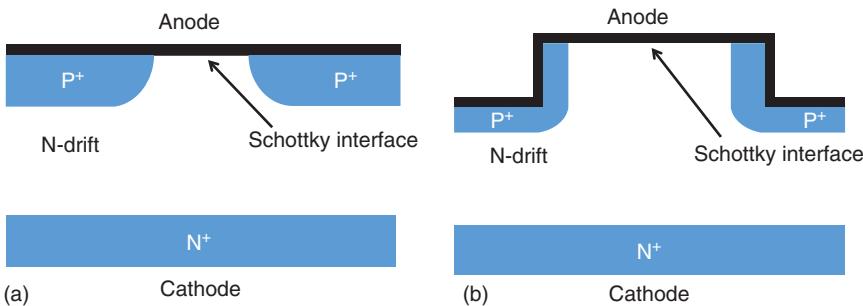
**Figure 12.9**  $I$ - $V$  characteristics for different temperatures of an 8 A/600 V MPS SiC diode. The various temperature curves all merge in one straight line corresponding to the nearly temperature independent substrate resistivity. Source: Rupp et al. [7]. © 2006, IEEE.

forward surge conditions, the embedded PiN diodes turn on, enabling the device to conduct the extreme surge current while maintaining low  $V_F$ , thus enabling it to survive a transient event that would otherwise cripple a pure unipolar diode [6].  $I$ - $V$  characteristics for different temperatures of an 8 A/600 V MPS SiC diode are shown in Figure 12.9 [7]. The onset of minority carrier injection reduces with temperature because of the reduced effectiveness of the shunt across the  $p^+$  $n$  junction, caused by increased unipolar resistance in the  $n$ -region. In the minority carrier injection mode at high current density, the remaining drift layer resistance becomes negligible compared to the substrate resistance, which leads to temperature insensitive forward characteristics, as shown in Figure 12.9 [7].

### 12.2.1.2 Trench JBS Diodes

It was discussed in Section 12.2 that the JBS or MPS structure shields the Schottky interface from the high  $E$ -field, which in turn improves the reverse blocking performance. In 4H-SiC dopant, diffusivity is negligible. The junction depth of  $p^+$  $n$  junction is limited by practical ion implantation energies and implant straggle and is fairly shallow, which limits the  $E$ -field protection at the Schottky interface. As a result, majority of leakage current comes from the Schottky contact area, which can be high at operating junction temperatures. The high leakage current makes it very challenging to develop large amperage Schottky diodes with a reasonable cost in 4H-SiC. In addition, further cost reduction by reducing the die size is extremely difficult unless the Schottky leakage current is significantly reduced.

Trench JBS diodes in 4H-SiC [8–11] were developed to alleviate this problem. To improve shielding of the Schottky interface,  $p^+$  regions with deep junction depth



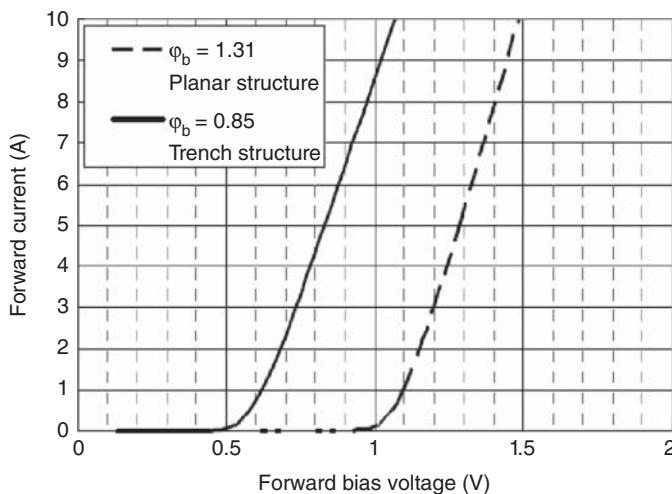
**Figure 12.10** Cross-sectional views of (a) planar JBS and (b) trench JBS diodes.

and high aspect ratio are necessary. A comparison of planar JBS diode structure and trench JBS diode structure is given in Figure 12.10. In trench JBS diodes, the trenches are formed using dry etching, which include reactive ion etching (RIE), then the p-type impurities are implanted along the sidewall and bottom of the trenches. With the same ion implantation energy, the junction barrier can be largely extended below the Schottky interface and a substantial reduction in image force barrier lowering [8].

A comparison of blocking performance of 650 V, 10 A 4H-SiC planar and trench JBS diodes fabricated on the same wafer was reported [8]. The trench JBS diode clearly showed improvements in the blocking performance, showing an increase of approximately 150 V in blocking voltage. This suggests that for the same blocking voltage rating, the trench JBS diode structure allows drift layers with heavier doping concentration so that the differential specific on-resistance can be reduced, resulting in smaller chip sizes. Similar comparisons were made using 1200 V, 20 A diodes. In addition, the leakage current distribution for the trench structure becomes much tighter than that of the planar structure, indicating the lower  $E$ -field at the Schottky interface significantly reduced the role of imperfections of the wafer, such as doping and thickness variation of the drift layer and the effects of crystal defects [8].

### 12.2.1.3 Use of Low Work Function Metal for Anode Metal

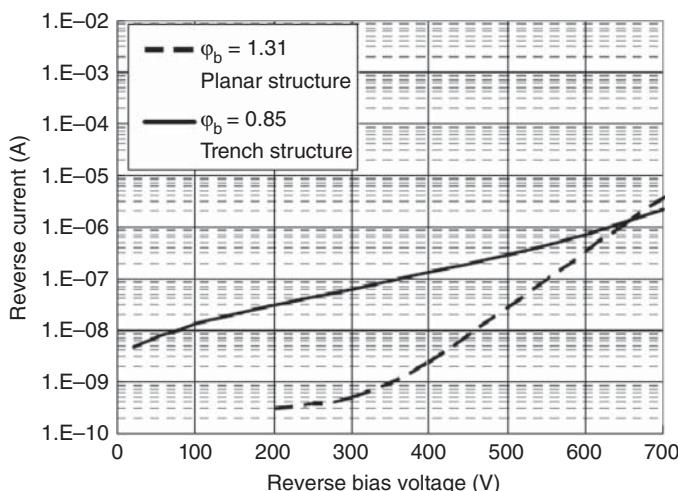
Continuous efforts are being made to reduce forward voltage drop ( $V_F$ ) of the 4H-SiC JBS diodes. Such reductions lead to smaller die size, which results in a reduction in cost, and a reduction in switching losses due to decreased device capacitances. One of the approaches to achieve this goal is to use heavier doped, thinner drift layer to reduce drift layer resistance, which results in lower differential on-resistance, discussed in Section 12.2.1.2. The other approach is to use lower barrier height metal for the Schottky interface, such as tantalum (Ta)- [12] and molybdenum (Mo)-based materials [13, 14], to reduce the knee voltage or threshold voltage of the diodes. The reduction in  $V_F$  was demonstrated using two Schottky interfaces, one with a barrier height of 1.31 eV, and the other with a barrier height of 0.85 eV [9]. The diodes had an active area of  $3.05 \text{ mm}^2$  and used  $5 \mu\text{m}$  thick drift layer with a doping concentration of  $1.0 \times 10^{16} \text{ cm}^{-3}$ . The diode with lower barrier height utilized the trench JBS structure to minimize leakage current in the reverse bias. A trench JBS diode with



**Figure 12.11** Forward  $I$ - $V$  characteristics of the planar structure and the trench structure. The difference of threshold voltage is related to barrier height. Source: Nakamura et al. [9]. © 2011, IEEE.

a lower barrier height metal showed 0.48 V smaller threshold voltage compared to the planar structure, as shown in Figure 12.11. Figure 12.12 shows the  $I$ - $V$  characteristics in the reverse bias. The trench structure has higher reverse leakage current at lower bias due to the lower barrier height Schottky interface. At higher biases, the leakage current of the trench structure is less than that of the planar structure due to more effective shielding of the Schottky interface.

It should be noted that the rate of increase in leakage current, as a function of temperature, is greater for low barrier height Schottky interface devices [14].



**Figure 12.12** Reverse  $I$ - $V$  characteristics of the planar structure and the trench structure. Source: Nakamura et al. [9]. © 2011, IEEE.

The increased leakage current leads to static power loss in the blocking state, which can impact system efficiency. When designing a JBS diode using low barrier height Schottky metal, proper shielding of the Schottky interface must be provided to keep the power losses due to reverse leakage current less than 1% of the nominal power losses [14].

## 12.3 Unipolar Switches: Power MOSFETs

A power MOSFET is an easy-to-drive device with high switching speeds, which makes it a very attractive option for power switching applications. The main advantage of the power MOSFET structure is the high impedance gate, which requires zero gate current in the steady state, and the gate drives are only required to provide relatively small amount of gate current to charge and discharge the capacitances. The current conduction in the power MOSFET structure occurs through transport of majority carriers in the drift region and does not involve minority carrier injection. Hence, there are no delays associated with storage or recombination of minority carriers in power MOSFETs. It is also easy to parallel multiple power MOSFETs because of the positive temperature coefficient of the forward voltage drop, due to the decrease in carrier mobility at elevated temperatures, which prevents current hogging and subsequent thermal runaways. In addition, the power MOSFETs do not go through second breakdown like bipolar junction transistors and offer excellent safe operating area.

On-resistance of a power MOSFET increases quite rapidly with blocking voltage of the device. For power MOSFETs in silicon, which is the most commonly used semiconductor material, the on-resistance of a power MOSFET can be very small if the design voltage of the device is 200 V or less [15]. Of course, power MOSFETs in silicon can be designed for voltages greater than 200 V. However, this results in unacceptably high on-resistance, large chip area, and significant increases in parasitic capacitances. Researchers in silicon power devices addressed this issue by placing an injecting junction at the drain side of the device, which reduced the drift layer resistance by minority carrier injection, or conductivity modulation of the drift layer [16, 17], resulting in the development of insulated gate bipolar transistors (IGBTs). The other approach used to reduce the on-resistance of silicon power MOSFETs is the use of superjunction (SJ) structure [18], which utilizes alternating n- and p-layers with relatively heavy doping concentrations. Excellent results have been achieved for devices with blocking voltages up to 900 V [19].

An IGBT provides significantly lower forward voltage drops compared to a conventional power MOSFET in higher blocking voltage ( $>600$  V) rated devices by injecting minority carriers from the backside (collector) into the drift region during the forward conduction. However, this reduction in on-state forward voltage drop comes with some serious drawbacks listed below.

- The on-state forward voltage drop in IGBTs includes a voltage drop across a forward biased pn junction. At higher current levels, IGBTs have lower conduction losses than power MOSFETs due to lower forward voltage drop. However, at lower

current levels, where forward voltage drop of power MOSFETs can be lower than the voltage drop across a pn junction, IGBTs have higher conduction losses than power MOSFETs.

- The additional pn junction blocks reverse current flow. Unlike power MOSFETs, IGBTs cannot conduct currents in the reverse direction. In applications where reverse current flow is needed, an external anti-parallel diode is required, which results in increases in the chip count and the system cost, as well as a reduction in power density. Developments in reverse conducting IGBTs (RC-IGBTs) [20], which require significantly more complicated fabrication processes, can address this weakness.
- The minority carriers injected into the drift region requires significant delays during the turn-on and turn-off transients. The delay in the turn-on results in voltage overshoots, and the delay in the turn-off results in tail currents. This results in longer switching times and substantially higher switching losses, when compared to a power MOSFET.

Power devices in wide bandgap materials, such as silicon carbide (SiC), gallium nitride (GaN), and gallium oxide ( $\text{Ga}_2\text{O}_3$ ), can address these issues. The wide bandgaps of these materials result in high breakdown  $E$ -fields, which allows thinner drift layer with significantly higher doping concentration. This allows designs of unipolar power devices with extremely low on-resistance, which addresses most of the issues discussed above. Fabrication processes, including techniques to form high-quality gate oxide films and selective doping methods, are well established in silicon carbide, which culminated in successful development and commercialization of silicon carbide power MOSFETs, while more developments are needed in other wide bandgap materials [21, 22].

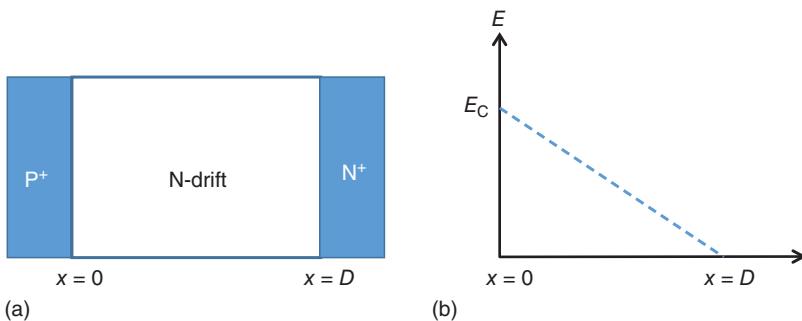
Various semiconductor materials, including III-V compounds and ternary alloys, as well as silicon were considered for vertical power FET structures, and it was shown that the power handling capability of the devices increases as the third power of the energy bandgap, and linearly with increase in electron mobility [23]. A figure of merit was developed to compare semiconductor materials for uses in unipolar power switching devices [23–25]. The figure of merit can also be used to gauge the level of optimization of a power device by comparing its performance to a theoretical maximum performance determined by the material properties.

Figure 12.13 shows a simple blocking structure and E-field distribution used for the derivation of the figure of merit. The structure consists of a blocking pn junction, a drift layer with a uniform doping concentration of  $N_D$  and a thickness of  $D$ , and an  $\text{N}^+$  layer which serves as the field-stop layer or backside contact. The maximum blocking voltage of this structure is achieved when the maximum  $E$ -field in the structure is equal to the critical field for avalanche voltage ( $E_C$ ), at which point breakdown occurs. The  $E$ -field reduces linearly as  $x$  increases, and the drift layer thickness  $D$  is selected so that  $E$ -field reduces to zero when  $x$  equals  $D$ .

The peak  $E$ -field, or  $E_C$ , can be calculated using Gauss's law

$$E_C = \frac{qN_D D}{\epsilon_s} \quad (12.1)$$

where  $\epsilon_s$  is the dielectric constant of the semiconductor material.



**Figure 12.13** Simplified blocking structure represented as a PiN diode (a), and  $E$ -field profile in blocking mode (b).

The breakdown voltage ( $V_B$ ) of the structure can be calculated using Poisson's equation

$$V_B = \frac{qN_D D^2}{2\epsilon_s} \quad (12.2)$$

The area normalized resistance of the drift layer can be calculated as below

$$R_{on} \cdot A = R_{on,sp} = \frac{D}{q\mu_n N_D} \quad (12.3)$$

where  $\mu_n$  is the bulk electron mobility of the semiconductor material.

From Eqs. (12.1) and (12.2), we can see that

$$D = \frac{2V_B}{E_C} \quad (12.4)$$

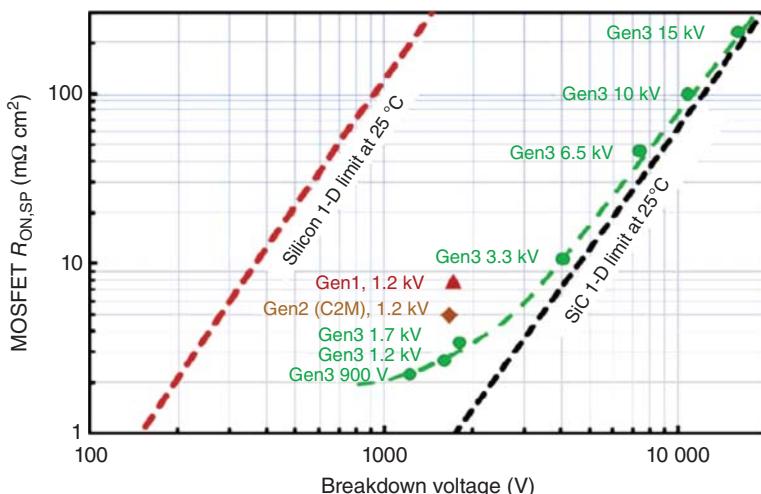
and

$$qN_D = \frac{\epsilon_s E_C^2}{2V_B} \quad (12.5)$$

When we insert (12.4) and (12.5) into Eq. (12.3), we get

$$R_{on,sp} = \frac{D}{qN_D \mu_n} = \frac{2V_B}{E_C} \cdot \frac{2V_B}{\epsilon_s E_C^2} \cdot \frac{1}{\mu_n} = \frac{4V_B^2}{\mu_n \epsilon_s E_C^3} \quad (12.6)$$

Theoretical specific on-resistance ( $R_{on,sp}$ ) values calculated using Eq. (12.6) are plotted in Figure 12.14 for silicon and 4H-SiC. Performance points of Wolfspeed (Cree) Power MOSFETs with blocking voltages ranging from 900 V to 15 kV are also shown on the plot. For devices with blocking voltages of 6.5 kV or higher, the performance points are close to the ideal silicon carbide 1-D limit, since the on-resistance of the devices is dominated by the drift resistance. For devices with blocking voltages of 3.3 kV or lower, the performance points deviate from the ideal 1-D limit due to other internal resistance components, such as MOS channel resistance and spreading resistance, to be discussed in Section 12.3.1.

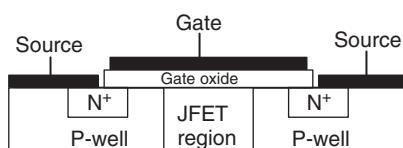


**Figure 12.14** Specific  $R_{ds}$ , on as a function of breakdown voltage. Included are points describing performance points using the avalanche breakdown voltage, of Wolfspeed (Cree) power MOSFETs at room temperature. Source: Lichtenwalner et al. [26].

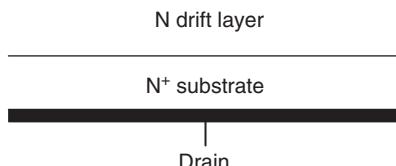
### 12.3.1 4H-SiC Power MOSFET Structures

#### 12.3.1.1 DMOSFETs

Figure 12.15 shows a simplified cross section of a power double implanted MOSFET (DMOSFET) in silicon carbide. The n<sup>+</sup> sources and MOS channel regions are built on implanted p-wells. The n<sup>+</sup> source regions and the p-wells are tied together using common contacts to source, to keep the potential difference between the two regions at minimum. The device turns on when a positive bias exceeding the threshold voltage of the device is applied to the gate electrode. In the on-state, electrons flow from the n<sup>+</sup> source regions through the MOS channel formed in the p-well into the junction field-effect transistor (JFET) region. The length of the MOS channel is determined by the distance from the edges of the n<sup>+</sup> regions and the p-wells, and the JFET regions are defined as the n-type region formed between



**Figure 12.15** Simplified cross section of a 4H-SiC DMOSFET.



adjacent p-wells. The electrons then spread into the drift layer and then flow into the n<sup>+</sup> substrate and exit the structure through the drain electrode. In the off-state, a bias less than the threshold voltage of the device is applied to the gate electrode, which removes the inversion channel in the MOS region in the p-well and isolates the n<sup>+</sup> regions from the JFET regions. The device turns into a PiN diode structure, which can block the voltage when a positive bias is applied to the drain electrode and allow current to flow through when a negative bias is applied to the drain electrode. It should be noticed that the depletion regions from the p-wells merge and provide shielding to the gate oxide layers. The doping concentration and the width of the JFET region should be set carefully to provide sufficient shielding to the gate oxide in the off-state, as well as low resistance during the on-state operation of the device [27].

**4H-SiC DMOSFET Resistance Components** There are several resistance components in the DMOSFET structure. The main components include MOS channel resistance, JFET resistance, drift resistance, and spreading resistance. There are other resistance components, such as contact resistance and substrate resistance, but those will be ignored in this calculation for simplicity.

The channel resistance ( $R_{ch}$ ) represents the resistance of the MOS inversion layer in the channel. In the on-state operation of the power DMOSFET, for low drain bias ( $V_{DS}$ ) values structure,  $R_{ch}$  can be expressed as below.

$$R_{ch} = \frac{L \cdot P}{2 \cdot \mu_{n,ave} \cdot C_{ox} \cdot (V_g - V_{th})} \quad (12.7)$$

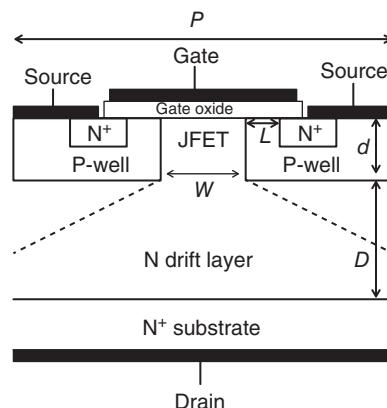
where  $L$  is the channel length and  $P$  is the device cell pitch, as shown in Figure 12.16.  $\mu_{n,ave}$  is the average MOS inversion layer mobility, and  $C_{ox}$  is the oxide capacitance per unit area ( $\epsilon_{ox}/t_{ox}$ ), and  $V_{th}$  is the device threshold voltage.

The JFET resistance ( $R_{JFET}$ ) represents the resistance through the narrow region between the p-wells. This resistance is determined by the doping concentration in the JFET region ( $N_D$ ), the width of the region ( $W$ ), and the depth of the p-well ( $d$ ) and can be expressed as below.

$$R_{JFET} = \frac{d \cdot P}{q \cdot \mu_{n,bulk} \cdot N_D \cdot W} \quad (12.8)$$

where  $\mu_{n,bulk}$  is the bulk electron mobility in the JFET region.

**Figure 12.16** 4H-SiC DMOSFET dimensions for on-resistance calculations.



Equation (12.8) ignores the impact of the depletion region formed at the metallurgical junction of the p-well and the n-drift layer, which becomes wider with a positive drain bias applied for normal on-state operation, increasing the JFET resistance. The JFET resistance reduces when a negative drain bias is applied, and as a result, the width of the depletion region reduces. This is the case when the power MOSFET is used as a synchronous rectifier.

The drift resistance ( $R_{\text{drift}}$ ) represents the resistance through the drift layer. For this calculation, a parallel plate operation with uniform current density is assumed. This resistance can be expressed as below.

$$R_{\text{drift}} = \frac{D}{q \cdot \mu_{n,\text{bulk}} \cdot N_D} \quad (12.9)$$

where  $D$  is the drift layer thickness. This is identical to Eq. (12.3).

The spreading resistance ( $R_{\text{spread}}$ ) represents the increase in on-resistance when electron flow exits the narrow JFET gap into a much wider drift layer, shown as the dotted line in Figure 12.16. Due to conductivity anisotropy in 4H-SiC [28, 29], electron mobility in the vertical direction is approximately 15% greater than the electron mobility in the lateral direction. The current spreads with a 41° angle, and the resistance in the cone depicted in Figure 12.16 can be calculated as below.

$$R = \frac{P}{q \cdot \mu_{n,\text{bulk}} \cdot N_D} \int_0^X \frac{1}{W + 1.74y} dy \quad (12.10)$$

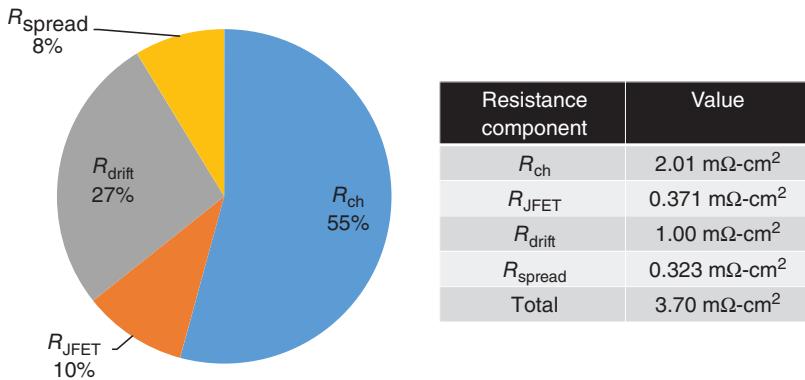
where  $y$  is the depth under the metallurgical junction and  $X$  is the depth at which the width of the cone equals the cell pitch  $P$ . With a spreading angle of 41° angle, it can be shown that  $X$  equals  $0.575(P - W)$ . With this assumption, Eq. (12.10) simplifies to the following expression.

$$R = \frac{P}{1.74q \cdot \mu_{n,\text{bulk}} \cdot N_D} \ln\left(\frac{P}{W}\right) \quad (12.11)$$

Since the spreading resistance represents the increase in resistance due to current spreading, the ideal resistance of the resistance needs to be subtracted from Eq. (12.11). Hence, the spreading resistance can be expressed as below.

$$\begin{aligned} R_{\text{spread}} &= \frac{P}{1.74q \cdot \mu_{n,\text{bulk}} \cdot N_D} \ln\left(\frac{P}{W}\right) - \frac{P-W}{1.74q \cdot \mu_{n,\text{bulk}} \cdot N_D} \\ &= \frac{P}{1.74q \cdot \mu_{n,\text{bulk}} \cdot N_D} \left( \ln\left(\frac{P}{W}\right) - 1 + \frac{W}{P} \right) \end{aligned} \quad (12.12)$$

Assuming  $\mu_{n,\text{ave}}$  of  $12 \text{ cm}^2/\text{V s}$ ,  $\mu_{n,\text{bulk}}$  of  $700 \text{ cm}^2/\text{V s}$  at room temperature, a cell pitch ( $P$ ) of  $10 \mu\text{m}$ , a JFET gap ( $W$ ) of  $3 \mu\text{m}$ , a junction depth ( $d$ ) of  $1 \mu\text{m}$ , a drift layer thickness of  $9 \mu\text{m}$ , a drift layer doping concentration ( $N_D$ ) of  $8 \times 10^{15} \text{ cm}^{-3}$ , a MOS channel length ( $L$ ) of  $0.5 \mu\text{m}$ , a  $V_g - V_{\text{th}}$  of  $12 \text{ V}$ , and a  $C_{\text{ox}}$  of  $8.63 \times 10^{-8} \text{ F/cm}^2$ , we can estimate the values for the resistance components, normalized for the area, as given in Figure 12.17. Given thickness and doping concentration of the drift layer, we can deduce that this device has a rated voltage of about  $1200 \text{ V}$ . The drift resistance of this device accounts for only 27% of the total on-resistance. The on-resistance of the MOSFET is heavily influenced by other parasitic resistance components, and



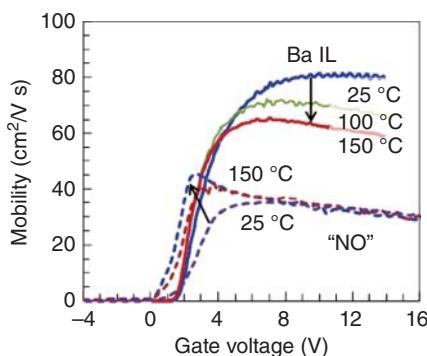
**Figure 12.17** 4H-SiC DMOSFET resistance components. Assumptions:  $\mu_{n,ave}$  of  $12 \text{ cm}^2/\text{V s}$ ,  $\mu_{n,bulk}$  of  $700 \text{ cm}^2/\text{V s}$ , a cell pitch ( $P$ ) of  $10 \mu\text{m}$ , a JFET gap ( $W$ ) of  $3 \mu\text{m}$ , a junction depth ( $d$ ) of  $1 \mu\text{m}$ , a drift layer thickness of  $9 \mu\text{m}$ , a drift layer doping concentration ( $N_D$ ) of  $8 \times 10^{15} \text{ cm}^{-3}$ , a MOS channel length ( $L$ ) of  $0.5 \mu\text{m}$ , a  $V_g - V_{th}$  of  $12 \text{ V}$ , and a  $C_{ox}$  of  $8.63 \times 10^{-8} \text{ F/cm}^2$ .

out of the parasitic resistance components, the MOS channel resistance is the most dominant factor, accounting for 55% of the total on-resistance.

**4H-SiC DMOSFET Optimization** For optimization of power DMOSFETs in 4H-SiC, it is very important to minimize the MOS channel resistance. First successful approach for reducing the MOS channel resistance was to utilize self-aligned ion implantation to reduce the MOS channel length [30]. This approach resulted in 2 kV power MOSFETs in 4H-SiC with a specific on-resistance of  $10.3 \text{ m}\Omega\text{-cm}^2$  and provided an important basis for the commercialization of power MOSFETs in silicon carbide.

Attempts were made to improve MOS interface properties by incorporating impurities other than nitrogen into the gate oxide to achieve greater MOS channel mobility than what can be obtained using NO or  $\text{N}_2\text{O}$  anneals. Doping of the oxide layers with phosphorus [31] and boron [32, 33] has been investigated. A MOS channel mobility of  $98 \text{ cm}^2/\text{V s}$  was achieved using phosphorus doping approach [30] and boron doping approach resulted in a MOS channel mobility of  $102 \text{ cm}^2/\text{V s}$  [32], and a 4.5 kV power DMOSFET was demonstrated [33]. Approximately a factor of 3 improvements in MOS channel mobility over nitridation using NO or  $\text{N}_2\text{O}$  was observed using this approach. However, it was determined that these approaches were not suitable for commercial 4H-SiC power MOSFETs since a reasonable threshold voltage stability could not be achieved (P. Godignon, private communications).

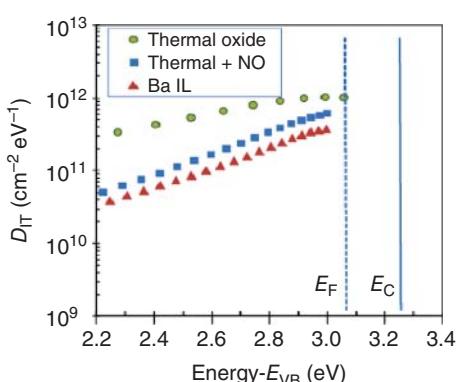
Usage of alkaline earth elements, such as strontium (Sr) and barium (Ba), as interface passivation materials for 4H-SiC MOSFETs was also investigated [34–36]. The passivation was performed by placing a very thin interlayer material directly on the 4H-SiC surface, followed by deposition of gate dielectric layer, typically  $\text{SiO}_2$ , which was annealed in  $\text{O}_2/\text{N}_2$  ambient for densification [34]. Sr passivation of the MOS interface showed a very promising result, resulting in a MOS channel mobility of  $40 \text{ cm}^2/\text{V s}$ , which was comparable to the values achievable using an NO anneal [34]. Passivation using Ba turned out to be significantly more efficient, resulting in a



**Figure 12.18** MOS channel mobility comparing samples with Ba interlayer to those with an NO anneal, as a function of temperature (25, 100, and 150 °C). Source: Lichtenwalner et al. [26].

MOS channel mobility of 85 cm<sup>2</sup>/V s at room temperature, which is approximately double the value from an NO annealed sample [34]. A comparison of MOS channel mobility at temperatures ranging from 25 to 150 °C is shown in Figure 12.18. A test lateral MOSFET with conventional NO anneal process and a device with Barium interlayer (Ba IL) passivation process were used for this comparison [34]. The samples were fabricated on  $5 \times 10^{15} \text{ cm}^{-3}$  doped p-type epilayers on 4H-SiC substrates. The MOS channel mobility of the Ba IL-passivated sample decreases with temperature, as expected due to phonon scattering effects. This is in contrast to the NO annealed sample, which showed an increase in MOS channel mobility with temperature due to the higher interface density near the conduction band. Figure 12.19 shows the interface state density ( $D_{it}$ ) distributions from high to low capacitance-voltage (CV) measurement for the MOS capacitors formed on lightly doped n-type epilayers. Results were compared to capacitors with as-grown thermal oxide. Both the NO annealed capacitor and the Ba IL-passivated capacitor showed significantly lower  $D_{it}$ , with the Ba IL processed device showing the lowest  $D_{it}$ .

Vertical 4H-SiC DMOSFETs were fabricated using the Ba IL process [36]. The devices were stressed under a negative gate bias of -15 V at 150 °C. A threshold voltage shift of less than 0.2 V was observed after 150 hours, demonstrating very good stability of threshold voltage. MOS capacitors with an area of 4 mm<sup>2</sup>, fabricated with Ba IL passivation process, were tested under ramped  $V_g$  sweep conditions



**Figure 12.19** Interface state density extracted from the high-low C-V measurements of NMOS capacitors, comparing samples with thermal oxidation only to those with NO anneal and Ba interlayer. Source: Lichtenwalner et al. [26].

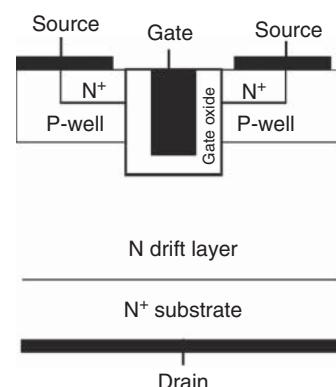
(ramped time dependent dielectric breakdown [TDDB] measurements) [36]. More than 100 capacitors were measured for the breakdown statistics. The gate oxide formed with the Ba IL process with deposited oxide showed a reasonable maximum breakdown  $E$ -field, close to 10 MV/cm with a small temperature dependence from 25 to 150 °C. However, the breakdown field is lower than that of the thermal oxides with an NO anneal, and more extrinsic failures were noticed for the devices with the Ba IL process. At this time, it is not clear whether this is due to a fundamental weakness of the Ba IL process or due to a weakness of the deposited gate oxide process [36].

### 12.3.1.2 Trench MOSFETs

Trench MOSFET structures shown in Figure 12.20, can provide devices with very tight cell pitch because it places the MOS channel on the etched sidewalls. Additional real estate necessary for proper MOSFET operations, such as gate-to-source overlap and gate-to-ohmic metal gap, can also be placed on the sidewalls. Such design can result in a substantial increase in gate-to-source capacitance. This is actually highly desirable feature for high speed switching applications since it enhances immunity of the power MOSFET from erroneous turn-on during a high  $dv/dt$  turn-off event, provided that the increase in gate-to-drain capacitance could be avoided [37]. The first trench MOSFETs in silicon carbide, using 6H-polytype, were reported by Palmour et al. [38]. The first trench MOSFETs in 4H-SiC were also demonstrated by Palmour et al. [39].

It was also experimentally demonstrated that the MOS channel mobility can be significantly higher on the etched sidewall compared to the Si-face of 4H-SiC [40]. The simplified trench MOSFET structure shown in Figure 12.20 does not have a JFET region, which also helps reducing the on-resistance. It is expected that a well-optimized 4H-SiC trench MOSFET structure can offer significantly lower on-resistance compared to a 4H-SiC DMOSFET with the same voltage rating. However, it should be noted that one of the most important functions of the JFET region is to provide an adequate protection of the gate oxide from high  $E$ -field in the blocking mode, and the structure in Figure 12.20 does not have any protection for the oxide at the trench bottom, and this issue must be addressed before finalizing any 4H-SiC trench MOSFET designs.

**Figure 12.20** Simplified cross section of a 4H-SiC trench MOSFET.



**4H-SiC Trench MOSFET Resistance Components** Although trench MOSFETs have a different structure from DMOSFETs, many of the resistance components for the trench MOSFETs can be calculated the same way they were calculated for the DMOSFETs. The main components include MOS channel resistance, drift resistance, and spreading resistance. There is no JFET region in the simplified trench MOSFETs. As mentioned in Section 12.3.1.2, this simplified structure (Figure 12.20) does not have a mean to shield the gate oxide at the trench bottom. When a shielding structure is implemented to protect the trench bottom oxide, it can be represented as a JFET structure and a JFET resistance component can be added. However, this protection structure can take several forms and will not be included in this section. Other resistance components, such as contact resistance and substrate resistance, are ignored for trench MOSFET resistance component calculations, as was the case for the DMOSFETs.

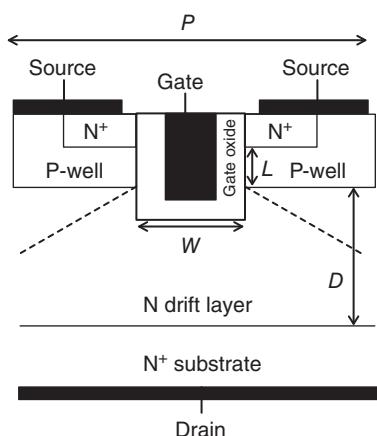
The channel resistance ( $R_{ch}$ ) represents the resistance of the MOS inversion layer in the channel. In the on-state operation of the power trench MOSFET, for low drain bias ( $V_{DS}$ ) values structure,  $R_{ch}$  can be expressed as below.

$$R_{ch} = \frac{L \cdot P}{2 \cdot \mu_{n,ave} \cdot C_{ox} \cdot (V_g - V_{th})} \quad (12.13)$$

where  $L$  is the channel length and  $P$  is the device cell pitch, as shown in Figure 12.21.  $\mu_{n,ave}$  is the average MOS inversion layer mobility, and  $C_{ox}$  is the oxide capacitance per unit area ( $\epsilon_{ox}/t_{ox}$ ), and  $V_{th}$  is the device threshold voltage.

The drift resistance ( $R_{drift}$ ) represents the resistance through the drift layer. For this calculation, a parallel plate operation with uniform current density is assumed and can use the identical expression used for the DMOSFETs used in Section 12.3.1.1 (Eq. (12.9)).

The spreading resistance ( $R_{spread}$ ) for the trench MOSFET can be derived the same way it was derived for the DMOSFET. The MOS gate trench width should be used for the trench MOSFETs in place of the JFET width in the DMOSFET. The spreading



**Figure 12.21** 4H-SiC trench MOSFET dimensions for on-resistance calculations.

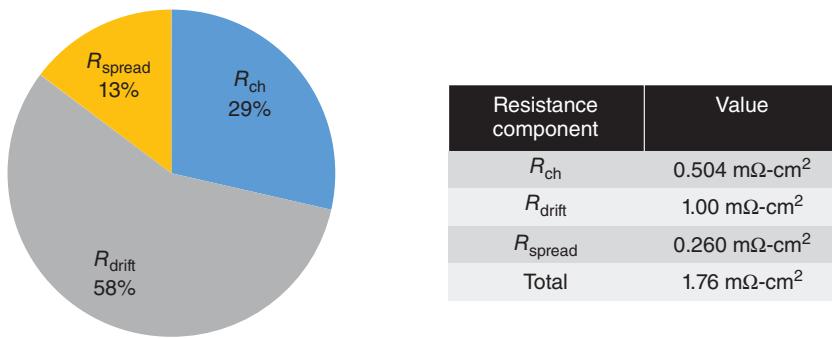
resistance can be expressed as below.

$$\begin{aligned} R_{\text{spread}} &= \frac{P}{1.74q \cdot \mu_{n,\text{bulk}} \cdot N_D} \ln\left(\frac{P}{W}\right) - \frac{P - W}{1.74q \cdot \mu_{n,\text{bulk}} \cdot N_D} \\ &= \frac{P}{1.74q \cdot \mu_{n,\text{bulk}} \cdot N_D} \left( \ln\left(\frac{P}{W}\right) - 1 + \frac{W}{P} \right) \end{aligned} \quad (12.14)$$

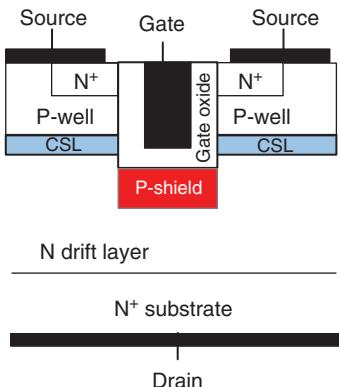
where  $W$  is the MOS trench width, as shown in Figure 12.21.

The resistance values of the trench MOSFET, with the same drift layer as the DMOSFET discussed in Section 12.3.1.1 can be calculated with the following assumptions.  $\mu_{n,\text{ave}}$  value increases to  $24 \text{ cm}^2/\text{Vs}$  (from  $12 \text{ cm}^2/\text{Vs}$  for DMOSFETs), and the cell pitch  $P$  decreases to  $5 \mu\text{m}$  (from  $10 \mu\text{m}$  for DMOSFETs), with a trench width  $W$  of  $1 \mu\text{m}$ . All the other parameters stay the same:  $\mu_{n,\text{bulk}}$  of  $700 \text{ cm}^2/\text{Vs}$  at room temperature, a drift layer thickness of  $9 \mu\text{m}$ , a drift layer doping concentration ( $N_D$ ) of  $8 \times 10^{15} \text{ cm}^{-3}$ , a MOS channel length ( $L$ ) of  $0.5 \mu\text{m}$ , a  $V_g - V_{\text{th}}$  of  $12 \text{ V}$ , and a  $C_{\text{ox}}$  of  $8.63 \times 10^{-8} \text{ F/cm}^2$ . Using these values, we can get the values for the resistance components, normalized for the area as shown in Figure 12.22. The MOS channel resistance of this device accounts for only 29% of the total on-resistance. The trench MOSFET structure showed approximately 53% reduction in on-resistance compared to the DMOSFET using the same drift layer.

**4H-SiC Trench MOSFET Optimization** The simple trench MOSFET structure, discussed in Section 12.3.1.2, works very well in silicon, since the breakdown  $E$ -field for  $\text{SiO}_2$  is 2 orders of magnitude greater than that of silicon; hence, oxide breakdown is not an issue in silicon devices. However, the breakdown  $E$ -field of 4H-SiC is approximately a factor of 3 lower than the theoretical breakdown  $E$ -field of  $\text{SiO}_2$ . The  $E$ -field increases further at the  $\text{SiO}_2/\text{SiC}$  interface by more than a factor of 2 due to the difference in dielectric constant between the two materials. This represents a huge reliability issue of 4H-SiC trench MOSFETs. For reliable operations, the gate oxide



**Figure 12.22** 4H-SiC trench MOSFET resistance components. Assumptions:  $\mu_{n,\text{ave}}$  of  $24 \text{ cm}^2/\text{Vs}$ ,  $\mu_{n,\text{bulk}}$  of  $700 \text{ cm}^2/\text{Vs}$ , a cell pitch ( $P$ ) of  $5 \mu\text{m}$ , a MOS trench width ( $W$ ) of  $1 \mu\text{m}$ , drift layer thickness of  $9 \mu\text{m}$ , a drift layer doping concentration ( $N_D$ ) of  $8 \times 10^{15} \text{ cm}^{-3}$ , a MOS channel length ( $L$ ) of  $0.5 \mu\text{m}$ , a  $V_g - V_{\text{th}}$  of  $12 \text{ V}$ , and a  $C_{\text{ox}}$  of  $8.63 \times 10^{-8} \text{ F/cm}^2$ .



**Figure 12.23** Cross section of the 4H-SiC trench MOSFET with trench bottom protection. The device includes a p-type implant in the bottom of the trench and an n-type current spreading epilayer (CSL) beneath the p-base. Sources: Tan et al. [41], Kyogoku et al. [42].

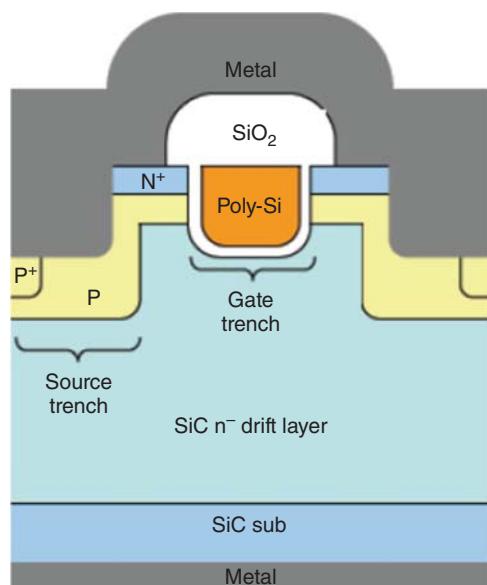
at the trench bottom must be properly shielded from the high voltage during the off-state.

Figure 12.23 shows a 4H-SiC trench MOSFET structure with a p-type implanted in the bottom of the gate trench. The p-shielding region was connected to the source region and provided excellent protection to the gate oxide at the bottom of the trench. It should be noted that this p-type protection layer and the p-base of the trench MOSFET can form a very narrow JFET region, which can add significant amount of JFET resistance, increasing the total on-resistance of the structure. This issue was addressed by placing a thin, heavier doped n-type current spreading layer (CSL) beneath the p-base layer [41]. The device used a 10  $\mu\text{m}$  thick drift layer and demonstrated a blocking voltage of 1400 V and an on-resistance of 15.7  $\text{m}\Omega\cdot\text{cm}^2$ . It should be noted that the gate-to-drain capacitance is very small, but switching losses will increase if the resistance between the protection p-region and source is very high. Layout must be optimized for this structure to achieve optimal on-state and switching performances [42].

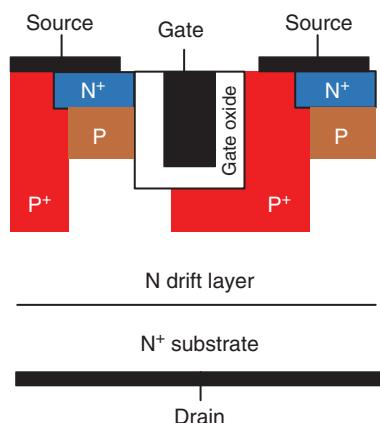
Figure 12.24 shows a 4H-SiC trench MOSFET structure with double-trench protection approach [9]. The bottom of the gate trench was shielded by a deeper source trench, placed approximately 2  $\mu\text{m}$  away from the gate trench. The MOS channel mobility on the etched sidewall was 11  $\text{cm}^2/\text{Vs}$ , which was considerably lower than that expected for a trench MOSFET in 4H-SiC. With this structure, a specific on-resistance of 0.79  $\text{m}\Omega\cdot\text{cm}^2$  was achieved for a 630 V 4H-SiC trench MOSFET, and an on-resistance of 1.41  $\text{m}\Omega\cdot\text{cm}^2$  was achieved for a 1260 V trench MOSFET, respectively.

Figure 12.25 shows a 4H-SiC trench MOSFET structure with asymmetric protection implants. In this device, only one side of the trench sidewall is used as MOS channel, which is exactly aligned to the  $\langle 1120 \rangle$  crystal plane [43]. The deep p-wells are used to limit the  $E$ -field in the gate oxide at the bottom and the corners of the trench. This cell structure has a small ratio of the Miller charge ( $Q_{GD}$ ) to gate-source charge ( $Q_{GS}$ ). It should be noted that this structure adds significant amount of JFET resistance. However, the added JFET regions resulted in reduced saturation currents, which improved the short circuit withstand time ( $t_{scwt}$ ).

**Figure 12.24** Cross section of the 4H-SiC trench MOSFET with double-trench protection. Source: Nakamura et al. [9]. © 2011, IEEE.



**Figure 12.25** Cross section of the 4H-SiC trench MOSFET with asymmetric protection p-well implants. Source: Based on Peters et al. [43].



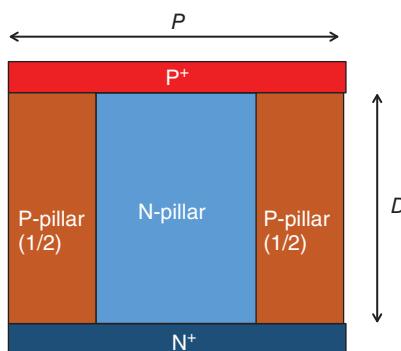
The a-face of 4H-SiC (sidewalls of trench MOSFET/UMOSFETs) has lower density of interface states ( $D_{it}$ ) closer to the conduction band edge than the Si-face of 4H-SiC. However, the a-face has significantly more midgap states, which may not impact the MOS channel mobility, but result in significant sub-threshold hysteresis [44, 45]. A preconditioning routine is required to measure threshold voltage from 4H-SiC trench MOSFET. Although this may not impact the device reliability or stability [44], it is preferred to minimize the hysteresis for easier control of the devices. Further developments in MOS surface passivation techniques are recommended, to minimize the impact of midgap interface states.

### 12.3.2 Advanced Power MOSFET Structures in 4H-SiC

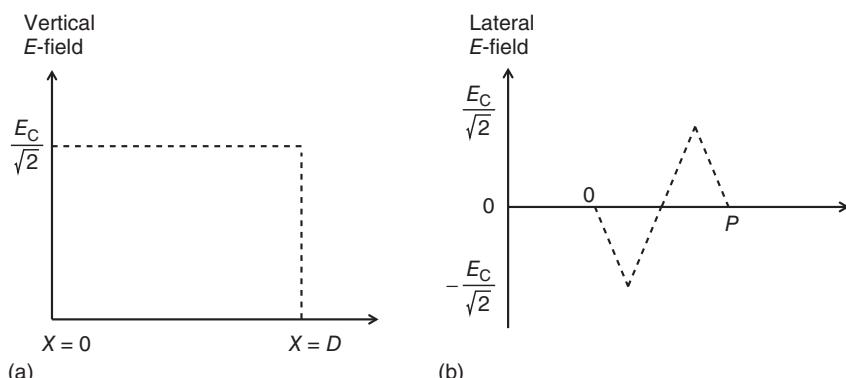
#### 12.3.2.1 Superjunction MOSFETs in 4H-SiC

Superjunction (SJ) structure [18] overcomes the trade-off relationship between breakdown voltage and on-resistance of the conventional semiconductor devices by utilizing a number of alternatively stacked, p- and n-type thin semiconductor layers with heavy doping concentrations. By controlling the degree of doping and the thickness of these layers, low on-resistance and high breakdown voltage can be achieved.

A simplified cross section of a superjunction (SJ) drift layer is shown in Figure 12.26. It is assumed that the entire drift layer has the full SJ structure, and equal widths are used for both N- and P-pillars. In unipolar devices, on-state conduction happens only through the N-pillar. A perfect charge balance is assumed for the N- and P-pillars, and it is assumed that both layers are fully depleted at a relatively low value of drain bias. Once the full depletion is achieved, a rectangular  $E$ -field profile is achieved in the vertical direction as shown in Figure 12.27, instead of triangular or trapezoidal  $E$ -field profile observed in conventional power device structures. As for lateral  $E$ -field, center of each pillar should have zero field (for both P- and N-pillars) and peak  $E$ -field should be placed at the lateral metallurgical junction between adjacent P- and N-pillars, as shown in Figure 12.27.



**Figure 12.26** Simplified cross section of a superjunction drift layer.



**Figure 12.27**  $E$ -field profile of a superjunction structure in blocking mode. Vertical  $E$ -field profile (a), and lateral  $E$ -field profile (b).

For simplicity, peak  $E$ -field of  $\frac{E_C}{\sqrt{2}}$  is assumed for both vertical  $E$ -field and lateral  $E$ -field to keep the peak  $E$ -field at  $E_C$  within the structure.

Doping concentration for the N- and P-pillars can be calculated below.

$$N_A = N_D = \frac{\epsilon_s \cdot E_C / \sqrt{2}}{q \cdot P/4} = \frac{4\epsilon_s \cdot E_C}{\sqrt{2} \cdot q \cdot P} \quad (12.15)$$

Blocking voltage of this structure is given below.

$$V_B = \frac{E_C \cdot D}{\sqrt{2}} \quad (12.16)$$

On-resistance can be calculated from the doping concentration and the dimensions of the structure, and can be expressed as below.

$$R_{on} = \frac{D \cdot P}{q \cdot N_D \cdot P/2 \cdot \mu_n} = \frac{2D}{q \cdot N_D \cdot \mu_n} \quad (12.17)$$

From Eqs. (12.15) and (12.16)

$$q \cdot N_D = \frac{4\epsilon_s \cdot E_C}{\sqrt{2} \cdot P} \quad \text{and} \quad D = \frac{\sqrt{2} \cdot V_B}{E_C} \quad (12.18)$$

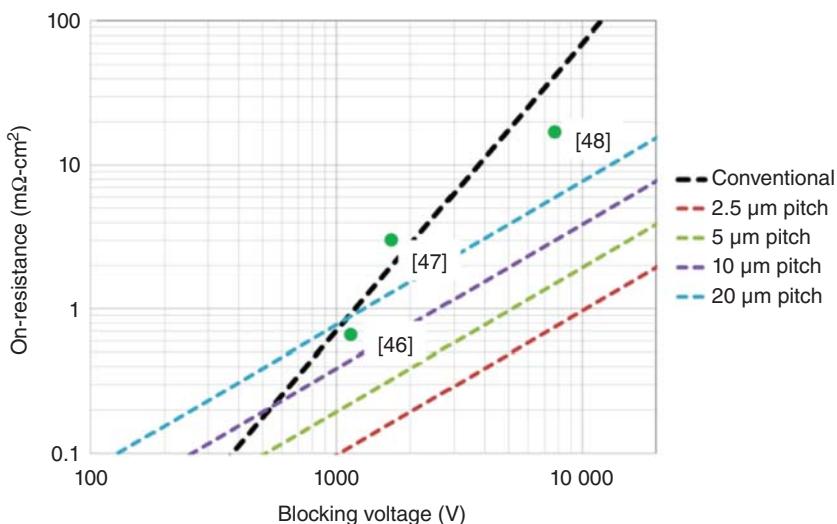
Apply this to Eq. (12.17) we get

$$R_{on} = \frac{2V_B}{E_C} \cdot \frac{P}{4\epsilon_s \cdot E_C \cdot \mu_n} \cdot 2 = \frac{V_B \cdot P}{\epsilon_s \cdot E_C^2 \cdot \mu_n} \quad (12.19)$$

Theoretical specific on-resistance as a function of blocking voltage for conventional structure and SJ structures with pitch ranging from 2.5 to 20  $\mu\text{m}$  in 4H-SiC is shown in Figure 12.28. Performance points of recent experimental results are also shown in the plot [46–48]. It is shown that the on-resistance can be further reduced by using tighter pitch SJ designs. Also, the on-resistance reduction over conventional structure is more significant for higher voltage devices. As discussed in Sections 12.3.1.1 and 12.3.1.2, 4H-SiC MOSFETs have significant parasitic on-resistance components, such as MOS channel resistance. It is expected that relatively small improvements in device performances will be observed for 4H-SiC SJ MOSFETs with blocking voltages of 1.2 kV or lower. More substantial impacts are expected for higher voltage devices, with blocking voltages of 6 kV or higher.

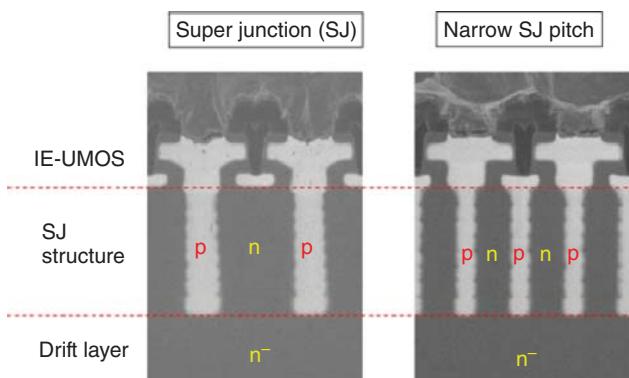
Superjunction MOSFETs in 4H-SiC, using multiple implants and epi regrowth steps, have been experimentally demonstrated [46, 47, 49, 50]. Dopant diffusion cannot be utilized in the fabrication of superjunction structures in 4H-SiC due to negligible diffusion coefficients in 4H-SiC [49]. Hence, for this type of approach, the superjunction drift layer requires several iterations of thin epigrowth and ion implantations. In Ref. [46], the each iteration of epigrowth was limited to 0.7  $\mu\text{m}$  and 7 iterations of epigrowth and implantation steps were performed to form a drift layer for a 1200 V class device. A blocking voltage of 1170 V and an on-resistance of 0.63  $\text{m}\Omega\text{-cm}^2$  were reported for this structure [46].

Performance of 4H-SiC superjunction MOSFETs and a conventional trench MOSFET was compared [47, 50]. 1200 V class 4H-SiC superjunction MOSFETs



**Figure 12.28** Specific on-resistance of a function of breakdown voltage calculated for conventional structure and superjunction structures, with pitch ranging from 2.5 to 20  $\mu\text{m}$ . Includes performance of experimental results. Sources: Masuda et al. [46], Harada et al. [47], Kosugi et al. [48].

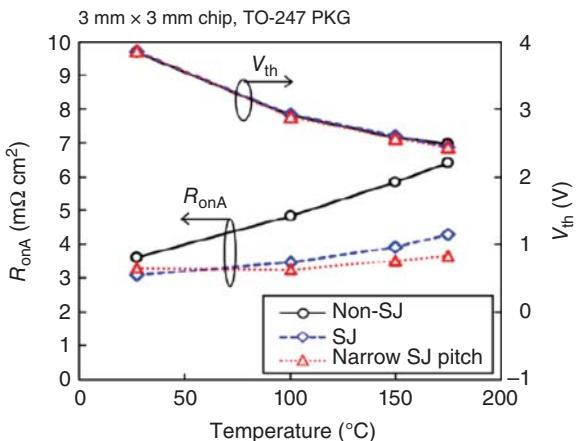
with 2.5 and 5  $\mu\text{m}$  pitches were fabricated, as shown in Figure 12.29. The superjunction devices showed very little reduction of on-resistance and slower switching characteristics compared to the conventional devices at room temperature [47]. This was predicted above since the on-resistance of 4H-SiC power MOSFETs with lower blocking voltage is dominated by MOS channel resistance, and drift resistance accounts for a small fraction of the on-resistance. However, the superjunction devices showed measurable advantages in on-resistance at elevated temperatures, as shown in Figure 12.30, where the MOS channel resistance reduces due to a reduction on threshold voltage, and drift resistance increases due to a decrease in bulk mobility



**Figure 12.29** Scanning electron microscopy (SEM) images of 4H-SiC superjunction MOSFETs with different pitches. Source: Kobayashi et al. [50].

**Figure 12.30**

On-resistance and threshold voltage as a function of temperature for a conventional device and superjunction MOSFETs.  
Source: Kobayashi et al. [50]. © 2019, IEEE.

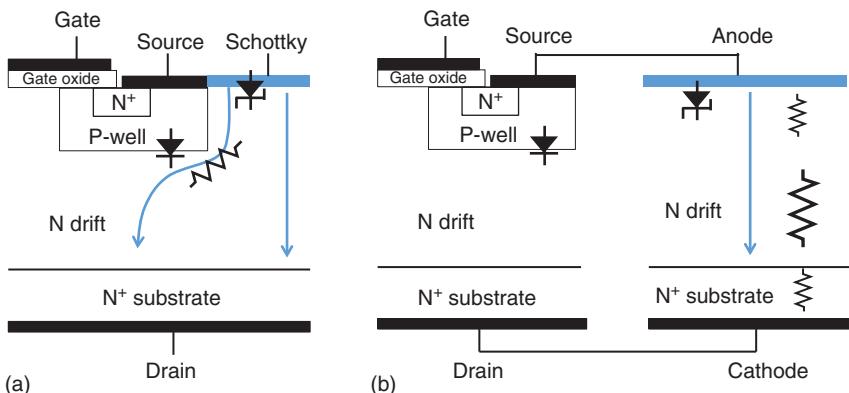


at elevated temperatures. Superjunction devices showed significantly smaller rate of increase in on-resistance over temperature compared to the conventional device. The superjunction device with tighter pitch and higher drift doping concentration showed smaller rate of increase compared to the SJ device with larger pitch.

As discussed above, the benefits of superjunction structure are greater for higher voltage ( $>6$  kV) devices. It is technically possible to build devices using multiple regrowth approach, but such approach is not realistic due to manufacturing costs associated with the approach. For such thick superjunction structures, “trench etch and refill” approach is more reasonable. A 6.5 kV 4H-SiC MOSFET with partial superjunction structure, with 23  $\mu\text{m}$  thick superjunction region and 41  $\mu\text{m}$  thick,  $2 \times 10^{15} \text{ cm}^{-3}$  doped drift region was experimentally demonstrated [48, 51]. A trench pitch of 5  $\mu\text{m}$  was used. For proper epi-fill of the trenches, the trenches must be precisely aligned to  $\langle 1\bar{1}\bar{2}0 \rangle$  direction. 4H-SiC power DMOSFET structure with a cell pitch of 10  $\mu\text{m}$  was built on the superjunction drift layer to complete the fabrication of the device. The completed 4H-SiC partial SJ MOSFET showed an on-resistance of 17.8  $\text{m}\Omega\text{-cm}^2$  with a blocking voltage of 7.8 kV. The on-resistance values measured from this device is significantly lower than the theoretical 1-D limit for 4H-SiC drift resistance.

### 12.3.2.2 Integrated JBS Diodes in 4H-SiC Power MOSFETs

4H-SiC power MOSFETs with integrated JBS diodes are being investigated to prevent the growth of stacking faults caused by basal plane dislocations, as well as improve the reverse recovery performance of the built-in body diode [52–56]. Schematic behaviors of a 4H-SiC MOSFET with integrated JBS diode and a conventional MOSFET with an external JBS diode are depicted in Figure 12.31. To suppress the pn junction from injecting minority carriers, the applied voltage across the pn junction should be less than its built-in potential. For 4H-SiC power MOSFETs with integrated JBS diodes, this is relatively easy since the only requirement is to keep the voltage drop across the Schottky contact and the JFET region below the Schottky contact to less than the pn junction built-in potential. When external JBS diodes are used, voltage drop of the entire structure and associated inductances must be



**Figure 12.31** Cross section of (a) a MOSFET embedding SBD, (b) a conventional MOSFET coupled with an external SBD.

less than the built-in potential of the pn junction. Experimental demonstration of such structure was shown for the 4H-SiC planar MOSFETs [52, 53, 56] and 4H-SiC trench MOSFETs [54, 55]. 4H-SiC MOSFETs with integrated JBS diodes showed superior switching performances over the conventional option, which used external JBS diodes [53]. With savings in the chip size and performance advantages, 4H-SiC power MOSFETs with integrated JBS diodes were recommended for high speed switching applications [53]. However, a significant reduction in short-circuit withstand time ( $t_{scwt}$ ) was reported for 4H-SiC power MOSFETs with integrated JBS diodes [55, 56]. At a short-circuit situation, the leakage current through the Schottky barrier increases due to high junction temperature and the increased Schottky leakage current further increases the junction temperature, which increases the Schottky leakage further, resulting in a destructive positive feedback loop between Schottky leakage current and junction temperature [55]. Usage of higher barrier height Schottky metal was suggested to alleviate this issue, which in turn reduces the effectiveness of the bypass capability of the integrated JBS diode.

## 12.4 Summary

We reviewed JBS diodes and power MOSFETs in 4H-SiC. In 4H-SiC JBS diodes, the focus has been on improving surge capability and overall power handling capability of the devices. Minority carrier injection from p<sup>+</sup> grid and conductivity modulation of the drift layer enhanced surge current capability of 4H-SiC JBS diodes. Use of trench shield structure, which allowed the use of more aggressively doped drift layer, resulted in significantly reduced conduction losses of the diodes. The conduction losses were further reduced by the use of lower barrier metals, such as Mo compounds, as Schottky barrier metal. It should be noted that an increase of leakage current was also observed with this approach, but the power losses due to this leakage was kept less than 1% of the conduction losses of the diodes.

4H-SiC DMOSFET and trench MOSFET structures were reviewed. In 4H-SiC DMOSFETs, devices with voltage ratings ranging from 900 V to 15 kV have been developed. Devices with blocking voltages of 6 kV or greater show performances very close to the 1-D ideal limit, but the devices with lower voltage ratings showed significantly higher on-resistance than the 1-D limit due to the parasitic resistance components. Surface passivation techniques using phosphorus, boron, and alkali metal elements like barium were attempted to produce higher MOS channel mobility over the current NO<sub>x</sub>- and N<sub>2</sub>O-based passivation techniques. Boron- and phosphorus-doped gate oxide devices showed higher MOS channel mobility, but failed to provide sufficient threshold stability. Ba IL passivation technique showed very encouraging results, demonstrating both high MOS channel mobility and good threshold voltage stability, but suffered from density of defects in the gate dielectric. At this point, it is not clear if this was due to a fundamental weakness of the Ba IL process or due to weaknesses in the gate oxide deposition technique used in conjunction with the Ba IL process. 4H-SiC trench MOSFETs have promises of lower on-resistance based on tighter gate packing density and higher MOS channel mobility on etched sidewalls of the gate trench. The challenges in the 4H-SiC trench MOSFET design are in the protection of the trench bottom gate oxide with minimum impact on the device on-resistance. Devices using trench bottom p-implants, double-trench protection, and asymmetric implant protection were developed with very good results. Another challenge in the 4H-SiC trench MOSFETs is the high density of midgap interface traps. The high  $D_{it}$  at midgap causes significant subthreshold hysteresis, and for proper threshold measurements, preconditioning steps are needed. Further developments in surface passivation are needed to overcome this issue.

Superjunction MOSFETs were demonstrated in 4H-SiC. 4H-SiC superjunction MOSFETs with lower blocking voltage (around 1.2 kV) used multi-epi growth approach to form the structure. Since the devices were limited by the performance of the 4H-SiC MOS channel, very little performance improvements were observed at room temperature. However, it was observed that the 4H-SiC superjunction MOSFETs have much lower rate of increase in on-resistance at elevated temperatures than conventional structure. Trench etch and epitaxial refill approach was used for a 6.5 kV 4H-SiC superjunction MOSFET. The device used partial superjunction structure, and superjunction drift layer covered only about 1/3 of the drift layer thickness, but still showed about 50% reduction in  $R_{ds}$ , on over state-of-the-art conventional 6.5 kV 4H-SiC power MOSFET.

4H-SiC power MOSFETs with integrated JBS diodes were also discussed. The structure provides a very effective way of bypassing the built-in pn junction diode, suppressing the growth of stacking faults and minimizing reverse recovery of the body diode. However, the integration of JBS diodes resulted in significant reduction in short-circuit withstand time.

Power devices in 4H-SiC have come a long way, and significant progress has been made in recent years. 4H-SiC power devices are being accepted in many applications, which include automotives and trains. Most of the development in 4H-SiC power device development, so far, was focused on improving device performance.

It is expected that future development work in 4H-SiC power device development will include more research in device ruggedness and reliability as well as performance enhancements, to enable faster adoption of 4H-SiC power devices in wider range of applications.

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## 13

### Ultra-High-Voltage SiC Power Device

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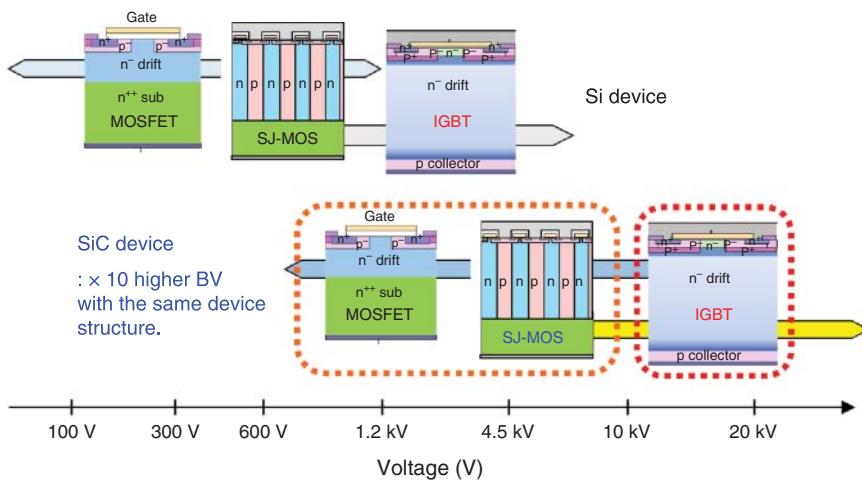
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#### 13.1 Introduction

To reduce CO<sub>2</sub> emissions as a countermeasure against global warming and to meet the increasing energy demand caused by the information explosion and the shift to electric vehicles, large scale introduction of renewable energy and energy storage is necessary. At the same time, energy-saving technologies need to be improved to increase the efficiency of energy use. In addition, to control unstable renewable energy and improve energy resilience, there is a need to develop energy management technologies that combine the Internet of Things (IoT) and energy technologies to realize a power system for a safer and more secure society.

In these circumstances, the main transmission system is expected to increase inter-regional interconnections, including the enhancement of long-distance direct current (DC) transmission, and increases in the volume of large-scale offshore wind generation interconnected to the grid. In the load-supply system, large-scale commercial solar power and storage batteries are expected to be installed extensively. In addition, in the last one-mile distribution system, energy management businesses such as demand response (DR) and virtual power plants (VPPs) that utilize small- and medium-sized solar power generation and storage batteries including those for residential use, are expected to expand in order to provide electricity within the region. Given that these next-generation power networks are designed with the best mixture of DC and AC, power converters are a key component. These power electronics should be compact, highly efficient, highly reliable, and low cost. Therefore, the role of power electronics and power electronic equipment has become increasingly important in the energy value chain with the fusion of energy and information.

Power electronics and power devices are the two sides of the ongoing evolution in energy distribution and consumption. The recent power electronics evolution,



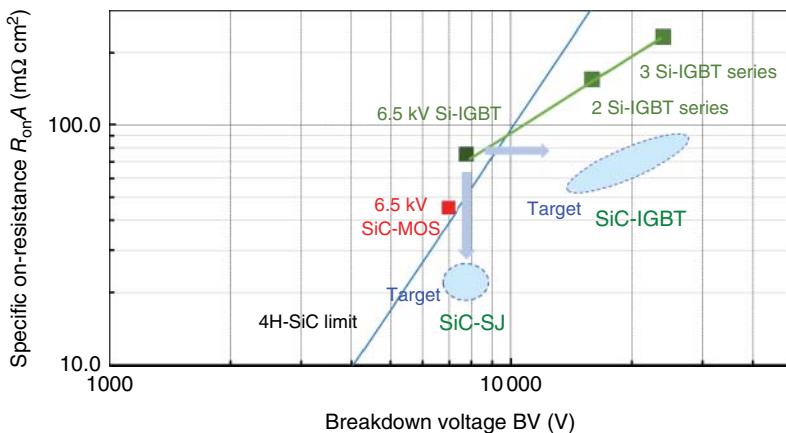
**Figure 13.1** Comparison of advanced Si and SiC devices.

in particular, has been supported by the improvement of the trade-off between the reduction of conduction loss and switching loss in silicon (Si)-IGBT (Insulated Gate Bipolar Transistor). However, since the performance improvement of Si-IGBTs has reached a physical limit, expectations for wide band gap semiconductor devices are increasing. Silicon carbide (SiC) has a band gap three times larger than that of Si and a three times higher thermal conductivity. The breakdown electric field of SiC is 10 times higher than that of Si, allowing SiC devices to achieve 10 times higher breakdown voltages (BVs) than Si devices with the same structure, as shown in Figure 13.1, along with a high junction temperature. Therefore, by replacing 600 V–3.3 kV Si bipolar devices with unipolar SiC-MOSFETs (metal-oxide semiconductor field effect transistors) and SBDs, the size and cost of power electronics components are expected to be reduced significantly with low conduction loss and switching loss, thus social implementation has begun [1].

Another advantage of utilizing SiC-MOSFET body diodes is that the external SBD can be omitted. The use of a recombination enhancing layer and a built-in SBD structure suppresses forward degradation problems [2–4].

Conversely, the next generation SiC power devices, similar to the history of Si devices, the application of SJ (super junction) and IGBT structures are being considered to maximize the potential of SiC. By applying the SJ structure, a significant reduction of the drift layer on-resistance below the unipolar limit can be expected in the 1.2–6.5 kV range. Furthermore, if we apply the IGBT structure to SiC, over 10 kV MOS-controlled switching devices can be realized, which is difficult to attain with Si devices [5–9]. The application of high-voltage and ultra-high-voltage devices to high-voltage power electronics equipment used in next-generation power systems is expected to result in smaller size, higher efficiency, and lower cost.

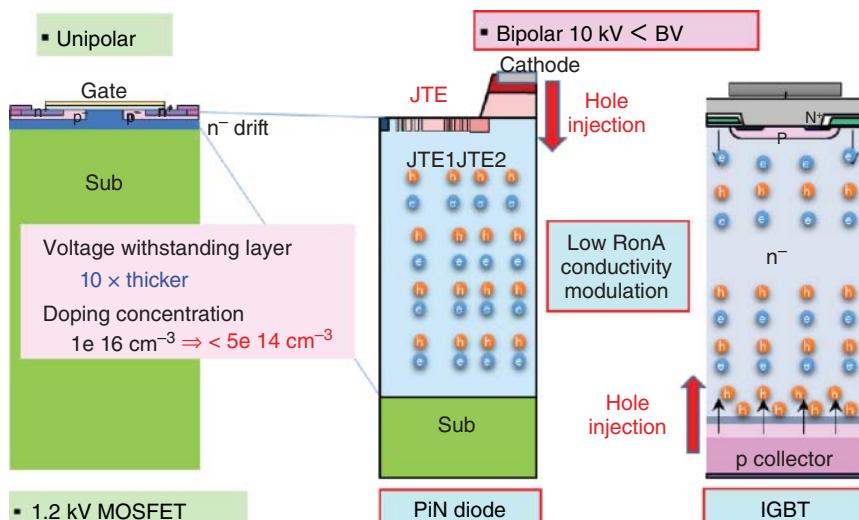
In this chapter, elemental technologies related to ultra-high voltage SiC-PIN diodes and SiC-IGBTs are described, and static and dynamic characteristics such as BV and forward characteristics are explained based on simulation and experimental results (Figure 13.2).



**Figure 13.2** Specific on-resistance of SiC SJ-MOSFET and SiC-IGBT compared with Si-IGBT and normal SiC-MOS.

## 13.2 Ultra-high-voltage SiC PiN diode and SiC-IGBT

Structural comparison between a 1.2 kV class SiC MOSFET and an ultra-high-voltage bipolar device which operates at voltages  $> 10 \text{ kV}$  is shown in Fig. 13.3. A 1.2 kV MOSFET has an n-layer thickness of approximately  $10 \mu\text{m}$ , whereas an ultra-high-voltage device at 10 kV and higher requires an n-layer thickness which is 10 times higher and an impurity concentration of  $5e 14 \text{ cm}^{-3}$  or less. In a unipolar device where only electrons contribute to conduction, the on-resistance of the  $100 \mu\text{m}$  n-layer is more than  $100 \text{ m}\Omega \text{cm}^2$  at elevated temperatures and the current



**Figure 13.3** Structural comparison of unipolar 1.2 kV SiC-MOSFET and over 10 kV SiC-PiN and SiC-IGBT.

density cannot be increased. In contrast, in bipolar devices, the carrier density can be increased by conductivity modulation and the resistance can be greatly reduced by injecting holes into the n-layer. In a PiN diode, the hole is injected from the cathode at the top, whereas in an IGBT, the hole is injected from the collector at the back. In conductivity modulation, the lifetime carrier has a significant impact.

In the following chapters, the requirements for the n-layer thickness and concentration, edge termination voltage structure, and the carrier lifetime for sufficient conductivity modulation in ultra-high-voltage devices will be explained based on simulations and experimental results.

### 13.3 Reverse Characteristics of SiC Bipolar Device

#### 13.3.1 Relationship Between Thickness and Density of Drift Layer and Breakdown Voltage

Compared with Si, SiC has an order of magnitude greater breakdown electric field. Therefore, the thickness of the drift layer can be lower, and the density of the drift layer can be higher. In this section, the relationships between the theoretical BV of pn junctions with  $N_a \gg N_d$  and the thickness and doping concentration of the drift layer are presented.

Since the depletion layer can be considered to extend only into the n-type drift layer, the equation for the one-dimensional electrostatic field in the depletion layer can be expressed as

$$\frac{dE(x)}{dx} = \frac{\rho(x)}{\epsilon_r \epsilon_0} = \frac{eN_d}{\epsilon_r \epsilon_0} = \text{const.} \quad (13.1)$$

$$-\frac{dV(x)}{dx} = E(x) \quad (13.2)$$

where  $\epsilon_r$  and  $\epsilon_0$  denote the relative permittivity and permittivity of vacuum, respectively. Here, if the depletion layer width  $D <$  the drift layer thickness  $W$ ,  $E(D) = 0$ , and  $V(0) = 0$ , they can be arranged as

$$E(x) = \frac{eN_d}{\epsilon_r \epsilon_0}(x - D) \quad (13.3)$$

$$V(x) = \frac{eN_d}{2\epsilon_r \epsilon_0}(2D - x)x \quad (13.4)$$

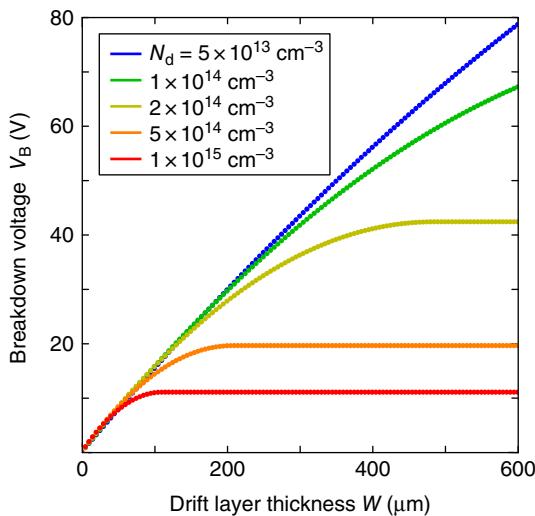
Here, the electric field takes a negative maximum value  $-E_{\max}$  at  $x = 0$ , and the voltage takes a maximum value of  $V_{\max}$  at  $x = D$ . By using these conditions, and deleting  $D$ , these equations can be arranged as

$$V_{\max} = \frac{eN_d}{2\epsilon_r \epsilon_0} \left( \frac{\epsilon_r \epsilon_0}{eN_d} E_{\max} \right)^2 = \frac{\epsilon_r \epsilon_0}{2eN_d} E_{\max}^2. \quad (13.5)$$

Here, it is reported that the breakdown electric field  $E_B$  of 4H-SiC is given as a function of the doping density  $N_d$  by [10].

$$E_B = \frac{2.49 \times 10^8}{1 - \frac{1}{4} \log \left( \frac{N_d}{10^{22}} \right)} [\text{V/m}]. \quad (13.6)$$

**Figure 13.4** Theoretical breakdown voltage calculated from thickness and doping density of the drift layer.



Since  $E_{\max} = E_B$  at the breakdown, the breakdown voltage  $V_B$  can be expressed as

$$V_B = V_{\max} (E_{\max} = E_B) = \frac{\epsilon_r \epsilon_0}{2eN_d} E_B^2 \quad (13.7)$$

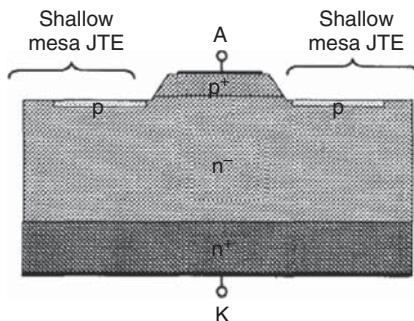
Next, if the depletion layer width  $D >$  the drift layer thickness  $W$ ,  $V_B$  can be similarly expressed as

$$V_B = V(W) = W \left( E_B - \frac{eN_d W}{2\epsilon_r \epsilon_0} \right) = W \left[ \frac{2.49 \times 10^8}{1 - \frac{1}{4} \log \left( \frac{N_d}{10^{22}} \right)} - \frac{eN_d W}{2\epsilon_r \epsilon_0} \right] \quad (13.8)$$

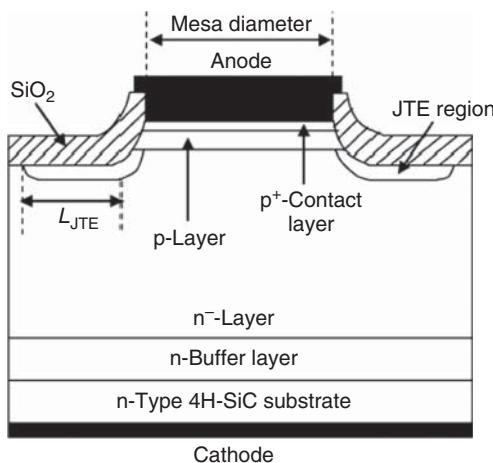
Figure 13.4 shows the theoretical BV calculated from the drift layer thickness and drift layer density. It is seen that 4H-SiC has a high BV. Nevertheless, BV is highly dependent on the termination structure; therefore, optimization of the termination structure will continue to be important in the future. Then, the termination structure has to be evaluated by comparing with the theoretical and experimental BV, and it is also important to verify the high breakdown electric field of SiC by approximating the measured value to the theoretical value.

### 13.3.2 Termination Structure of SiC Bipolar Devices

As discussed above, SiC has a very high theoretical BV value. However, it is difficult to achieve the theoretical BV because the high-voltage SiC PiN diodes have to form a mesa to separate the devices, and the electric field concentrates at the bottom edge of the mesa, causing breakdown. A JTE (Junction Termination Extension) structure, called the mesa-JTE, is formed around the mesa, as shown in Figure 13.5 [11]. A single-zone JTE formed with a single concentration has a BV of 19.5 kV (65% of the theoretical BV) [11]. It has been reported that a two-zone JTE with a JTE divided into two zones, with the outer concentration lower than the inner concentration and the maximum electric field value of the JTE reduced, is able to hold a



**Figure 13.5** Cross-sectional structure of PiN diodes with mesa-JTE structure. Source: Sugawara et al. [11]. © 2001, IEEE.

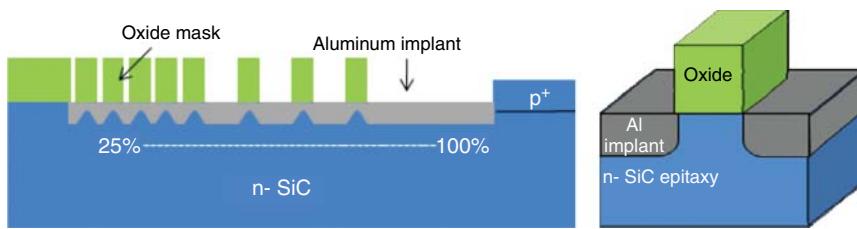


**Figure 13.6** Cross-sectional structure of PiN diodes with inclined mesa structure. Source: Hiyoshi et al. [13]. © 2008, IEEE.

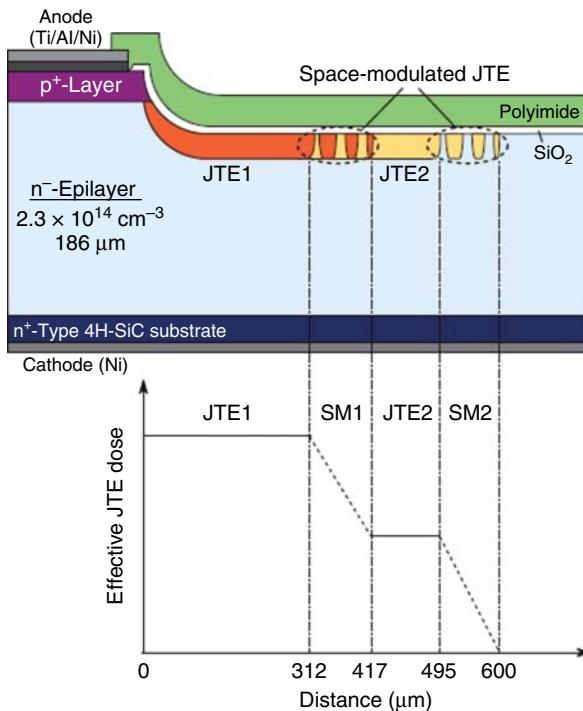
voltage of up to 20 kV (72% of the theoretical BV) [12]. It is also reported that a BV of 10.2 kV (73% of the theoretical BV) can be achieved even in a single zone when the mesa end is gently inclined as shown in Figure 13.6 [13]. Making the JTE multi-zone improves the BV but increases the number of ion implantations. Therefore, as shown in Figure 13.7, the concentration of the JTE is changed by adjusting the width of the mask for ion implantation and the JTE is multi-zoned with one ion implantation. It has been reported that a BV of 6.4 kV (90% of the theoretical BV) could be achieved using this method [14]. Furthermore, a BV of 21.7 kV (81% of the theoretical BV) has been achieved by introducing guard rings with gradually varying widths and spacing into the JTE, called as space-modulated JTE, as shown in Figure 13.8 [15]. By comparing the BV with the theoretical BV, it is possible to evaluate the JTE structure and demonstrate the high breakdown electric field strength of SiC.

### 13.4 Carrier Lifetime Dependence on the Characteristics of Bipolar Device

Power electronics devices such as inverters must be evaluated for their suitability in terms of power loss, expressed as the sum of the on-state and switching losses.



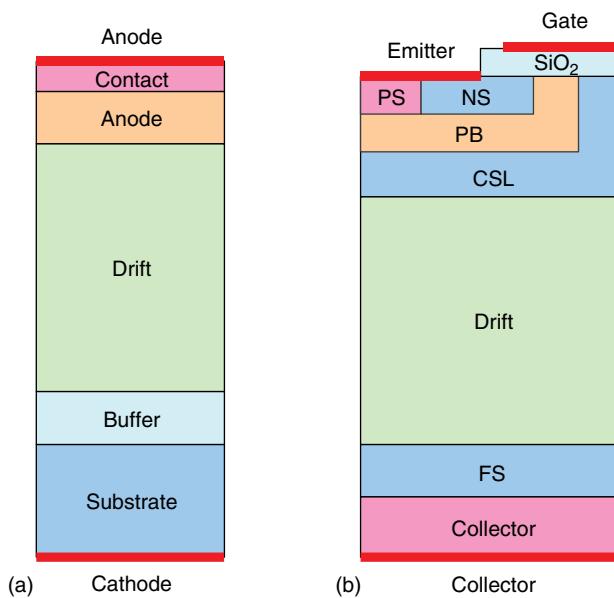
**Figure 13.7** Cross-sectional structure of PiN diodes with multi-zone JTE structure with adjusted mask width. Source: Snook et al. [14]. © 2012, Trans Tech Publications Ltd.



**Figure 13.8** Cross-sectional structure of a PiN diode with a space-modulated JTE structure. Source: Niwa et al. [15]. © 2012, The Japan Society of Applied Physics.

In the case of diodes, the on-state loss is determined by the forward current–voltage characteristic and the switching loss is determined by the reverse recovery characteristic. For a bipolar device, such as PiN diode and IGBT, as shown in Figure 13.9, the forward voltage decreases and the reverse recovery loss increases, as the temperature increases. Improving this trade-off will be a key development. Since the carrier lifetime is important for devices such as 4H-SiC pn diodes with pn structure, it is necessary to evaluate the carrier lifetime in real devices. Therefore, a technology is required for evaluating the carrier lifetime by using electrical characteristics.

In this section, the static characteristics, dynamic characteristics, and their evaluation techniques are described.



**Figure 13.9** Relationship between the carrier life and the current density of the SiC PiN diode. (a) PiN diode and (b) IGBT.

### 13.4.1 Forward Characteristics of pn Diode

#### 13.4.1.1 Analysis of Characteristics Under Low-Level Injection

Due to the wider band gap of SiC, the formation and recombination of carriers in the depletion layer cannot be ignored. Therefore, the static electrical characteristics of SiC pn diodes deviate from the ideal characteristics. The forward current density  $J_f$  of the pn diode at the forward bias is expressed as the sum of the diffusion current and recombination current, and it can be shown that [16]

$$J_f = e \left( \frac{D_p}{L_p N_d} + \frac{D_n}{L_n N_a} \right) n_i^2 \exp\left(\frac{eV}{kT}\right) + \frac{eW}{2} s v N_t n_i \exp\left(\frac{eV}{2kT}\right) \quad (13.9)$$

where  $e$  is the charge of the electron,  $D_p$  and  $L_p$  are the diffusion coefficient and diffusion length of the hole, respectively,  $D_n$  and  $L_n$  are the diffusion coefficient and diffusion length of the electron, respectively,  $N_a$  is the acceptor density of the p layer,  $N_d$  is the donor density of the n layer,  $n_i$  is the intrinsic carrier density,  $V$  is the applied voltage,  $k$  is the Boltzmann constant,  $T$  denotes the temperature,  $W$  is the depletion layer thickness,  $s$  and  $v$  are the carrier capture cross section and thermal velocity, and  $N_t$  is the trap density.

Here, the diffusion coefficient can be expressed as

$$L_p = \sqrt{D_p \tau_p} \quad (13.10)$$

$$L_n = \sqrt{D_n \tau_n} \quad (13.11)$$

In addition, from the SRH model [17], the carrier lifetime  $\tau$  can be expressed as

$$\tau = \frac{1}{svN_t} \quad (13.12)$$

The recombination current equation can be shown that

$$J_f = e \left( \frac{1}{N_d} \sqrt{\frac{D_p}{\tau_p}} + \frac{1}{N_a} \sqrt{\frac{D_n}{\tau_n}} \right) n_i^2 \exp\left(\frac{eV}{kT}\right) + \frac{eWn_i}{2\tau} \exp\left(\frac{eV}{2kT}\right) \quad (13.13)$$

Assuming that the carrier lifetime is short and the term of the diffusion current in the recombination current is negligible, it can be shown that

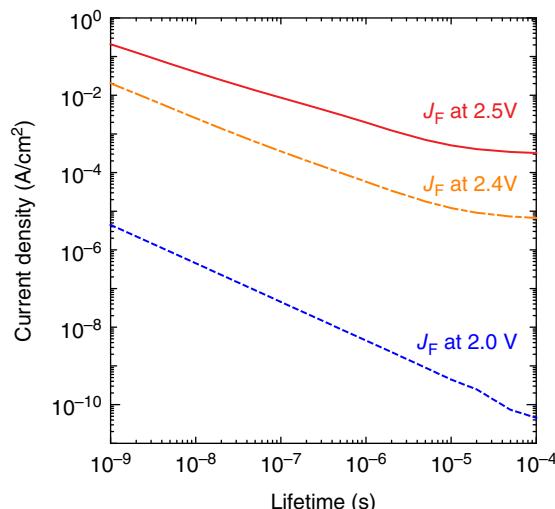
$$J_f = \frac{eWn_i}{2\tau} \exp\left(\frac{eV}{2kT}\right) \quad (13.14)$$

The current density at the same voltage is inversely proportional to the carrier lifetime ( $\tau$ ), independent of the thickness of the drift layer. Figure 13.10 shows the relationship between the carrier life and the current density of the SiC PiN diode calculated by TCAD. It can be seen that the current density at 2.0 V is inversely proportional to the carrier lifetime. In contrast, the current density at 2.5 V is nearly inversely proportional to the 1/2 power of the carrier life. This suggests that the recombination current dominates at 2.0 V and the effect of the diffusion current does not become negligible at 2.5 V. 4H-SiC has a large band gap and a small intrinsic carrier density near room temperature (RT), thus the second term in the recombination current equation dominates. In addition, by using Eq. (13.5), the forward current  $J_f$  of the pn diode can be expressed as

$$J_f \propto \exp\left(\frac{eV}{nkT}\right) \quad (13.15)$$

where  $n$  is an ideal factor. In general, the forward current of a PN diode is dominated by the diffusion current in the equation when  $n$  is 1. When  $n$  is 2, the recombination current in equation is dominated.

**Figure 13.10** Relationship between the carrier life and the current density of the SiC PiN diode.



### 13.4.1.2 Analysis of Carriers in the Drift Layer Under High-Level Injection

First, we analyze the carrier distribution of the drift layer under high-level injection [18]. Under high-level injection, assuming that the carrier lifetimes of electrons and holes are equal, the continuity equation of the electron and hole, can be expressed as

$$\frac{\partial n}{\partial t} = \frac{n}{\tau} + \mu_n \frac{\partial(nF)}{\partial x} + D_n \frac{\partial^2 n}{\partial x^2} \quad (13.16)$$

$$\frac{\partial p}{\partial t} = \frac{p}{\tau} + \mu_p \frac{\partial(pF)}{\partial x} + D_p \frac{\partial^2 p}{\partial x^2} \quad (13.17)$$

From the charge-neutral condition, by assuming that  $p = n$  holds under high-level injection, by removing  $\partial(nF)/\partial x$ , it can be shown that

$$(\mu_n + \mu_p) \frac{\partial n}{\partial t} = -(\mu_n + \mu_p) \frac{n}{\tau} + (\mu_p D_n + \mu_n D_p) \frac{\partial^2 n}{\partial x^2}. \quad (13.18)$$

By arranging Eq. (13.18), it can be shown that

$$\frac{\partial n}{\partial t} = \frac{n}{\tau} + \frac{\mu_p D_n + \mu_n D_p}{\mu_n + \mu_p} \frac{\partial^2 n}{\partial x^2} \quad (13.19)$$

Here, Einstein's relation can be expressed as

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{kT}{e} \quad (13.20)$$

By using Eq. (13.20), Eq. (13.19) can be arranged as

$$\frac{\partial n(x, t)}{\partial t} = -\frac{n(x, t)}{\tau} + D_a \frac{\partial^2 n(x, t)}{\partial x^2} \quad (13.21)$$

This equation is called as diffusion equation.  $D_a$  is defined as the ambipolar diffusion coefficient, which can be expressed as

$$D_a = \frac{\mu_p D_n + \mu_n D_p}{\mu_n + \mu_p} = \frac{2D_n D_p}{D_n + D_p} = \frac{2\mu_n \mu_p}{\mu_n + \mu_p} \frac{kT}{e} \quad (13.22)$$

Under the steady-state condition, it can be written as

$$\frac{\partial n}{\partial t} = 0 \quad (13.23)$$

Equation (13.21) can be fixed by

$$\frac{\partial^2 n}{\partial x^2} - \frac{n}{D_a \tau} = \frac{n}{L_a^2} \quad (13.24)$$

where  $L_a$  is the ambipolar diffusion length, which can be expressed as

$$L_a = \sqrt{D_a \tau} \quad (13.25)$$

Here, the electron and hole current density ( $J_n$  and  $J_p$ ) can be expressed as

$$J_n = en\mu_n F + eD_n \frac{\partial n}{\partial x} \quad (13.26)$$

$$J_p = ep\mu_p F - eD_p \frac{\partial p}{\partial x} \quad (13.27)$$

where  $F$  denotes the electric field and  $\mu_n$  and  $\mu_p$  denote the mobility of electron and hole, respectively. The boundary conditions can be assumed as

$$J_n(0) = 0, \quad J_p(0) = J_a \quad (13.28)$$

$$J_n(d) = J_a, \quad J_p(d) = 0 \quad (13.29)$$

where  $J_a$  denotes the total current density. By using these equations, the electron density can be expressed as

$$n(x) = \frac{\tau J_a}{eL_a} \cdot \frac{\frac{\mu_n}{\mu_p} \cosh\left(\frac{x-d}{L_a}\right) + \cosh\left(\frac{x}{L_a}\right)}{\left(\frac{\mu_n}{\mu_p} + 1\right) \sinh\left(\frac{d}{L_a}\right)}, \quad (13.30)$$

where  $d$  denotes the drift layer thickness.

Here, the stored charge  $Q$  in the drift layer can be expressed as

$$Q = \int_0^d eS n(x) dx = S\tau J_a \quad (13.31)$$

The stored charge is independent of the thickness of the drift layer and the mobility but depends on the current and carrier lifetime.

#### 13.4.1.3 Relationship Between Carrier Life, Drift Layer Thickness, and Drift Layer Voltage Drop

By using Eqs. (13.26) and (13.27), and the charge-neutral condition  $p = n$ , it can be shown that

$$J_a = J_n + J_p = e(\mu_n + \mu_p)nF + e(D_n - D_p)\frac{\partial n}{\partial x} \quad (13.32)$$

By assuming that the carrier lifetime is sufficiently long, and  $x, d = L_a$ , it can be shown that

$$n = \bar{n} = \frac{Q}{edS} = \frac{\tau J_a}{ed} \quad (13.33)$$

$$\frac{\partial n}{\partial x} = 0 \quad (13.34)$$

$$F = \frac{V_{\text{drift}}}{d} \quad (13.35)$$

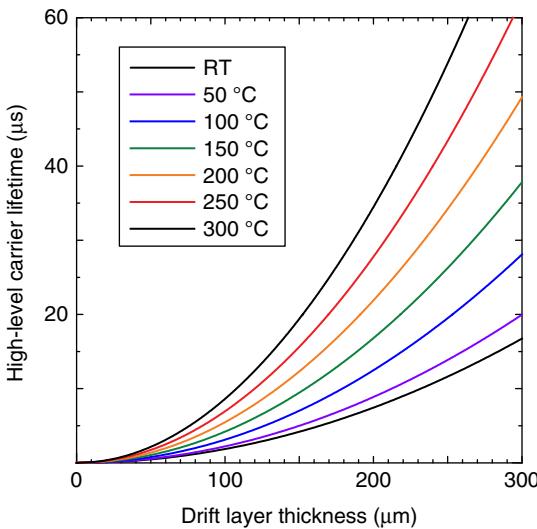
By using Eq. (13.32), it can be shown that

$$J_a = (\mu_n + \mu_p)\frac{\tau J_a}{d^2} V_{\text{drift}} \quad (13.36)$$

where  $V_{\text{drift}}$  denotes the voltage drop of the drift layer, which can be expressed as

$$V_{\text{drift}} = \frac{d^2}{(\mu_n + \mu_p)\tau} \quad (13.37)$$

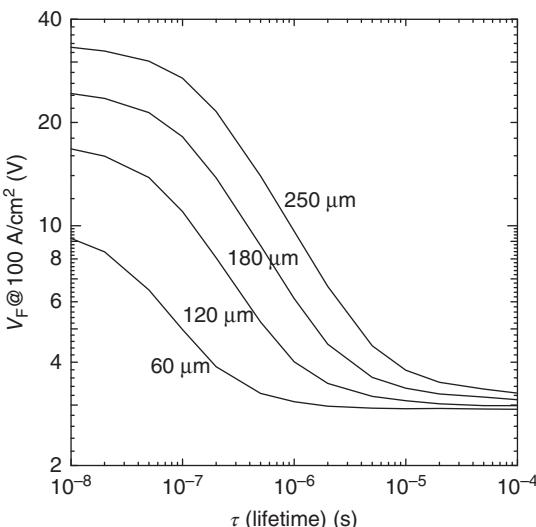
The voltage drop of the drift layer at high-level injection is proportional to the square of the drift layer thickness  $d$  and inversely proportional to the carrier lifetime. The mobility of electrons and holes at 300 K is set at  $950 \text{ cm}^2/\text{Vs}$  and  $125 \text{ cm}^2/\text{Vs}$ ,



**Figure 13.11** Dependence of carrier lifetime on drift layer thickness at each temperature.

respectively, and the temperature coefficient of the mobility of electrons and holes is set at 2.40 and 2.15, respectively [19], and the voltage drop of the drift layer is set at 0.05 V. The drift layer thickness dependence of the carrier lifetime at each temperature is shown in Figure 13.11. If the drift layer thickness is 250 μm, the carrier lifetime would require 12 μs at RT and 44 μs at 250 °C.

On the other hand, the voltage drop in the drift layer increases as the carrier lifetime is shortened. Therefore, the lifetime can be evaluated by measuring the on-voltage and differential on-resistance under high-level injection. In an actual device,  $x = d = L_a$  does not hold and Eqs. (13.33)–(13.35) may not hold. Figure 13.12 shows the results of the carrier lifetime dependence of the forward voltage at 100 A/cm<sup>2</sup> using TCAD. As a result,  $V_F$  is larger than that of Eq. (13.37).



**Figure 13.12** Carrier lifetime dependence of forward voltage at 100 A/cm<sup>2</sup> calculated by TCAD.

### 13.4.2 Reverse Characteristics of pn Diode

#### 13.4.2.1 Reverse Leakage Current Characteristics

The reverse current density  $J_r$  of the pn diode is expressed as the sum of the diffusion current and the generated current, and can be expressed as [7]

$$\begin{aligned} J_r &= e \left( \frac{D_p}{L_p N_d} + \frac{D_n}{L_n N_a} \right) n_i^2 + \frac{en_i W}{\tau_e} \\ &= \sqrt{ekT} \left( \frac{1}{N_d} \sqrt{\frac{\mu_p}{\tau_p}} + \frac{1}{N_a} \sqrt{\frac{\mu_n}{\tau_n}} \right) n_i^2 + \frac{en_i W}{\tau_e} \end{aligned} \quad (13.38)$$

where  $\tau_e$  denotes the electron-hole pair generation time and Einstein's relationship (13.20) is used. The first term is approximately  $1.6 \times 10^{-49} \text{ A/cm}^2$ , and the second term is  $1.1 \times 10^{-23} \text{ A/cm}^2$ , where  $T = 300 \text{ K}$ ,  $N_d = 1 \times 10^{14} \text{ cm}^{-3}$ ,  $N_a = 5 \times 10^{18} \text{ cm}^{-3}$ ,  $\mu_n = 950 \text{ cm}^2/\text{Vs}$ ,  $\mu_p = 125 \text{ cm}^2/\text{Vs}$ ,  $\tau_n = 1 \text{ s}$ ,  $\tau_p = 0.3 \text{ s}$ ,  $n_i = 5.5 \times 10^{-9} \text{ cm}^{-3}$ ,  $W = 120 \mu\text{m}$ , and  $\tau_e = 1 \text{ s}$ . Since the 4H-SiC has a large band gap and a small intrinsic carrier density near RT, the generated current (second term) dominates. The reverse current of a real 4H-SiC pn diode is measured to be on the order of  $10^{-9} \text{ A/cm}^2$ . This is thought to be because of the current flowing around the mesa, through the JTE and the surface. In addition, depending on the rise rate of voltage during reverse characterization, a charging current flows into the depletion layer of the PN junction. Since this can be on the order of  $10^{-9} \text{ A/cm}^2$ , it is necessary to take measures such as decreasing the charging current by increasing the rising time.

### 13.4.3 Dynamic Characteristics of pn Diode

#### 13.4.3.1 Reverse and Forward Recovery of Characteristics

The dynamic characteristics of PiN diodes include reverse recovery, forward recovery, and OCVD (open-circuit voltage decay). These are these methods for calculating the carrier lifetime.

In the reverse recovery characteristics, the carriers stored during the forward conduction are considered to be equal to the carriers extracted by the reverse recovery current and the analysis is performed. The carrier lifetime  $\tau_{rr}$  calculated from the reverse recovery characteristics can be expressed as

$$Q = I_f \tau_{rr} = \int i_{rr} dt = \frac{1}{2} I_{rm} t_{rr} \quad (13.39)$$

By using this equation, it can be expressed as [20]

$$\tau_{rr} = \frac{I_{rm} t_{rr}}{2I_f} \quad (13.40)$$

where  $Q$  is the charge stored in the drift layer during forward conduction,  $I_f$  is the forward current,  $i_{rr}$  is the current under reverse recovery,  $I_{rm}$  is the peak reverse recovery current, and  $t_{rr}$  is the reverse recovery time.

In the forward recovery characteristics, the carriers injected from the electrodes under forward recovery are considered to be equal to the carriers stored during

forward conduction. The carrier life  $\tau_{fr}$  calculated from the forward recovery characteristics can be expressed as

$$Q = I_f \tau_{fr} = \int i_{fr} dt = I_f t_{fr} \quad (13.41)$$

By using this equation, it can be shown that [21]

$$\tau_{fr} = t_{fr} \quad (13.42)$$

where  $i_{fr}$  is the current under forward recovery and  $t_{fr}$  is the forward recovery time.

### 13.4.3.2 Open-Circuit Voltage Decay

In OCVD, the decrease in voltage after opening the circuit is related to the decrease in carrier density due to the dissipation of carriers; thus, the analysis is performed [22]. A PiN diode with a  $p^+/n^-/n^+$  structure is considered as a device, and it is assumed to be in a high-level injection under forward conduction. For zero current, the electric field at the  $n^-$  layer, i.e. the voltage drop at the  $n^-$  layer, can be ignored, and the voltage between terminals is applied at the  $p^+/n^-$  and  $n^-/n^+$  interfaces. Further, we calculate the voltages applied to the  $p^+/n^-$  and  $n^-/n^+$  interfaces. The voltage difference at the  $p^+/n^-$  interface was determined by using the electric field  $F$ , it can be expressed as

$$V_{b1} - V_{j1} = - \int F dx \quad (13.43)$$

where  $V_{b1}$  is the diffusion voltage at the  $p^+/n^-$  interface and  $V_{j1}$  is the applied voltage at the  $p^+/n^-$  interface. Next, the hole current flowing through the  $p^+/n^-$  interface can be expressed as

$$J_p = ep\mu_p F - eD_p \frac{dp}{dx} \quad (13.44)$$

In OCVD, the current is zero, therefore, the electric field  $F$  can be expressed as

$$F = \frac{D_p}{\mu_p} \cdot \frac{1}{p} \cdot \frac{dp}{dx} = \frac{kT}{e} \cdot \frac{1}{p} \cdot \frac{dp}{dx} \quad (13.45)$$

where Einstein's relationship is used. By using Eq. (13.45), Eq. (13.43) can be arranged as

$$V_{b1} - V_{j1} = - \int F dx = - \frac{kT}{e} (\ln p_n - \ln p_0^+) \quad (13.46)$$

where  $p_0^+$  is the equilibrium hole density in the  $p^+$  layer and  $p_n$  is the hole density on the  $n^-$  layer side of the  $p^+/n^-$  interface.

Next, the  $n^-/n^+$  interface can be similarly expressed as

$$V_{b2} - V_{j2} = - \int F dx = \frac{kT}{e} (\ln n_0^+ - \ln n_n) \quad (13.47)$$

where  $V_{b2}$  is the diffusion voltage at the  $n^-/n^+$  interface,  $V_{j2}$  is the applied voltage at the  $n^-/n^+$  interface,  $n_0^+$  is the equilibrium electron density at the  $n^+$  layer, and  $n_n$  is the electron density on the  $n^-$  layer side of the  $n^-/n^+$  interface.

The sum of the diffusion voltage at the junction,  $V_{b1} + V_{b2}$ , was obtained by using the true carrier density  $n_i$ , and can be expressed as

$$p_0^+ n_0^+ = n_i^2 \exp \left\{ \frac{e}{kT} (V_{b1} + V_{b2}) \right\} \quad (13.48)$$

And it can be arranged as

$$V_{b1} + V_{b2} = \frac{kT}{e} \{ \ln p_0^+ + \ln n_0^+ - 2 \ln n_i \} \quad (13.49)$$

By using Eqs. (13.46), (13.47), and (13.49), the sum of the voltage applied at the  $p^+/n^-$  interface and the  $n^-/n^+$  interface can be expressed as

$$V_{j1} + V_{j2} = \frac{kT}{e} \{ \ln p_n + \ln n_n - 2 \ln n_i \} \quad (13.50)$$

In the case of high-level injection, ignoring the recombination at the interface, the carrier lifetime  $\tau_{HL}$ , can be expressed as

$$-\frac{dp_n}{dt} = \frac{p_n}{\tau_{HL}} \quad (13.51)$$

$$-\frac{dn_n}{dt} = \frac{n_n}{\tau_{HL}} \quad (13.52)$$

And they can be arranged as

$$\frac{1}{\tau_{HL}} = -\frac{d(\ln p_n)}{dt} \quad (13.53)$$

$$\frac{1}{\tau_{HL}} = -\frac{d(\ln n_n)}{dt} \quad (13.54)$$

Then, the time differentiation of  $V_{j1} + V_{j2}$  results in

$$\frac{d(V_{j1} + V_{j2})}{dt} = -\frac{kT}{e} \cdot \frac{2}{\tau_{HL}} \quad (13.55)$$

And it can be arranged as

$$\tau_{HL} = -\frac{2kT}{e} / \frac{dV_T}{dt} \quad (13.56)$$

where  $V_T = V_{j1} + V_{j2}$  is the voltage between the diode terminals, and  $dV_T/dt$  is the rate of reduction of the voltage between the terminals.

In the case of low-level injection, the carrier lifetime  $\tau_{LL}$ , ignoring the recombination at the interface, can be expressed as

$$-\frac{dp_n}{dt} = \frac{p_n}{\tau_{LL}} \quad (13.57)$$

And they can be arranged as

$$\frac{1}{\tau_{LL}} = -\frac{d(\ln p_n)}{dt} \quad (13.58)$$

Then, the time differentiation of  $V_{j1} + V_{j2}$  results in

$$\frac{d(V_{j1} + V_{j2})}{dt} = -\frac{kT}{e} \cdot \frac{1}{\tau_{LL}} \quad (13.59)$$

And it can be arranged as

$$\tau_{LL} = -\frac{kT}{e} / \frac{dV_T}{dt} \quad (13.60)$$

### 13.4.3.3 Comparison of Reverse and Forward Recovery Characteristics and OCVD

In the reverse recovery characteristic, the carriers taken out by the reverse recovery current become smaller than the stored carriers due to recombination at the pn junction and other effects. With the same idea, the externally injected carriers by the forward recovery current become greater than the stored carriers. Therefore, it is expected that there is a relationship  $\tau_{RR} < \tau_{OCVD} < \tau_{FR}$  in the carrier lifetime calculated from each characteristic. In this section, the relationship between the calculated carrier lifetimes and the SRH carrier lifetimes is calculated by using TCAD simulations.

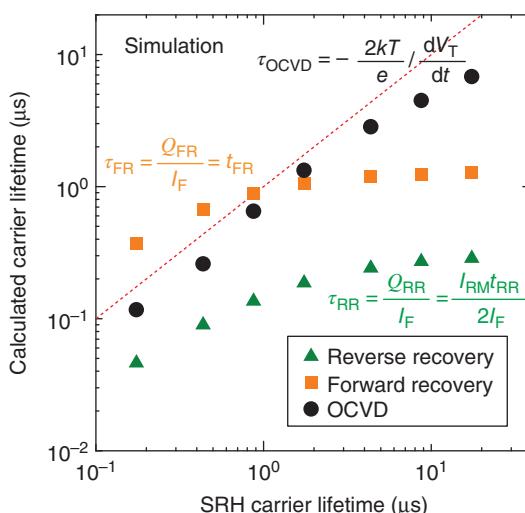
Figure 13.13 shows the relationship of the SRH carrier lifetimes with the carrier lifetimes calculated from the reverse recovery characteristics, forward recovery characteristics, and OCVD using the simulation. Here, we plot the effective electron carrier lifetimes  $\tau_{e,dop}$  as the SRH carrier lifetimes, which are calculated from

$$\tau_{e,dop} = \frac{\tau_e}{1 + \left( \frac{N_A + N_D}{N_{ref}} \right)^\gamma} \quad (13.61)$$

$$\tau_{h,dop} = \frac{\tau_h}{1 + \left( \frac{N_A + N_D}{N_{ref}} \right)^\gamma} \quad (13.62)$$

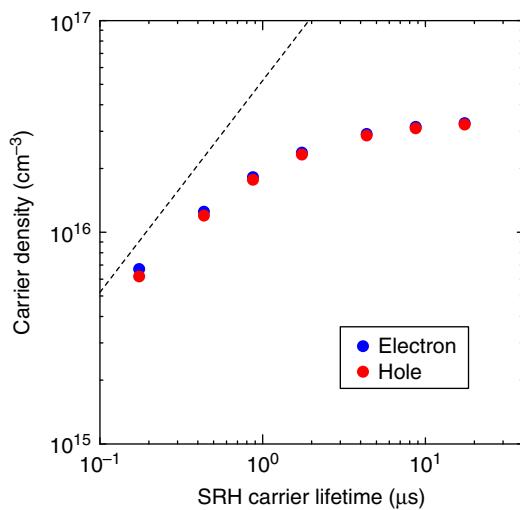
$$\frac{\tau_e}{\tau_h} = 3 \quad (13.63)$$

The red dotted line indicates that the calculated carrier lifetime is the same as the SRH carrier lifetime. The carrier lifetime calculated from OCVD increases with an increase in the SRH carrier lifetime. When the SRH carrier lifetime is small, the relationship  $\tau_{RR} < \tau_{OCVD} < \tau_{FR}$  holds. However, when the SRH carrier lifetime



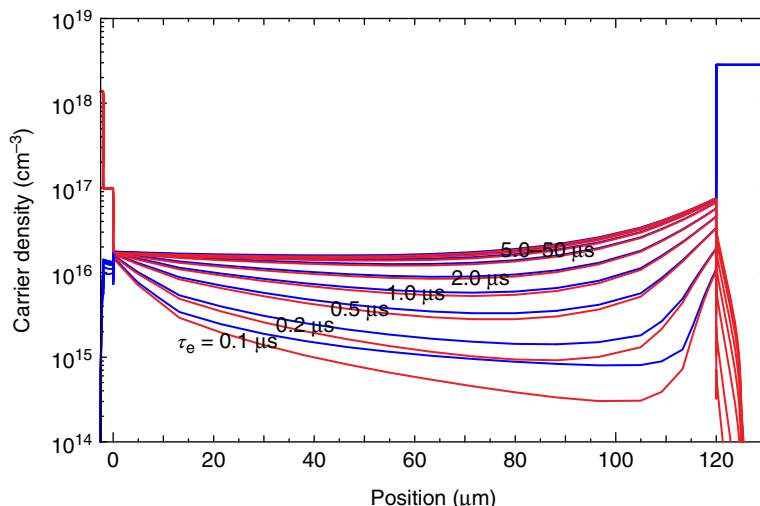
**Figure 13.13** Relationship between the carrier lifetimes calculated from the reverse and forward recovery characteristics and OCVD, and the SRH carrier lifetimes: SRH carrier lifetimes are plotted on the effective electron carrier lifetimes  $\tau_{e,dop}$ .

**Figure 13.14** Dependence of the averaged density of electrons and holes in the drift layer at  $100 \text{ A/cm}^2$  on the SRH carrier lifetime in the simulation: the dotted line plots the relationship between the SRH carrier lifetime, and the carrier density calculated from Eq. (13.33).

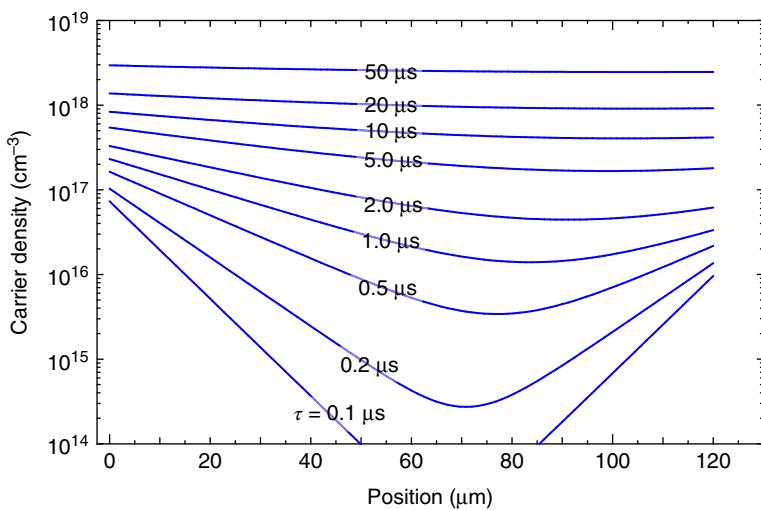


increases, the carrier lifetime calculated from the reverse and forward recovery characteristics gradually becomes saturated, which can be shown as  $\tau_{\text{RR}} < \tau_{\text{FR}} < \tau_{\text{OCVD}}$ .

We first investigated the charge stored in the drift layer at  $100 \text{ A/cm}^2$ . Figure 13.14 shows the dependence of the averaged electron and hole densities in the drift layer at  $100 \text{ A/cm}^2$  on the SRH carrier lifetime. The dotted line plots the relationship between the SRH carrier lifetime and the carrier density calculated from (13.33). The averaged electron and hole densities in the drift layer deviate from Eq. (13.33) and tend to be saturated as well as the carrier lifetime calculated from the reverse and forward recovery characteristics. Figure 13.15 shows the carrier density distribution calculated from the TCAD simulation. This figure shows that the



**Figure 13.15** Dependence of the distribution of electron and hole densities in the drift layer at  $100 \text{ A/cm}^2$  on the SRH carrier lifetime in the TCAD simulation.



**Figure 13.16** The distribution of carrier density calculated from Eq. (13.30): the mobility of electrons and holes is set to  $\mu_n = 950 \text{ cm}^2/\text{Vs}$  and  $\mu_p = 125 \text{ cm}^2/\text{Vs}$ , respectively.

distribution of carrier densities does not change as the SRH carrier lifetime increases more than 5  $\mu\text{s}$ . In Eq. (13.30), the electron and hole mobilities are set to  $\mu_n = 950 \text{ cm}^2/\text{Vs}$  and  $\mu_p = 125 \text{ cm}^2/\text{Vs}$ , respectively, and the distribution of carrier density is shown in Figure 13.16. The carrier densities calculated from device simulations (Figure 13.15), show that the carrier density on the  $n^-$  drift layer side of the  $p^+ / n^-$  interface saturates at around  $1.5$  to  $1.7 \times 10^{16} \text{ cm}^{-3}$ , and that on the  $n^-$  drift layer side of the  $n^- / n^+$  interface saturates at around  $6.5$  to  $7.0 \times 10^{16} \text{ cm}^{-3}$ . On the other hand, as shown in Figure 13.16, the carrier density on the  $n^-$  drift layer side of the  $p^+ / n^-$  interface increases from  $7 \times 10^{16}$  to  $3 \times 10^{18} \text{ cm}^{-3}$ . Therefore, it can be concluded that the charge stored in the drift layer does not increase even though the carrier lifetime increases because the voltage and current are increased without sufficient carriers being injected into the drift layer due to the voltage drop at the interface. As shown in Figure 13.13, as the carrier lifetime increases, the carrier lifetimes calculated from the reverse and forward recovery characteristics become saturated, whereas those calculated from OCVD do not saturate as the SRH carrier lifetime increases. Therefore, OCVD is suitable as a method to estimate the carrier lifetime accurately from the dynamic characteristics.

### 13.5 Design and Device Performance of Bipolar Device

Bipolar devices in an inverter consist of IGBTs for switching and diodes for regurgitation. In this section, we describe the characteristics of these two devices.

In order to reduce the conduction losses in 4H-SiC bipolar devices, it is necessary to reduce the on-voltage by increasing the carrier lifetime and causing sufficient conductivity modulation throughout the drift layer. Although 4H-SiC is an indirect

transition type semiconductor, its carrier lifetime is very short, only a few  $\mu\text{s}$ . Particularly, 4H-SiC bipolar devices with high voltages of over 10 kV require an improvement in the carrier lifetime due to the thick drift layer. The main factor limiting the carrier lifetime of 4H-SiC is the point defect  $Z_{1/2}$  center, which traps electrons and acts as a hole trap. The  $Z_{1/2}$  centers are caused by carbon vacancies and are introduced by thermal equilibrium conditions during epitaxial growth, so it is difficult to realize long carrier lifetimes. In order to reduce the  $Z_{1/2}$  center density, two methods are proposed to reduce the carbon vacancies by supplying interstitial carbon to 4H-SiC, taking advantage of the high diffusion coefficient of interstitial carbon in 4H-SiC. One method is the thermal oxidation of the 4H-SiC surface, wherein the excess carbon generated by the thermal oxidation is diffused into the 4H-SiC as interstitial carbon. The other method is the ion implantation of carbon atoms on the surface of 4H-SiC, and the implanted carbon is diffused into 4H-SiC as interstitial carbon by annealing. Both methods give a carrier lifetime of 20  $\mu\text{s}$  for the bulk, excluding the effect of surface recombination. However, there are few reports on the electrical properties of 4H-SiC bipolar devices with thick drift layers, which are required for a longer carrier lifetime and high voltages. In this section, the electrical characteristics of 4H-SiC bipolar devices with extended carrier lifetime are investigated by device simulations.

In addition, the total loss of an IGBT or PiN diode is expressed as the sum of the on-state and switching losses. Therefore, the evaluation of IGBTs and PiN diodes is important not only for the on-state losses but also for the switching losses. In this section, we also investigate the on-state and switching losses of IGBT and PiN diodes with different BVs for different carrier lifetimes of the drift layer.

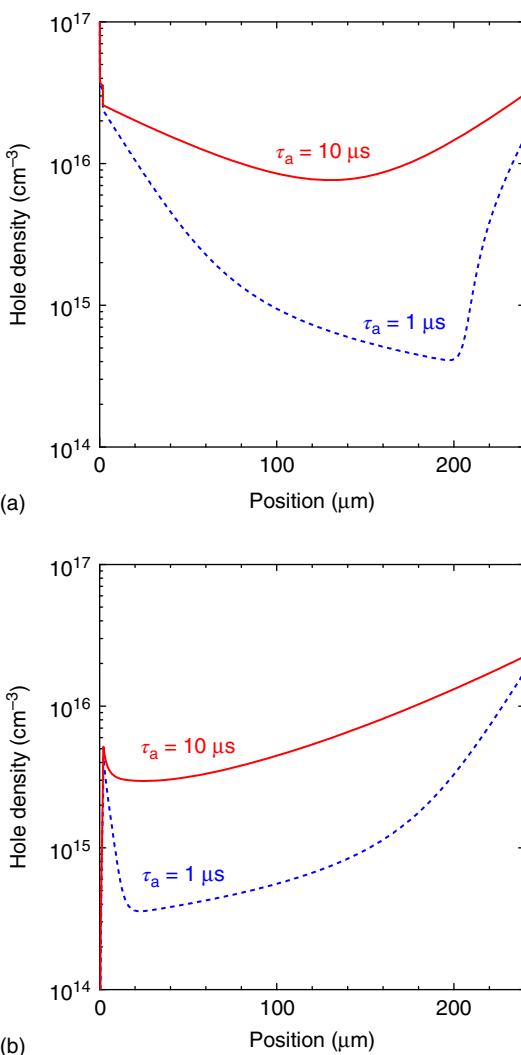
### 13.5.1 Carrier lifetime dependence

The hole density distributions in the drift layers of PiN diodes and IGBTs are shown in Figure 13.17. The blue and red lines indicate that the ambipolar carrier life ( $\tau_a$ ) is 1 and 10  $\mu\text{s}$ , respectively. Both carrier distributions exhibit a concave shape and approach a flat shape as the carrier lifetime  $\tau_a$  increases. A longer carrier lifetime leads to conductivity modulation and an increase in the hole density. In addition, the carrier densities of both the p-anode side of the PiN diode and the p-collector side of the IGBT are similar because the density of the p-layer, as well as the hole injection from the p-layer, is comparable. On the other hand, the electron density on the emitter side of the IGBT is significantly lower than that on the n-cathode side of the PiN diode because the injected electrons on the n-cathode side of the PiN diode and the emitter side of the IGBT are very different.

The forward characteristics of the PiN diodes and the on-state characteristics of the IGBTs are shown in Figure 13.18. As the carrier lifetime increases, the forward voltage and the on-state voltage decrease.

The electron and hole currents in the drift layer are dominated by the drift current, and ignoring the diffusion current, the total current can be expressed as

$$J_a = J_n + J_p = e(n\mu_n + p\mu_p)F = en(\mu_n + \mu_p)F \quad (13.64)$$



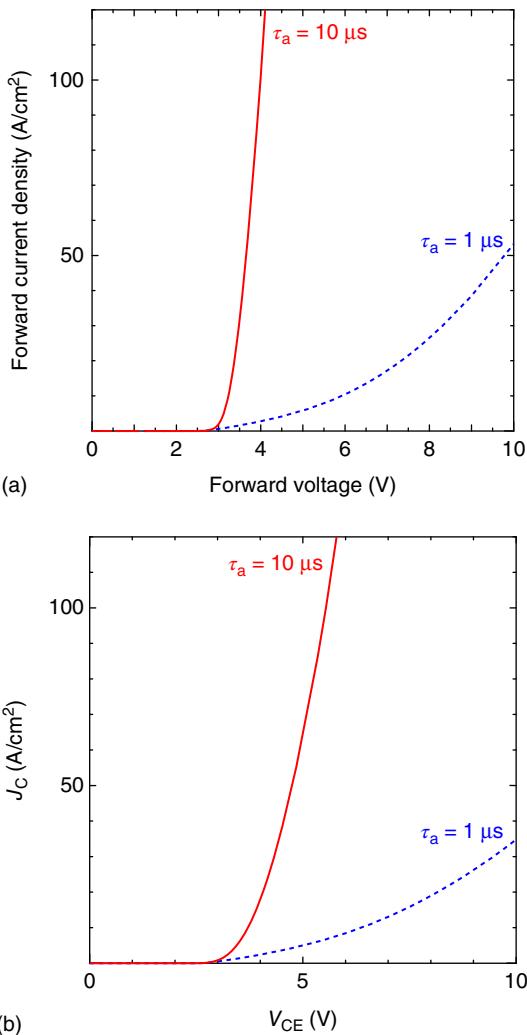
**Figure 13.17** Hole density distribution of (a) PiN diode and (b) IGBT.

where  $n = p$  from the charge neutral condition. Then, the voltage drop in the drift layer can be expressed as

$$V_{\text{drift}} = \int F dx = \int \frac{J_a}{en(\mu_n + \mu_p)} dx = \frac{J_a}{e(\mu_n + \mu_p)} \int \frac{dx}{n} \quad (13.65)$$

As the carrier density  $n$  increases, the voltage drop of the drift layer  $V_{\text{drift}}$  decreases. From Eq. (13.31), as the carrier lifetime increases, the carrier density in the drift layer increases and the forward voltage of the PiN diode and the on-voltage of the IGBT decrease, as shown in Figure 13.18. In addition, since the carrier density on the n-cathode side of the PiN diode is greater than that on the emitter side of the IGBT, the forward voltage of the PiN diode is smaller than the on-voltage of the IGBT.

**Figure 13.18** Forward characteristics of (a) PiN diode and (b) IGBT.

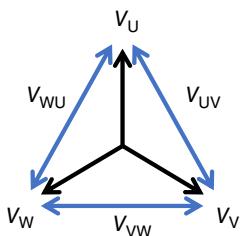


Therefore, it is important to reduce the on-voltage of the IGBT by increasing the carrier density on the emitter side of the IGBT and increasing the carrier lifetime.

### 13.5.2 Loss Estimation of Bipolar Device

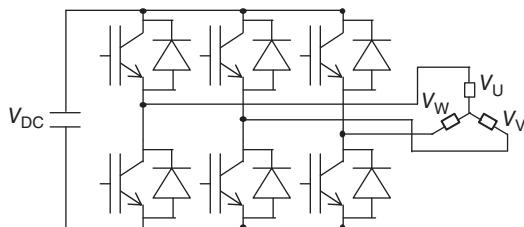
The total loss of an IGBT or PiN diode is expressed as the sum of the on-state loss and switching loss. Therefore, the evaluation of IGBTs and PiN diodes is important for both the on-state losses and switching losses. In this section, the on-state and switching losses of IGBT and PiN diodes with different BVs are investigated for different carrier lifetimes of the drift layer.

As an application, a three-phase DC–AC PWM inverter is taken as an example and the total losses of IGBTs and PiNs with different BVs are compared. Figure 13.19 shows the relationship between the phase-to-neutral voltage and the phase-to-phase



$V_U, V_V, V_W$  : Phase-to-neutral RMS voltage  
 $V_{UV}, V_{VW}, V_{WU}$  : Phase-to-phase RMS voltage

**Figure 13.19** Vector diagram of 3-phase AC.



**Figure 13.20** Circuit diagram of 3-phase DC-AC PWM inverter.

voltage, which can be given by

$$V_{UV} = V_{VW} = V_{WU} = \sqrt{3}V_U = \sqrt{3}V_V = \sqrt{3}V_W \quad (13.66)$$

Figure 13.20 shows the circuit diagram of the three-phase DC-AC PWM inverter. The DC and AC voltages can be expressed as

$$M \times \frac{V_{DC}}{2} = \sqrt{2}V_U = \sqrt{2}V_V = \sqrt{2}V_W \quad (13.67)$$

where  $M$  is the modulation ratio. In the case of connecting to a nominal voltage of 6.6 kV, each voltage of the 3-phase DC-AC PWM inverter is as shown in Table 13.1. For a 100 kVA class 6.6 kV 3-phase DC-AC PWM inverter, the RMS value of the phase current can be expressed as

$$I_{RMS} = \frac{100 \text{ kVA}}{\sqrt{3} \times 6.6 \text{ kV}} = 8.75 \text{ A} \quad (13.68)$$

Then, the maximum peak value of the phase current can be expressed as

$$I_p = \sqrt{2} \times 8.75 \text{ A} = 12.4 \text{ A} \quad (13.69)$$

In the following calculations, the DC supply voltage is assumed to be 13.5 kV and the peak value of the phase current is 12.4 A.

**Table 13.1** AC and DC Voltages of the 3-phase DC-AC PWM inverter in the case of connecting to a nominal voltage of 6.6 kV.

AC phase-to-phase (line-to-line)		AC phase-to-neutral		DC voltage
Nominal voltage (RMS voltage)	Peak voltage	RMS voltage	Peak Voltage	$M = 0.8$
6.6 kV	9.33 kV	3.81 kV	5.39 kV	13.5 kV

The loss of IGBT and PiN diodes in PWM inverters can be expressed as [23]

$$\begin{aligned} P_{\text{onIGBT}} &= \frac{1}{2\pi} \int_0^\pi I_p \sin x \times V_{\text{on}} \sin x \times \frac{1 + D \sin(x + \theta)}{2} dx \\ &= I_p V_{\text{on}} \left( \frac{1}{8} + \frac{D}{3\pi} \cos \theta \right) \end{aligned} \quad (13.70)$$

$$\begin{aligned} P_{\text{swIGST}} &= \frac{1}{2\pi} \int_0^\pi \frac{E_{\text{sw}} \sin x}{T_c} \\ &= \frac{f_c E_{\text{sw}}}{\pi} \end{aligned} \quad (13.71)$$

$$\begin{aligned} P_{\text{onPiN}} &= \frac{1}{2\pi} \int_\pi^{2\pi} (-I_p \sin x) \times (-V_F \sin x) \times \frac{1 + D \sin(x + \theta)}{2} dx \\ &= I_p V_F \left( \frac{1}{8} - \frac{D}{3\pi} \cos \theta \right) \end{aligned} \quad (13.72)$$

$$\begin{aligned} P_{\text{swPiN}} &= \frac{1}{2\pi} \int_0^\pi \frac{E_{\text{rr}}}{T_c} dx \\ &= \frac{f_c E_{\text{rr}}}{2} = \frac{f_c I_{\text{RM}} V_{\text{DC}} t_{\text{rr}}}{8} = \frac{f_c V_{\text{DC}} Q_{\text{rr}}}{4} \end{aligned} \quad (13.73)$$

Here, the on-state characteristics of the IGBT and PiN diodes are assumed to be linear, the switching loss of IGBT is assumed to be proportional to the current, and the reverse recovery loss of the PiN diodes is assumed to be constant regardless of the current. In this loss calculation, the switching losses of IGBT and PiN diodes are calculated only as turn-off losses and reverse recovery losses, respectively, because the turn-on losses are more dependent on the characteristics of the PiN diode than on the characteristics of the IGBT and therefore cannot be evaluated for losses derived from the IGBT. It is assumed that the turn-off loss of the IGBT is proportional to the DC voltage and turn-off current, and the reverse recovery loss of the PiN diode is proportional to the DC voltage.

Figures 13.21 and 13.22 show the trade-off between the on-voltage and switching loss of PiN diodes and IGBTs, respectively. For the estimation of losses, the carrier frequency  $f_c$  was set at 1 kHz, the modulation factor  $D$  was set at 0.8, and the power factor  $\cos \theta$  was set at 0.95. The red, green, and blue dotted lines in the figure represent the combination of on-voltage and switching losses that takes the minimum total loss for each voltage class. The black dotted line represents the combination of on-voltage and switching loss where the on-voltage is equal to the switching loss. For both IGBTs and PiN diodes, as the carrier life increases, the on-state voltage decreases, but the switching loss increases. The calculated total losses are minimized when the carrier life is longer than 10  $\mu\text{s}$  for IGBT and 2  $\mu\text{s}$  for PiN.

Table 13.2 shows the results of the calculation of the total loss per arm for a 100 kVA class 6.6 kV 3-phase DC–AC PWM inverter. The losses with 24 kV devices were reduced by about 36% compared with those with 6.5 kV devices. Because the switching losses of 24 kV devices are greater than those of 6.5 kV devices, the difference between the 1 series of 24 kV devices and the 4 series of 6.5 kV devices

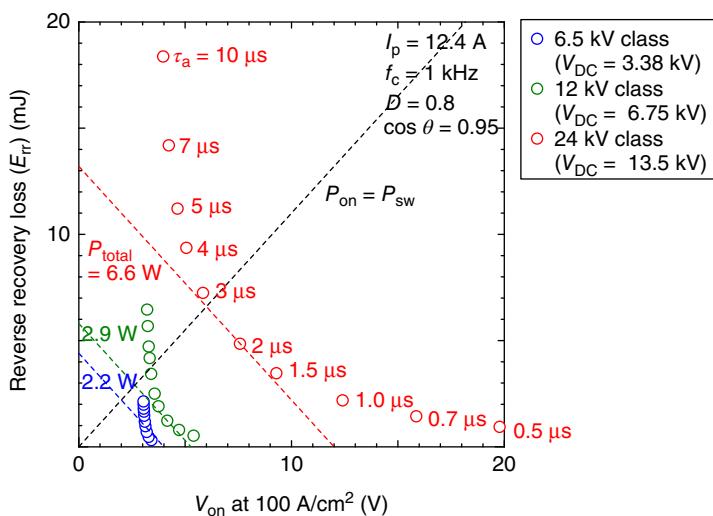


Figure 13.21 Trade-off between on-state voltage and switching loss in PiN diodes.

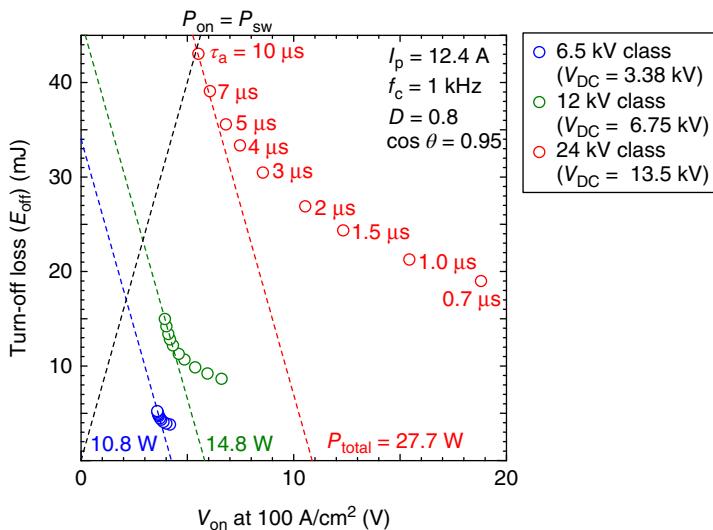


Figure 13.22 Trade-off between on-state voltage and switching loss in IGBTs.

may be reduced and reversed when the carrier frequency is increased. However, an increase in the number of series is still a problem due to the installation of snubber capacitors and the complexity of the control circuit, and a smaller number of series is still better, so 24 kV-class devices are more advantageous. Moreover, if the gate resistance is made small ( $51 \Omega$ ), the switching loss is reduced by an order of magnitude. In this case, it is expected that the losses of 24 kV-class devices will be small, even at high carrier frequencies.

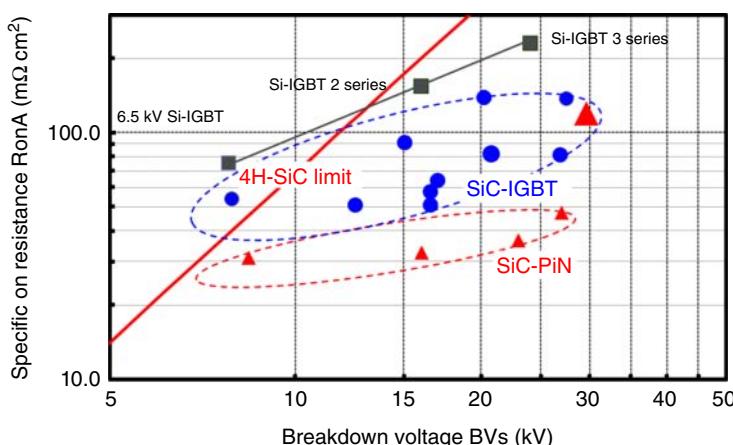
**Table 13.2** Results of the calculation of the total loss per arm for a 100 kVA class 6.6 kV 3-phase DC–AC PWM inverter.

BV class		6.5 kV	12 kV	24 kV
Series number		4	2	1
IGBT 10 µs	On-state	36.8	20.2	14.1
	Switching loss	6.5	9.4	13.6
	Total loss	43.3	29.7	27.7
PND 2 µs	On-state loss	6.9	3.9	4.2
	Switching loss	2.3	2.5	2.4
	Total loss	9.2	6.4	6.6
Sum		52.5	36.1	34.3
Ratio to 6.5 kV		1.00	0.69	0.65

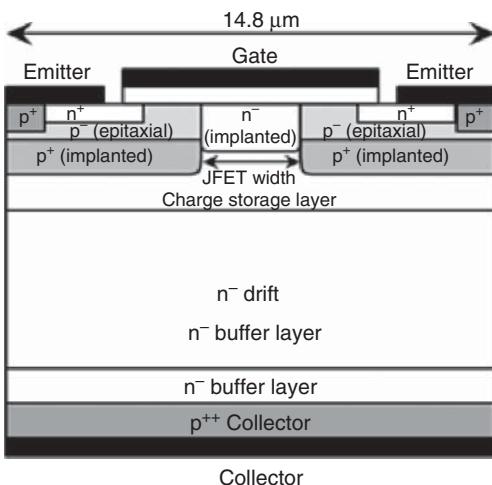
## 13.6 Current Status of SiC Bipolar Device

In this chapter, we report on the current status of ultra-high-voltage bipolar devices and on other challenges.

In Figure 13.23, the characteristics of PiN diodes and IGBTs reported so far are plotted with the BV on the horizontal axis and the characteristic on-resistance at 100 A/cm<sup>2</sup> on the vertical axis, showing a comparison between the limit curve of SiC and the series of Si-IGBTs. With respect to the BVs, the voltage range of 4.5–29.6 kV was reported for PiN diodes and 6.5–27 kV was reported for IGBTs [6–9, 15, 24, 25]. Regarding the specific on-resistance, PiN diodes have been made to have low on-resistance as described before, but IGBTs have not yet been made



**Figure 13.23** Reported Break down voltage vs. on-resistance at 100 A/cm<sup>2</sup> of IGBTs and PiN diodes.



**Figure 13.24** Cross-sectional view of the SiC-IGBT.

to have a sufficiently low on-resistance. In the following section, the 16 and 20 kV class SiC-IGBTs are introduced.

### 13.6.1 Device Performance of 16 kV Class SiC-IGBT

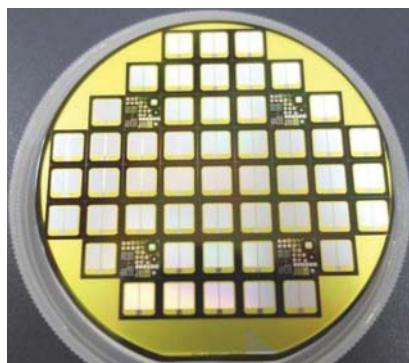
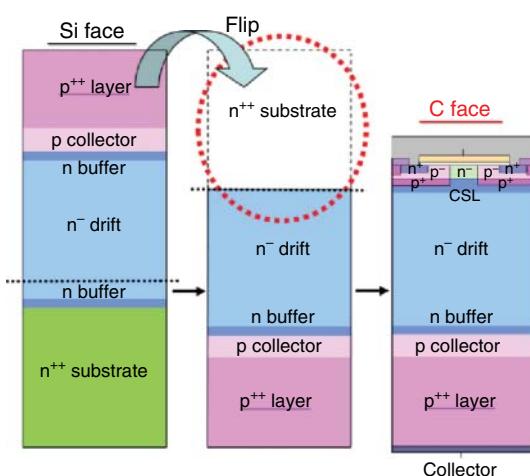
Figure 13.24 is a schematic cross-sectional view of a SiC-IGBT. Since the BV layer at 16 kV is as thin as 150  $\mu\text{m}$ , a flip-type epitaxial wafer with a thick p<sup>++</sup> epitaxial layer was used as a collector side substrate to pass through the device process. The flip-type wafer fabrication method is as follows. First, an n-type layer with a thickness > 170  $\mu\text{m}$  and a field stop layer were grown on the Si surface n<sup>++</sup> substrate. A p<sup>+</sup> current collector layer was formed. Subsequently, a p<sup>++</sup> layer ( $2 \times 10^{19} \text{ cm}^{-3}$ ) was grown to achieve thickness of > 200  $\mu\text{m}$ . Then, the substrate was turned over, the n<sup>++</sup> substrate was removed, and the surface was polished with chemical mechanical polishing (CMP). After the edge treatment, a charge accumulation layer (CSL) was employed to enhance the charge accumulation effect [8] (Figure 13.25).

The device structure was optimized by TCAD simulation. In particular, the blocking voltage and the JFET width dependence of  $V_f$  were investigated to obtain the optimal structure for the ultra-high-voltage SiC-IGBT. In device fabrication, implantation and epitaxial (IE) MOSFET structure was employed [26]. On the CSL layer, p<sup>+</sup>-based aluminum ions (Al<sup>+</sup>) were selectively implanted to form the base of the p-well. A 0.5  $\mu\text{m}$  thick p-epitaxial layer was then grown as the topmost p-layer. The JFET region was formed by selective implantation of nitrogen ions (N<sup>+</sup>) into the p-layer. The fabricated device has a striped unit cell with a pitch of 14.8  $\mu\text{m}$ . A two-zone (JTE) structure was used for the termination.

Figure 13.26 shows the image of the 16 kV SiC-IGBT (8 mm × 8 mm) and the blocking voltage [8].

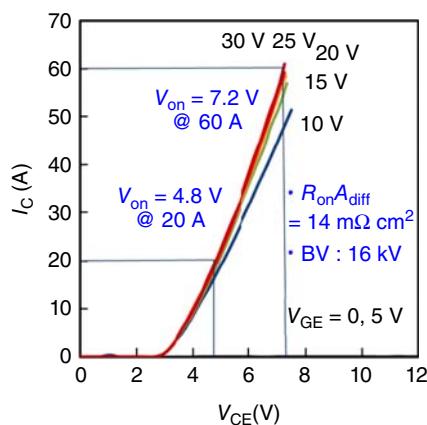
The pulsed on-state  $I$ - $V$  characteristics of the 16 kV SiC-IGBT are shown in Figure 13.27, where an on-state current of 20 A was obtained at a low on-state voltage ( $V_{\text{on}}$ ) of 4.8 V and 60 A at  $V_{\text{on}} = 7.2$  V. Further,  $R_{\text{onAdiff}}$  was 14  $\Omega\text{cm}^2$

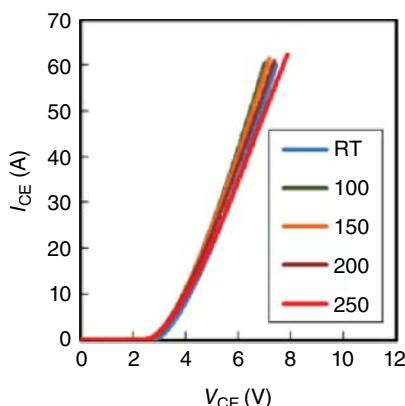
**Figure 13.25** Trade-off between on-state voltage and switching loss in IGBTs.



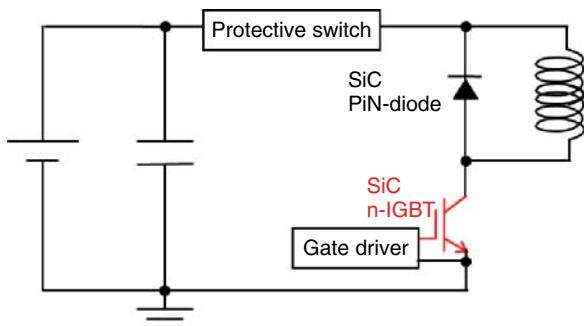
**Figure 13.26** 16 kV SiC-IGBT (8 mm × 8 mm) and reverse BV characteristics.

**Figure 13.27** Pulsed on-state  $I-V$  characteristics of the 16 kV SiC-IGBT.





**Figure 13.28** Temperature dependence of forward characteristics at  $V_{GE} = 30\text{ V}$ .



**Figure 13.29** Circuit configurations for switching measurements.

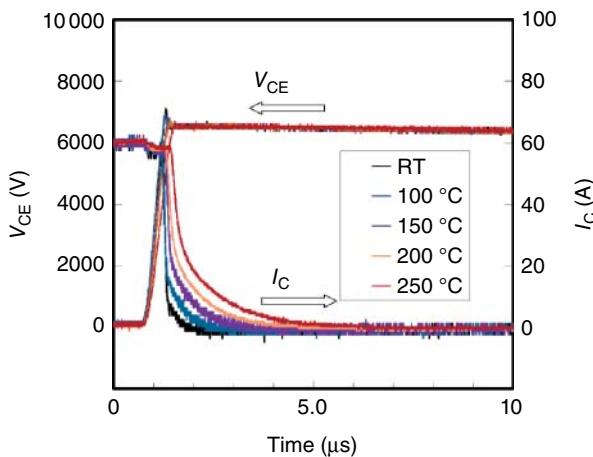
at  $100\text{ A/cm}^2$  ( $V_{GE} = +30\text{ V}$ ). Figure 13.28 shows the forward characteristics of IE-IGBT from RT to  $250^\circ\text{C}$ .

As for the dynamic characteristics, an ultra-high-voltage power module was assembled to evaluate the switching characteristics of the  $16\text{ kV}$  SiC-IGBT. The power module consists of a tungsten base plate and a direct bonding copper (DBC) base using  $\text{Si}_3\text{N}_4$ , and a copper electrode, and the DBC base and the power device are molded with resin and housed in a module case. The module case is designed to maintain a sufficient distance between the electrodes to prevent creeping discharge.

The chopper circuit configuration used to evaluate the switching characteristics of the IE-IGBT is shown in Figure 13.29. A separate SiC PiN diode ( $5.3\text{ mm} \times 5.3\text{ mm}$ ) module was used as a freewheel diode in the circuit. A  $300\Omega$  gate resistor was used for both turn-on and turn-off switching, and a  $\text{VCE}$  of up to  $\text{kV}$  was applied.

$V_{GEoff} = -10\text{ V}$  and  $V_{GEon} = +25\text{ V}$  were applied as gate voltages, and the turn-off switching temperature was set from RT to  $250^\circ\text{C}$ .

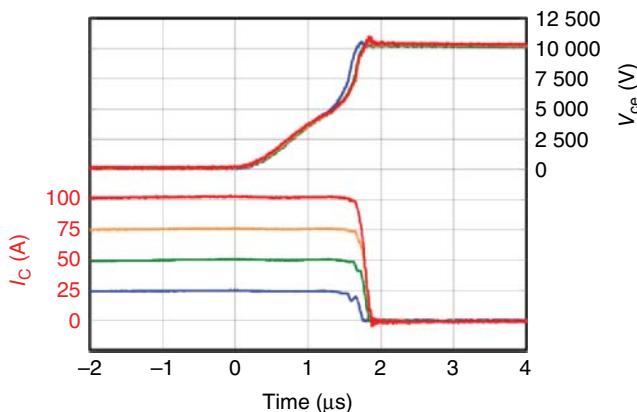
The turn-off switching waveforms of an  $8\text{ mm} \times 8\text{ mm}$  n-channel  $16\text{ kV}$  SiC-IGBT are shown in Figure 13.30 in the temperature range from RT to  $250^\circ\text{C}$ . A smooth turn-off waveform was obtained with  $\text{VCE} = 6.5\text{ kV}$  and  $\text{ICE} = 60\text{ A}$ . The turn-off energy was  $36\text{ mJ/pulse}$  at RT, but increased to  $199\text{ mJ/pulse}$  at  $250^\circ\text{C}$ . The increase



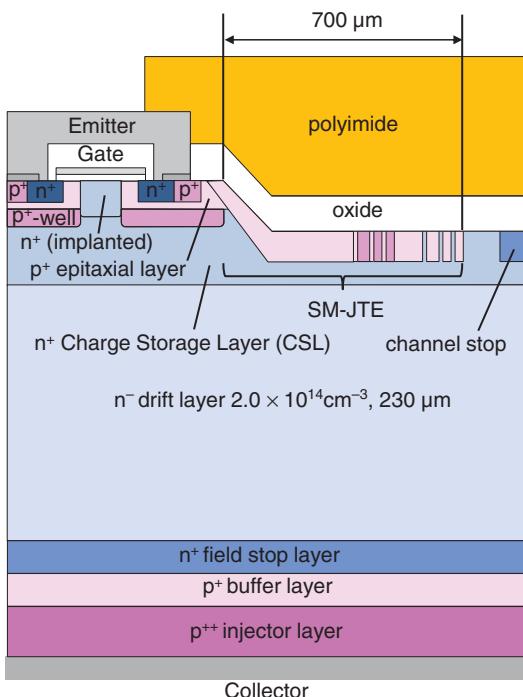
**Figure 13.30** Turn-off switching waveforms of an 8 mm × 8 mm n-channel 16 kV SiC-IGBT.

in the tail current is mainly due to the prolongation of the carrier lifetime and the injection of holes increased with increasing temperature, which resulting in a higher carrier density in the voltage withstand layer.

To demonstrate high power switching, we fabricated 1 in 1 module including four 16 kV SiC-IGBT (5.3 mm × 5.3 mm) chips connected in parallel and one PiN diode. The turn-off waveforms having a voltage of 10 kV are shown in these figures with current and temperature dependence. As shown in Figure 13.30. We successfully obtained a 10 kV, 100 A (1 MW) switching waveform. The slight change in the (dV/dt) of the collector voltage ( $V_{CE}$ ) transients at about 1.2–1.5 ms, corresponds to the punch-through of the voltage-blocking layer (Figure 13.31).



**Figure 13.31** High power switching waveform of 4 16 kV SiC-IGBTs and PiN diode.

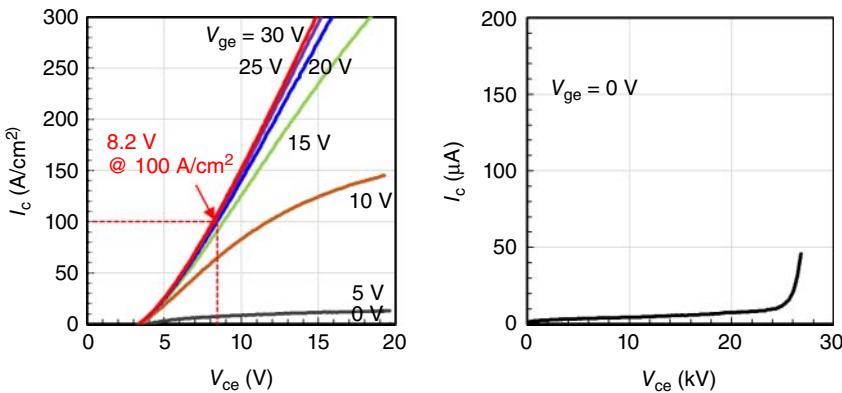


**Figure 13.32** Cross-sectional image of over 20 kV class SiC-IGBT.

### 13.6.2 Device Characteristics of higher-than-20 kV Class SiC-IGBT

In this section, the prototype of a higher-than-20 kV class SiC-IGBT is introduced. A withstand voltage layer of 20 kV requires a thickness of 200 μm or higher. However, unlike the 16 kV class, the device process can be performed with a freestanding epitaxial layer, if the thickness is more than 200 μm. Figure 13.32 shows a cross-sectional view of the 20 kV class SiC-IGBT. The actual method of fabricating a freestanding epitaxial substrate was as follows.

First, a BPD/TED conversion layer was formed, and then an n-layer with a nitrogen concentration of  $2e 14 \text{ cm}^{-3}$  and a thickness of 270 μm was formed on the silicon surface (Si surface), which is conductive to obtain low nitrogen concentration. After adjusting the withstand layer to about 250 μm, to achieve sufficient conductivity modulation for the purpose of low conduction loss as described above, carbon ion implantation and post annealing were carried out at 1650 °C [27]. The lifetime was enhanced by up to 9.6 μs, as measured by μ-PCD. After removing the n<sup>++</sup> substrate by grinding, CMP was performed and an n<sup>+</sup> field stop layer was deposited on the carbon face. In addition, a p<sup>++</sup> layer was formed as a collector layer. Subsequently, the Si surface was further ground and subject to CMP, and the thickness of the voltage withstand layer was 230 μm, and  $1.5e 16 \text{ cm}^{-3}$  was formed as the CSL layer. Then, the active region of device was created with an IE structure.



**Figure 13.33** Forward and reverse characteristics of higher-than-20 kV class SiC-IGBT.

A space-modulated JTE was used as the peripheral withstand voltage structure [25]. The edge length was set to 700  $\mu\text{m}$ .

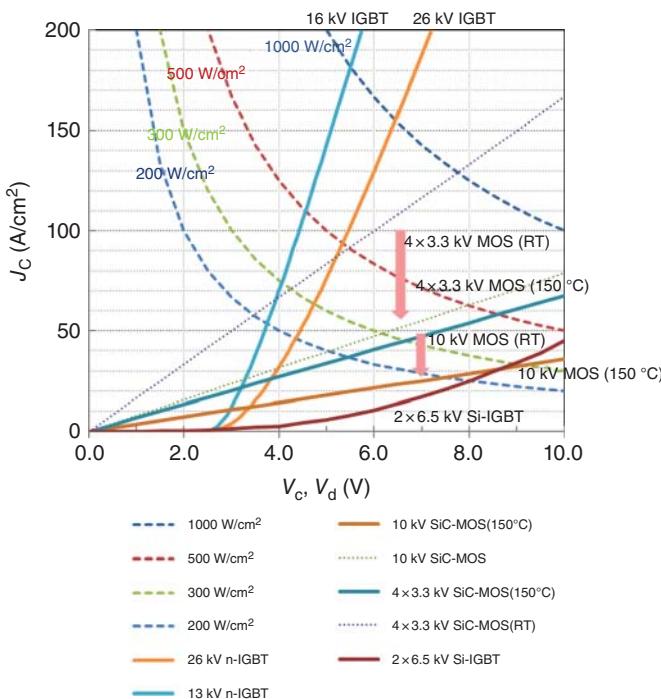
Figure 13.33 shows the forward and reverse BV characteristics of the 20 kV SiC-IGBT obtained. A withstand voltage of 26.8 kV could be obtained, an on-voltage of  $V_{\text{on}} = 8.6 \text{ V}$  at  $100 \text{ A/cm}^2$ , and a differential on-resistance of  $36.9 \text{ m}\Omega \text{ cm}^2$  were obtained at RT [28].

### 13.6.3 Other Bipolar Devices Issues

The 16 and 20 kV SiC-IGBTs were introduced as ultra-high-voltage bipolar devices. In both cases, the withstanding voltage was secured and a specific (yet low) low conduction loss was obtained. However, the turn-off switching loss has high-temperature dependence and needs further improvement. To achieve low-conduction and low-switching losses at turn-off, it is necessary to make the conductivity modulation electron-dominant. To achieve this, as in the case of Si, it is necessary to apply an injection-enhancement effect structure with a long carrier lifetime, and to limit the hole injection from the collector side.

To fully exploit the performance of ultra-high-voltage IGBTs, it is necessary to develop not only the device design but also the peripheral technology, especially the heat extraction technology. Figure 13.34 compares the IV characteristics of an ideal 16 and 20 kV SiC-IGBT with SiC-MOSFETs and Si-IGBTs of the 16 kV equivalent series. The dotted lines show the cooling capacity curves. Normally,  $2\text{--}300 \text{ W/cm}^2$  is the limit for air cooling, and  $800 \text{ W/cm}^2$  and  $800 \text{ W/cm}^2$  for double-sided cooled power cards. If there is a cooling method that exceeds  $1000 \text{ W/cm}^2$ , the potential of SiC-IGBTs can be maximized.

We hope that these ultra-high-voltage SiC bipolar devices will be used in the high-voltage power electronics for next-generation electricity network, and will contribute to the realization of a low-carbon and safer society.



**Figure 13.34**  $I-V$  curve comparison of ideal SiC-IGBT, series of equivalent BV of 16 kV SiC-MOSFET and Si-IGBTs with cooling capability curves.

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# 14

## SiC Reliability Aspects

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### 14.1 Ruggedness and Overload Events

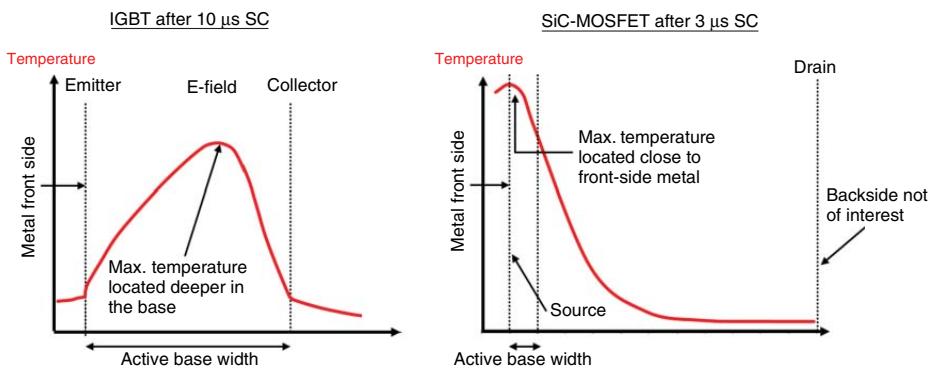
#### 14.1.1 Short-circuit Ruggedness of SiC MOSFETs

Today, only a small number of manufacturers state a short-circuit capability in the datasheet of their respective SiC metal–oxide–semiconductor field-effect transistors (MOSFETs). One reason is the small intrinsic short-circuit capability compared to state-of-the-art insulated gate bipolar transistors (IGBTs). The root cause can be found in the unfavorable temperature distribution during and after a short-circuit event.

In the case of an SiC MOSFET, almost the entire short-circuit energy is generated and dissipated in the first some micrometers below the frontside chip surface. For a 1200 V SiC MOSFET, the “active” base width is just in the range of 10 µm.

In this region, most of the short-circuit power loss is generated. This leads to a high temperature at the frontside chip region which will stress especially the power metal, gate oxides, and other frontside topologies, see Figure 14.1 and [1, 2], respectively. Due to the strong temperature gradient in the SiC substrate, the backside of the chip remains almost at starting temperature. The IGBT distributes the temperature more homogeneously across the total chip thickness and has, defined by the electric field distribution, the temperature maximum in the range of two-thirds from the frontside in the total chip thickness, see Figure 14.1. Therefore, to improve the short-circuit ruggedness of an SiC MOSFET, especially the frontside with its interconnections must be thermally optimized.

However, chip-internal characteristics can be adjusted as well. There are typical  $R_{DS,ON}$  vs. short-circuit time trade-offs also known from the common silicon MOSFET structure. The most popular ones are the channel-width trade-off, the  $V_{GS,TH}$  trade-off, and the gate-bias trade-off. Additionally, it is also possible to adjust the  $n$ -source resistance, as mentioned in [3]. In general, any short-circuit time can be achieved at the expense of  $R_{DS,ON}$ .



**Figure 14.1** Schematic temperature distribution after short-circuit event of an IGBT (left) and an SiC MOSFET (right).

If the standard equation for the saturation regime of an MOSFET is used [4]

$$I_{D,\text{sat}} = \frac{k}{2}(V_{GS} - V_{GS,\text{TH}})^2 \quad (14.1)$$

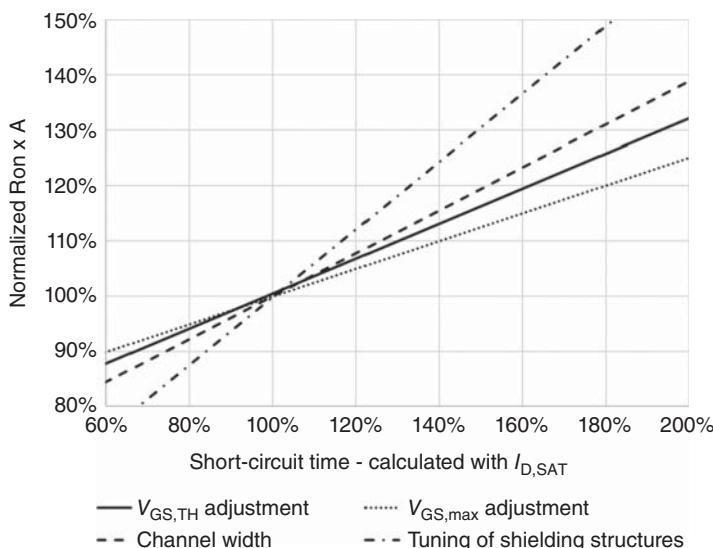
with channel conductivity ( $W$ , channel width,  $C_{\text{OX}}$ , oxide capacitance,  $\mu_n$ , electron-channel mobility)

$$k = \frac{W \cdot C_{\text{OX}} \cdot \mu_n}{L}, \quad (14.2)$$

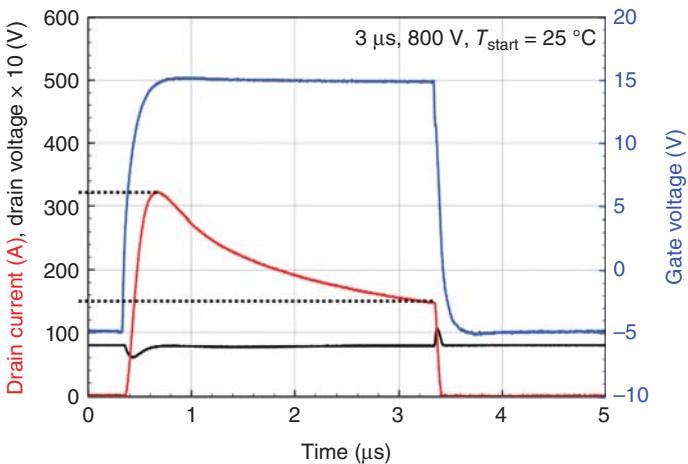
then the standard trade-offs for increasing the short-circuit withstand time which is proportional to the saturation current can directly be derived. On the other side, the trade-offs have also a consequence on the channel resistance  $R_{\text{CH}}$  with

$$R_{\text{CH}} = \frac{1}{\frac{W}{L} \cdot C_{\text{OX}} \cdot \mu_n \cdot (V_{GS} - V_{GS,\text{TH}})}. \quad (14.3)$$

If the channel width is reduced, the saturation current is directly lowered. For increase of threshold voltage,  $I_{D,\text{sat}}$  is lowered. A gate-bias reduction also leads to a reduced saturation current. The gate-bias control method is already applied for SiC MOSFET short-circuit protection, where  $V_{GS}$  is instantly lowered, if a short-circuit event is detected [5, 6]. Some of the abovementioned trade-offs were simulated using TCAD in Figure 14.2, where  $R_{\text{DS,ON}}$  vs. the short-circuit withstand time is plotted for a high-voltage SiC MOSFET, similar to [3]. It has to be mentioned that a low  $R_{\text{DS,ON}}$  at the cost of short-circuit time is only possible to some amount since, e.g. sufficient field-shielding structures or minimal gate-oxide thicknesses for achieving high gate-oxide reliability are limiting. Furthermore, the trade-offs are strongly dependent on the cell design and voltage class. Figure 14.2 shows a schematic dependency.



**Figure 14.2** Simulated  $R_{\text{DS,ON}}$  vs. short-circuit time trade-offs, base for simulation is a high-voltage SiC MOSFET.



**Figure 14.3** Typical short-circuit type 1 waveform of SiC trench MOSFET.

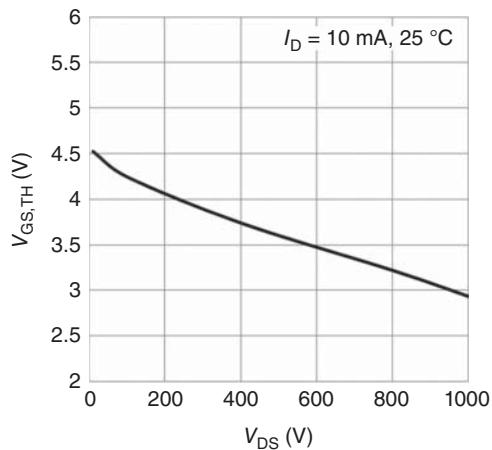
In comparison to the IGBT [7], the short-circuit type 1 waveform looks significantly different, see Figure 14.3. After a high short-circuit current peak at the beginning of the event the saturation current drops strongly to the half of the peak value after 3  $\mu$ s. The reduction can be explained by a decrease in the channel mobility with temperature, see Eq. (14.1), and even more by the known junction gate field-effect transistor (JFET)-driven current-limiting effect, see [8]. The JFET is constructed by the shielding p-regions in the different SiC MOSFET structures and is used to protect the gate oxides from high electric fields. This JFET region can also be used to adjust the short-circuit ruggedness, see Figure 14.2. To achieve a low  $R_{DS,ON}$  with high channel width, the relation “saturation current vs. application-near nominal current” is typically higher for the SiC MOSFET than for an IGBT in the same voltage class. For example, SiC MOSFETs show  $I_{D,sat}/I_{nom}$  relations in the range of 10–15. For 10  $\mu$ s short-circuit rugged IGBTs, the relation is more 3–5, which helps to keep the overall short-circuit energy dissipation low.

Additionally, the saturation current is strongly voltage dependent. The reason can be found in the typically pronounced drain-induced-barrier lowering (DIBL) effect which is directly connected with the use of short *n*-channels in SiC MOSFETs, see Figures 14.4 and 14.5 as well as [9]. If the drain-source voltage is increased, the electric field/space-charge region approaches closer to the channel region and shortens the channel effectively. Thus,  $V_{GS,TH}$  is lowered and  $I_{D,sat}$  rises with the drain-source voltage, see Eq. (14.1). This is important when the short-circuit detection levels at the gate drivers are implemented, especially when a current detection is used. The DIBL can be expressed by the following relation:

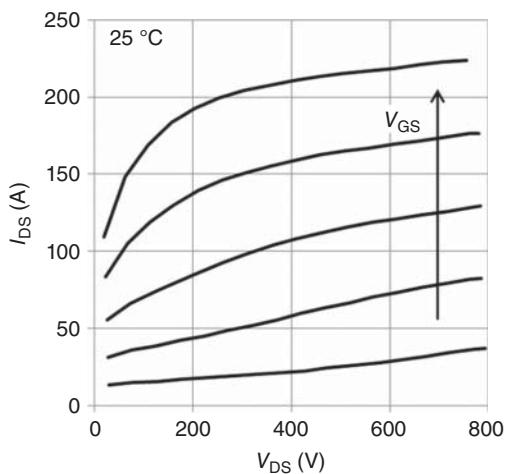
$$\text{DIBL} = \frac{\Delta V_{GS,TH}}{\Delta V_{DS}} \left[ \frac{\text{mV}}{\text{V}} \right]. \quad (14.4)$$

For the 1200 V SiC MOSFET shown in Figure 14.4, the DIBL is, e.g. 1.63 mV/V demonstrating that from  $V_{DS} = V_{GS}$  (pinch-off point) condition to  $V_{DS} = 800$  V the threshold voltage is lowered by 1.3 V. The DIBL may vary between different MOS

**Figure 14.4** DIBL effect,  $V_{GS,TH}$  is lowered with higher drain-source voltage.

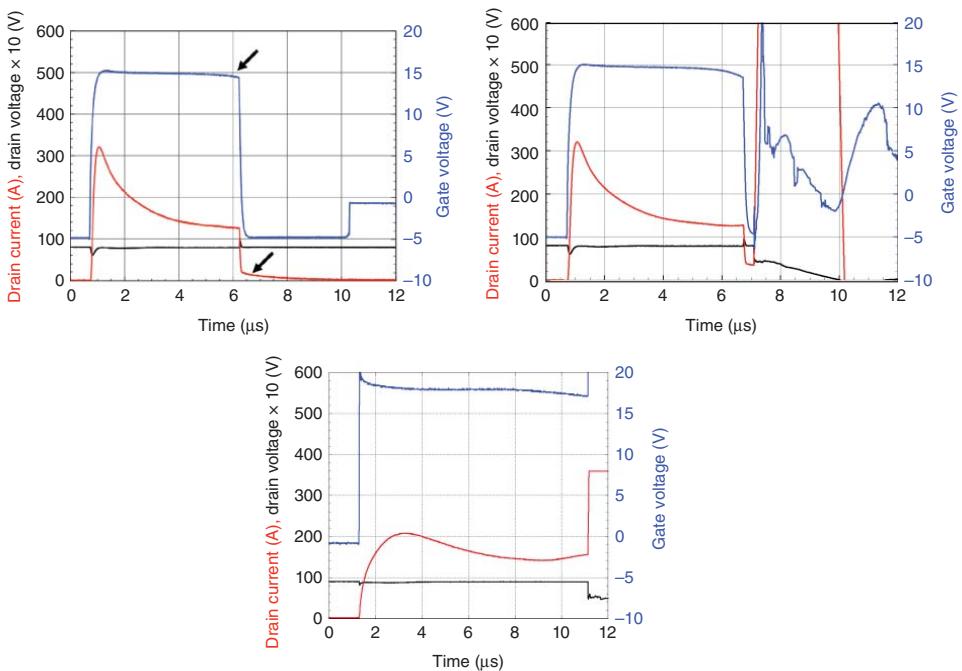


**Figure 14.5** Rising saturation currents  $I_{D,sat}$  with increased drain-source voltage.



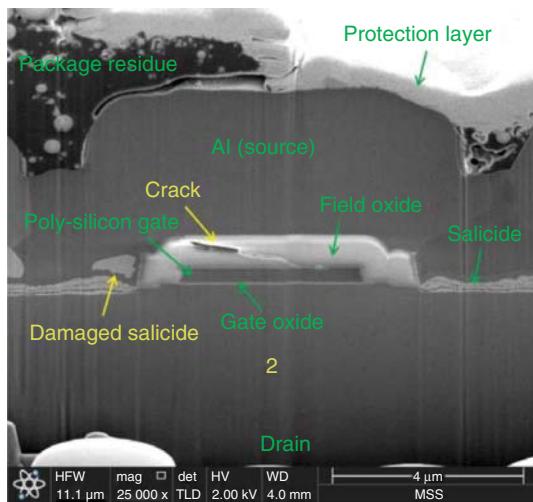
cell structures and p-shielding regions [9]. In general, this effect is also known for silicon low-voltage MOSFETs [10].

For SiC MOSFETs, different short-circuit destruction modes are known [11]. One mode is the gate-source fail after turning off an event which has lasted too long, see Figure 14.6 left and [12]. Reasons can be found in the high thermomechanical stress from the power metal on the interlayer dielectrics which can lead to cracks and finally to a hard gate-source short, compare [12, 13] and Figure 14.7. With hard gate short, the device is in off-state and may prevent a hard DC link short in the power circuit. Precondition, however, is that the damage is concentrated to the gate structure. Other gate failures can be explained by a damage of the thin gate oxide. First evaluations connect high gate-source leakage currents and gate oxide pre-damages with a Schottky emission from the gate poly into the SiC bulk [14]. Fowler-Nordheim tunneling as a main driver for high leakage currents was excluded since the electric fields are assumed to be too low; furthermore, this tunneling effect is not much temperature dependent.



**Figure 14.6** SiC MOSFET: different kinds of short-circuit destruction; Left: gate-source fail after withstanding the short circuit, Right: hard destruction at turn-off, Center: thermal runaway during the short-circuit event.

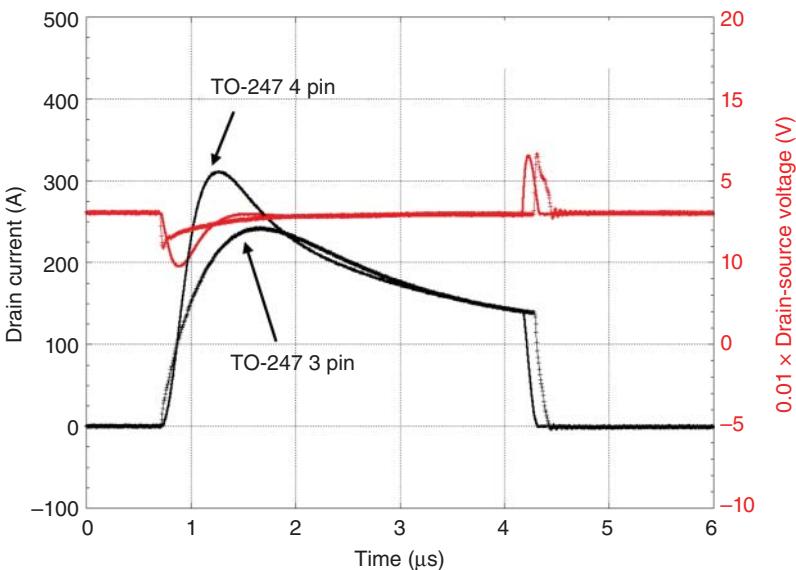
**Figure 14.7** Possible failure picture with gate-source short after a long-lasting short-circuit pulse. The interlayer dielectric between the gate electrode and the power metal was cracked. Source: Picture from Reigosa et al. [13].



In general, dips in the gate voltage during the short-circuit event and upcoming “tail” currents are signs of heavy stress (arrows in Figure 14.6 left), which may also lead to early damage and go hand in hand with parameter drifts of, e.g.  $V_{GS,TH}$ . It is important to stay away from these early warnings. The drain tail current is connected with the parasitic npn-transistor part at the above mentioned high temperatures in the range of 1000 °C. Electrons are injected directly from the  $n^+$ -source into the device which cause a high drain-source leakage current, although the gate voltage is set to zero or even a negative value. Additionally, failures during turn-off or during the pulse may appear under different conditions (stray inductance, DC-link voltage, short-circuit time, etc.), see [11] und Figure 14.6 center and right.

Since the SiC MOSFET has the ability to turn on very fast, the package may also improve the short-circuit withstand capability as shown in Figure 14.8. If the device is turned-on without common-source inductance (with sense source) like in a TO-247 4-pin housing, the peak of the short-circuit current can be much higher compared to a package with a higher common-source inductance like the 3-pin version of the TO-247. The reason can be found in the missing self-heating effect at the beginning of the event for a 4-pin housing. For the 3-pin device,  $di/dt$  is lowered by the feedback of a source inductance on the gate loop. Therefore, the device has more time to heat up which lowers the peak current due to the reduction of the electron mobility. At the end of the short-circuit event, both housings show similar saturation current levels. However, since the 3-pin device dissipates less energy during the whole event, the overall robustness in this package is a little higher. A similar effect can be achieved when using a higher gate-turn-on resistor; however, this will increase also the switching losses in general. A higher common-source inductance is the better choice.

Another effect which is very special for SiC MOSFETs is the  $V_{GS,TH}$  hysteresis [15, 16]. For lower off-gate-source voltages, the  $V_{GS,TH}$  is lower when turning on into a short circuit. This results in a significantly increased peak current from 280 A



**Figure 14.8** Short-circuit waveforms in different packages,  $V_{DC} = 800$  V,  $V_{GS} = -5/15$  V.

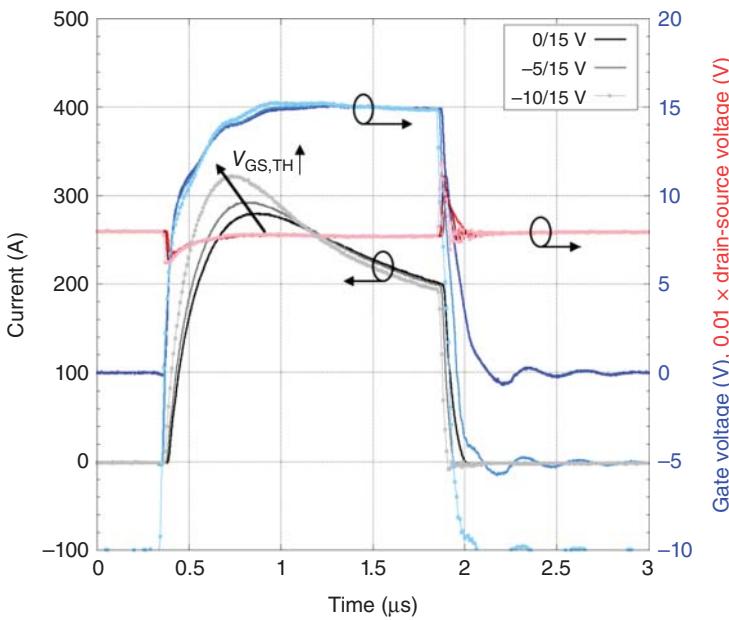
at 0 V  $V_{GS,off}$  to 325 A at  $-10$  V  $V_{GS,off}$ , see Figure 14.9. If SiC MOSFETs are used in parallel connections, this effect has to be considered in particular.

To overcome the hard trade-off between  $R_{DS,ON}$  and short-circuit withstand capability, intelligent gate driver schemes are proposed from different manufacturers and institutes, see [5, 6, 17].

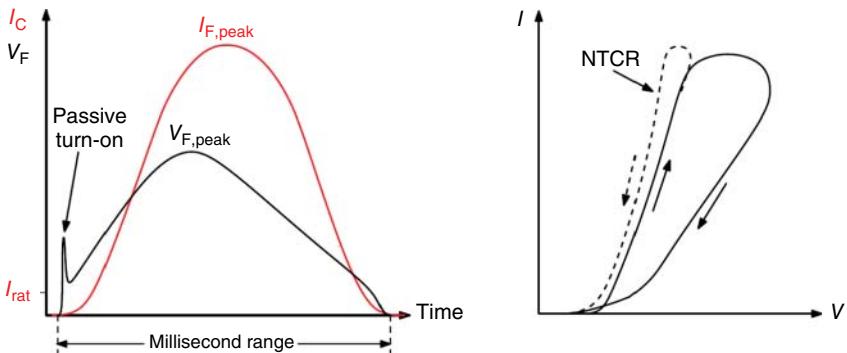
To verify a high short-circuit ruggedness, it may also be useful to check some repetitive short-circuit events. Parameters like  $V_{GS,TH}$  and leakage currents have to be stable after e.g. 10–20 short-circuit events. Just to rely on a low short-circuit time alone may be critical, since the top-side structure is exposed to a very high temperature swing with possible crack initiation, see Figure 14.7.

### 14.1.2 Surge-current Ruggedness

During converter operation, the power semiconductor devices can be imposed to high over currents with a duration in the millisecond range, defined as surge currents. To withstand these currents, devices like diodes and thyristors are rated for the case of surge current. Typically, a maximum allowed (non-repetitive) peak current during a 10 ms sine half-wave is given in the datasheet ( $I_{FSM}$ ). This standard pulse is related to grid errors with a 50 Hz grid frequency. In addition to this specific current, an  $i^2t$ -value is often given in the datasheet. In the past, different publications already explained the behavior of silicon bipolar devices in general during high overcurrents, see, e.g. [18]. A schematic waveform of a silicon pin-diode is given in Figure 14.10 left. The corresponding  $I-V$  curve, which can be used for a more detailed analysis, is shown in Figure 14.10 right. In principle, two cases can occur in the  $I-V$  diagram: positive or negative differential resistance behavior.



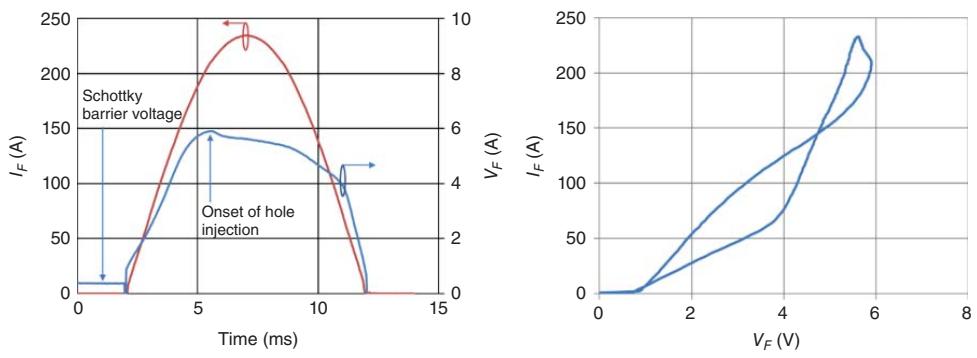
**Figure 14.9** Impact of  $V_{GS,TH}$  hysteresis on short-circuit.



**Figure 14.10** Schematic surge-current event (left) and corresponding  $I$ - $V$  curve (right). NTCR means negative temperature coefficient resistance.

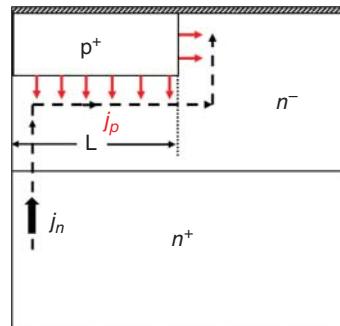
This depends also on the specific temperature characteristic of the device. For the negative case, inhomogeneous current distribution may occur. Regarding the parallel connection of single chips, the second case can be more critical.

For SiC MPS (Merged-PN-Schottky) diodes, a crossing point between the falling and rising branch occurs at higher currents due to the onset of hole injection of the p-regions, see Figure 14.11 and [19]. The highly pronounced incomplete ionization of SiC p-doped regions (e.g. Al doping) at room temperature also leads to a better p-emitter efficiency at higher temperatures which amplifies the effect of a negative differential resistance.



**Figure 14.11** Surge-current event at 1200 V/20 A rated SiC MPS diode (left) and corresponding  $I$ - $V$  curve (right).

**Figure 14.12** MPS diode: schematic way of electrons around p-island.



Often, these diodes are used in boost-converter/PFC topologies and they are exposed to high currents e.g. if the DC-link capacitor has to be re-charged quickly after a grid-voltage drop.

In [20], the on-set voltage of the hole injection was approximated by integrating along the way of the electrons around the p-islands as shown in Figure 14.12 and Eq. (14.5).

$$V_p = \int_0^L R \cdot j_n \cdot x \, dx = \frac{1}{2} \cdot R \cdot j_n \cdot L^2 \quad (14.5)$$

Here,  $R$  is the resistivity in  $\Omega/\square$  and  $L$  is the dimension of the pn-region, where  $R$  can be approximated by  $\rho/d$  for the thin epi-layer thickness  $d$ . The p-region will inject as soon  $V_p$  is equal to the difference of built-in voltage of the pn-junction and the threshold voltage of the Schottky junction. Finally, the necessary electron current density can be expressed with

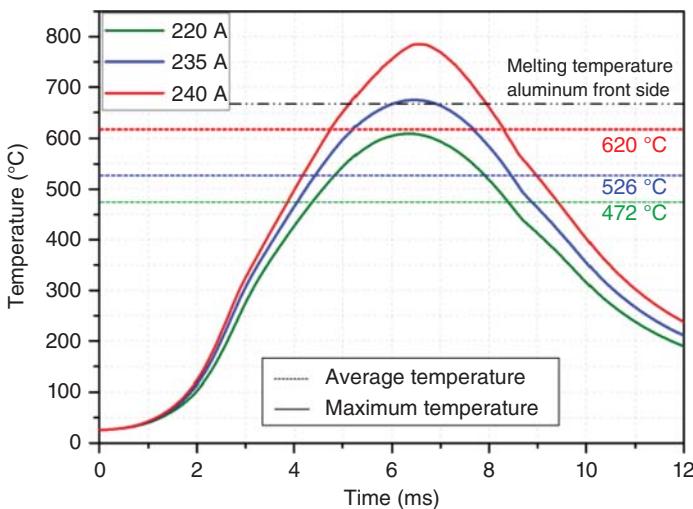
$$j_n = \frac{2 \cdot (V_{bi\_pin} - V_{Schottky})}{R \cdot L^2}. \quad (14.6)$$

Failure patterns during surge currents are typically found in the modification of the frontside metallization and bond-wire aging/destruction. Reason is the high temperature rise of the frontsidenear layers, described also in [21]. Temperatures up to 500 °C and more are reached easily during an event close to the destruction limit, see Figure 14.13 and 14.14.

Additionally, the surge-current ruggedness of the internal body diode of SiC MOSFETs is put more into the focus [22, 23]. Since this diode is used as a free-wheeling diode, it must be able to withstand surge-currents generated in special failure cases and to carry, e.g. the failure current of a motor load. A typical surge-current event at the body diode is shown in Figure 14.15.

A similar failure pattern like for SiC MPS diodes is observed during the surge-current event of the body diode under different pulse lengths. The prominent failure mechanism at very high surge-current pulses is molten source metallization which also might shorten the gate-source path at the gate runners/fingers, see Figure 14.16. However, the thermal limitation of the body diode is similar to the SiC MPS diode, if applied in the same housing (here TO-247).

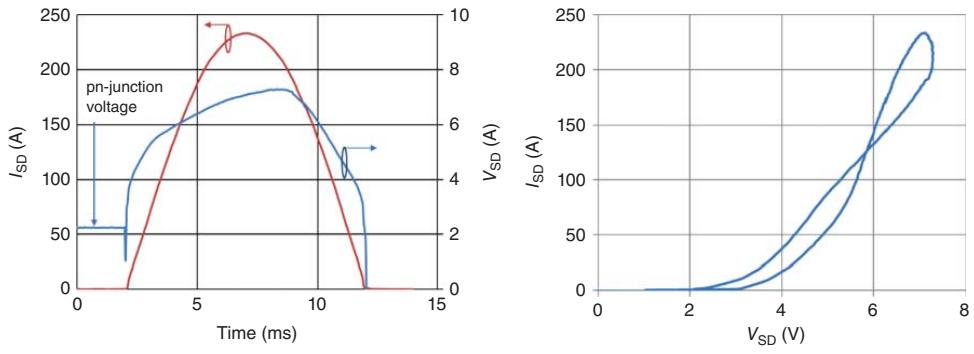
Since the diode characteristic can be controlled via the gate potential of the MOSFET, it is also possible to start the surge-current event with a positive  $V_{GS}$  as shown in



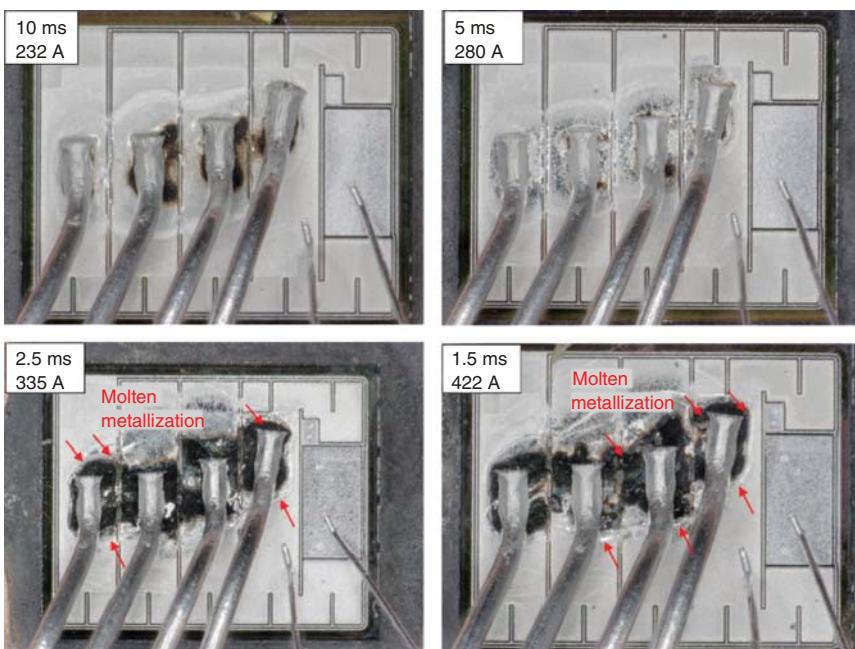
**Figure 14.13** Simulated temperatures during a 10 ms surge-current event with different peak currents for a 1200 V/20 A MPS diode. For simulation, an ANSYS model was used taking into account metallization, bond wires and the thermal properties (solder, etc.) until the lead frame. Source: Palanisamy et al. [21].



**Figure 14.14** Failure pictures after single-event destructive surge-current pulses with a 1200 V/20 A SiC MPS diode.



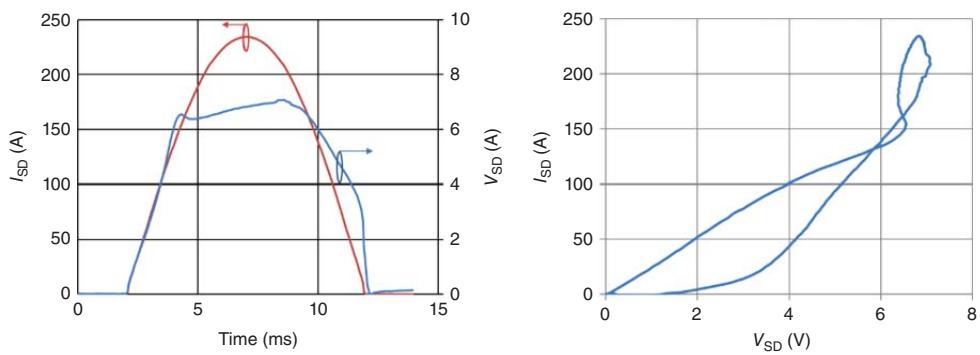
**Figure 14.15** Last pass surge-current waveform of a 1200 V/20 A SiC MOSFET body diode at  $V_{GS} = -5$  V.



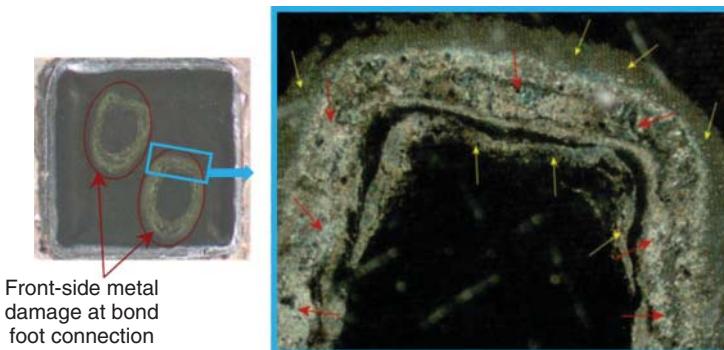
**Figure 14.16** Surge-current destruction behavior of 40 mΩ class, 1200 V SiC MOSFET under different pulse lengths. Surge current applied to body diode (third quadrant) with  $V_{GS} = -9$  V.

Figure 14.17 at  $V_{GS} = 15$  V. The most distinct difference is the missing pn-junction voltage at the beginning of the event and the visible p-region injection start, similar to the SiC MPS diode in Figure 14.11. In the 1200 V class, no huge difference between opened/closed channel operation and the maximal possible surge currents was found [9]. For higher voltage classes, it is possible that an opened n-channel hinders the p-regions from injecting holes more effectively due to the higher voltage drop across the drift region, leading to a reduced ruggedness. It has to be taken into account that for body diodes a new failure mode is added, which can be found in a damage of the gate-source path [22]. Therefore, after every surge-current pulse, the blocking capability of the drain-source path and the gate-source path has to be checked.

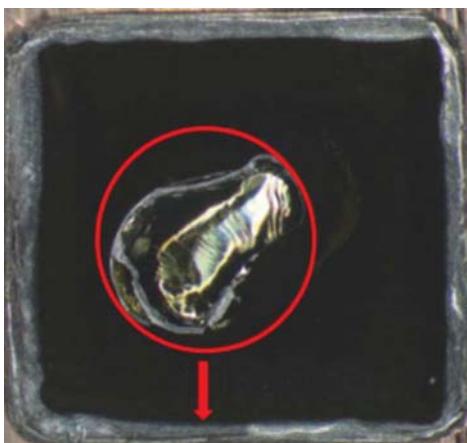
Especially, if SiC MPS diodes are used in booster topologies, repetitive over/surge currents may be possible. It was found that SiC MPS diodes could withstand a high number of high-energy surge-current pulses [24]. The main final failure mechanism is a thermomechanical destruction at the bond-wire feet which may also lead to a loss of the blocking capability, see Figure 14.18. Additionally, in some cases also cracks in the SiC substrate were found, compare Figure 14.19. A very high temperature swing in connection with different coefficients of thermal expansion (e.g. backside solder, SiC substrate, lead frame) is the root cause. Similar failures were also reported for silicon diodes exposed to high surge currents. In practice, the current peak and



**Figure 14.17** Last pass surge waveform of a 1200 V/20 A SiC MOSFET in the third quadrant  $V_{GS} = 15$  V. The body diode part of the device starts to conduct current at c. 4 ms.



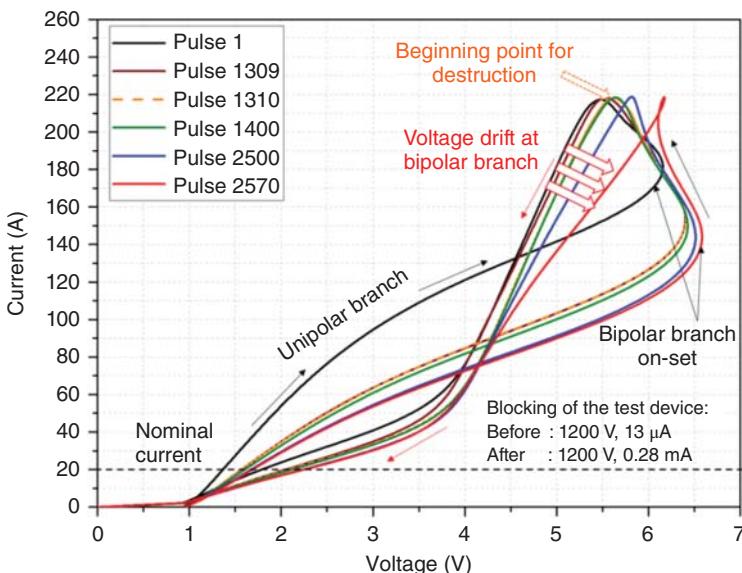
**Figure 14.18** Optical microscope image from chip backside (after removal of backside metal) after doing 533 pulses with 240 A peak current at a 20 A/1200 V SiC MPS diode.



**Figure 14.19** Shell-like crack at backside of the chip after doing 2570 pulses with 220 A/10 ms at a 20 A/1200 V SiC MPS diode.

thus the temperature for repetitive surge currents will be smaller to stay within the datasheet limits. Therefore, a high number of possible repetitive over-current events is expected. For future optimization, a thicker frontside high-melting metallization, e.g. copper, would be an improvement. An improved chip-backside connection to a lead frame or DCB also helps to increase the maximum possible surge-current energy, at least for pulses in the millisecond range. Sintering or diffusion soldering would be an adequate option.

It was reported that for very high repetitive surge currents in the bipolar regime, the growth of stacking faults is somehow unavoidable [24]. A countermeasure could be a very thick but expensive buffer region. Fortunately, compared to the normal operation condition, a surge-current event is rather seldom. Figure 14.20 shows the  $I/V$  curves of a 20 A/1200 V SiC MPS diode under a very high repetitive surge-current stress. An increased leakage current was found after the test and a shift of the forward voltage drop in the unipolar and bipolar region was observed as well. However, it is hard to distinguish between thermomechanical and bipolar degradation just from



**Figure 14.20**  $I/V$  curves of 220 A peak/10 ms sine-shape repetitive surge currents at 20 A/1200 V SiC MPS diode. An increase in leakage current and  $V_F$  shift in unipolar and bipolar regime was observed. Source: Palanisamy et al. [24].

the  $I/V$  curves. Only a detailed failure analysis, including an electroluminescence investigation of the forward-current flow, can give further insights.

Repetitive surge-current tests with SiC MOSFETs have been carried out in [25]. The applied current was higher than 10 times the channel's rated current for a time of 10  $\mu$ s. No substantial electric characteristic degradation could be observed in the devices that survived 1000 repetitive 10  $\mu$ s surge-current pulses with subsequent 80% rated reverse voltage applied as soon as the current pulse is extinguished. Three suppliers were tested. This result confirms that SiC devices are quite rugged in surge-current conditions.

### 14.1.3 Avalanche Capability

The avalanche capability of a device can be a big advantage for the application and for the self-protection against overvoltages which might be too high. With regard to silicon devices, MOSFETs are typically rated for avalanche in the datasheet. For higher voltage classes above 650 V, IGBTs or silicon pin-diodes are used, where no avalanche capability is rated. At most, some manufacturers allow to drive the device with some milliamper into the breakdown. However, this is not comparable with a hard avalanche rating, where the device is able to withstand more than the nominal current at the breakdown branch.

SiC devices are predestined to allow avalanche clamping also for high voltage classes above 1200 V and up to high currents. First 3.3 kV SiC MOSFETs have already been avalanche rated [26]. Due to the high critical field strength in SiC, the drift-zone

doping  $N_D$  can be adjusted to very high values. In the 1200 V class, base dopings in the range of  $1 \times 10^{16} \text{ cm}^{-3}$  are found. In avalanche, holes  $p_{av}$  and electrons  $n_{av}$  are generated. Holes are flowing to the source, respectively anode, and electrons to the drain, respectively cathode [27]. Within the space-charge region, the generated carriers  $p_{av}$  and  $n_{av}$  can be included in the basic Poisson equation according to their polarity, in a one-dimensional expression as

$$\frac{dE}{dx} = \frac{q}{\epsilon_0 \cdot \epsilon_r} (N_D + p_{av} - n_{av}). \quad (14.7)$$

At the source (anode) side border of the space-charge region, no electrons arrive and the reverse/avalanche current is carried by holes only. The small contribution of diffusion current and recombination center-induced leakage current will be neglected. Then at this position holds

$$p_{av} = \frac{j_R}{q \cdot v_{sat}(p)} \quad (14.8)$$

where  $j_R$  denotes the reverse/avalanche current and  $v_{sat}(p)$  denotes the saturation velocity of holes at the given high electric field. At the drain (cathode) side border, the arriving reverse current is a pure electron current. The density of generated electrons is

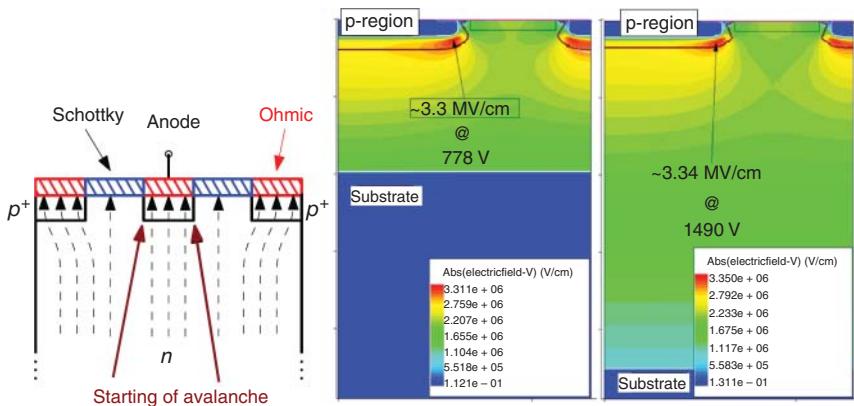
$$n_{av} = \frac{j_R}{q \cdot v_{sat}(n)} \quad (14.9)$$

with  $v_{sat}(n)$  of  $2 \times 10^7 \text{ cm/s}$  for SiC at  $T = 300 \text{ K}$ . This results in a current density of  $32 \text{ kA/cm}^2$  required to have the same amount of electrons as the background doping, which is the condition for possible branches with a negative differential resistance (NDR) [27]. This is about 60 times the rated current density (e.g.  $500 \text{ A/cm}^2$ ). MOSFETs and MPS diodes can be designed to have the avalanche breakdown in the volume. Even with local current crowding due to the NDR effect, such values will hardly be achieved. Therefore, SiC devices show stable  $I/V$  curves at the breakdown branch up to very high current density values. In the MOSFET, the turn-on of the parasitic npn-transistor has to be considered as well. However, due to the short channel length, this requires also extreme high current densities.

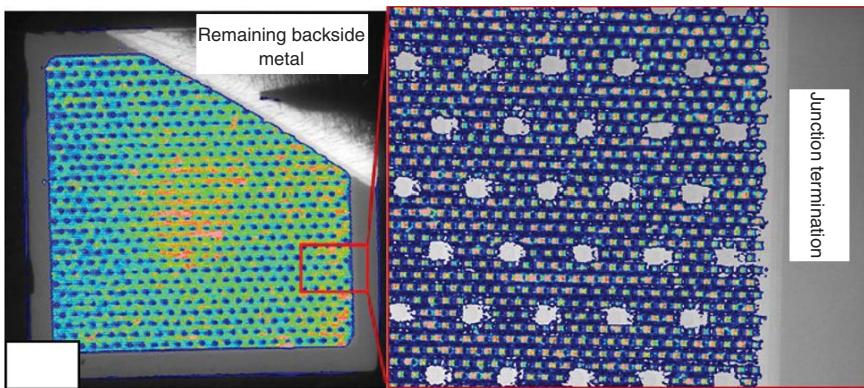
Practically, taking the overall high power dissipation during an avalanche event into account, it was found that for a microsecond time under avalanche, 1200 V SiC MPS diodes could withstand more than 10 times the nominal current without destruction [28].

A second prerequisite for a high avalanche ruggedness, besides a high drift-zone doping, is to have the location of the avalanche breakdown within the active area of a chip. The junction termination is not able to carry high currents. This is fulfilled for most of the SiC devices. Due to the necessity of shielding Schottky junctions or gate oxides with deep p-regions, the initial breakdown point can be typically found in the active area for MPS diodes and SiC MOSFETs, see Figure 14.21.

If the electroluminescence picture of the chip is recorded at the breakdown event (Figure 14.22, [29]), it can be seen that it is not completely uniform over the chip. An anisotropy in the ionization rates leads to a preferred starting region [30, 31]. With



**Figure 14.21** Left: onset of avalanche breakdown in the active area of a SiC MPS diode due to deep p-regions, right: TCAD simulation at breakdown condition with electric field strength, 650 V vs. 1200 V SiC MPS diode. Source: Rupp et al. [29]. © 2014, IEEE.

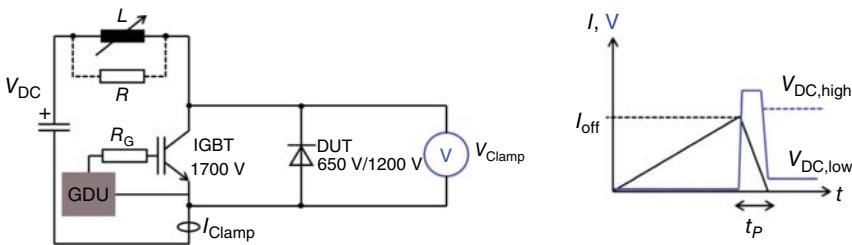


**Figure 14.22** Electroluminescence picture at breakdown of SiC MPS diode. Slightly higher rate of impact ionization at the right side of the chip. Source: Rupp et al. [29]. © 2014, IEEE.

increased temperature during avalanche, the region changes by changed (increased) impact ionization rates and distributes the dissipated energy more homogeneously.

Since diodes cannot be actively switched into an unclamped-inductive switching mode, an auxiliary switch, e.g. a high-voltage IGBT, can be used to trigger the avalanche, see circuit in Figure 14.23.

A typical unclamped-inductive switching event with an 8 A/1200 V SiC MPS diode is shown in Figure 14.24. With the help of the temperature dependence of the breakdown voltage, it is possible to estimate the temperature during a clamping event (Figure 14.24 right), which is in the range of 230 °C. However, this value is just an average value since a homogenous temperature and current distribution are assumed. Compared to silicon power devices, a much lower temperature



**Figure 14.23** Unclamped-inductive switching test circuit for diodes and schematic clamping waveform.

dependency of the breakdown voltage is found (e.g. 1.2 V/K vs. 0.33 V/K in the 1200 V class), which is quite favorable for avalanche condition. The voltage during a clamping event will stay more stable.

Another positive effect of SiC devices is the very low intrinsic carrier density. This makes it possible to block, e.g. a high DC-link voltage after withstanding an unclamped-inductive switching event, see Figure 14.25. The temperature rise during the clamping event is not high enough to raise the intrinsic carrier density  $n_i$  to values where the leakage current level will lead to thermal runaway. Even though the saturation current term  $j_s$  is dependent on  $n_i^2$  as given in the overall leakage current density  $j_r$  of a pn-junction (Schottky contact contribution neglected) [32]:

$$j_r = j_s + j_{SCR} = q \cdot \left( n_i^2 \cdot \frac{D_p}{L_p \cdot N_D} + n_i \cdot \frac{w_{SCR}}{\tau_{SCR}} \right) \quad (14.10)$$

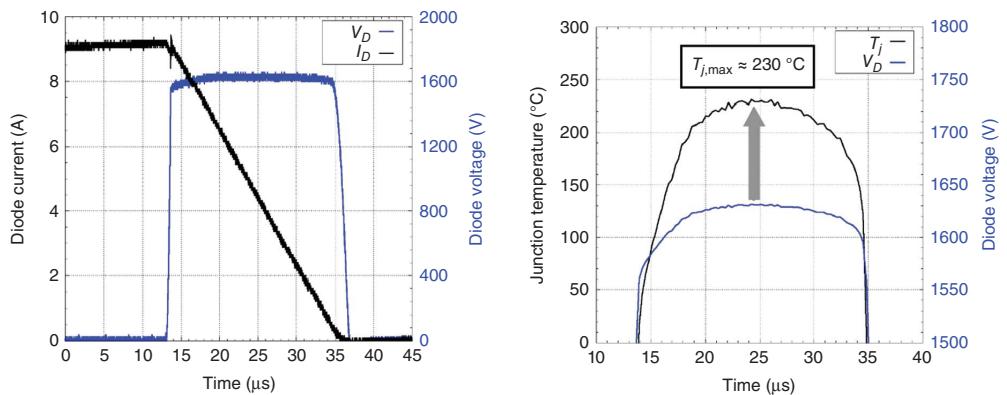
with  $q$  is elementary charge,  $D_p$  is diffusion constant of holes,  $L_p$  is diffusion length of holes,  $N_D$  is base doping,  $w_{SCR}$  is space-charge region,  $\tau_{SCR}$  is generation lifetime in the space charge region.

For silicon devices, unclamped-inductive switching may lead to thermal runaway more early, caused by too high leakage currents afterward.

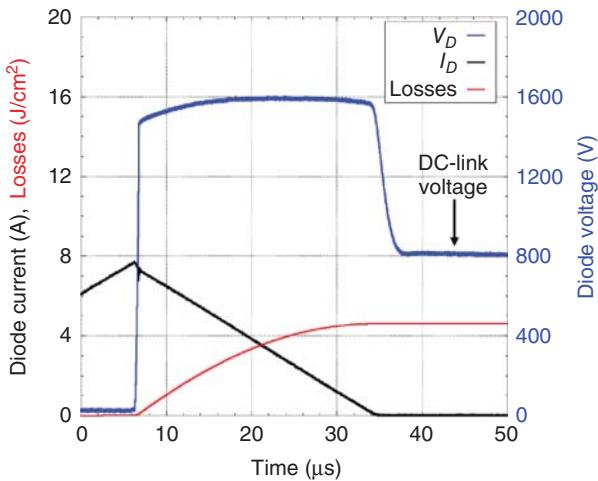
To be able to evaluate the avalanche performance over a wider current and pulse range, a test series with different inductances can be recorded, see Figure 14.26. The failed chips of the study show a burn mark within the active area and not in the junction termination, compare Figure 14.26 right. For small inductance values, the current in avalanche can be very high and trigger further destructive failure modes, e.g. turn-on/latch-up of the parasitic npn-transistor in the case of MOSFET devices [33]. The energy during such a pulse can be calculated with

$$E_{AV} = \frac{1}{2} \cdot L \cdot I_{off}^2 \cdot \frac{V_{Clamp}}{V_{Clamp} - V_{DC}}. \quad (14.11)$$

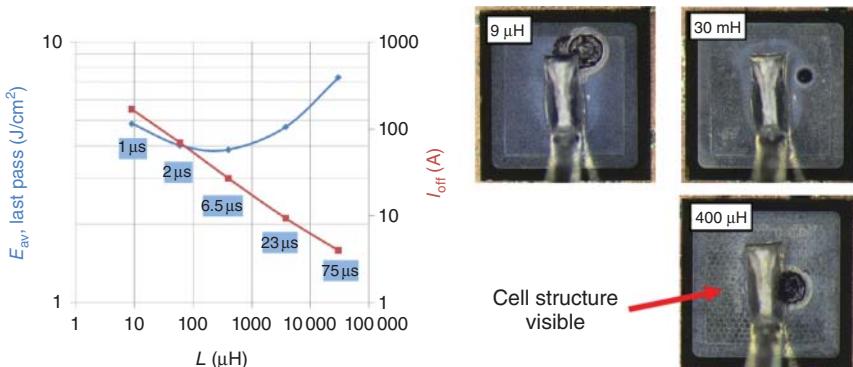
For MPS diodes, the maximum energy during clamping was found to be reduced at medium inductances [28]. At these clamping times and currents, following the  $Z_{th}$  characteristic, the frontside metal is stressed most which can also be seen in the failure pattern for 400 µs. For even higher inductances and lower currents, deeper



**Figure 14.24** Left: lastpass unclamped-inductive switching pulse of an 8 A/1200 V SiC MPS diode with  $L = 3.8 \text{ mH}$ , Right: temperature estimation with the help of temperature-dependent breakdown voltage  $0.33 \text{ V/K}$  measured before. Source: Basler et al. [28].



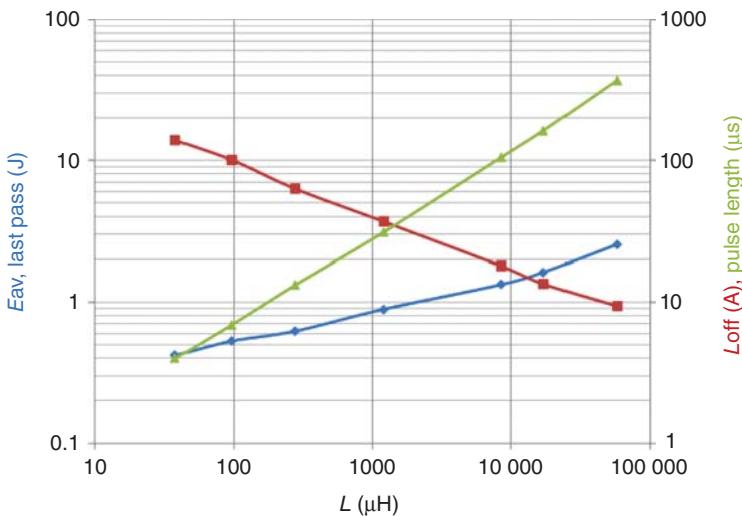
**Figure 14.25** Unclamped-inductive switching event of an 8 A/1200 V SiC MPS diode with blocking the DC-link voltage of 800 V after the clamping event,  $L = 3 \text{ mH}$ . Source: Basler et al. [28].



**Figure 14.26** Left: last-pass energy and currents of an 8 A/1200 V SiC MPS diode under unclamped-inductive switching. Right: different failure patterns. Source: Basler et al. [28].

layers of the complete assembly are used (SiC substrate, lead frame) and the energy is increased again.

A similar  $E = f(L)$  plot for a  $40 \text{ m}\Omega$  SiC MOSFET is shown in Figure 14.27 and single waveforms in Figure 14.28. This device is able to resist clamping currents above 100 A without destruction. In principle, the SiC MOSFET shows a comparable avalanche robustness as the MPS diodes. This holds for planar and trench concepts, shown, e.g. in [34]. A latch-up for a SiC MOSFET is more unlikely since the built-in voltage of the  $n^+$ -source/p-body junction is very high ( $\approx 2.7 \text{ V}$  at  $25^\circ\text{C}$ ) compared to silicon and needs to be exceeded during an unclamped-inductive switching



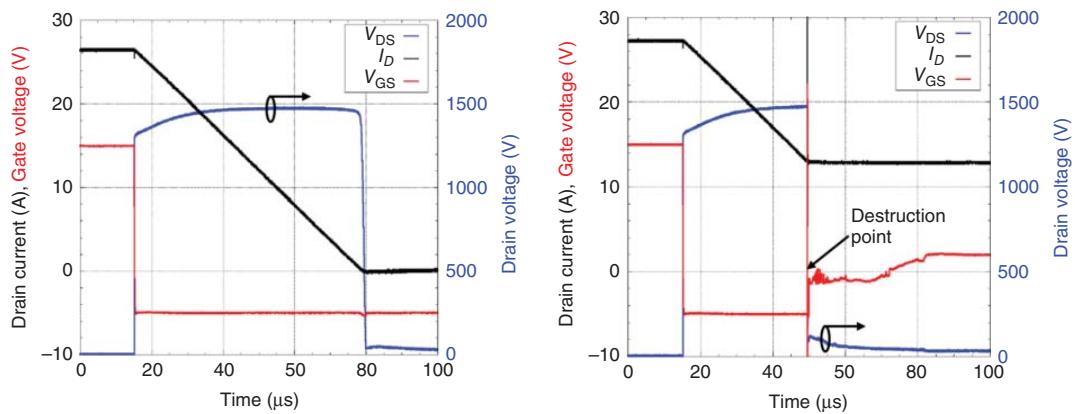
**Figure 14.27** Unclamped-inductive switching with last-pass energy of a 40 mΩ/1200 V SiC MOSFET.

event. After performing a high-energy clamping event, the leakage currents should be checked, especially the gate-source leakage path of an SiC MOSFET.

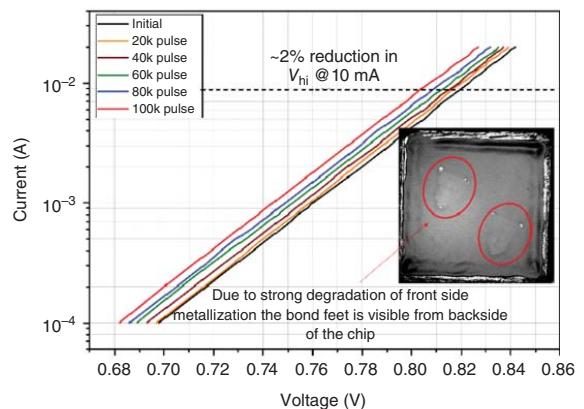
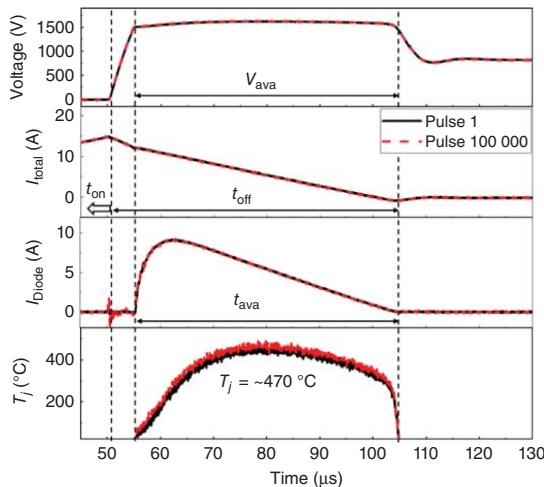
Since SiC devices have a proven high single-event avalanche capability, a next step would be to also define a repetitive/periodic avalanche energy. First studies [28, 35, 36] already show a high performance. For SiC MPS diodes, it was proven that the high-energy repetitive avalanche is very stable, showing no bipolar degradation. Only thermomechanical fails, such as modifications of the bond-wire connection or frontside metal were observed, see Figure 14.29 [36], caused by the strong temperature swing, similar to a high-current short-pulse power cycling. Due to the modifications, the Schottky barrier height or threshold voltage  $V_{GS,TH}$  may change as well, as shown in Figure 14.29 right.

Still, more studies have to be conducted to also verify the gate oxide and general parameter stability of SiC MOSFETs under a repetitive avalanche condition. For silicon low-voltage MOSFETs, it was shown that especially shielded-gate technologies are susceptible to parameter change. The main reason is the change of the charge characteristic at the trench oxide due to, e.g. hot carriers (holes). As a consequence, the breakdown voltage or gate-threshold voltage may change [37]. Since the shielding structures of SiC MOSFETs are setting the point of the avalanche breakdown deeper into the device and keep it away from the gate oxides, it is expected that these types of MOSFETs behave more stable. First results already confirm this [35]. Furthermore, the avalanche current does not directly flow at the channel region.

However, material defects (e.g. crystal defects) have to be minimized to achieve a high avalanche robustness in general [38]. Wafer-level unclamped-inductive switching tests may be helpful as shown in [39].



**Figure 14.28** Unclamped-inductive switching event of 40 mΩ/1200 V SiC MOSFET,  $L = 3.5$  mH, Left: last-pass event, Right: destruction event.



**Figure 14.29** Left: Repetitive unclamped-inductive switching event of 1200 V SiC MPS diode,  $L = 3.1 \text{ mH}$ ,  $V_{\text{DC}} = 820 \text{ V}$ ,  $t_{\text{interval}} = 1 \text{ second}$ ,  $T_{\text{case}} = 25^\circ\text{C}$ , Right: Degradation of the Schottky barrier and degradation pattern (modification of bond wire connection – red circles) of chip after the test is shown from the back side. Source: Palanisamy et al. [36].

## 14.2 Cosmic-Ray Stability

Cosmic-ray stability is an important reliability criterion. SiC is discussed to be “radiation-hard” in applications for semiconductor detectors working in harsh environments like nuclear, space and particle physics [40]. For SiC, where the carrier concentration is very low, the change of the leakage current with radiation dose was observed to be minimal. Sometimes, statements such as “radiation hard” are made for SiC power devices. However, this cannot be applied for the radiation tolerance of power devices against cosmic ray effects. These effects are quite different. The most important cosmic ray failure mechanism for power devices is the “single event burnout” (SEB) [41] or also named “single event effect” (SEE) [42] which is a complete different phenomenon. In recent work, SiC devices have been evaluated to show high total ionizing dose (TID) tolerance, but low SEE tolerance [42].

Cosmic ray faults not only occur in space but also on the earth surface. High-energy primary cosmic ray particles from deep space collide with atmospheric particles and generate a variety of secondary high-energy particles. Neutrons are most relevant for generating device damage on the earth surface. The neutron flux density is in the range of  $20 \text{ cm}^{-2}/\text{h}$  at sea level [43] and increases strongly with altitude. At 12.2 km (40 000 ft, the upper flight level of civil airplanes), there is a neutron flux density of  $7200 \text{ cm}^{-2}/\text{h}$  for a latitude of  $45^\circ$  [44]. The maximum neutron flux density is found at an altitude of 18 km. Further relevant parts are high-energy protons, which contribute to the total cosmic radiation with 20% to 30% at sea level and 50% at 12.2 km altitude. Creation and absorption compete in the showers in the higher atmosphere. Regarding space application, the majority of energetic particle flux at low earth orbit consists of proton flux [45]. Protons as charged particles can be shielded; however, aluminum shielding of 2.5 mm thickness is no proper protection against proton flux, since a large fraction of proton flux exhibits a high energy above the 100 MeV range [45].

To evaluate cosmic ray failure rates, tests with a large number of devices at high DC voltage were carried out. First, tests at high altitudes were arranged, since the terrestrial cosmic particle flux increases with altitude above sea level. In parallel, tests with particle accelerators were carried out and neutron sources emitting neutron beams with atmospheric-like spectrum are used as well. Such sources can be found at the Research Center for Nuclear Physics RCNP (Osaka University, Japan), or at the Los Alamos Neutron Science Center (LANSCE, United States). Nowadays, cosmic ray stability is mostly evaluated by using particle accelerators or neutron sources, since this delivers relevant results in a short amount of time.

The cosmic ray failure (SEB, SEE) occurs in a device while it is exposed to a high voltage and consequently a high internal electric field strength. The impact of particles colliding with a lattice atom creates, at high electric fields, an electron–hole plasma. Impact ionization is enhancing the effect, in detail different for Si and SiC.

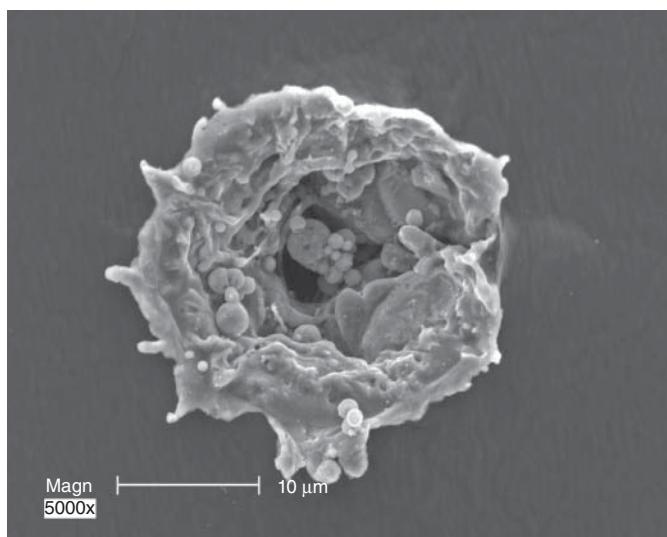
For high-voltage Si devices, the space charge is wide, e.g. in the range of  $100 \mu\text{m}$  for a 1200 V device. After impact and resulting plasma, an extreme high gradient density of charge density emerges at the borders between the plasma and the space

charge, leading to very high and steep field peaks. If the electric field exceeds a certain threshold value, impact ionization creates enhanced carrier density. One field peak runs to the anode, the other to the cathode. A so-called “streamer” is formed in analogy to a discharge in a gas. The device is flooded locally with free carriers within some hundred picoseconds; hence, a local current tube occurs. Still, the time in the range of 200 ps [46] is too short for a temperature increase that would lead to destruction. However, arriving at the pn- and nn<sup>+</sup> junction, the streamer shortens both sides of the device and is, at the first moment, combined with an avalanche generation at both sides. For an abrupt nn<sup>+</sup> junction, the cathode-side injection delivers the main part of the generated current. It is assumed that this or other type regenerative mechanism is finally responsible for the destruction of the device. Details are described in [47].

For SiC, the width of the space charge is 1 order of magnitude lower. The initially generated plasma already shortens the space charge [48].

The failure pattern shows, if the device is protected by a fuse, a narrow pinhole in Si as well as in SiC. An example for a SiC MPS diode is shown in Figure 14.30 [49]. In simulations of cosmic ray failures in SiC MPS diodes by Shoji, similar effects like in Si diodes were found [49]. The SEB current produced by impact ionization at the nn<sup>+</sup> interface is common to both Si and SiC power diodes. It corresponds to the destruction caused by an Egawa-type field with a field peak on both sides [50]. The effect is denoted as dynamic avalanche of the third degree in [47]. In [49], the same effect is denominated as “local second breakdown.”

Experiments were carried out to compare SiC devices with Si devices. For 1200 V Si IGBTs, a sharp increase of cosmic ray failures is found above a threshold voltage of 70% of  $V_{\text{rated}}$  [51], in accordance with [52]. At 85% of  $V_{\text{rated}}$  for 1200 V SiC MOSFETs, first failures were detected [53]. However, 1200 V Si diodes with a threshold above



**Figure 14.30** Cosmic-ray failure of a SiC MPS diode. Source: Figure from Shoji et al. [49].

100% of the rated blocking voltage are found [51]. The specific design is of strong influence.

A detailed comparison is reported in [54]. The devices are compared not only for the rated voltage but also for the measured breakdown voltage. This is a reasonable method since many SiC devices are rated for lower voltage than the breakdown voltage given by the volume of the device. The rated voltage compared to the measured breakdown voltage  $V_{BD}$  for the investigated 1200 V Si IGBTs was found to be 88% to 89%, for the 1200 V SiC MOSFET it is 73%. For 1700 V, the Si IGBT used 79% of the breakdown voltage as rated voltage, while the SiC MOSFET used 64%. This shows that the high critical field strength of SiC is only partially exploited in the investigated SiC designs. The results analyzed in dependence of  $V_{DC}/V_{BD}$ , meaning normalized to applied DC voltage  $V_{DC}$  compared to the measured breakdown voltage  $V_{BD}$ , are as follows: for 1200 V devices, a small advantage for the SiC MOSFET was found, see Figure 14.31a. For 1700 V devices, the failure rate becomes significant at similar  $V_{DC}/V_{BD}$  (Figure 14.31b).

For Si, the different devices were fitted by [55] with the empirical equation

$$r = C_3 \cdot e^{\frac{C_2}{C_1 - V_{bat}}} \quad (14.12)$$

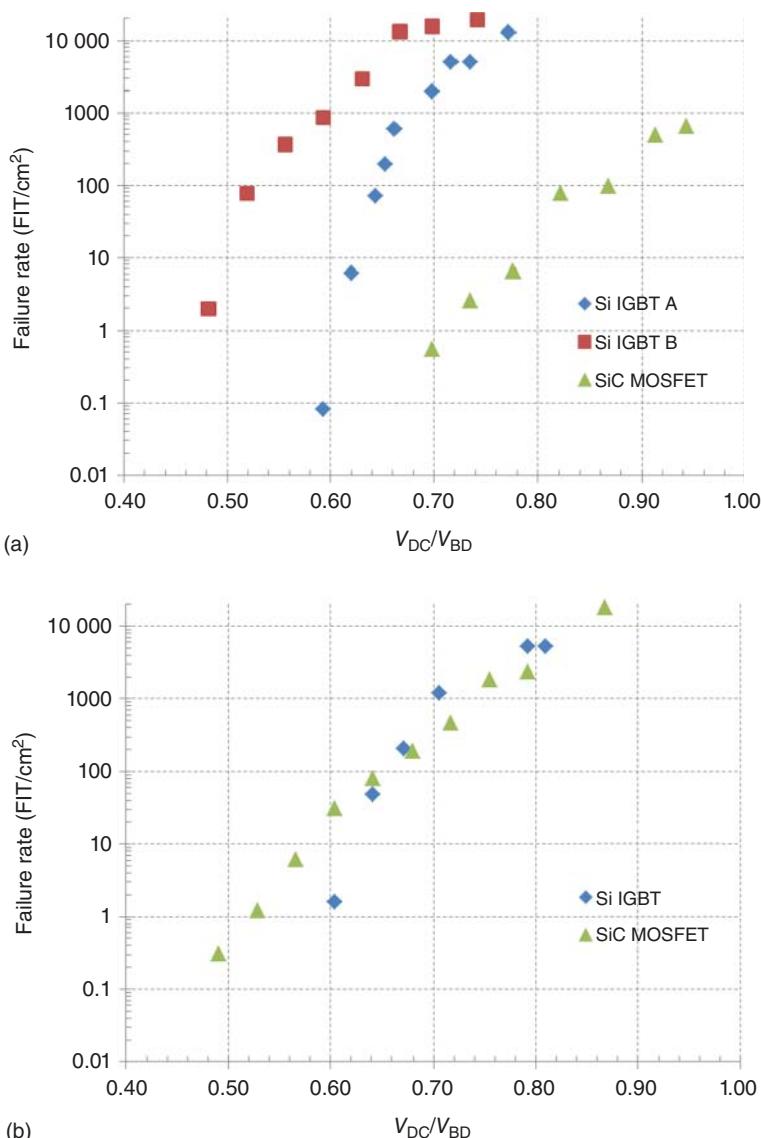
where  $C_1$ ,  $C_2$ , and  $C_3$  are empirical constants. The function has a pole at the voltage  $C_1$  in Eq. (14.12). Below  $C_1$  the model is not valid, and the failure rate is zero. All recent experiments with Si [49, 51, 52] can be well described with a function of type Eq.(14.12). For SiC, the pole  $C_1$  is not visible in the same way. If given, it occurs at lower  $V_{DC}/V_{BD}$ . Up to now, the models do not explain this difference, and further research is needed. However, the effect has to be considered for SiC in aircraft applications where the cosmic ray particle flux is several decades higher.

The physics of cosmic ray failures seems to be very similar for Si and SiC. However, with the perspective of increased crystal quality in the future, for SiC the full potential of the material will also be used. More data for SiC and for Si are of high interest. For the same rated current, there is a lower device area for SiC. Therefore, it may remain a small advantage for SiC at terrestrial levels.

### 14.3 Thermomechanical Reliability

The thermomechanical reliability of a device is determined by its packaging technology. The challenges for SiC packages are significantly higher than that for Si. This is due to these factors:

- The capability of fast switching requires a very low internal inductivity; therefore, the package has to be compact and internal leads/bond-wire loops have to be short. Additionally, a very symmetrical arrangement of internal connectors at paralleling of devices is required. This holds for the main terminals as well as for the gate wiring.
- For the same current, SiC devices are smaller. This means a higher current density, which is combined with a higher power-loss density.



**Figure 14.31** Comparison of Cosmic ray failure rates for Si IGBTs and SiC MOSFETs normalized to applied DC voltage  $V_{DC}$  compared to the measured breakdown voltage  $V_{BD}$ . (a) 1200 V rated devices and (b) 1700 V rated devices. Source: Figures according to data from Felgemacher et al. [54].

**Table 14.1** Thermomechanical material data.

	<b>Si</b>	<b>4H-SiC</b>	<b>GaN</b>
Thermal conductivity (W/mmK)	0.13	0.37	0.13 <sup>a)</sup>
Specific heat [J/(kg*K)]	700	690	490
CTE (ppm/K)	2.6	4.3	3.17
Young's modulus $E$ (GPa)	162	501	181

a) on Si substrate.

- SiC is a very stiff material exposing every interface to higher stress under conditions of mismatch of coefficients of thermal expansion and temperature swings.

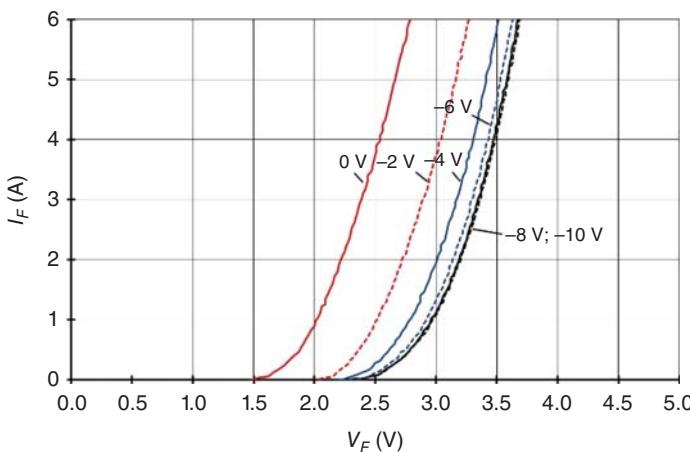
A comparison of the thermomechanical characteristics is given in Table 14.1.

In SiC, both the thermal conductivity and Young's modulus are in fact anisotropic, but this fact is usually neglected. The thermal conductivity of SiC is about three times higher. However, also the Young's modulus describing mechanical stiffness is more than three times larger than it is for Si. Thermal-mechanical simulations in [56] of a chip soldered on a DCB substrate showed that the mechanical energy, determined by the stress-strain integral  $\Delta W$ , is more than three times higher at the corner of a SiC device than for a Si device for the same geometry and the same temperature swing. Since  $\Delta W$  represents the force driving the initiation and propagation of a crack in a solder layer, the crack propagation rate in SiC is expected to be faster by the same factor.

### 14.3.1 Temperature-sensitive Electrical Parameters

The power-cycling test is the main test to determine the lifetime of a device when exposed to load cycles in the application. The power chips are actively heated by the losses generated in the power devices themselves in a power-cycling test. It is therefore necessary to measure the temperature. Usually, the devices are packaged. The surface temperature of the housing will deviate strongly from the temperature of the semiconductor die, especially for short electric load pulses. Therefore, a temperature-sensitive electrical parameter (TSEP) is necessary. For Si devices, the established method is the determination of the junction voltage of a pn-junction  $V_j(T)$  which decreases strongly with increasing temperature due to the increasing intrinsic-carrier density in semiconductors [47]. The pn-junction of a diode or the base-emitter junction of a bipolar transistor is used [57]. This method has been established since the beginning of power device development. The so-called determined temperature is called virtual junction temperature  $T_{vj}$ . The measurement has to be executed in the range of 1/1000 rated current. The thermal resistance in data sheets of European manufacturers is initially determined with the  $V_j(T)$  method. It is reinvestigated in detail for Si IGBTs in [58].

Note that in fact a device has a significant vertical and lateral temperature profile and every location has a different temperature, especially for large chips with an area



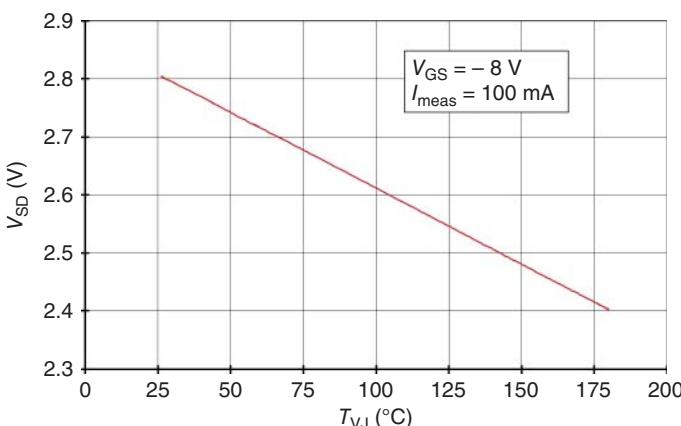
**Figure 14.32** Forward characteristics of the inverse diode of the SiC MOSFET IMW120R045M1 (Infineon) for different gate voltages,  $T = 145^\circ\text{C}$ .

$>0.5 \text{ cm}^2$ .  $T_{vj}$  determined with the  $V_j(T)$  method was found to be close to the area average calculated from the measurements with infrared camera at the surface of an opened device.

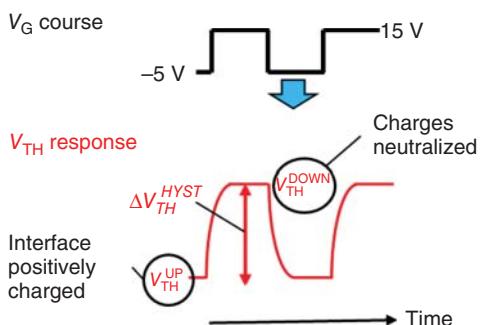
For the SiC MOSFET, the voltage drop of the inverse diode  $V_{SD}(T)$  at a low measurement current can be used as TSEP, which is recommended in [59]. However, the gate-channel of the SiC-MOSFET is not completely off at  $V_{GS} = 0 \text{ V}$  and a voltage in conduction direction of the inverse diode The voltage drop up to the built-in voltage of the pn-junction opens the channel partially and enables a part of the current to pass the slightly inverted channel. The current–voltage characteristic of the inverse diode depending on the gate voltage is shown in Figure 14.32. It indicates that only for the gate voltage of  $-6 \text{ V}$  and lower the characteristics of the diode do not change anymore and the junction voltage  $V_j(T)$  can be measured.

Since the current through the MOS channel will depend on the threshold voltage, it has to be ensured that the channel is turned off even if there is a drift of  $V_{GS,TH}$ . Therefore, a negative gate voltage below  $-6 \text{ V}$  is recommended. Figure 14.33 shows  $V_j(T)$  for a SiC MOSFET measured with  $V_{GS} = -8 \text{ V}$ .

There are also other possible temperature-sensitive electrical parameters. The gate threshold voltage  $V_{GS,TH}$  is strongly temperature dependent, but it is affected by a trapping phenomenon: after a power cycle with positive  $V_{GS}$  over several seconds, it was found that SiC MOSFETs might need up to seconds to recover to the initial  $V_{GS,TH}$  value. Point defect states are negatively charged during a positive  $V_{GS}$ , neutralized at the inversion to a negative  $V_{GS}$ . Turning on from a negative  $V_{GS}$  will lead to the measurement value  $V_{TH,up}$ , after turn-off from a positive  $V_{GS}$ , the value  $V_{TH,down}$  will occur [60]. This  $V_{GS,TH}$  hysteresis  $\Delta V_{TH,HYST}$  displayed in Figure 14.34 is reversible as shown in [61].  $V_{GS,TH}$  measurements have to be performed in a predefined procedure (e.g.  $-5 \text{ V} \rightarrow +15 \text{ V}$ , comparable is only  $V_{TH,UP}$  with  $V_{TH,UP}$  or  $V_{TH,DOWN}$  with  $V_{TH,DOWN}$ ).



**Figure 14.33** Calibration function  $V_j(T)$  for the 1200 V SiC MOSFET IMW120R045M1 (Infineon) at  $V_{GS} = -8$  V.



**Figure 14.34** Threshold voltage hysteresis depending on  $V_{GS}$  before measurement.

However, there is also an irreversible  $\Delta V_{GS,TH,BTI}$  drift which is called bias temperature instability – BTI. Observed is a positive drift PBTI and negative drift NBTI. It is shown in Figure 14.35.

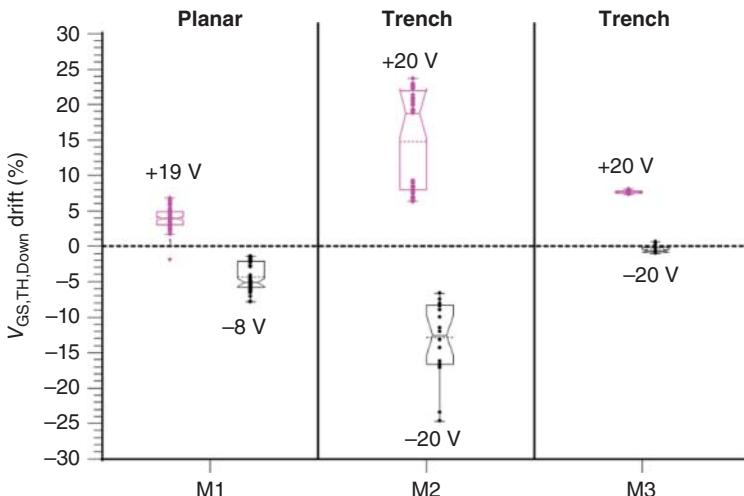
This drift remains in the range of +25% resp. -25% even at long times and it differs from manufacturer to manufacturer. It is predictable for application. However, because of this effect, the  $V_{GS,TH}$  is not suitable as TSEP.

During power cycling,  $R_{DS,ON}$  will be affected by a bond-wire lift-off and the by gate-threshold voltage  $V_{GS,TH}$  drift.  $R_{DS,ON}$  is already included in the  $V_{DS}$  determination. The on-state resistance  $R_{DS,ON}(T)$  is not suitable since it will increase at bond wire failures, and the separation of degradation effects will be complex. Furthermore,  $V_{GS} - V_{GS,TH}$ , which defines  $R_{DS,ON}$  according to Eqs. (14.13) and (14.3), is influenced by a gate-threshold voltage  $V_{GS,TH}$  drift.

The measured  $R_{DS,ON}$  consists of

$$R_{DS,ON} = R_{\text{pack}} + R_{\text{epi}} + R_{\text{CH}} + R_A + R^* \quad (14.13)$$

where  $R_{\text{pack}}$  is the resistance due to bond wires, metallization, etc.,  $R_{\text{epi}}$  is the resistance of the base layer,  $R_{\text{CH}}$  is the channel resistance,  $R_A$  is the resistance of the



**Figure 14.35** Bias temperature instability test of different manufacturers. 500 hours at 150 °C, 200 pieces per type.  $V_{GS,TH}$  readout at  $V_{TH,DOWN}$  point. Source: Aichinger et al. [61]. © 2018 Elsevier.

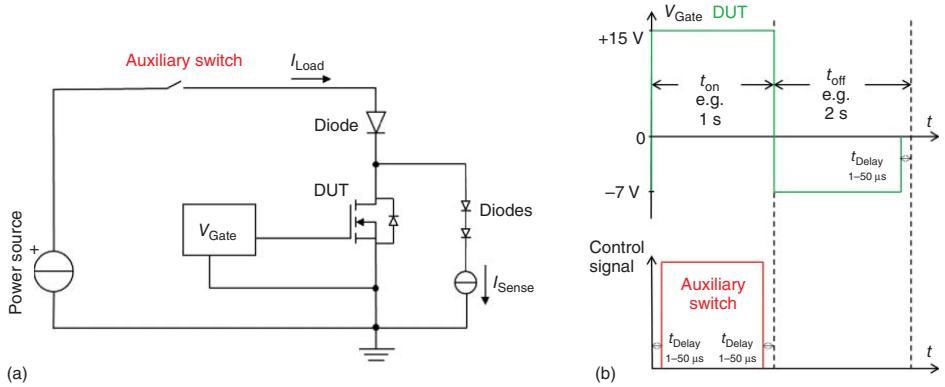
accumulation layer, and  $R^*$  summarizes the other components, e.g. the substrate. If there is a  $R_{DS,ON}$  increase, it might be due to  $R_{pack}$  which is a typical power-cycling ageing effect, or due to an  $R_{epi}$  increase caused by stacking faults [62] or due to a  $V_{GS,TH}$  increase which modifies  $R_{CH}$ , see Eq. (14.3) [47].

Increased  $V_{GS,TH}$  will lead to a higher  $R_{DS,ON}$  and thus also to a higher power loss. This in turn actively influences the temperature swing and thus the lifetime of the packaging technology. Since different effects contribute to it,  $R_{DS,ON}$  is unsuited as TSEP. An investigation on parameters showing a drift, which makes them unsuitable as a reliable temperature indicator, is given in [63].

### 14.3.2 Execution of Power-cycling Tests

During power-cycling tests, the device under test is mounted on a heat sink as in a real application. A load current is conducted by the power chips, and the power losses heat up the chip. During each cycle, considerable temperature gradients are generated inside the module. While in a temperature cycling test, all layers in the test object have the same temperature; in a power-cycling test, different layers will have a different temperature and a different thermal expansion. Therefore, different failure mechanisms can be triggered.

Figure 14.36 shows the schematic and the control pattern for SiC MOSFETs [59]. The power losses are created in the forward mode which has a positive temperature coefficient,  $R_{DS,ON}$  is increasing with  $T$ , while the body diode has a negative temperature coefficient.  $V_j(T)$  is measured in reverse diode mode. Figure 14.36a shows the setup for one device under test (DUT), there may be several devices arranged in a series connection. In series with the current source for  $I_{sense}$  are some diodes for protection, the amount of diodes must be sufficient so that their sum of forward



**Figure 14.36** Power-cycling setup for SiC MOSFET with  $V_{SD}$ -method (a) schematic (b) control pattern. Source: Based on Herold et al. [59].

knee voltages is larger than the voltage drop across the DUT. Figure 14.36b shows the course of the control signals. First,  $V_{GS}$  is set on with the specified voltage  $V_{GS,use}$  of the manufacturer. Next, the auxiliary switch is closed. Now the load current flows. The auxiliary switch is turned off. After a short delay, 1–50 µs, a negative voltage is applied, e.g. –7 V for the temperature measurement via  $V_j(T)$  of the body diode of the MOSFET.

Meanwhile, the setup in Figure 14.36 has been used by different groups, e.g. in [64] and [65].

For SiC Schottky and MPS diodes, the junction voltage of the Schottky junction can be used as TSEP. The setup is then identical to the setup for IGBTs and Si diodes. It is recommended to control the junction voltage after the test, since a drift at the barrier at high repetitive load is not excluded.

### 14.3.3 Evaluation of SiC Power-cycling Tests

For measuring  $V_j(T)$ , there is again a delay time  $t_d$  between turning off of the load current and the moment of measurement. The cooling down during  $t_d$  is higher for SiC devices as compared to Si devices. For SiC power modules, it was found in the range of 4–5 K, even up to 6 K for a  $t_d$  of 1 ms, due to the higher power densities in SiC [66]. This is significant now, especially if packages with SiC and Si are compared. A correction of this measurement error is possible with the square-root- $t$  method [67].

$$T_{vj(t)} - T_{vj(0)} = \frac{2 \cdot P_v}{(\rho \cdot \pi \cdot \lambda \cdot c_{\text{spec}})^{\frac{1}{2}} \cdot A} \cdot t^{\frac{1}{2}} \quad (14.14)$$

Equation (14.14) holds under boundary condition of a planar heat source at the surface of a semi-infinitely thick cylinder assuming a one-dimensional heat flow. Since the heat source in SiC devices is in a narrow region close to the device surface, Eq. (14.14) is found to hold for SiC devices with good accuracy [66]. It has to be mentioned that for Si IGBTs the use of Eq. (14.14) leads to a significant error, since the heat generation is across the whole thickness of the device.

For an exact evaluation of power cycling with SiC devices, the used delay time  $t_d$  between load current and  $T_{vj}$  measurement has to be added in documentation, if the measured values have been corrected with the square-root- $t$  method or with a  $Z_{\text{TH}}$ -model or another method which is applicable. And, to be fair comparing Si and SiC, the higher  $t_d$ -caused error has to be considered as well.

To be compliant with the European standard AQG 324, two parameters have to be supervised and monitored in the test documentation:  $V_{DS}$  determined at  $T_{\text{low}}$  to indicate aging of electrical interconnections, and the virtual junction temperature, respectively, thermal resistance indicating the integrity of the thermal path.

However,  $V_{DS}$  in the MOSFET is given by  $R_{DS,ON} * I_D$ , and it is important to take care of some SiC-related semiconductor effects according to Eqs. (14.13) and (14.3):

- The term  $R_{epi}$  can increase due to bipolar degradation.
- The term  $R_{CH}$  can be modified by  $V_{TH}$  drift. In power-cycling tests, on-time  $t_{on}$  and off-time  $t_{off}$  are in the range of one to some seconds, and positive  $V_{GS}$  resp. negative  $V_{GS}$  is applied at the device accordingly. If there is a long-term drift, a  $V_{GS,TH}$  increase will lead to a  $V_{DS}$  cold increase, and a  $V_{GS,TH}$  decrease will lead to a  $V_{DS}$  cold decrease. Therefore,  $V_{GS,TH}$  is to be controlled at intermediate measurements and the resulting effect to be considered in the evaluation.

Finally, an effect of bipolar degradation on the  $T_{vj}$  determination can occur for special devices. For  $T_{vj}$  measurements, the body diode is exposed to a negative  $V_{GS}$ . A measurement current  $I_{sense}$  of 100 mA for a typical small size SiC chip in a TO-housing is already in the range of 1 A/cm<sup>2</sup>. In [68], an increase of the junction voltage  $V_j$  at low temperature was found for one of several high-voltage (3.3 kV) SiC devices. This means that  $T_{vjmin}$  will be measured as low. However, this is the only test having noticed this up to now. High-voltage SiC devices are more sensitive to bipolar degradation [62]. Just a small amount of tests of high-voltage SiC MOSFETs are reported up to now. Nevertheless, it is recommended to control the inverse diode characteristics before and after test.  $V_{SD}$  of the inverse diode should be controlled at  $V_{GS} = -8$  V to  $-10$  V and at rated current to consider this effect in the evaluation.

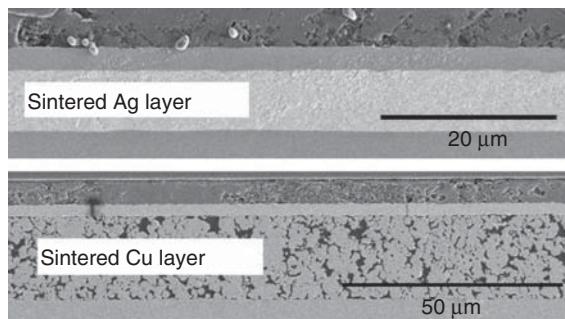
## 14.4 New Power-module Technologies with Sufficient Reliability

When using established power-module technology as soldering and wire bonding, the power-cycling capability is reduced to approximately  $1/3$ , if Si devices are replaced by SiC devices [69]. This is explained by the higher Young's modulus of SiC, see Table 14.1, and it is confirmed by other groups, e.g. [65, 70]. Improved technologies are necessary to achieve high power-cycling lifetime with SiC devices.

### 14.4.1 Improved Die-attach Technologies

The Ag-sinter technology to replace solder layers is executed by densification of Ag powder layers with micro- or nanoparticles. It forms a porous rigid interconnection layer of high reliability [71]. The properties of this interconnection layer are superior to solder interfaces in all parameters. The specific thermal conductivity of the sinter layer can be as high as 220 Wm<sup>-1</sup>/K and is therefore almost a factor of 4 times higher than that of a conventional SnAg3.5 solder layer. Together with a characteristic layer thickness of <20 µm, the sinter technology exhibits a reduced thermal resistance between the chip and the substrate compared to conventional solder layers of typically >50 µm thickness. The electrical conductivity is also improved due to the low specific electrical resistance of silver [47]. For Si applications, it was shown that this is increasing the lifetime by a factor of 20 and more [72]. In [64], this technology was applied to a power module with SiC MOSFETs, where on the top side

**Figure 14.37** Sintered Ag-layer and sintered Cu-layer. Source: Figure from Konno et al. [73].



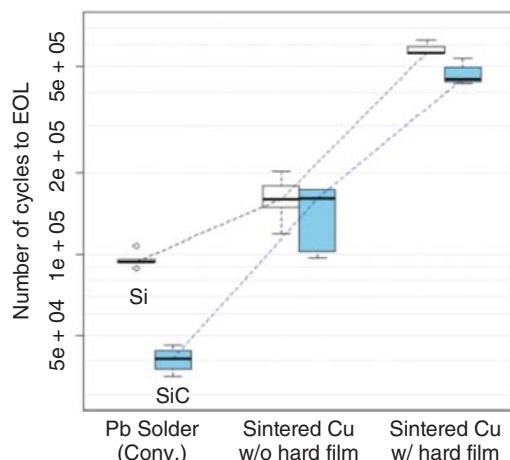
125  $\mu\text{m}$  aluminum bond wires were applied. An excellent power-cycling capability was achieved.

Instead of Ag-sintering, Cu-sintering is also applied. Cu has a reduced CTE, an increased yield stress, and increased melting point, compared to Ag. It is more difficult to prepare a low-porosity interconnection layer; a comparison is shown in Figure 14.37 [73].

From Figure 14.37, it can be seen that the layers are different, the sintered Ag-layer of the test sample was without visible pores, and the sintered Cu-layer includes pores (12%). Nevertheless, the Cu-layer achieved a more than 4 times larger temperature cycling capability ( $-40$  to  $200^\circ\text{C}$ ) than Ag. The Cu-sintered layer including pores showed a higher durability than a fine Ag-sintered layer. The higher yield strength and lower CTE of Cu make these results plausible.

Cu-sintering is used in [65, 70]. Results are shown in Figure 14.38. Si is compared with SiC for different technologies. For soldering, the reduced power-cycling capability of SiC is confirmed. For Cu-sintering, the lifetime is significantly increased and Si and SiC become comparable. The lifetime limit is now the bond wiring on the top side by applying a hard film over the bond wires it was further improved. Both Ag- and Cu-sintering improve the power-cycling capability significantly. For both technologies it was shown that the sinter layer is no longer a lifetime limiting factor.

**Figure 14.38** Progress in power-cycling capability, comparison of Si and SiC. Test conditions  $T_{j,\max} = 175^\circ\text{C}$ ,  $\Delta T = 125\text{ K}$ ,  $t_{on}$  1–2 seconds. Source: Figure from Yasui et al. [65]. © 2018, IEEE.



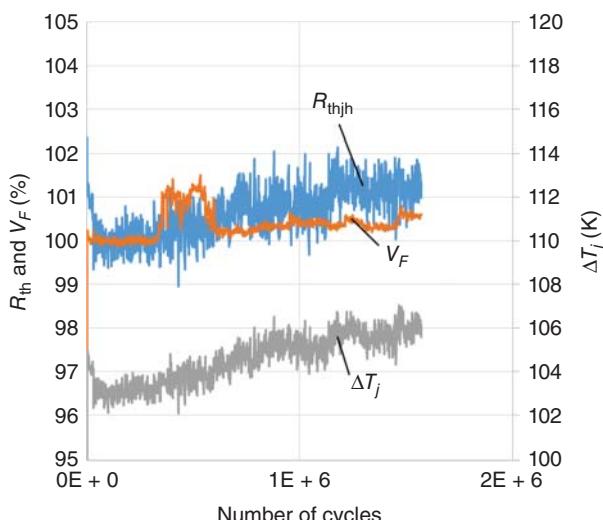
### 14.4.2 Improved Top-Side Interconnections

In the Semikron DPD (direct pressed die) technology, both the bottom-side and the top-side interconnections are executed with silver sintering. On the top side, there is a flexible foil. This allows a narrow distance between the + and – path of the current in a module, and the parasitic inductance can be set very low. In [74], a module inductance of 1.4 nH was achieved. For a complete system including the DC link, the inductance is about 4.5 nH. This compact integration technology facilitates the use of the fast switching capability of SiC devices. The power cycling capability shows a clear progress.

Infineon has introduced Cu bond wires on a top-side Cu metallization of the device. Together with Ag-sintering, it is named “XT technology.” Results of this technology are shown in Figure 14.39.

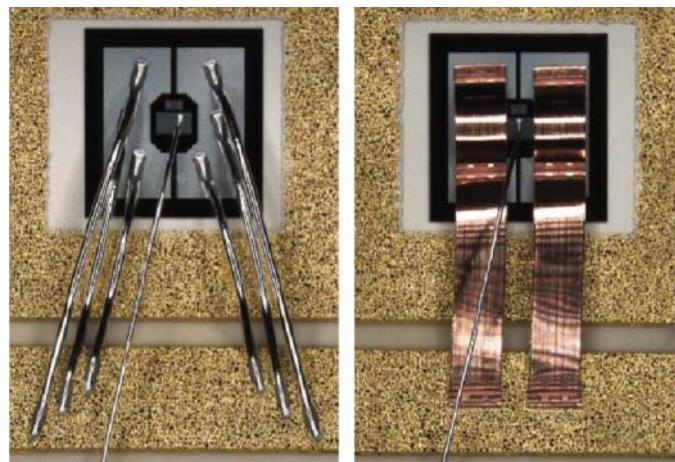
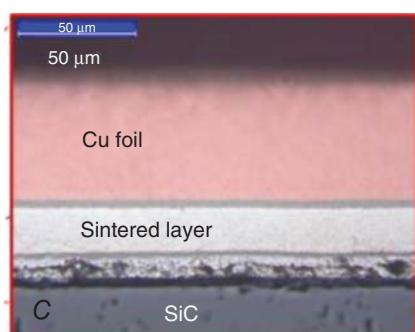
The power-cycling test in Figure 14.39 was finished because of the test time which took too long. No signs of end of life are visible. The  $V_F$  increase remained smaller than 1%.

Cu bond wires require higher ultrasonic power and pressure at the wire-bond process; they cannot be executed on a usual Al metallization layer. To allow Cu wire bonding on devices with Al metallization, a technology to plate the Al with a noble metal and silver sintering to a thin Cu foil was introduced [75], which is named “Danfoss bond buffer (DBB)” or “die top system (DTS)”. Cu bond wires are applied on the Cu foil. The technology leads to a significant power-cycling capability. As failure mechanism, cracks in the to-side Al metallization were identified, as shown in Figure 14.40.

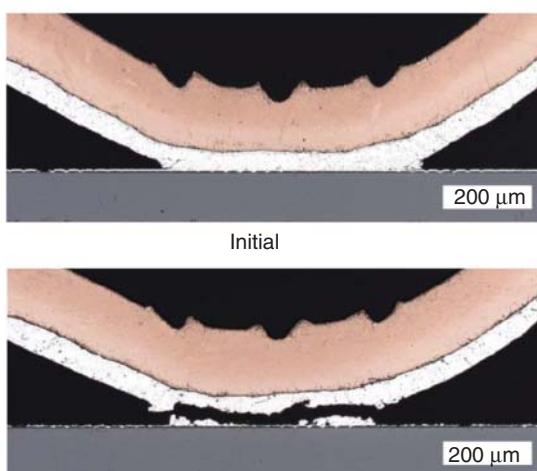


**Figure 14.39** Power cycling of SiC Schottky diodes packaged with “XT technology” – Cu Bonds, Ag-sintering, EasyPACK housing.  $T_{j,max} = 150^\circ\text{C}$ ,  $t_{on}$  1.5 seconds. Test executed by C. Herold at TU Chemnitz.

**Figure 14.40** Sintered Cu-foil on top of a SiC device. Source: Figure from Streibel et al. [75].



(a)



(b)

**Figure 14.41** AlCu ribbons for possible replacement of Al wires. (a) top view and (b) cross section, showing the lifetime limiting cracks. Source: Figure from Clausner et al. [78].

Cu and SiC show very different CTEs; therefore, work on a 100 µm molybdenum top plate instead of the 50 µm Cu foil is reported in [76]. Molybdenum exhibits a low CTE which is well adapted to the CTE of Si as well as SiC.

Al-cladded Cu bond wires are also possible [77]. A further interesting alternative could be the use of AlCu ribbons [78], where the electrical parameters are dominated by Cu, and the bond process is executed as Al to Al process. Figure 14.41 shows this technology.

For both Al-cladded Cu bond wires and AlCu ribbons, no noble metal surface is necessary and established packaging tools can be used. Power-cycling results for both are only available for Si devices up to now. In both cases, an increase of a factor of 6–10, depending on the conditions, can be achieved compared to the Al bond wire.

In summary, SiC is more challenging regarding packaging technologies. For reliability, similar or higher compared to Si, new packaging technologies are necessary. However, modules with new technologies can achieve a very high power-cycling reliability. The final solutions on the market will be a trade-off between a high lifetime and the production effort/costs.

## Acknowledgments

The presented material in the above paragraph, including pictures, was widely supported by several researchers from Infineon and Chemnitz University of Technology, namely, Caspar Leendertz, Rudolf Elpelt, Roland Rupp, Shanmuganathan Palanisamy, Christian Herold, Peter Seidel, and Maximilian Goller.

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# 15

## Industrial Systems Using SiC Power Devices

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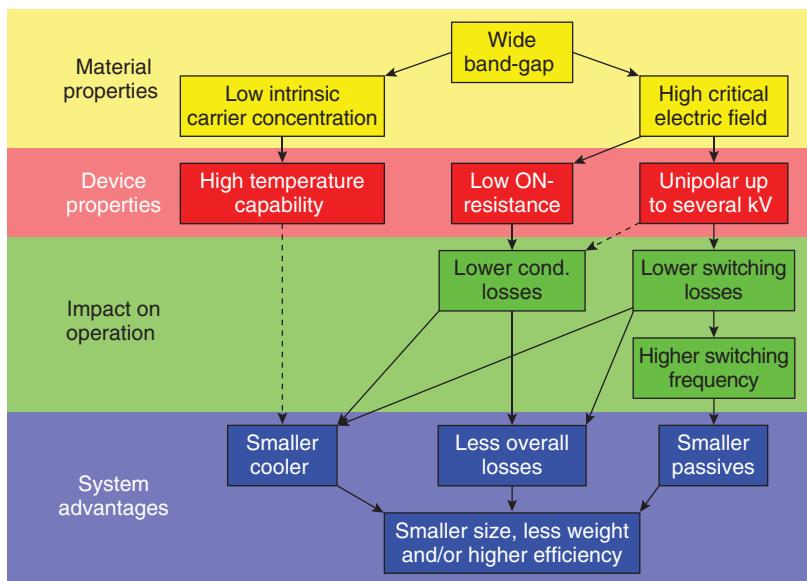
### 15.1 Introduction

Based on its unique properties, SiC offers unparalleled opportunities for industrial electronics just the way it does for most medium- and high-power applications. However, individual applications profit in individual ways, and some still existing drawbacks of SiC prevent its advantages from being fully exploited. In other words, the appraisal of potential benefits from SiC devices is necessarily a case-to-case judgement. Nevertheless, the exploitation of the SiC advantages goes along the same few lines for all applications, though to an individual extent. In Figure 15.1, the main lines of benefit are sketched.

#### 15.1.1 Benefits of SiC Devices

Due to the stronger bonds between the atoms in the SiC single crystal, more energy is required to excite electrons from the valence band to the conduction band. That is what has been modelled as the eponymous “wide bandgap.”

On the one hand, this means more heat is required to achieve the same intrinsic carrier concentration like in silicon. In SiC, about 600 °C equals room temperature in silicon. Thus, SiC devices inherently have an excellent high temperature capability – at least theoretically. Today, standard packaging materials still prevent true high-temperature applications in the mainstream, while the SiC devices utilised for high-end applications come at a significant premium on the packaging cost. Furthermore, the power cycling capability of SiC devices is lower compared to silicon for the same temperature swing because SiC is much stiffer. This limits the utilisation of higher temperatures because in operation a high peak temperature usually goes together with high temperature swings, which lead to a correspondingly higher level of thermomechanical stress [1]. The same argument limits the reduction of the cooling effort, i.e. simpler or smaller, in any case cheaper coolers, because the reduced cooling would lead to higher temperature swings for the same loss level. Therefore,



**Figure 15.1** Impact of the SiC properties on the system.

the link between high temperature capability and smaller cooler is sketched only as dotted line in Figure 15.1.

On the other hand, a higher electric field is required to accelerate electrons such that they can kick other electrons out of their bonds. The critical electric field, at which this so-called impact ionisation occurs, is in SiC about 10 times higher than in silicon and allows for about 100 times higher doping levels as well as 10 times thinner active layers for a given blocking voltage. Both effects together reduce the series resistance of the active layer in Schottky diodes and metal oxide semiconductor field-effect transistors (MOSFETs) by a factor of roughly 500 at a given breakdown voltage or increase the blocking capability at a given on-resistance by a factor of about 12. Therefore, SiC devices with blocking capabilities exceeding 1 kV can still be unipolar, while in silicon, this is clearly the realm of devices like pin diodes or insulated gate bipolar transistors (IGBTs), which are flooded in on-state with electron–hole–plasma (conductivity modulation) to reduce the series resistance.

While the plasma is an advantage during conduction, its dynamics establish a massive drawback at turn-off. The additional charge causes substantial switching losses when extracted from the device, and the plasma's “inertia” limits the switching speed significantly. From unipolar SiC devices, only the doping charge or “capacitive” charge has to be extracted and the switching speed is no longer limited by the device, but by the surrounding circuitry. Thus, the time at high voltage and high current can be reduced to the nanosecond scale and the switching losses can be factors lower than with the plasma-modulated silicon devices. However, there is a lower barrier for the switching losses of the unipolar MOSFET, which results from the energy stored in the output capacitance. This amount of energy is lost when the MOSFET is turned on again, i.e. once in every cycle.

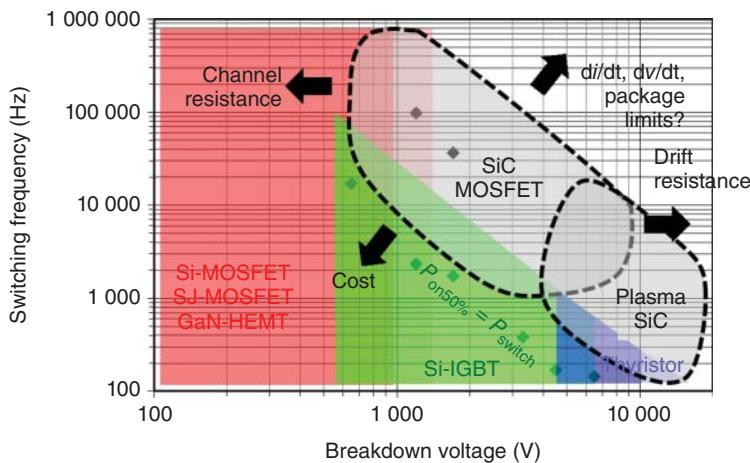
Furthermore, the injection of electron–hole–plasma requires a forward-biased junction that shows up in pin diodes and IGBTs as a threshold of the well-known 0.7 V before significant current can flow through the device. Of course, this causes additional conduction losses. The SiC MOSFET does not show this issue and has at least at low current density, i.e. under partial load conditions, an additional advantage. Again, the line towards lower conduction losses in Figure 15.1 is dotted because in MOSFETs the advantage is usually compensated by the series resistance towards higher current density and because SiC Schottky diodes do not show this advantage (Schottky barrier) at all. Furthermore, the advantage transforms into a disadvantage for very high-voltage SiC devices. Beyond 10 kV blocking capability, the series resistance in unipolar SiC devices increases to such high values that a plasma flooding is required too. Due to the wide bandgap (WBG), the junction voltage is now about 3 V instead of the 0.7 V [2]. This is the reason why the plasma flooding in SiC makes sense at very high blocking voltages only and has not yet gained any ground in commercial devices. Of course, the bipolar degradation is yet another argument.

Both the lower conduction losses and the lower switching losses have a positive impact on the cooling requirements. Simpler coolers, e.g. air instead of water coolers, or just smaller coolers can be utilised and significant system advantages can be achieved beyond the higher system efficiency. System advantages are anyway a major argument to justify the use of SiC devices.

Due to the more complex manufacturing process, SiC wafers will remain more expensive per area than silicon or GaN on silicon. To a certain degree, this can be compensated by smaller chip sizes sacrificing the on-resistance, but loss density and the necessity to get the current into the chip are limiting the shrinking. Usually, a similar power density will be the guideline for dimensioning, and, thus, for the foreseeable future, SiC chips will remain more expensive per ampere than silicon ones. Consequently, the deployment of SiC devices has to gain system advantages to prevail.

In this context, the low switching losses of SiC devices can help because the switching frequency can be much higher without running directly into a temperature or efficiency problem. At higher switching frequency, the energy, which capacitors and inductors have to store during the shorter cycle, can be proportionally smaller and so can be the volume of those passive components – at least their active volume. Doubling the frequency would reduce the energy storage to half of its original value, size, and hopefully also its cost. Unfortunately and due to e.g. windings, the volume is going down in reality more like with the square root of the frequency [3] not even considering other system constraints. Nevertheless, a substantial system advantage can be achieved.

However, as the switching losses are not zero and anyway limited towards lower values by the capacitive charge that is lost in every cycle, the “affordable” frequency is certainly a trade-off between conduction losses and switching losses. Figure 15.2 gives an idea about the achievable frequencies. The data points show IGBTs and SiC MOSFETs of the different voltage classes. For each data point, the frequency is calculated such that the (hard) switching losses at nominal current and typical direct



**Figure 15.2** Application ranges for SiC devices. Data points are calculated to be the points of equal switching and conduction losses.

current (DC-link voltage are equal to the conduction losses at nominal current and 50% duty cycle. The shaded area ends where switching losses reach 10 times the conduction losses. In this simple estimation, 1200 V IGBTs can go to 20 kHz, while 1200 V SiC MOSFETs can go all the way up to 1 MHz. However, IGBTs can be optimised for low conduction losses and high switching losses (high plasma concentration for low-frequency applications) or high conduction losses and low switching losses (low plasma concentration for high-frequency applications). Of course, this would change the figure significantly. Furthermore, soft or resonant switching is another factor that changes the loss balance substantially and is not reflected in the figure. After all, the appraisal of potential benefits from SiC devices is indeed a case-to-case judgement.

### 15.1.2 Competition by Other Technologies

Figure 15.2 also indicates potential limitations or rather competition of the SiC devices. Towards lower frequency, the SiC MOSFET cannot exploit its low switching losses and the silicon IGBT can prevail due to its cost advantage. Towards lower blocking capability, the still high channel resistance of SiC MOSFETs, mainly resulting from the low channel mobility, becomes dominant and limits the overall resistance downwards to about  $1 \text{ m}\Omega \text{ cm}^2$  such that devices like the silicon super junction (SJ) MOSFET (currently about  $8 \text{ m}\Omega \text{ cm}^2$  at 600 V with prospective  $4 \text{ m}\Omega \text{ cm}^2$ ) or the GaN high electron mobility transistor (HEMT, prospectively  $\ll 1 \text{ m}\Omega \text{ cm}^2$ ) have an edge over the SiC MOSFET in those voltage classes [2]. At really low voltages, even the simple silicon MOSFET is better! Towards higher blocking capability, the series resistance of the SiC MOSFET's drift zone gets too high, so that plasma flooding is beneficial even for SiC and given the junction voltage of 3 V, which has to be overcompensated by less series resistance, before an advantage is achieved. Finally, towards higher frequency, the SiC MOSFET faces

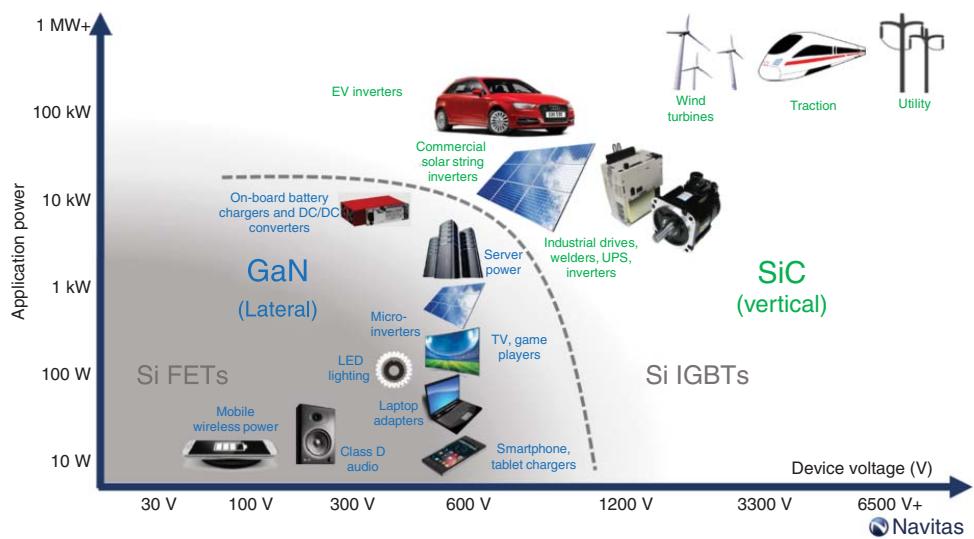
several limitations by the packaging and the surrounding circuitry [1]. All kinds of stray inductances and stray capacitances limit the switching speed, either directly by slowing down the switching process at some point or indirectly by causing oscillations, critical electromagnetic interference (EMI), or instabilities, which can only be controlled by slower switching, i.e. smoother switching transients. In fact, these kinds of package-induced problems are already an issue for silicon devices, and switching slopes beyond 50 or  $100\text{ V ns}^{-1}$  require better packages than just normal surface-mounted device (SMD) ones. Furthermore, components outside the SiC device might degrade from such high-voltage slopes, with the insulation of the windings of electrical machines being an extreme example.

Thus, the decision to utilise SiC devices is quite complex and can be summarised in Murphy's law for WBG devices: anything that can be made from silicon will be made from silicon, in the most reliable and cost-efficient way. The competition is nicely sketched in Figure 15.3, which locates the various applications in a voltage class vs. power-level diagram (a voltage vs. current diagram would give a similar message). SiC devices will serve the  $>1000\text{ V}$  and  $>10\text{ kW}$  applications, and the main competitor in that range is the silicon IGBT. Towards lower voltage and lower power, GaN competes with silicon field-effect transistors (FETs), and as long as the channel resistance is high in SiC MOSFETs, they will face problems there, although the market of  $650\text{ V}$  SiC MOSFETs is growing rapidly, with Tesla alone generating a nine-digit Euro revenue with their Model 3 using  $650\text{ V}$  SiC MOSFETs. Only the SiC Schottky diodes prevail in this market due to their unipolarity and high-frequency capability, but in some applications, they are already replaced by FETs used as synchronous rectifiers to avoid the diodes' threshold.

The following sections will provide an overview of how SiC can serve different applications and their respective requirements and in which cases competing technologies might offer a better solution. Of course, this work can only outline some general trends. For a wider overview and more details, refer to e.g. [5] and [6].

## 15.2 DC/DC Converters

It might sound contradictory to consider DC/DC converters as high-frequency systems, but it is absolutely not. In many other systems, the switching frequency is given or at least strongly influenced by the system frequency, while in DC/DC systems, the frequency is a free parameter and is ideally not even detectable outside the DC/DC converter. As discussed in the introduction already, a higher switching frequency increases the switching losses, but it also reduces the required size of the passives, i.e. inductors, capacitors, and filters significantly and might be also beneficial with respect to EMI issues. This way, the system cost can be reduced substantially and the overall system cost can be smaller compared to a silicon-based solution even though the SiC devices are still more expensive. This was already the business case for the first commercial SiC device, the 600-V Schottky diode. In an early application example [7], the cost of a classical boost converter used as the power factor correction (PFC) stage of a switched-mode power supply (SMPS)



**Figure 15.3** Application ranges for SiC devices in competition with silicon IGBTs, silicon FETs, and GaN devices. Source: Kinzer and Oliver [4]. © 2016, IEEE.

could be reduced by 9% by going up from 140 to 500 kHz, although the SiC Schottky diode was 2.5 times (5 times per ampere) more expensive than the silicon diode and required a more expensive silicon SJ MOSFET to reach the high switching frequency. This business case paved the way for generations of SiC devices and started the race to make the switching frequency of DC/DC converters as high as affordable, reaching values into the megahertz range. However, in the meantime, the switching frequencies are rather coming down again to values well below 100 kHz. Other improvements, especially on the coils and the control scheme, allow for size reduction such that the extremely high switching frequency is no longer required and can be reduced for the sake of lower switching losses.

In any case, switching frequency of an individual device is not a value by itself but increases the switching losses and might compromise the overall efficiency. Here, the topology the devices are operating in and its control scheme have a massive impact. As an example, Figure 15.4 shows the trends in PFC stages [8], the circuit that allows to draw sinusoidal currents from the grid to avoid harmonic distortion. Today, such circuits are legally required for switch mode power supplies beyond 75 W and for lighting applications beyond 18 W already. One trend is integrating the rectifier bridge into the boost converter (“bridge-less”) to reduce the number of diodes in the current path and, thus, to avoid diode on-state losses. Another trend is replacing diodes by switches to avoid the higher losses due to the diodes’ threshold voltage. Ironically, this leads to PFC stages without any of the Schottky diodes that started the SiC market [9]. Furthermore, this opens up options on the control scheme. However, the details about continuous conduction mode (CCM), triangular current mode (TCM), boundary current mode (BCM), etc. go beyond the scope of this chapter but have clearly an impact on the performance of the converter and the requirements for the “ideal switch.” In fact, the latest topologies use different switches for defining the current path (low on-state required, low switching frequency) and for doing the actual boosting (low switching losses required, high switching frequency) and the frequencies range from a few 100 kHz up to about a megahertz.

As indicated in Figure 15.4, the optimum device for the bridge-less PFC is not necessarily an SiC MOSFET. In the 600-V class, several other device options are available: GaN HEMTs, silicon SJ MOSFETs, or, in some cases, even silicon IGBTs. With respect to the technology, the 600-V class is, thus, the most competitive market. In this application range, the device properties have to perfectly fit the requirements of the topology, and a little drawback in one parameter might make the competing device better suited already – and prevailing. An overview of the latest devices and the applications they are best suited for is given in Figure 15.5. Depending on the specific application, different figures of merit (FoM) are decisive and the overall cost is anyway giving a strong bias towards silicon solutions. Thus, 600 V is a difficult battle ground for SiC, and only a few applications are clearly suitable.

One of those suitable applications is the DC/DC converter with galvanic insulation, which is usually the main stage behind the PFC in an SMPS. The galvanic insulation is provided by a transformer, and on the primary side, one or more switches generate a high frequency input, while on the secondary side a

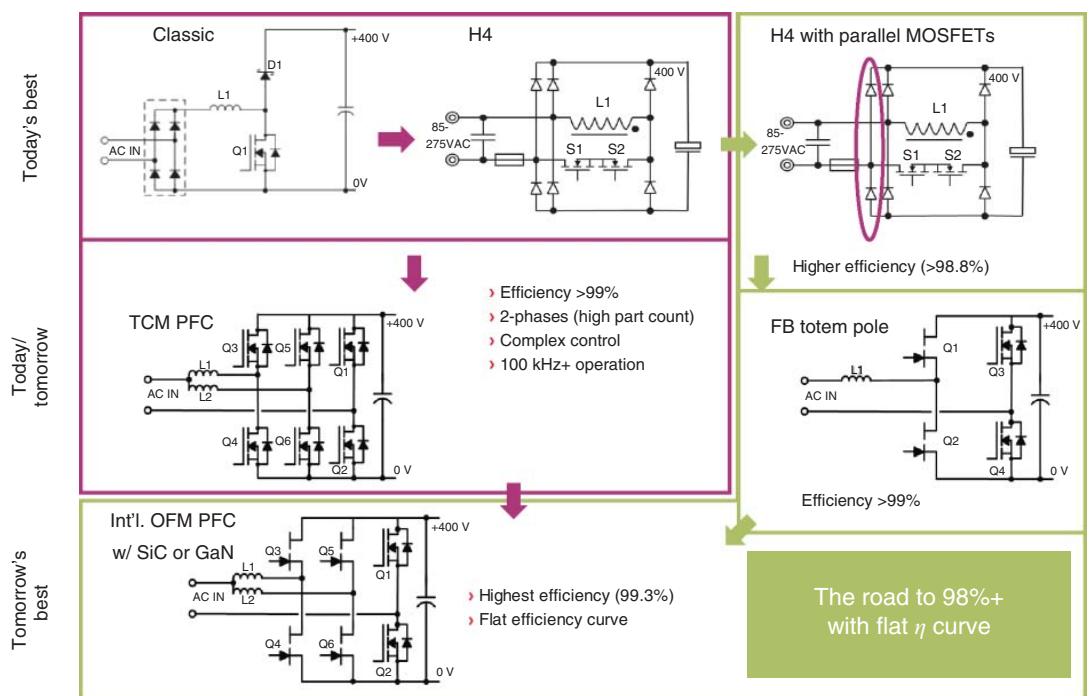


Figure 15.4 Trends in bridge-less power factor correction (PFC) stages. Source: Deboy et al. [8]. © 2016, IEEE.

Device	$V_{(BR)DSS}$ (V)	$R_{DS(on)} * Q_{rr}$ ( $\text{m}\Omega * \mu\text{C}$ )	$R_{DS(on)} * E_{oss}$ ( $\text{m}\Omega * \mu\text{J}$ )	$R_{DS(on)} * Q_g$ ( $\text{m}\Omega * \text{nC}$ )	$R_{DS(on)} * Q_{os}$ ( $\text{m}\Omega * \mu\text{C}$ )
CoolMOS™ 7	600	100%	100%	100%	100%
CoolMOS™ 7-fast diode	600	10%	104%	108%	104%
CoolGaN™ Gen 1	600	0%	84%	6%	13%
CoolSiC™ Gen 1	650	2%	133%	41%	21%

Allows WBG usage in topologies with repetitive hard commutation (e.g. CCM totem-pole PFC) → BOM savings for highest efficiency

SiC/GaN in servers, on-board charging

Minimum switching losses in hard-switching topologies (e.g. classic boost PFC) → higher efficiency with GaN

Si for best cost-performance ratio

Reduced driving losses especially at light-load conditions. Allows WBG to reach higher efficiency at increased frequency → power density increase (weight and size reduction)

High power density e.g. GaN for chargers

Enables better soft-switching (e.g. half-bridge LLC), where WBG leads to higher efficiency combined with high frequencies

SiC and GaN e.g. in telecom

Both SiC and GaN allow an easier way than Si to top efficiency

The three products have similar behaviour in hard-switching topologies such as classic PFC

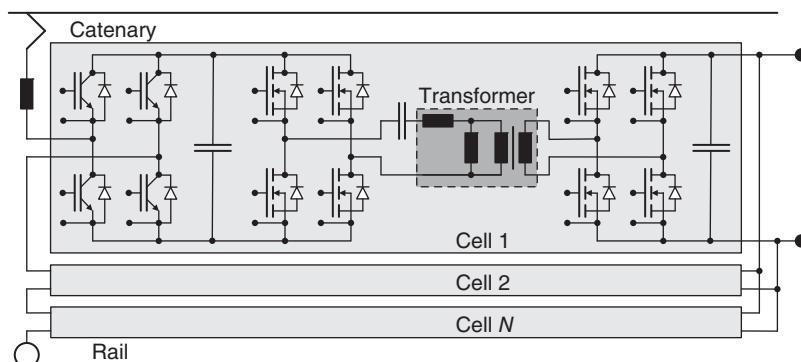
For power density, SiC is better than Si but the champion is GaN

SiC and GaN are both better than Si to reach both high efficiency and high density

Figure 15.5 Technology comparison between silicon, SiC, and GaN devices. Source: Courtesy of Infineon.

rectification is provided. For low power, flyback converters as the simplest variant with only one switch, recently preferably extended to resonant mode, or forward converters as the more efficient variant were utilised for insulated DC/DC conversion. For higher power, the main stream is feeding the transformer by a half-bridge or a full-bridge topology [9, 10], which generate the high-frequency input. Again, the higher the frequency is, the smaller the transformer can be. To be even more efficient, the primary side can be extended by an inductor and a capacitor to form a resonant system and to operate in soft switching mode. This is then called the LLC topology and is the main stream for highest efficiency. On the secondary side, the rectifier can be a simple diode bridge or an active half or full bridge. The active bridges are more efficient and offer more functionality, in particular energy can also be fed back to the primary side. Of course, active bridges are also more expensive. A schematic is shown in Figure 15.6 as the inner part (between the capacitors) of a power electronic traction transformer (PETT) cell.

Such LLCs operate at frequencies from a few 10 kHz to beyond a megahertz [13], and they are suited for a wide range of applications. At the 600-V class, GaN constitutes a strong competition, but as soon as the voltage or power level increases, SiC has an advantage. Examples are the auxiliary power supply in trains [14], with 99% efficiency (96% for the entire AC/AC system) at 50 kHz and 1200 V MOSFETs or 6.6 kW electric vehicle (EV) chargers [13], with 98% efficiency at 625 kHz and 650 V MOSFETs. However, it becomes really exceptional, when 10-kV SiC MOSFETs are used to supply 25 kW to 400 V (e.g. data centres) directly from a 7-kV DC source [15]. The converter operates at 48 kHz and has a measured efficiency of 99% with 99.2% easily achievable by using different SiC devices on the secondary side. In such applications, admittedly a niche yet, no other technology can rival SiC performance – except from the good old transformer and its unbeatable reliability, which is pivotal in data centres, no matter if that comes at the price of lower efficiency. After all, there are several DC/DC applications in which SiC can excel, and the market perspective looks great over the entire range of voltage classes.



**Figure 15.6** PETT topology according to [11, 12], with the primary-side low-frequency AC/DC converter equipped with an IGBT full bridge and the high-frequency DC/DC converter equipped with SiC MOSFET full bridges.

## 15.3 Solid-State Transformer (SST)

The basic idea of the solid-state transformer (SST) dates back to the late 1960s and is all about replacing a bulky, inefficient low-frequency transformer by a smaller, lighter, and more efficient transformer operating at significantly higher frequency [16]. Obviously, those advantages come at the extra effort to generate a higher frequency input for the transformer from the low-frequency supply. The extra effort on the secondary side depends a lot on the load to be supplied and might be even smaller in case it is just a rectification. After all, the SST is a kind of a high-power variant of the SMPS and the variety of topologies has become similarly diverse.

The main differences between the topologies occur on the primary side and concern the way of how the higher frequency is generated. The original way is direct conversion by chopping the low-frequency AC such that a higher frequency AC results. This is a single-stage process with low losses but causes a lot of harmonics. The alternative way is to rectify the low-frequency AC first and then generate the higher frequency AC from the resulting DC-link. Although this is a two-stage process with respective losses and requires a DC-link, the design freedom in the second stage due to the decoupling by the DC-link is dominant and allows for a much better system.

To reduce the switching losses, resonant or soft switching can be applied instead of the hard-switching mode. The semiconductors switch at a moment without a voltage drop across them or without a current flow through them and, thus, the switching losses disappear – at least under ideal conditions. In fact, the control of the current waveform is usually even more sophisticated [11] and opens the path to even higher frequency without the disadvantage of reduced efficiency and is, thus, widely deployed.

The third difference is how the high voltage is applied to the primary side. Is the full voltage applied to a single transformer, or is a series connection of lower voltage SSTs connected to the high-voltage mains and then connected in parallel on the secondary low-voltage side? A third, yet rarely used alternative is deploying a modular multi-level converter (MMC or M<sup>2</sup>LC, cf. Section 15.8.1) on the primary side, which resembles a distributed DC-link.

SSTs are a combination of these three properties, and it depends a lot on the particular application, i.e. voltage level and frequency of the mains, which variant is best suited. The fields of traction and smart grids will be discussed in the following sections.

### 15.3.1 Traction

Maybe the most obvious application for an SST and the first one realised is replacing the bulky low-frequency main transformer of a train. This is particularly valuable in Germany, Switzerland, Austria and parts of Scandinavia, where the AC voltage of the catenary is 15 kV at a frequency as low as 16.7 Hz. In those cases, the SST can reduce volume and weight substantially and can go under floor or on top of the roof of the train to free up space for passengers. Furthermore, a substantial efficiency

improvement can be achieved and functionalities are available that go far beyond a simple transformer.

An example of such an SST for traction applications is shown in [9] under the name of PETT. Whereas the early SSTs for traction were based on thyristors and increased the frequency to only 400 Hz, the PETT used 6.5-kV IGBTs and the transformer frequency went up to 1.75 kHz (thermally limited). To cope with the peak voltage of  $15 \text{ kV} \cdot \sqrt{2} = 21.2 \text{ kV}$  (plus fluctuation margin), the PETT used an input series output-parallel (ISOP) topology with 9 SSTs (one for redundancy) of 150 kVA each, giving a total power of 1.2 MVA. The topology also used soft switching to reduce switching losses with zero voltage at turn-on and low current at turn-off. In total, the efficiency of the prototype achieved 96% (98% for the DC/DC converter part), which is 2–4% better than with the traditional solution, while the power density went up as well as the weight went down by a factor of more than two.

Although this is quite a progress over the traditional technology already, SiC can further improve the PETT. This potential step forward is documented, e.g. in [11] on a PETT designed for 25 kV and 50 Hz (catenary in western and eastern Europe). It has quite a similar topology based on soft switching like the previous PETT but uses 3.3-kV SiC MOSFETs and has a much higher transformer frequency. In fact, the ideal frequency is no longer determined by the semiconductors and their losses but by the transformer properties and the exact control scheme. For the DC/DC “converter part”, efficiencies of well above 99% at frequencies between 10 and 20 kHz have been achieved.

Obviously, the PETT is a promising field of application for SiC devices and an attractive market. However, the reliability of the bulky and lossy low-frequency transformer is unbeatable and, given the worldwide efforts to improve dependability of the train service, the train operators will not accept higher failure rates due to the PETT. Thus, a special focus has to be on the PETT’s reliability, if necessary by means of redundancy as demonstrated in the early PETTs already.

### 15.3.2 Power Grid

Although in both cases the grid frequency is low, the situation of an SST in the power grid is obviously different from the PETT. While high efficiency and reliability are extremely relevant for both applications, volume and weight are of less concern for a grid transformer and a conventional high-power transformer can already reach an efficiency of 99% and above [17]. Here, it is more the additional functionality or controllability that makes the SST superior to the conventional transformer. Typical examples are phase shift, voltage regulation, or control of reactive power as it is required, e.g. in grids with a strong feed-in of renewable energy. Thus, the SST is usually quoted together with the smart grid, and the goal is a smart transformer without sacrificing efficiency too much. However, some of the control features like the voltage regulation can be achieved by mechanical tap-changers or power electronics processing only a smaller fraction of the power [17]. Furthermore, the SST is not a drop-in replacement for conventional transformers because the protection schemes are incompatibly different. Thus, the grid concept has to be reconsidered

anyway, and in the future, some of the controllability features might be taken over by the increasing number of feed-in inverters themselves. Thus, the SST in power grids does not look like an attractive market for any kind of semiconductors, though SiC would bring the technology closer to the efficiency benchmark set by the conventional transformer. However, the situation looks better if the SST is not connecting two AC grids (of the same frequency) but is feeding a DC grid from an AC grid (cf. Section 15.7), i.e. there is no secondary inverter, while the conventional transformer would require the rectification step.

## 15.4 Wireless Charging

Due to the air gap of a few centimetres or even beyond 10 cm required for practicality, the vast majority of wireless charging systems, especially in the high-power range relevant for the application of SiC devices, is based on inductive coupling and, thus, is usually called inductive power transfer (IPT) [18, 19]. Such a system can be considered a galvanic insulated DC/DC converter or SST using a high-frequency transformer, which can be split in two parts such that the primary and the secondary side of the system can be separated. Indeed, creating the transformer from two independent and in-field service not necessarily well-aligned coils introduces a number of restrictions for the charging system, concerning the design of the coils and the core, the material selection, EMC regulations, and particularly safety [20]. It is getting even more challenging if the secondary side is moving while charging like in case of trains [21, 22] or cars [23] or if harsh conditions like snow or (even ferromagnetic) debris compromises the transmission [24]. But even if the EV is at rest in its protected garage or the tram has a stop at a clean station, the charging system has to cope with varying system properties, i.e. changing coupling, parasitics and resonances, which requires an adaptive or resonant network or an even smarter control. Consequently, most of the specific work has been done on the coils and the control, which goes clearly beyond the scope of this chapter.

The rest of the IPT system, in particular its topology, is pretty much the same as an SST, though the IPT has sometimes a three-phase design [22]. However, there is some impact on the rest of the system as well and the most striking is the still much lower efficiency than the 99% achieved in galvanic insulated DC/DC stages or the only slightly lower values of a complete SST. A silicon equipped 1 MW system feeding in to a 2.8-kV busbar of a high-speed train shows 82.7% efficiency at a frequency of 61.5 kHz [21] and the 50-kW system feeding into the 800-V busbar of a tram shows 88% efficiency at only 25 kHz [24]. Because the coil system is the main issue, moving to SiC is indeed improving the efficiency of the semiconductors but has only little impact on the overall efficiency of the IPT system and mainly academic work has been done [25, 26]. However, a higher frequency also provides more freedom in the coil design and helps to improve the power transfer over the coil system [27]. At the 85 kHz, the Society of Automobile Engineers (SAE) Standard J2954 is going to ask for, SiC becomes inevitable for high-power systems with, respectively, high DC voltages. An example is reported in [27], where a 50-kW all-SiC system for up to

800 V on both sides showed a DC-to-DC efficiency of 95.8% and a power density of  $9.5 \text{ kW dm}^{-3}$ . Apparently, also system advantages like reduced size or reduced cooling effort on board or at stations, i.e. remote locations, might justify the utilisation of SiC components already. Given the potential number of systems, this might become an interesting application for SiC devices.

## 15.5 Inductive Heating

### 15.5.1 Domestic Systems

One could think of an induction heating system as a wireless charging system with the secondary winding being permanently shorted by an ohmic resistor converting the transferred energy into heat. But depending on the exact application, there are substantial differences. The well-known induction cookers at home operate in the frequency range above 25 kHz to avoid audible noise, but usually also well below 50 kHz to keep switching losses low. This rather low frequency requires the use of ferromagnetic cookware, which has a rather high resistivity to generate sufficient ohmic heat out of the induced eddy currents and which adds additional heating (about one-third of the total heating) due to hysteresis loss in the cyclic reversal of the magnetic field. Such frequencies can still be handled by silicon (reverse conducting) IGBTs optimised for soft switching and operated e.g. in a single-ended quasi-resonant topology [28]. Thus, SiC devices can indeed improve the efficiency of induction cookers [29], but due to the higher cost and due to the anyway dominant induction coil losses, SiC devices are not yet widespread in this application. However, given the large number of cookers in the world, SiC devices envisage a large potential market once the device cost is coming down – and if GaN devices are not providing superior solutions. GaN devices might also be the strongest competition in the trend towards all metal (e.g. aluminum, copper, or even multi-layer) capability, which requires frequencies up to the megahertz range [30]. However, due to the increasing coil losses, the overall efficiency would not profit significantly and also the trend towards areal induction or flexible cooking surface [30] is neither fostering SiC application nor is improving overall efficiency.

### 15.5.2 Industrial Systems

Industrial heating systems are different not only in power level, from a few kilowatts to several megawatts, but in some cases also in frequency, from 500 Hz to some megahertz. The frequency is in general dependent on the application and on the material to be heated. Melting and forging require very high power (several megawatts and very low frequency in the range of 0.5–5 kHz), while brazing, surface hardening, and induction shrink fitting [31] require frequencies in the range of 10–100 kHz and tube welding requires very high frequency and power (150–400 kHz and 0.2–2 MW). In medical systems, the frequency is usually even higher with some systems going far beyond 1 MHz [31]. The IGBT can be applied up to about 100 kHz if operated

in a resonant circuit [32] and can go beyond only if several IGBTs are working in parallel in an interleaved mode [32], i.e. distribute the losses by reducing the duty cycle for an individual device. Higher frequencies beyond the reach of IGBTs used to be the realm of the silicon MOSFET for its low switching losses. However, the high conduction losses especially at higher voltage levels and the anyway increasing switching losses establish a limitation for the frequency and to rather low efficiency. Here, the SiC MOSFET can achieve a massive improvement. On the one hand, the efficiency can be higher, especially when operated in zero-voltage switching (ZVS) and reduces the operational expenditure in terms of energy consumption and cooling effort [32, 33]. On the other hand, the number of devices, i.e. total chip area, can be much smaller and compensates for the higher cost of SiC devices per chip area. This effect is even boosted by the reduced cooling effort, reduced occupied space, and smaller driving circuitry, which can already now lead to a system advantage and reduced capital expenditure [32]. However, the mission profile of induction heaters has often a stop-and-go characteristic and would require a high power-cycling capability, which is still a challenge for SiC devices if not counterbalanced by the usually lower temperature swings or more elaborate assembly technologies. Together with the reduced number of devices, even an improved reliability is predicted and would reduce operational expenditure even further. Based on all the advantages mentioned earlier, industrial or medical induction heating seems to be a promising, though small market for SiC devices. An example of a novel SiC-based technology for induction heating converters is shown in Figure 15.7.

## 15.6 Photovoltaic

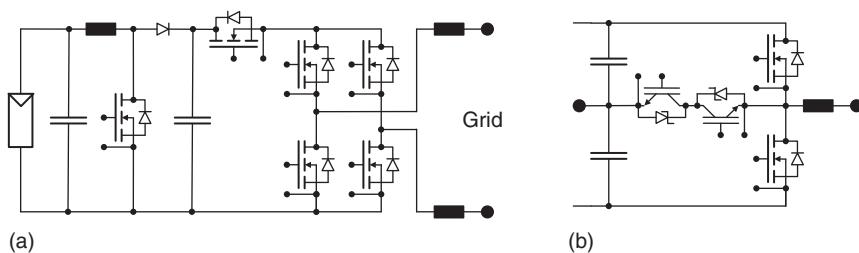
### 15.6.1 Residential Systems

A simple PV inverter for residential systems (<10 kW) is a two-stage system with one (or more) boost converter and maximum power point (MPP) tracker in the first stage (Figure 15.8a) feeding a DC-link capacitor. For this stage, the advantages for DC/DC converters apply, i.e. increasing the frequency would allow for shrinking the coils and capacitors. However, for cost and loss reasons, residential systems tend to be transformer-less and the DC-link voltage for direct grid connection has to be at least slightly higher than the 325 V peak value of the 230 V<sub>RMS</sub>. Usually, the window for the DC-link voltage is 350–500 V, but can go up to 600 V under some operation conditions. In that case, silicon SJ MOSFETs or rather silicon IGBTs are good enough (antiparallel diode operation not required) and cheaper, while the free-wheeling diode is indeed preferably a unipolar SiC Schottky diode for their low conduction losses and very low switching losses as well as the low stress it imposes on the switch due to the missing reverse recovery peak. The switching frequency is, however, usually not much higher than 50 kHz. The case for SiC switches is getting even weaker, if the first stage is composed of series connected DC/DC converters of even lower voltage. Here, silicon is clearly advantageous and GaN might offer an even superior solution. However, such topologies are yet irrelevant.

Today's IH converter technology	The SiC inverter	Technological improvements	Benefits to the customer
Mostly Si (IGBT/MOS) technology	SiC technology	Efficiency improvement to 99.5%	Less OPEX, due to lower electricity and cooling water consumption
Power module technology	Discrete devices technology	Lower stray inductance Higher efficiencies Higher frequency range No complex control strategies	Cost reduction Lower electricity consumption Lower cooling water consumption
Electrolytic or film caps technology	Antiferroelectric ceramic capacitor technology	Allows significant size reduction	Less industrial space requirements Converter easy handling
Distributed converter architecture (power section, controller, sensing circuits... in different blocks that have to be cabled)	Embedded or semi-embedded converter architecture	Automated production Production costs reduction Size reduction Production stability Improvement of reliability	Significant cost reduction Allows significant size reduction Less OPEX, due to higher reliability
Single power port converter architecture	Universality: multi power port technology	Improves usability of the converter	Allows different IH applications with a single converter
Analogue or digital controller	Cyber-physical controller	Advanced process features Remote FW/SW updating Preventive and predictive maintenance	Converter set-up time reduction Lower OPEX Allows a user friendly use of the converter
Conventional mechanical architecture	Mechanical Plug & Go technology		Allows a very fast substitution of a power converter in the case of failure

	Standard tech.	New tech.	Reduction
Size (mm)	450 × 200 × 750	210 × 300 × 25	
Volume	70 l	1.5 l	98%
Power density	1.4 kW/l	65 kW/l	
Weight	50 kg	2.5 kg	95%
kW/kg	2 kW/kg	20 kW/kg	
Efficiency	98%	99.1% @ 400 kHz	

**Figure 15.7** Advantages of a novel SiC-based technology for induction heating converters and improvements achieved with a 100-kW system.  
Source: Courtesy of SiCtech Induction, Valencia.



**Figure 15.8** (a) Transformer-less single-phase PV converter with an H5 topology on the inverter side to cope with capacitive ground currents. Such converters are usually equipped with silicon IGBTs, but here SiC MOSFETs are shown as proposed in [34]. (b) Advanced T-type NPC hybrid (silicon/SiC) phase leg for a three-phase inverter [35]. Source: Based on Saridakis et al. [34], (b) Freiche et al. [35]. © 2017 VDE-Verlag.

The low DC-link voltage has also an impact on the second stage, i.e. the grid-connected inverter. Based on the feed-in tariffs, lower conduction losses pay back directly, while higher switching frequency has only an indirect advantage. Because the grid has a fixed frequency of 50 or 60 Hz, the higher frequency only helps to reduce the DC-link capacitor and the main line choke or filter size and their cost. This system advantage would compensate at least partially for the higher cost of the SiC components, but at the same time higher switching frequency increases switching losses and reduces efficiency again. Thus, there is a small window for overall optimisation, and the switching frequency of the inverter is usually not even close to the 200 kHz “optimised” for SiC in [34] reaching overall peak efficiencies exceeding 99%, a value that had been achieved with early commercial SiC switches already [36].

However, PV inverters based on silicon devices are already quite efficient as well and offer peak efficiencies of more than 98% or even beyond 99%, the latter admittedly at a substantially higher part count and higher cost [37]. Thus, the higher cost of SiC converters is paying back over time only slowly by feeding in less than 1% more energy. Consequently, market penetration of SiC-equipped inverters is still low, i.e. awaits cost reduction of SiC components due to economy of scale without contributing to the scale. At the same time, GaN makes significant progress and might be the better alternative for residential systems in the long run, especially at lower mains voltage.

### 15.6.2 Commercial, Industrial, and Utility Size Systems

For larger systems, the situation is different, as the power is too high to be fed into the single-phase mains. Instead, a three-phase connection is required, which results in more components in the inverter. At least, the MPP trackers remain the same, though they are operating at higher voltage and might be more numerous. Furthermore, capacitive currents towards ground potential are easier to control in a three-phase system. Again, SiC has a positive impact on the losses, but the overall optimum including cost and system benefits might lead to other solutions. An inverter leg of one advanced solution [35] is shown in Figure 15.8b. Here, the phase

leg of SiC MOSFETs is supplemented by an active so-called T-type three-level neutral point clamp (NPC), consisting of silicon IGBTs and SiC Schottky diodes of half the rated voltage. With the additional output level, the voltage and current waveforms are improved and additional system benefits can be achieved. In other words, a full SiC solution is not necessarily superior.

For even larger professional systems, the DC-link voltage is not directly coupled to the mains voltage because the power has to be fed in at the medium voltage level (10/20 kV or higher), which requires a transformer anyway. However, to profit from the relaxed low voltage regulations inside the solar park, the peak voltage has to observe the 1000 V limit and, thus, 1000 V<sub>DC</sub> and 400 V<sub>RMS</sub> (Europe) or 480 V<sub>RMS</sub> (United States of America) including safety margin used to be the typical voltage levels from the MPP trackers to the inverters and from the inverters to the transformers, respectively. At these voltage (and power) levels, SiC starts to have a clear advantage over competing technologies and the trend is going towards even higher voltage like the new 1500 V standard for the DC level inside the solar park because at higher voltage, cost is reduced for the DC cabling [38]. Unfortunately, 1500 V requires series connection of semiconductors or more sophisticated topologies like three-level NPC or the modern ANPC both with inherent series connection because neither silicon IGBTs nor SiC MOSFETs with the required blocking capability of about 2.5 kV exist due to the lack of other applications requiring this voltage class (only recently 2.3-kV IGBTs were announced [39]). Nevertheless, due to reduced passives and cooling effort, the system cost for a 150-kW 1500 V<sub>DC</sub> SiC inverter can already be lower than with silicon alternatives [40], and further advantages like a higher reliability due to lower part count of the then simpler converter might come on top [41, 42]. Thus, medium- and large-size solar inverters are an attractive and substantial market for SiC components and, after all, could become a driving market for the SiC technology.

However, the exact system layout of a solar park is another important consideration and defines the power level of the individual units. In fact, the MPP tracking and the voltage boosting can be done for an individual string or for several strings (decoupled by diodes) together. Likewise, a single centralised inverter can feed in the entire power or several smaller inverters can share the job. On the one hand, a single inverter is better for averaging (over load) and reliability (less components) reasons, but, on the other hand, a bit of redundancy is also good, and doing the MPP tracking individually might be advantageous as well. For commercial and industrial systems into the megawatt range, something in between with one inverter per a few string MPP trackers seems to be the optimum [43] and can be served with the SiC converter mentioned earlier [40]. On the contrary, for utility scale systems in the multi-megawatt range, usually all strings are connected together and a single inverter also taking over the task of MPP tracking feeds in the entire power – through the directly attached medium voltage transformer. This gives the lowest system cost, and individual MPP tracking is not required because the strings are very homogeneous anyway (similar solar radiation, no shadowing, same temperature). Unfortunately, for SiC that means that the power level is yet too high. However, that will change over time and, thus, SiC is supposed to excel in larger solar parks, too [44, 45].

## 15.7 DC Grids

In solar parks, the DC cabling is neither exactly DC nor a grid with potentially bidirectional current flow because the cables are a number of point-to-point connections between the strings and their respective MPP trackers or from decoupled strings to the central MPP tracker. A true DC grid is not beneficial here because it would require a decentralised MPP tracking with many satellite installations. Furthermore, a single failure would trip the entire solar park or a number of DC breakers would be required to handle such cases, introducing more complexity and more conduction losses. However, there are cases in which DC grids indeed make sense.

### 15.7.1 Low- and Medium-Voltage DC Grids

One classical, though small, example is the shared DC-link for drives. In case, there are inverters, which are mainly taking out energy from the DC-link, and others, which are mainly feeding energy back, the shared DC-link is equalising the fluctuation and only the net energy consumption has to be replenished by the mains via the rectifier stage. The benefit over individually AC-coupled converters originates from the reduced number of conversion stages for the recovered energy, i.e. one inversion and one rectification less, and also the grid coupling can be a simple bridge rectifier.

This example shows a typical finding when considering DC grids or DC microgrids. The systems profit most, when loads and local feed-in are similar, i.e. the system has a low net consumption, and equalisation is done inside the grid. Then the power conversion losses are smaller and overall efficiency is increased [46]. Typical examples could be residential or commercial buildings with PV systems and battery storage. As this advantage is purely due to the structure and operation of the microgrid, the improvement by utilising SiC components is limited to the efficiency increase of the individual conversion stages, as discussed in Section 15.2, with the DC voltage level as the main driver for the case of SiC. In fact, there is no ideal voltage level as many loads are at 5, 12, 24 and 48 V, respectively, while high-power load requires a higher voltage level like 380 V, and the installation would have to provide two or more levels maybe even mixed with the traditional AC [47]. This would require many rectifiers/inverters or DC/DC converters, most of them operating in partial load, which compromises the overall efficiency. Nevertheless, SiC components could improve the efficiency of some of the individual converters and will be widely used once the cost has come down. However, advanced designs allow for reduced system cost in the kilowatt range already ([48]: 5 kW, 50 kHz, 99% peak efficiency) and should boost the utilisation of SiC devices for microgrid applications.

A completely different kind of DC grid is found in data centres. Those grids are almost entirely traditional distribution grids with solely top-down power flow from the mains in tree-like structures to the individual computers, with decreasing voltage levels. The efficiency is better than in the microgrids because large-size central inverters can be used. However, the number of DC/DC conversion steps and the individual efficiency of the steps define the overall efficiency, with the lower steps clearly unsuited for the application of SiC devices. For the higher steps, SiC technology

is indeed well suited and, given the high utilisation of the equipment, even small efficiency improvements will save substantial energy justifying the higher cost of SiC devices, if the system advantages are not sufficient already. However, an even bigger step forward would be reducing the number of steps. A good example is an SST supplying 400 V directly from the medium-voltage mains; in this case, 3.8 kV<sub>RMS</sub> via a 7-kV DC-link utilising 10-kV SiC MOSFETs [15]. Although this is an exotic application, yet it could be a promising application for very high-voltage SiC devices.

### 15.7.2 DC Breakers

The systems discussed in the previous section were either small and very local or had unidirectional power flow. Nevertheless, already in this case a protection scheme is required to disconnect a defective part and keep the rest of the grid operational. The protection scheme is getting even more important in case of larger and meshed grids [49]. Fuses and electromagnetic circuit breakers are the traditional components, but they cannot be reset electronically, they need the capability to extinguish the arc without the zero-crossing missing in DC, and their reaction time in the milliseconds range is rather slow. In fact, a protection scheme needs to be quick in case the short circuit is low inductive and the current is rising quickly but needs also the capability to dissipate high energy in case the short circuit is high inductive. Semiconductor-based solutions are the method of choice to achieve short tripping times and a number of solutions have been proposed, mainly with differences in their triggering mechanism [50–52]. In those circuit breakers, SiC switches, ideally normally on devices, can only utilise their low on-resistance, while the switching speed is more than sufficient with any semiconductor solution and the switching losses are no longer determined by the semiconductor itself. However, semiconductor solutions can be designed to offer additional features like soft start or current limitation, to cope with inrush currents during start up [53, 54]. This can be a useful system advantage because then the individual loads do not need this feature anymore. However, the main challenge for semiconductor-based solutions is the vast amount of energy, which needs to be dissipated in worst case and which is dissipated in the arc of mechanical switches. Even for the most robust silicon-IGCT-based solutions, the energy is too high to be dissipated in the semiconductor [55] and has to go somewhere else. For SiC devices with their smaller device volume, the energy, which can be dissipated, is even smaller. Usual approaches are RCD snubbers, transient voltage suppression (TVS) diodes, or metal-oxide varistors (MOVs) [49].

## 15.8 High-Voltage DC (HVDC)

### 15.8.1 HVDC Transmission

Today, high-voltage DC systems are still predominately point-to-point transmissions, although multiterminal installations exist [56, 57]. The DC voltage level of such high-voltage direct current (HVDC) systems is mainly determined by the insulation

capability of the transmission line, i.e. cables or overhead lines, and goes beyond 1 MV vs. ground in some installations already [56, 57]. The blocking capability of the individual semiconductor devices is rather a free parameter because the extremely high-voltage levels require massive series connection anyway. In thyristor-based line commutated converters (LCC), the blocking capability ranges up to almost 10 kV because the switching losses are low and the thyristors can be optimised for low conduction losses. In the IGBT-based self-commutated voltage source converters (VSC), the switching losses in two-level topologies are substantially higher and the trade-off between conduction and switching losses led to lower blocking capabilities of the IGBTs like 2.5 kV. Nevertheless, the converters suffer from higher overall losses and were installed only in cases of a weak grid on one side, e.g. land connections of off-shore wind parks, or in cases of black-start capability was required. In all other cases, especially in bulk power transmission, the more efficient thyristor-based converters were deployed. In none of the cases, SiC devices would have been an (economically) viable alternative, if they had been available at the time.

However, the introduction of the modular multi-level converter (MMC or M<sup>2</sup>LC) [58] changed HVDC completely and within a few years only. In the MMC, the semiconductors of one branch do not switch simultaneously anymore, but only one semiconductor switches at the time or a few series connected switches together. This way, large voltage leaps are avoided and the filter requirements are greatly reduced. Furthermore, an individual cell switches only rarely during a 50-Hz or 60-Hz cycle, i.e. two to maximum five times. The switching frequency of an individual semiconductor is reduced from e.g. 1350 Hz (27 pulses in a 50-Hz cycle) to only 100–300 Hz, and the switching losses are reduced by about an order of magnitude, too. Accordingly, there is full focus on reducing the conduction losses and quite relaxed requirements for the losses of a single switching event. Consequently, the voltage class of the IGBTs went up to e.g. 4.5 kV and the devices are optimised for good conduction. In such converters, SiC MOSFETs cannot profit from their low switching losses, and conduction losses are a matter of chip area, i.e. cost, while plasma-flooded bipolar SiC devices are particularly unattractive in those voltage classes due to the 3 V junction voltage in on-state. Thus, SiC devices do not play any role in MMCs for HVDC, although MOSFETs are better and could indeed reduce losses, volume, and weight [59].

However, the situation will change if the voltage rating of an individual device is much higher than in today's silicon-based MMC cells. Many systems still rely on series connection of several individual IGBTs to form an MMC cell. Devices offering blocking capability beyond 15 kV can reduce the required number of series connected devices and can be advantageous even in terms of losses. Of course, for such high blocking capabilities, even SiC devices have to be plasma-flooded bipolar devices, preferably IGBTs, and have to compensate the 3 V junction voltage by lower series resistance. A simple example shows the potential advantage: a 4.5-kV press-pack IGBT module used for HVDC has an on-state voltage drop of 3.7 V at rated current and 125 °C [60]. A series connection of four such silicon IGBTs could be replaced by an 18-kV SiC IGBT of the same current rating. To be on par with the four series connected silicon IGBTs regarding the conduction losses, the SiC

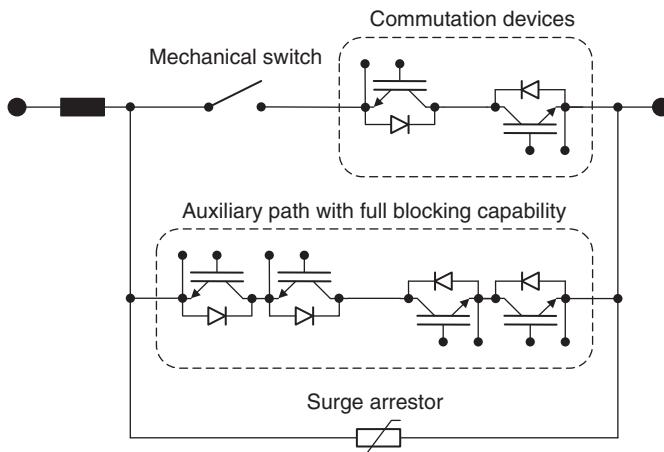
IGBT would need an on-state voltage of less than  $4 \times 3.7\text{ V} = 14.8\text{ V}$ . Simulations of 18-kV SiC IGBTs show that on-state voltages clearly below 10 V are feasible and that the switching losses are still a factor of five lower than with the silicon IGBTs. The effect can be even more pronounced at partial load. Published results, e.g. [61], support these findings. Of course, there are a number of challenges to be solved, like the limited minority carrier lifetime, the low injection efficiency of the substrate material, and especially all kinds of packaging issues, but in total the benefit could be substantial and the higher device cost would then be paid back over time by energy, which is not converted into heat. Thus, HVDC is technically challenging but might become a financially viable, though small, market for SiC devices.

### 15.8.2 HVDC Breakers

While HVDC is still mainly point-to-point transmission, the future will see more and more multiterminal installations and then also meshed HVDC grids. It sounds simple to just connect more terminals to anyway constant DC lines, but every failure of a terminal or a line would immediately lead to a shutdown of the entire system. While this might be acceptable for a point-to-point connection, it is not for a large-scale system. To keep the unaffected parts of the system operational, the affected parts have to be disconnected, before a cascaded shutdown takes place. This requires DC breakers [62], which are able to interrupt the current and support the high voltage – bidirectionally, because the current might flow in either direction and because a ground fault might occur on either side of the breaker.

This sounds an easy task for a mechanical switch, if it was quick enough and could extinguish the arc, but for semiconductor switches with their usually unidirectional operation, it requires workarounds like an anti-serial connection with anti-parallel diodes for the individual switches. Another unusual operation characteristic of the breakers is the rareness of switching events throughout the breakers' entire service live. The breakers stay either turned on or turned off, and thus, the switching losses are of no concern as long as they do not endanger the proper switching operation. The latter is particularly important because the energy dissipated in the breaker is not just its own switching losses but also a part of the energy stored in the DC lines or converters the breaker is trying to disconnect. Usually, the stored energy is much too high to be dissipated in the semiconductors alone and requires a surge arrestor. In other words, the full focus is on the conduction losses of the breaker, and neither silicon nor SiC devices are close to a sufficiently low on-state voltage.

One workaround is the hybrid breaker sketched in Figure 15.9 [63]. Under normal operation, the current is flowing through a fast mechanical switch and a few semiconductor devices. In a breaking event, the semiconductor devices are turned off and the voltage across them increases, while the current is still forced through them by the grid impedance. However, the additional voltage is sufficient to commutate the current into an auxiliary path with many semiconductor switches in series, enough that they can support the overvoltage during turn-off. Once the current has commutated into the auxiliary path, the mechanical switch is opened and interrupts the main path. Then the auxiliary path is carrying the full current and can



**Figure 15.9** Hybrid HVDC breaker according to [63]. Source: Based on Hassanpoor et al. [63].

be turned off without the current commutating back to the main path. When the rising voltage reaches the trigger level of the surge arrestor, the current commutes into the surge arrestor and the remaining energy of the grid impedance is dissipated there. The switching losses of the semiconductor devices are of no concern and the only parameter that matters is the on-state voltage of the semiconductors in the main path. SiC devices could benefit from their lower conduction losses but that is a matter of chip area and cost. The low switching losses of SiC devices are of no advantage at all, and thus, SiC devices do not seem to be of particular benefit for HVDC breakers. Even worse, semiconductor breakers face a strong competition by gas insulated mechanical breakers, which are very compact and much cheaper than semiconductor solutions [62]. Thus, it is at least questionable if semiconductor-based breakers can excel in HVDC, not to mention SiC-based ones.

## 15.9 Drives

### 15.9.1 Industrial Drives

Electric drives cover a wide range of power levels and applications. Low-power applications and home appliances operate at lower voltage and/or current levels. For those applications, silicon or GaN devices usually offer better, in particular cheaper, solutions and SiC devices will not gain a significant market share anytime soon (cf. Figure 15.3). At higher power levels, the situation is more promising for SiC devices. However, the grid side and the motor side have different mission profiles and restrictions, which usually lead to different optimisations and also different perspectives for SiC devices.

At first glance, the situation for the grid side is similar to photovoltaic systems. However, the majority of grid connections of drives are still passive rectifier bridges

or sometimes thyristor based. In those cases, a SiC solution is hardly competitive because silicon rectifiers can have quite a low on-state voltage drop and switching is not relevant. In case of an active grid connection using active components, the power factor can be controlled, the harmonics content can be limited, and a reversal of the energy flow is enabled, such that energy can be transferred back from the DC-link to the grid. Like in case of the photovoltaic inverter, the main benefits of the SiC components for those active grid connections are reduced conduction losses and smaller passives due to higher switching frequency. The smaller passives are the main line choke and the DC-link capacitor. For the grid connection, a lower inductance value is sufficient and the choke tends to be smaller in volume and cheaper. However, the choke requires a good high-frequency performance, i.e. a low parasitic capacitance for good EMI performance and a core material with low losses as well as a good cooling as the harmonics will cause high losses in the choke's core. Both factors will increase the cost again such that the financial gain on the choke is quite limited. With the shorter period in between switching events, also the necessity to store energy in the DC-link is reduced and, thus, the DC-link capacitor could be smaller, too. However, the storage of energy is not necessarily the limiting factor, but ripple currents and the losses they cause at the equivalent series resistor (ESR) of the capacitor are. Like with the choke, a better capacitor (technology) or at least a better cooling or less compact design would be required and limits the potential benefit.

Furthermore, the DC-link capacitor has to fulfill the requirements of the motor side in an analogous way, and reducing the size of the capacitor is subject to also higher switching frequency on the motor side. Unfortunately, increasing the switching frequency on the motor side is not as beneficial as on the grid side because the size of the motor is rather given by mechanical restrictions, while the high switching frequency will change the composition of nonideal currents and losses in the motor in a nonlinear way. Furthermore, the high voltage transients required to keep the switching losses low increase capacitive currents in the motor and towards ground, which do not just increase losses but can be even dangerous for the motor because part of the current can flow over the bearings, which might degrade over time. The steep voltage transients, sometimes even aggravated by travelling wave phenomena on the cable and resulting over voltage peaks, might also degrade the insulation of the windings, eventually causing a complete breakdown. However, the capacitance of the motor cable is a natural filter element damping the voltage transient. Unfortunately, the capacitance also increases the switching losses of the SiC components and might require their own damping elements – with additional losses in those elements but lower losses in the motor. At the end, the exact design is a complex optimisation and requires special attention in each case [64]. Although electrical drives might already profit from reduced switching losses of the SiC components even when they are not switching faster than IGBTs, it requires progress on the motor, its connection, and on the main line choke to fully exploit the advantages of the SiC components. In fact, the situation is even more demanding because further components inside the converter have to be optimised, namely, the gate drivers, which have to be capable of controlling the fast switching events without causing overshoots and

preventing short circuit events and the overall parasitics of the circuitry [65]. In other words, SiC has a potential for drives but it comes at significant cost, and at lower voltages ( $<1000\text{ V}$ ), again silicon or GaN [66] might offer even better (integrated) solutions.

Of course, the situation is again completely different when going to medium voltage drives and applying the MMC principle. In case the output frequency is high like in [67], the higher switching frequency achievable by SiC components without deteriorating the overall efficiency of the converter can reduce the cell-capacitor and the total volume of the MMC as well as the total harmonic distortion. However, even though SiC components can improve the converter in such particular applications, it is questionable if that could be a (financially) viable solution and the efficiency is already high with silicon components.

### 15.9.2 Wind Energy

In general, converters for wind turbines are not much different from high-voltage industrial converters and as a first approximation it does not matter, if they are converters for doubly-fed induction generators, for multipole generators without a gear box or just full-scale converters. Consequently, most of the considerations above hold true for wind turbine converters, too, and weight and size are an argument for the generator side converters in the nacelle only, although the converter is usually not a major fraction of the weight. For those generator side converters, the same restrictions imposed by the generator apply like in case of the motor side converters of drives. Given the low speed of the generators, high switching frequency is of less advantage and the main benefit would be lower conduction losses, especially under partial load conditions. However, this would require SiC MOSFETs with a large total chip area and would increase cost substantially.

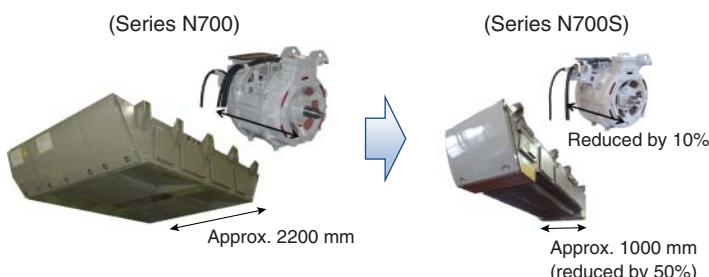
If the switching frequency of the generator side converter remains low, the DC-link capacitor cannot be shrunk and the only benefit from higher switching frequency of the grid side converter would be a smaller main line choke. However, the higher switching frequency would again require a good high-frequency performance, i.e. low parasitics and an advanced core material, and that would mostly cancel the financial advantage.

After all, higher switching frequency is of less benefit and the main advantage for wind power converters would be higher efficiency, originating from lower conduction losses and much lower switching losses of the SiC components. Especially if going up in blocking capability and reducing complexity of the converter SiC devices could excel, then maybe even as SiC IGBTs [68]. For the time being, the cost of SiC components is still too high to justify their application [69], and, consequently, there is no market penetration yet and not expected anytime soon. However, the situation changes if the wind turbines are not coupled to an AC grid but to a (local) DC grid with consecutive DC transmission, e.g. in case of a remote off-shore wind farm. This would require DC/DC converters, and here SiC devices might have an edge, in particular, if the DC-voltage level is much higher than 10 kV.

### 15.9.3 Traction

Like many other mobile applications, traction profits not only from a better efficiency of the converters equipped with SiC components but also from the smaller size and the lower weight of those converters. The most prominent example is the Japanese Shinkansen bullet train series N700S [70], which uses 1500 A, 3.3-kV SiC MOSFETs and started regular service in July 2020 – in time for the original schedule of the Olympics in Tokyo, just like the first Shinkansen did for the 1964 Olympics. Besides these advertising aspects, the SiC deployed for this application offers indeed several advantages. Based on the mission profile of a 515-km ride from Tokyo to Shin-Osaka, the losses of the converter were 30% lower than with the conventional solution. This result is particularly impressive because hybrid modules were used, i.e. still silicon IGBTs, but already SiC Schottky diodes. Due to the lower losses, the cooling could be reduced from forced air cooling to train draft cooling, which reduces the size of the converter considerably by omitting the fan and the air channels. Together with other improvements, the converter is only half the size of the original one (Figure 15.10) and has 30% less weight. This way, the converter fits underfloor of the carriage that carries the main transformer already, while previously the converter for the transformer carriage had to go into a neighbouring carriage causing additional wiring.

While the Shinkansen is cruising most of the time beyond  $200 \text{ km h}^{-1}$  [70] and, thus, profits from the better efficiency in partial load, similar results have been reported for light rail applications with their cruise-stop-idle-go-again mission profile. Using also hybrid modules for urban trains [71] yielded 35% reduced losses (+4% efficiency), 32% reduced volume, and 25% reduced weight, and using full SiC modules for a metro [72] yielded 51% reduced volume and 22% reduced weight as well as 63% reduced temperature increase over ambient, i.e. losses. Those are only first steps into SiC technology, and even larger improvements are expected while progressing on the learning curve. Together, with the longevity of rolling stock, the payback of higher efficiency over that period and, consequently, the willingness of train operators to invest into future-proof technology, this field of application is obviously one of the most promising for SiC devices. Due to the additional impact on the range or the storage size, the advantage is even larger in case of offline systems like diesel-electric, battery, or fuel cell trains and also off-road vehicles.



**Figure 15.10** Traction converter and motor of a Shinkansen N700 and their improvement due to the application of full SiC semiconductor devices (N700S). Source: Sato et al. [70].

## 15.10 Conclusions

After almost 20 years of commercialisation and almost 10 years of the MOSFET being available, SiC technology is on the one hand well established, but on the other hand also still rapidly developing. The economic progress is documented by large-scale investments [73] as well as extensive cooperation and supply agreements, e.g. [74], and drives the economy of scale. The resulting cost reduction of SiC devices makes additional applications economically viable for SiC and increases the market even further. This way, SiC has moved out of the hen-and-egg situation and out of the high-end niche markets into the main stream.

Technologically, the progress goes into several directions. Lower channel resistance allows to produce competitive low-voltage devices, in particular in the 650-V class, targeting an even bigger market, including EVs/hybrid electric vehicles (HEVs) and challenging silicon SJ MOSFETs and GaN HEMTs. On the other end of the voltage range, better material and processes enable higher blocking capability, which in turn provides SiC with an advantage over IGBTs and thyristor-based solutions in heavy traction, induction heating, or HVDC applications. Another direction of progress is the packaging. Initially, the TO-247 was good enough to start the business with a known footprint, but to fully exploit the advantages of the material beyond lower on-resistance, i.e. extremely fast switching and high temperature capability, low parasitic and temperature stable packages are required and progressively available. Furthermore, hybrid integration as well as higher voltage and higher currents are required to serve additional markets. With half-bridges of 6.5 kV and/or 1 kA, such devices are in sight already and just a matter of actually producing them. Finally and after some teething troubles, SiC is building up a track record of good reliability. This is a prerequisite for availability sensitive applications like automotive and, even more, aerospace, which already started to use SiC devices.

Thus, SiC is targeting an ever-growing range of applications. On the one hand, only very few of those applications would be unfeasible without the advantages of SiC devices. On the other hand, SiC devices are not yet a general replacement of silicon devices either, although SiC can beat silicon in more and more applications as the cost is coming down and by gaining system advantages. At the end, it is a case-to-case decision to use SiC devices, while silicon is improving as well and GaN shows an even more dynamic development, establishing a strong and for some applications even superior competition. And the decision to take is not necessarily an either or one. Like the examples in DC/DC converters and photovoltaic show, the optimum might be a mixed assembly, with e.g. silicon for high-current switches and SiC for high-frequency ones. Furthermore, the combination of silicon and SiC chips into one switch might be advantageous – at least economically and at least as an intermediate step [75, 76]. In any case, SiC devices have to keep the pace of their technical development, and at the same time, cost has to come down to prevail. As none of the fields of required improvement shows general road blocks, it is just a matter of actually doing it, of smart ideas on the way and of time to implement. SiC is here to stay – and to grow.

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## 16

### Special Focus on HEV and EV Applications: Activities of Automotive Industries Applying SiC Devices for Automotive Applications

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#### 16.1 Background (PDPlus LLC)

The automotive industry is said to undergo a major revolution once every 100 years. In 1876, the world's first steam-powered car was invented, and in 1886, the world's first car with an internal combustion engine, said to have pioneered modern cars, was invented. For more than 100 years since the invention, automotive industries have continued to improve engine performance, and comfortable and high-performance automobiles have been developed and produced. However, during this time, it is also true that negative impacts such as the consumption of fossil fuels, the emission of CO<sub>2</sub>, traffic accidents, and air pollution have increased. Until now, automotive industries have been expanding mainly in developed countries and regions, but it is expected that the number of vehicles will increase in newly developed countries and regions in near future. It is feared that the negative impact will further increase while contributing to the improvement of the quality of life of people in those regions. A new movement in automotive industry is CASE (connected cars, autonomous driving, sharing, and electrification). Among them, electrification is an activity that aims to introduce electric power to the power section and dramatically reduce fuel consumption, that is, CO<sub>2</sub> emissions. Until now, mainly hybrid electric vehicles (HEVs) have been prevalent in markets, but in the future, plug-in hybrid electric vehicles (PHEVs) and electric vehicles (EVs),

which are expected to reduce CO<sub>2</sub> emissions drastically, are expected to expand rapidly, and another type of zero-emission vehicle of fuel cell vehicles (FCVs) development and dissemination have begun.

Global vehicle production in 2017 was 91 million. However, the ratio of electrified vehicles was only 4%. To realize the below 2 °C scenario agreed at COP21, more than half of the expected production of 130 million vehicles in 2040 will be required to be electrified vehicles [1]. On the other hand, many economic analysts expect an electric vehicle ratio of 7–16% in 2030 [2]. Although there is a big gap between expectation and forecast, at least it is expected that the ratio of electrified vehicles will rapidly increase in the future.

For the further spread of electrified vehicles, it is required to improve the efficiency of electric power train components and to reduce the size, weight, and price of them. At present, Si power devices such as insulated-gate bipolar transistors (IGBTs) and PIN diodes are mainly used for electric power components in electrified vehicles. By replacing these Si power devices with silicon carbide (SiC) power devices, it becomes possible to satisfy these technical requirements. As a result, the performance of the power train is improved and the appeal of the electrified vehicles is increased. It is thought that SiC power devices will be able to contribute to the further spread of electrified vehicles.

At first, the efficiency improvement by introduction of SiC power devices in actual vehicles was evaluated for HEVs, and after that, SiC power devices were firstly introduced in FCVs as the mass-produced vehicle applications and mounted on a mass-produced EV motor inverter. Expectations are growing for big volume introduction of SiC power devices on vehicles now. On the other hand, despite the advantages of introducing SiC power devices on vehicles are great and clear and application of SiC power devices to vehicles has expected for the long term, SiC power devices have not spread into automotive applications so far. The main reason is that SiC power device cost is extremely high compared to Si power devices. In order to introduce SiC into electric vehicles, which are expected to explode in the near future, it is necessary to put further effort on the development of applications suitable for SiC, as well as the study of packaging technology and application technology to fully exploit the performance of SiC power semiconductors. These activities will contribute to reduce the total cost by downsizing the device by improving the performance and reducing the loss.

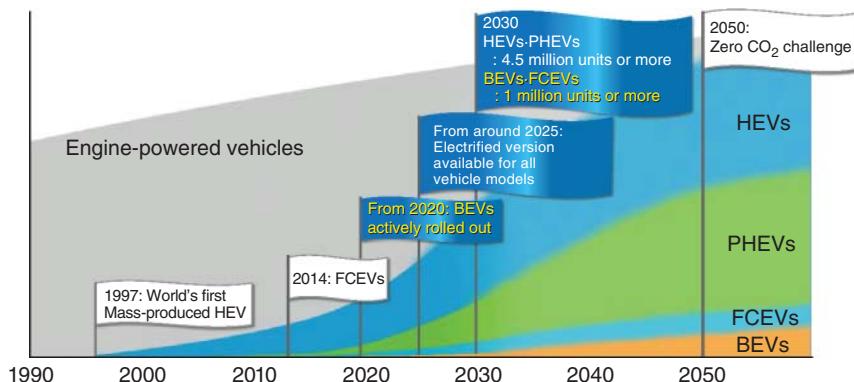
In this chapter, the very important five topics for automotive applications of SiC power devices are shown. The topics are “the challenge of SiC power devices introductions on prototype HEVs and FCVs”, “Introduction of Boost Converter Using SiC Semiconductor for New FCV Drive”, “development of module technologies to bring out SiC power device performances”, “SiC-MOSFET switching characteristics and gate driver circuits for automotive application”, and “R&D of SiC Power Devices for Automotive Applications”.

## 16.2 The Challenge of SiC Power Devices Introductions on Prototype HEVs and FCVs (TOYOTA MOTOR CORPORATION)

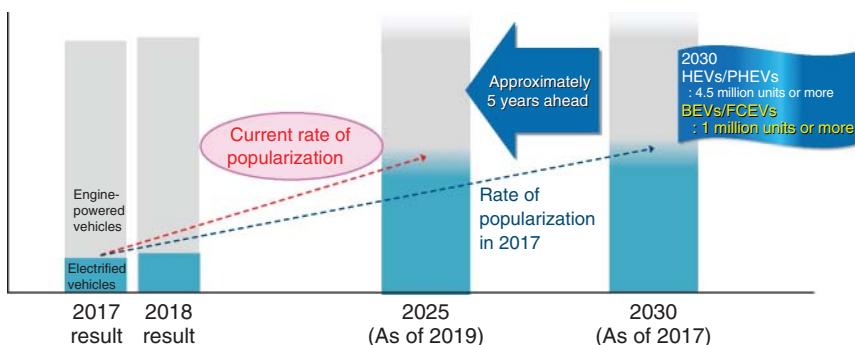
### 16.2.1 Progress of Electrification

With increasing awareness of environmental issues, reducing CO<sub>2</sub> emissions has become a major challenge for automotive industries. Figure 16.1 shows the milestones of Toyota Motor Corporation. It has set a long-term goal of reducing CO<sub>2</sub> emissions from new cars during driving by 90% in 2050 compared to 2010 [3]. As a milestone, it expects its sales of new electrified vehicles to be more than 5.5 million units in 2030, consisting of a combined 4.5 million units or more of HEVs and PHEVs, and a combined 1 million units or more of battery electric vehicles (BEVs) and fuel cell electric vehicles (FCEVs). The progress of electrification has been taken place faster than expected in 2018. In June 2019, Toyota announced that it would reach its forecasted numbers nearly five years earlier (Figure 16.2) [4]. A lot of car manufacturer is planning to launch some BEVs in the first half of the 2020s to meet the growing expectations for BEVs around the world. With the rapid progress of electrification, application of SiC devices is also being studied.

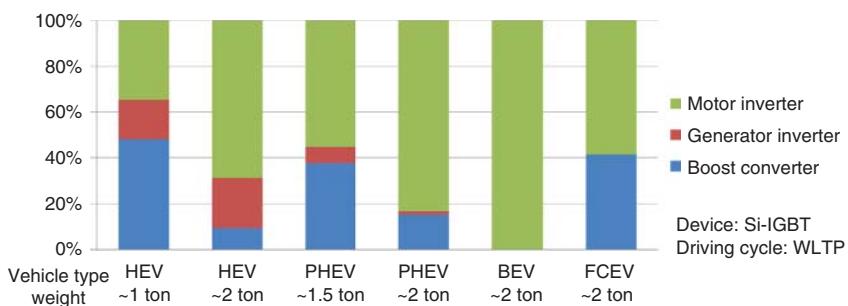
At present, the cost of a SiC device is more than twice as high as that of a Si device, and thus the SiC device is being adopted from more effective applications. Figure 16.3 shows the percentage of electrical energy loss for each type of electrified vehicle and each of the driving inverter, power generation inverter, and boost converter [5]. BEV driving inverters and FCEV boost converters are components that can significantly reduce energy loss. It is expected that the loss can be reduced by 70% or more by replacing Si devices with SiC devices.



**Figure 16.1** Milestones in popularizing electrified vehicles (announced in December 2017).



**Figure 16.2** Rate of popularization of Toyota's electrified vehicles (announced in June 2019).



**Figure 16.3** The ratio of the electrical loss of power control unit (PCU).

A secondary effect of improving fuel efficiency is to reduce the amount of battery installed in the case of BEV and to reduce the FC tank capacity in the case of FCEV. In addition, the FC boost converter that extracts high power from the FC stack has a considerably large volume and thus has a large size reduction effect. The adoption of SiC is determined by comparing the effects of using SiC devices, such as reducing expensive components and the volume, with the increased cost using SiC devices. In autonomous driving, which is being promoted at the same time as electrification, many sensors are used, and as a result, much power is required. As a DC–DC converter for converting to 12 V, 100 A class converter is used at present, but the current capacity is expected to increase rapidly and double.

### 16.2.2 Demonstration of Electrified Vehicles

In 2014, Toyota Motor showed that using SiC devices for inverter and boost converter of Prius, fuel efficiency could be improved by about 10% [6, 7]. Switching loss was measured to be reduced 70–85%. In 2015, we prototyped a CAMRY using

**Figure 16.4** SORA: Tokyo  
Toei FC bus.



**Figure 16.5** Heavy-duty FC trucks @LA Port.

SiC-metal–oxide–semiconductor field-effect transistor (MOSFET) and SiC-Schottky barrier diode (SBD) for inverters and a boost converter. All-SiC CAMRY can run on public roads and measured the effect of improving fuel economy on public roads [8]. Improvement of efficiency by applying SiC diodes to FC bus boost converters was also studied. By changing the diode to SiC-SBD, the efficiency was improved by 0.5% [9]. At present, FC buses are used on routes on the Toei Bus from Tokyo Station to Big Sight (Figure 16.4). At the Tokyo Olympics in 2020, many FC buses will be introduced and used for personnel transport.

In the fall of 2017, using this FC system, a demonstration was started to reduce CO<sub>2</sub> by changing the trailer truck at Los Angeles Port to an FC truck [10]. Two FC stacks used by Mirai were used, and a 670-horsepower driving system was prepared to electrify the trailer truck. The initial mileage for one charge was 320 km, but in 2018, by increasing the number of hydrogen tanks from four to six, it was possible to drive 480 km (300 miles) with one hydrogen charge (Figure 16.5). As described above, various demonstrations have been performed since about 2015, and preparations for using SiC devices on electrified vehicles in earnest are being made.

## 16.3 Introduction of Boost Converter Using SiC Semiconductor for New FCV Drive (HONDA MOTOR CO., LTD.)

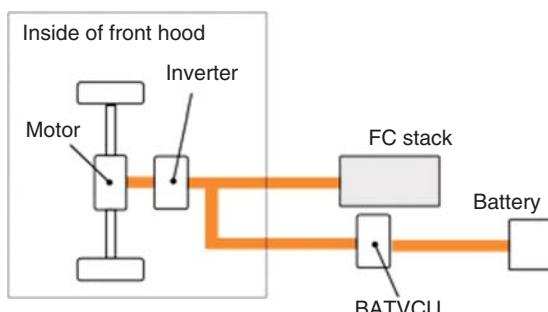
### 16.3.1 Introduction

In order to expand the use of FCVs that run on energy generated from hydrogen inside the vehicle, it is necessary to develop a convenient vehicle with a package that is the same as conventional internal combustion engine vehicles. In order to achieve this, further reduction in the size of the electric power train including the fuel cell (FC) stack is needed. To reduce the number of cells in the FC stack while still increasing the output of the traction motor, it is necessary to increase the voltage that is supplied from the FC stack to the traction motor. For this purpose, Honda has developed a large-output fuel cell voltage-boosting converter (fuel cell voltage control unit, hereafter referred to as “FCVCU”) was developed that boosts the output voltage of the FC stack. Here, we will describe the circuit technology and structure of the voltage-boosting converter that was adopted to achieve reductions in size and weight.

### 16.3.2 Configuration of the Electric Power Plant System for New FCV

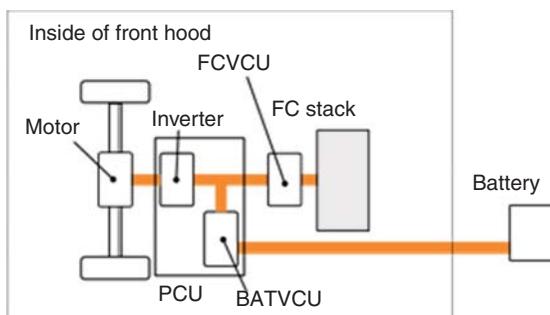
In the earlier 2009 model, the FC stack was positioned in the center tunnel in order to achieve a sedan package with low floor, low center of gravity, and low overall height [11]. However, the maximum occupancy was four persons. With the new model FCV, the FC stack and surrounding systems are more compact and are positioned together with the electric power train inside the front hood. This results in a roomy interior space that can seat five adults. The FCVCU provides large output while also adopting a thin, compact design that contributes to the layout. With the 2009 model, only the inverter and motor were mounted in the front motor room (Figure 16.6). However, in the new model FCV, the layout mounts all of the following components inside the front hood (Figure 16.7).

- FC stack
- Fuel cell voltage-boosting converter (FCVCU)
- Traction motor
- Inverter
- Battery voltage-boosting converter (BATVCU)



**Figure 16.6** Conventional electric power plant (2009 model FCV).

**Figure 16.7** New FCV electric power plant.



In the electric power plant system, the output voltage from the FC stack is boosted by the FCVCU and supplied to the traction motor inverter. This made it possible to achieve higher motor output and reduce the number of FC stack cells, creating a vehicle system that is compact and lighter weight.

### 16.3.3 FCVCU

In the 2009 model, the FC stack output section was connected directly to the traction motor inverter. In the new model FCV, the number of FC stack cells has been reduced by approximately 30% compared to the 2009 model. This results in lower FC stack output; however, the voltage boost provided by the FCVCU increases the inverter drive voltage to a maximum of 500 V. This achieves higher maximum motor output, which was increased from 100 to 130 kW (Table 16.1).

#### 16.3.3.1 Circuit Configuration

Figure 16.8 shows the FCVCU circuit diagram. The primary components are the intelligent power module (IPM), reactor, and smoothing capacitor. It also contains a 4-phase interleave circuit consisting of four single-phase chopper circuits in parallel [12]. The IPM is a full SiC-IPM composed of SiC-SBD and SiC-field-effect transistor (FET) next-generation power semiconductors, and the voltage control unit (VCU) achieves high efficiency through smaller passive component sizes and reduced loss achieved by increasing the frequency to above the audible range. Further reduction in size was achieved by adopting a 2-phase magnetic coupling reactor composed of a 2-phase reactor with a single core [13]. The secondary-side smoothing capacitor uses an indirect water cooling structure in consideration for generated heat (Table 16.2).

#### 16.3.3.2 Full SiC-IPM

With Si, IGBT and other minority carriers were primarily used in order to improve the increase in on-resistance resulting from higher withstand voltages. However, these components suffered from the problem of large switching losses, and as a result there were limits on high-frequency drive due to the generated heat. The FCVCU uses a full SiC-IPM as well as a high-speed device structure with SiC-SBD and SiC-FET majority carrier devices. This results in lower loss compared with the Si-IGBT and Si-FWD that were used in previous models (Figure 16.9). In particular, the large reduction in switching loss makes higher frequencies possible (Figure 16.10).

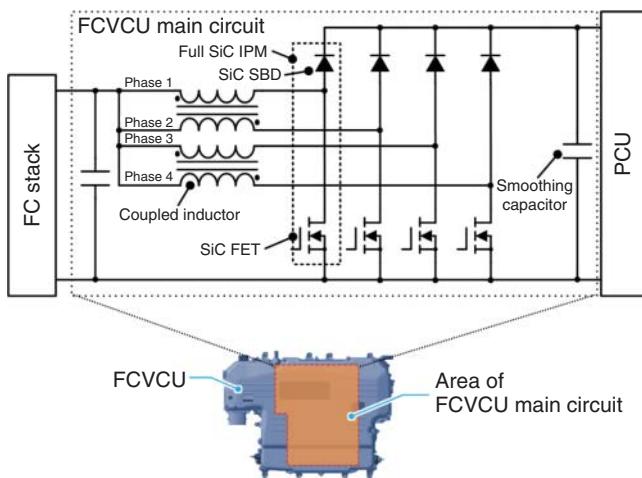
**Table 16.1** Major specifications.

Model	New FCV	2009 model
Length/width/height	4915 × 1875 × 1480 mm	4845 × 1845 × 1470 mm
Wheel base	2750 mm	2800 mm
Vehicle weight	1890 kg	1630 kg
Number of passengers	5	4
Maximum motor power	130 kW (177 PS)	100 kW (136 PS)
Maximum motor torque	300 Nm (30.6 kgm)	256 Nm (26.1 kgm)
Fuel cell stack	PEFC <sup>a)</sup>	PEFC <sup>a)</sup>
Power assist	Li-ion battery	Li-ion battery
Hydrogen supply system	High-pressure hydrogen tank	High-pressure hydrogen tank
Hydrogen filling pressure	70 MPa	35 MPa
Hydrogen storage volume	141 l	171 l
Driving range	750 km <sup>b)</sup>	620 km <sup>c)</sup>

a) Polymer electrolyte fuel cell.

b) JC08 mode.

c) 10/15 mode.

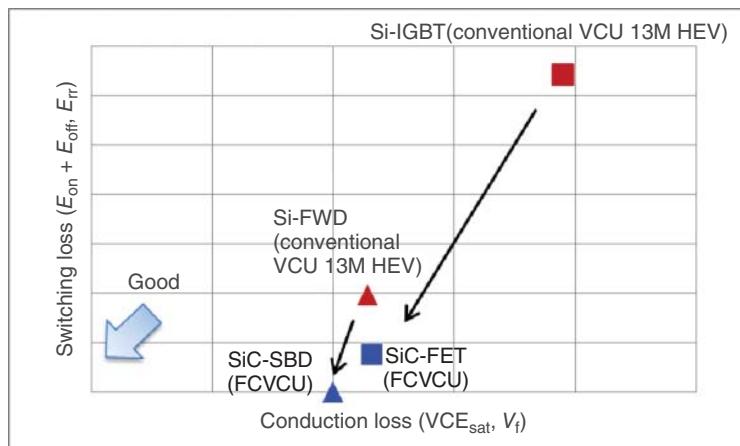
**Figure 16.8** FCVCU circuit.

### 16.3.3.3 Magnetic Coupling and Interleave Operation

A 2-phase magnetic coupling reactor is used, with Phase 1 and Phase 2 constituting one pair, and Phase 3 and Phase 4 constituting the other. The use of two reactors produces a 4-phase configuration. Each phase wraps a single core with two coils, reducing DC magnetic flux by applying current so that the magnetic fluxes generated by DC current in the core are oriented in opposite directions to each other. Displacing

**Table 16.2** Specifications of FCVCU.

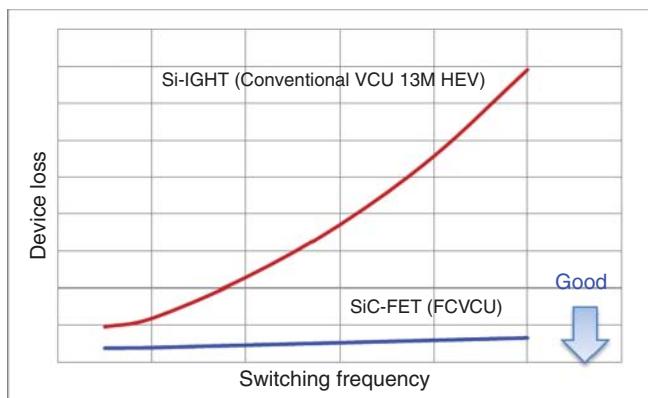
Item	Specification
Max output power	100 kW
Max boost voltage	500 V
Volume	15.8 l
	*FCVCU main circuit
Circuit system	4-phase interleave
Power module	Full SiC
Inductor	2-phase magnetic coupling
Capacitor	Indirect water cooling

**Figure 16.9** Power loss in semiconductor device.

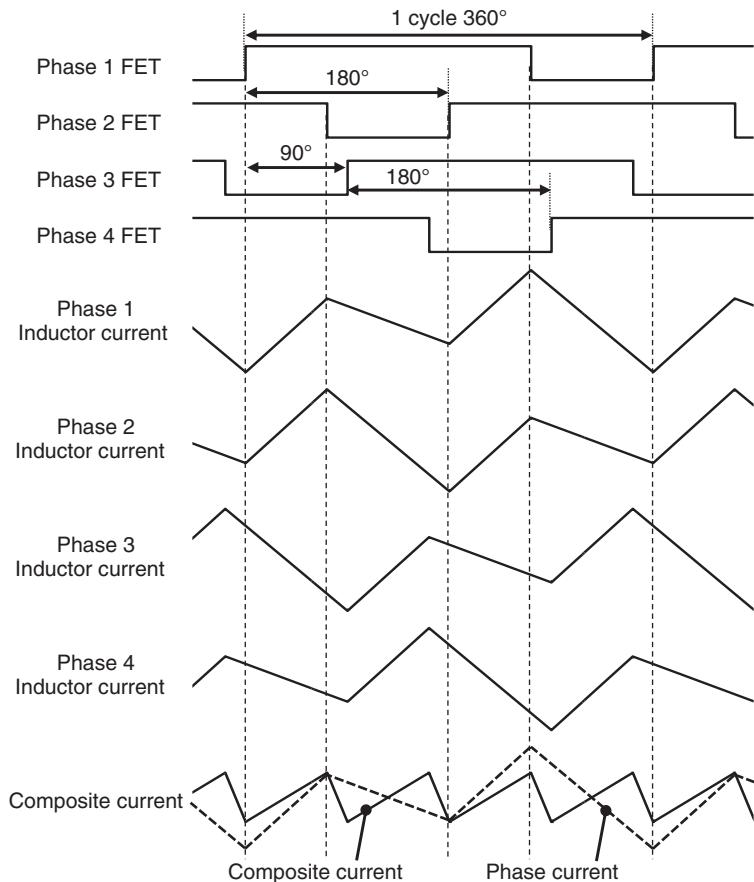
the switching timing of the coupled phases by  $180^\circ$  also reduces the AC component. The effects of the former allow a smaller reactor size, and the effects of the latter causes the ripple currents of the 4-phase reactor to cancel each other out, allowing a smaller smoothing capacitor. Figure 16.11 shows the switching waveform and phase current waveform for each phase in the 4-phase interleave circuit. The phases that operate displaced by  $90^\circ$  from each other in the following order: Phase 1 → Phase 3 → Phase 2 → Phase 4. This causes the ripple currents generated by each phase to cancel each other out, reducing the composite ripple of the four phases.

#### 16.3.3.4 Control Methods

In order to perform a high-efficiency voltage conversion with a multiphase converter, it is preferable to switch the number of operating phases according to the operating conditions. Where to set the points for switching the number of operating phases is related to the FCVCU input voltage, output voltage, and input current. The FCVCU

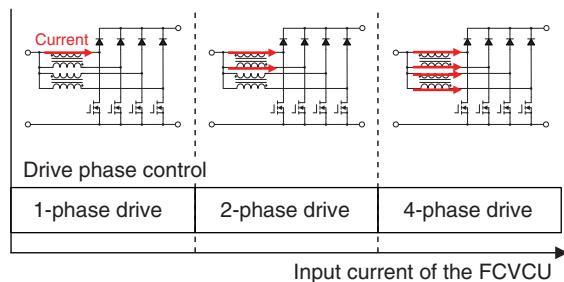


**Figure 16.10** Switching loss in semiconductor device.

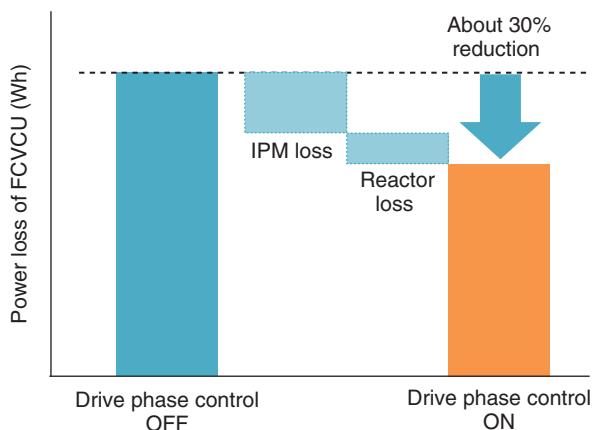


**Figure 16.11** Switching waveform.

**Figure 16.12** Image of drive phase control.



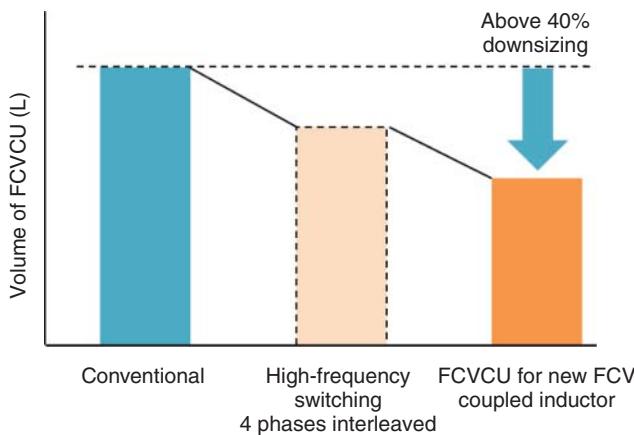
**Figure 16.13** Effects of drive phase control.



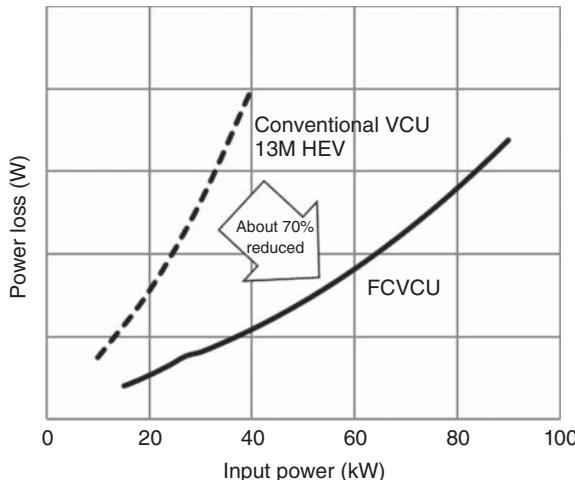
sets a number of operating phases that is suitable for the above three parameters in advance and performs control that switches the number of operating phases based on the input current value. By setting switching points in this way, it is possible to achieve efficient control while using only the current as the monitoring parameter. However, 3-phase operation is not performed with this control. As described above, the reactor is a 2-phase magnetic coupling reactor and it is necessary to apply equal current to the two coupled phases. For example, if phase switching control operated at three phases (Phase 1 to Phase 3), because no current would be applied to Phase 4 that is coupled to Phase 3, the effects of the magnetic coupling would be lost and the Phase 3 ripple current would increase compared to Phase 1 and Phase 2. As a result, if operation continues with three phases, Phase 3 will generate an increasing amount of heat. In order to avoid this, the control that switches the number of operating phases selects 1-phase, 2-phase, or 4-phase operation and does not perform 3-phase operation, (Figures 16.12 and 16.13).

#### 16.3.3.5 Effects on Smaller Size and Higher Efficiency

Figure 16.14 shows the effects on downsizing the FCVCU. The use of full SiC-IPM, a magnetic coupling reactor, and cooled capacitors achieves an overall FCVCU size that is approximately 40% smaller than previous technologies. Figure 16.15 shows the effects on increased FCVCU efficiency. For the same output, loss is reduced by approximately 70% compared to the HEV (13M HEV) VCU in the previous 2013 model, achieving both smaller size and higher efficiency [14].



**Figure 16.14** Downsizing effect on FCVCU.



**Figure 16.15** Power loss comparison with conventional VCU.

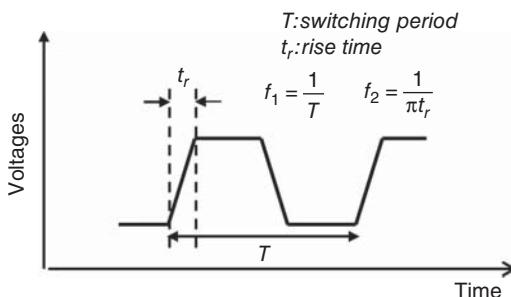
#### 16.3.3.6 Quietness

Ordinarily, the inverter and converter in an electric vehicle are driven at a switching frequency that is within the audible range (generally 20 Hz to 20 kHz), and measures are needed to counter the high-frequency noise that is generated by the reactor and capacitors. Because the FCVCU uses a SiC-IPM, it is capable of driving at higher frequencies than before. Driving the inverter and converter at frequencies higher than 20 kHz produces drive noise that is inaudible to human beings and contributes to improving vehicle quietness.

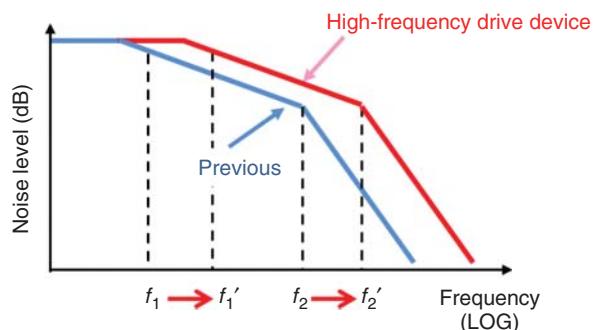
#### 16.3.3.7 Noise Countermeasures

In order to ensure voltage boost operation, switching operation in the chopper circuit is used to produce a drive voltage waveform that has a trapezoidal wave with prescribed, limited rise time  $t_r$  (Figure 16.16). The use of SiC makes it possible to set higher switching frequencies than conventional Si, shortening the transition

**Figure 16.16** Schematic of voltage waveform resulting from voltage boost.



**Figure 16.17** Change in higher harmonic trapezoidal wave resulting from high-frequency drive.



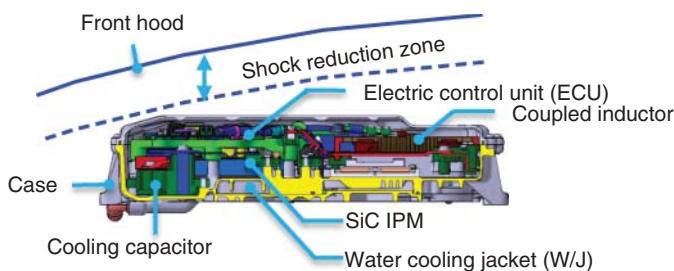
**Figure 16.18** High-voltage cable layout of FC stack and FCVCU.



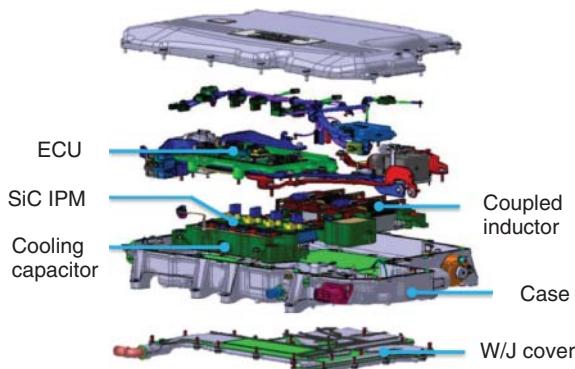
time ( $t_r$ ) resulting from the higher switching frequencies. As a result, the noise level is as shown in Figure 16.17, and the frequency of the generated noise is higher. Because the FC stack uses a structure in which there are electric output terminals on both sides of the stack, the output terminal positive and negative electrodes are largely separated. From a noise perspective, this increases the size of the current loop on the power input side and tends to increase the noise that is radiated from it (Figure 16.18). Therefore in this development, we placed a Y capacitor (ground capacitor) on the FCVCU high-voltage primary side (FC stack side) as a noise countermeasure. The electrostatic capacitance of the Y capacitor was set to a lower value than previous models in order to counter high-frequency noise.

#### 16.3.3.8 Structure of the FCVCU

By placing the FCVCU on top of the FC stack, it is possible to ensure the same bottom surface area as the FC stack. However in terms of height, it is necessary to place the FCVCU in a position that secures the necessary clearance from the front hood in order to satisfy the requirements for pedestrian collision protection performance. This means that the components must be positioned below this position, and it was therefore decided to create a thin design. Figure 16.19 shows the cross



**Figure 16.19** Cross section of FCVCU.



**Figure 16.20** FCVCU components.

section of the FCVCU. Figure 16.20 shows an exploded view of the FCVCU components. In order to reduce the FCVCU height, a thin design and parallel layout are used for the 4-phase reactor with 2-phase magnetic coupling. The 4-phase SiC-IPM is mounted next to the reactor, and furthermore the secondary-side smoothing capacitor is mounted next to the 4-phase SiC-IPM so that they are positioned on the same horizontal plane within the VCU case. In addition, the size and the position of the electric control unit (ECU) were adjusted so that it could be placed below the target line which traces the front hood.

#### 16.3.4 Conclusions

The following two approaches were used to achieve reduced size during the development of the FCVCU for the new model FCV.

- (1) The high-frequency drive using a SiC-IPM and the 4-phase interleave circuit resulted in smaller capacitors and reactor.
- (2) The reactor was further downsized through the use of 2-phase magnetic coupling.

As a result, this reduced the size of the fuel cell voltage-boost converter and enabled us to achieve the objective of installing the FCVCU on the FC stack inside the vehicle front hood. This also achieved high output of 100 kW and volume of 15.8 l. The higher output and technologies for a more compact, thinner design of

this FCVCU contributed to improving the drive performance, fuel economy, and product appeal of the new model FCV.

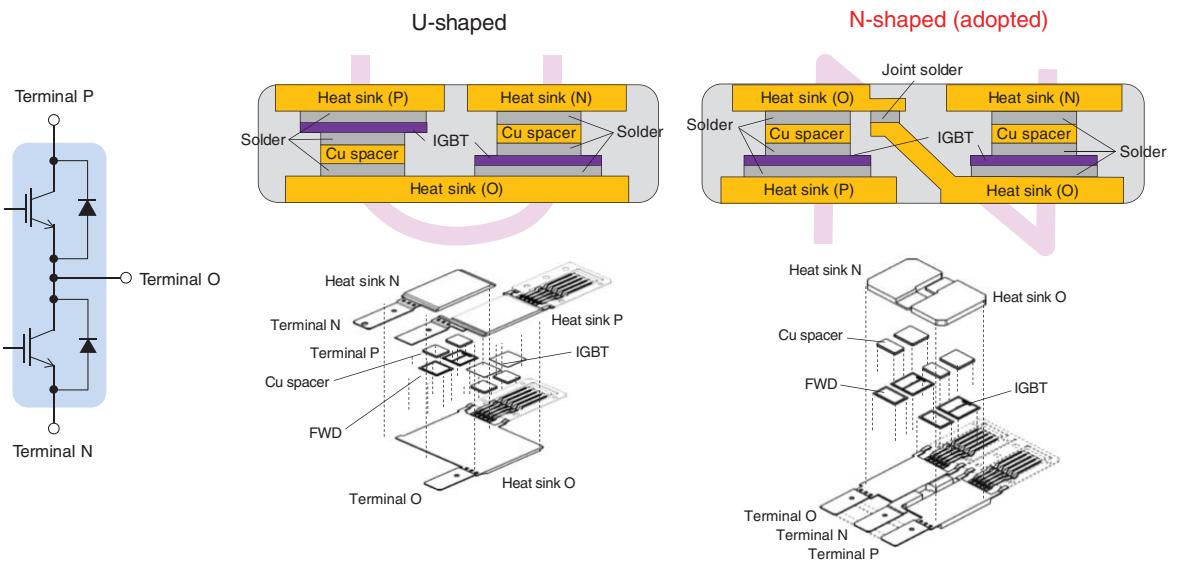
## 16.4 Development of Module Technologies to Bring Out SiC Power Device Performances (TOYOTA MOTOR CORPORATION)

### 16.4.1 Power Card Structure for Double-Side Cooling Technology

To take full advantage of the inherent high-frequency switching of SiC devices and the ability to use them at 200 °C or higher temperature, new technologies are required for mounting. For example, in a module, a parasitic inductance and a parasitic capacitance should be small so that the characteristics can be utilized, and a highly reliable configuration at a high temperature is required. The current fourth-generation Prius uses a 2-in-1 power card, realizing a compact, high-heat dissipation inverter [15]. In this power card, the upper-arm IGBT and diode and the lower-arm IGBT and diode are contained in one card. Initially, we examined the U-shaped structure shown on the upper left side of Figure 16.21, which has a simple structure. However, it was found that the placement of the chips on the left side and the right side upside down, making soldering difficult. Therefore, as shown in the upper right of Figure 16.21, an N-type structure was adopted, in which the chips could be arranged in the same direction. The N-type requires a joint to connect the left and right, but the soldering process is the same for the left and right chips, making it easier. In this structure, solder is used for joining; therefore, improvement of high-temperature resistance of resin and solder and reduction of parasitic inductance are key issues.

### 16.4.2 New Transient Liquid Phase Structure for High-Temperature Applications

As for bonding materials, development of new bonding technologies such as silver sintering and transient liquid phase (TLP) bonding is underway [16]. A structure in which an Al sheet with a thickness of about 100 µm is inserted into the TLP layer has been developed. It has become possible to decrease the stress which impacts TLP. Figure 16.22 shows a schematic of TLP bonding process. Sn layer is placed between nickel layers by sputtering or plating. These layers are heated to 300 °C with pressuring of 0.5 MPa. The only Sn layer melts at this temperature. Then, tin and nickel start to diffuse into each other. After the diffusional reaction is completed, Sn layer changes into  $\text{Ni}_3\text{Sn}_4$  intermetallic compound (IMC). The melting point of TLP layer is about 800 °C. This structure has high-temperature resistance. TLP layer is very stiff, so power device was cracked after power cycle test. Lower part of Figure 16.22 shows the countermeasure for this issue. Aluminum sheet was placed between TLP layers as a buffer layer for thermal stress. We call this method TLP-Ai (TLP bonding with aluminum interlayer).



**Figure 16.21** Structure of 2-in-1 power card.

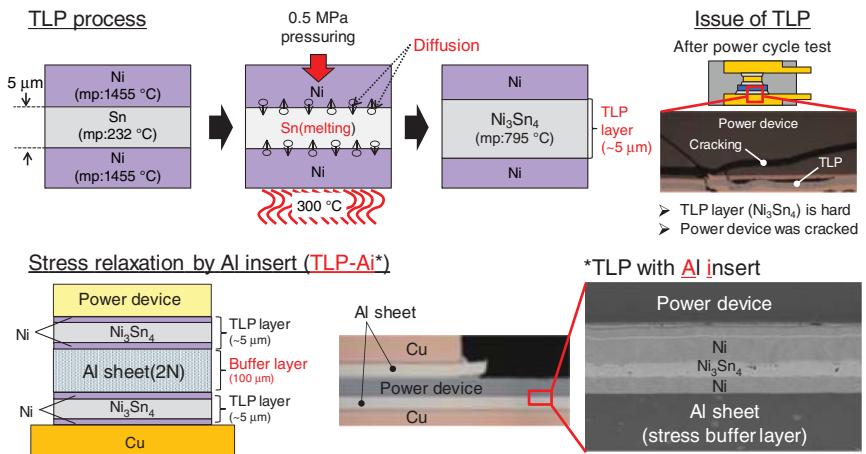


Figure 16.22 TLP bonding for power module.

### 16.4.3 Ni Micro-Plating Bonding

We developed a packaging technology which is called “Ni Micro-Plating Bonding (NMPB)” for SiC power module. That is one of the achievements of Strategic Innovation Promotion Program (SIP: 2014–2019), Japanese National Project. The leader of this project was Professor Tatsumi of Waseda University [17]. The die bonding and the wire bonding can be simultaneously bonded by nickel plating, so that the degree of freedom in designing the module is greatly improved. And also the high-temperature resistance of the bonding is significantly improved. The lead surface was designed to have chevron shape specially for NMPB. Structure of 2-in-1 module in this research and cross-sectional view of chevron-shaped lead frame are shown in Figure 16.23. The strong bonding interface was achieved thanks to this chevron shape. The plating solution was selected for the process of NMPB which has a property of preferentially plating a narrow gap.

Not only the miniaturization of the module is promoted, but also noise reduction is studied, which is a problem when the frequency is increased. And the heat

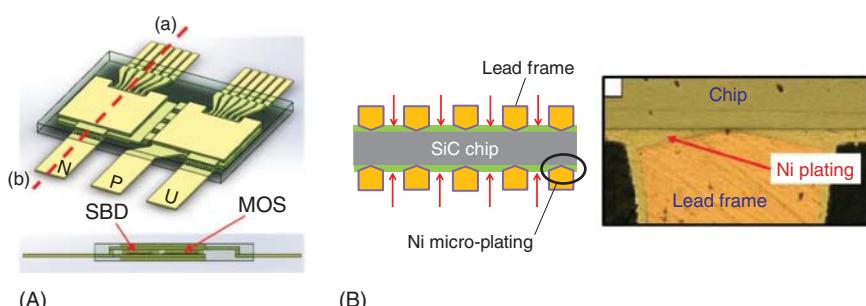
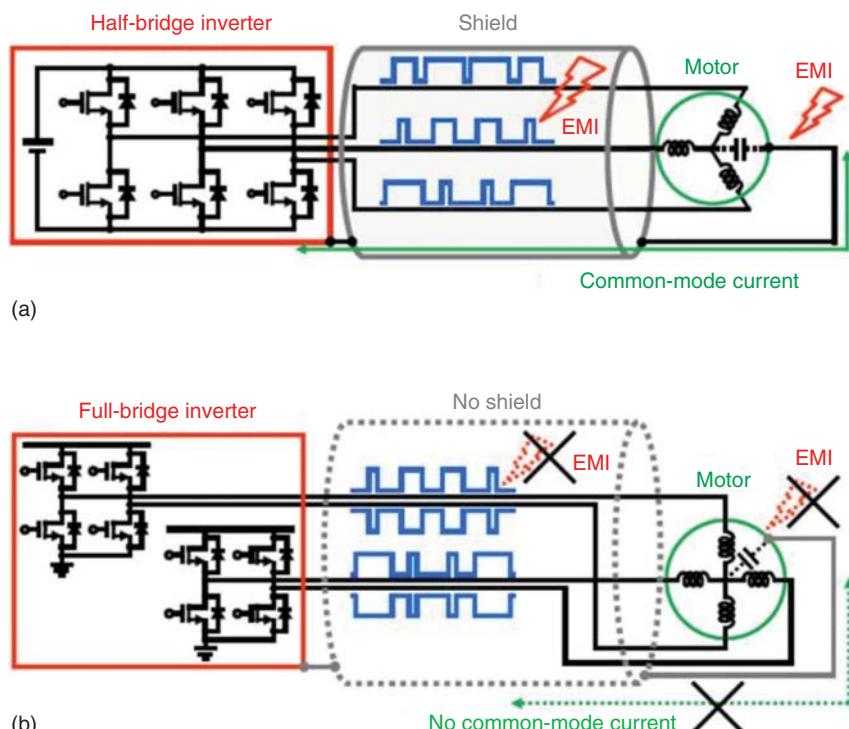


Figure 16.23 Ni micro-plating bonding (NMPB) technology. (A) Structure of 2-in-1 module and (B) cross section of NMPB.

radiation property should be improved because it is reduced due to the miniaturization. For these reasons, it is necessary to review the configuration of the entire inverter instead of simply replacing the Si element with the SiC element. Keio University proposed a circuit configuration to reduce common mode noise [18]. In this study, a full-bridge inverter circuit configuration was proposed (Figure 16.24). The wiring from the inverter to the motor was constructed by pairing cables with currents in completely opposite layers to cancel noise. Since the noise from the wiring is suppressed and the configuration is a full bridge, the noise due to the common mode is theoretically not generated. As a contradiction, there is a cost increase using the chip 4/3 times, but it can be expected that the cost of noise protection can be reduced by noise reduction, so it will not increase significantly. For example, at present, the wiring from the inverter to the motor is covered and shielded with a metal tube, but it is expected that such noise protection will not be necessary or can be simplified. In addition, it has been pointed out that it is necessary to make the characteristics of the paired chips uniform because the switching timing shift due to the variation in the characteristics of the chips is a factor of generating noise.

As the cost reduction of SiC devices progresses, many electric vehicles will use SiC. In addition, by adopting new technologies that can bring out the inherent characteristics of SiC devices, such as module and circuit configuration, the benefits of



**Figure 16.24** Inverter circuits. (a) Conventional half bridge inverter circuit and (b) EMI-less full-bridge inverter circuit.

SiC devices will be even greater. With regard to the electrification of aircraft, which is attracting attention now, the merit of weight reduction is even greater than that of automobiles. So, the merits to apply SiC devices are significantly large compared to automobile.

## 16.5 SiC-MOSFET Switching Characteristics and Gate Driver Circuits for Automotive Application (NISSAN MOTOR CO., LTD.)

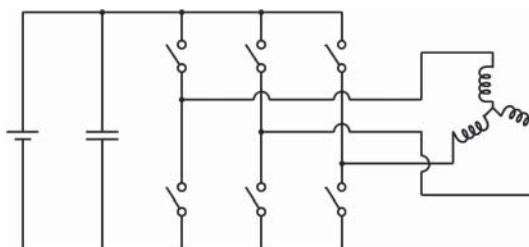
### 16.5.1 Introduction

Since the switching speed of SiC-MOSFETs is faster than that of Si-IGBTs, the former has the potential to provide lower switching loss and higher efficiency. However, high-speed switching of SiC-MOSFETs causes electromagnetic interference (EMI) and voltage and current surges. This section discusses the switching characteristics and gate driver circuits for EV/HEV applications.

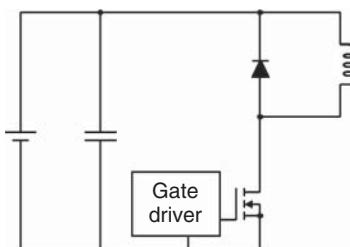
### 16.5.2 Basics of Switching Characteristics

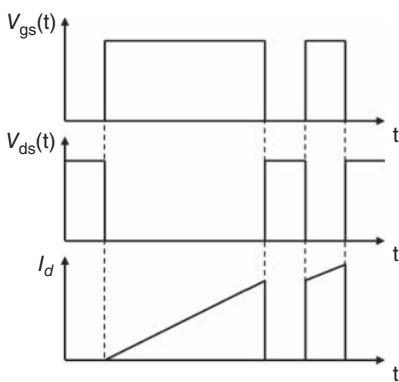
Figure 16.25 shows a 3-phase inverter circuit which has been commonly adopted for the traction inverters used on many of the EVs/HEVs commercialized to date. A double-pulse test circuit like that shown in Figure 16.26 is used to measure the switching characteristics of one phase of 3-phase inverters. The test circuit can measure the switching characteristics of the lower-arm transistor and the recovery characteristics of the upper diode. Schematic waveforms of the gate-source voltage ( $V_{gs}$ ), drain-source voltage ( $V_{ds}$ ), and drain current ( $I_d$ ) of the lower-arm transistor

**Figure 16.25** Three-phase inverter circuit for EVs/HEVs.

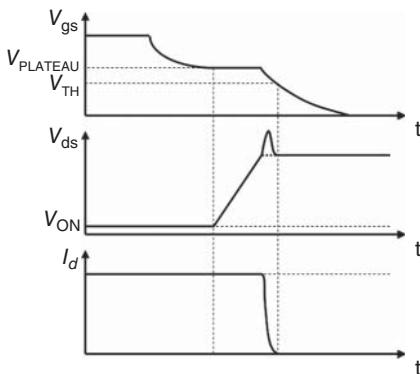


**Figure 16.26** Double-pulse test circuit.





**Figure 16.27** Schematic waveforms in double-pulse test.

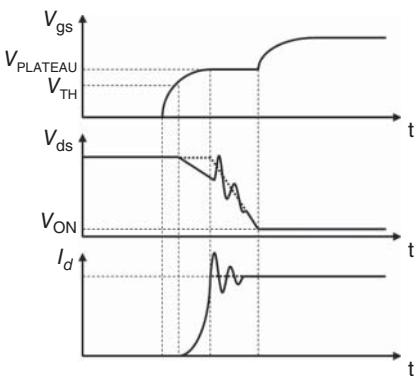


**Figure 16.28** Schematic waveforms of the turn-off characteristics.

obtained in a double-pulse test are shown in Figure 16.27. Turn-off and turn-on characteristics at the required current are measured by turning off and on the transistor at the specified current.

Figures 16.28 and 16.29 show schematic waveforms of the turn-off and turn-on characteristics of  $V_{ds}$ ,  $V_{gs}$ , and  $I_d$ . Parasitic inductance of the power loop consisting of the DC link capacitor, the transistor, and the diode in Figure 16.26 affects the switching waveforms. If the parasitic inductance is ideally zero, the  $V_{ds}$  waveform resembles the dotted line in Figures 16.28 and 16.29. However, since the actual parasitic inductance of the inverter is from several nanohenry to several tens of nanohenry, the  $V_{ds}$  waveform resembles the solid line in the figures. At turn-off, firstly  $V_{ds}$  increases as  $V_{gs}$  decreases. After  $V_{ds}$  becomes the same as the supply voltage, current starts to flow to the diode and  $I_d$  begins to decrease.  $V_{ds}$  increases and excessive voltage is applied to the transistor while  $I_d$  decreases because of  $LdI/dt$ , where  $L$  is the parasitic inductance. At turn-on, firstly  $I_d$  begins to increase as  $V_{gs}$  increases. During the increase in  $I_d$ ,  $V_{ds}$  decreases because of  $LdI/dt$ . After  $I_d$  becomes the same as the load current,  $V_{ds}$  starts to decrease. The reverse recovery current ( $I_{rr}$ ) of the diode is added to  $I_d$ . Subsequently, a sudden change in  $dI/dt$  may cause a voltage surge and current ringing with the resonant circuit formed by the parasitic inductance and the capacitance of the diode.

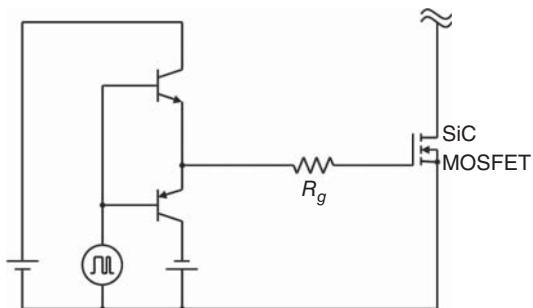
**Figure 16.29** Schematic waveforms of the turn-on characteristics.



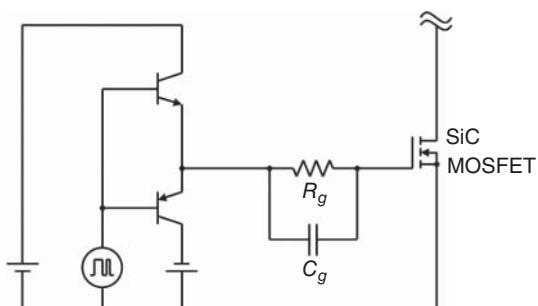
### 16.5.3 Various Gate Driver Circuits

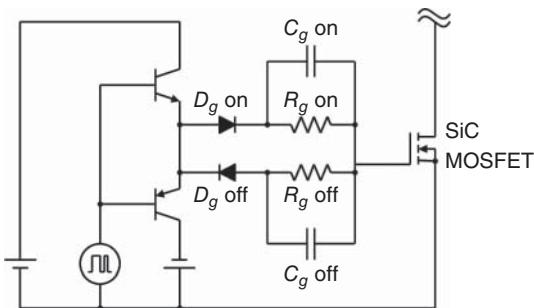
To suppress voltage surge at turn-off and ringing at turn-on, the gate resistance ( $R_g$ ) of the gate driver circuit is sometimes increased. A conventional gate driver circuit is shown in Figure 16.30. The gate current can be limited by increasing the gate resistance. As a result,  $dI/dt$  decreases and voltage surges and ringing can be suppressed. However, increasing the gate resistance leads to a longer switching time and higher switching losses. One proposed way of overcoming this trade-off is to add a speed-up capacitor ( $C_g$ ) connected in parallel to the gate resistance as shown in Figure 16.31 [19, 20]. The speed-up capacitor increases the gate current at the beginning of switching, thereby reducing switching losses. After that, the gate current is reduced gradually to suppress the voltage surge and ringing.

**Figure 16.30** Conventional gate driver circuit.

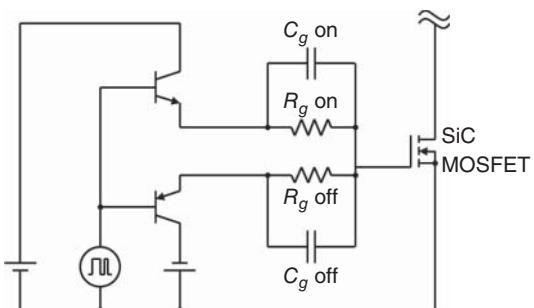


**Figure 16.31** Gate driver circuit with speed-up capacitor.





**Figure 16.32** Gate driver circuit with gate current paths separated by diodes.

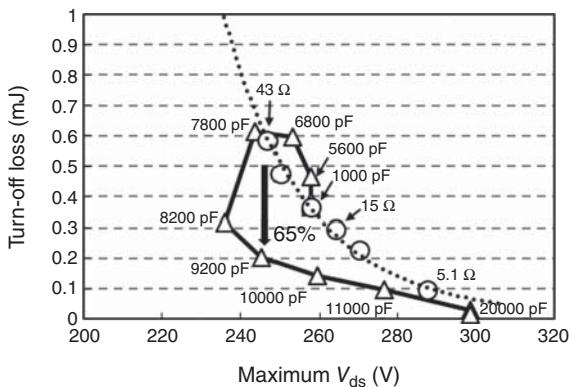


**Figure 16.33** Gate driver circuit with gate current paths separated by output terminals of push-pull transistors.

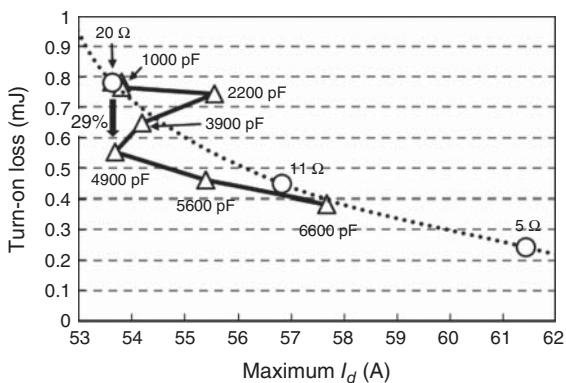
The circuit in Figure 16.32 also has gate current paths for turn-off and turn-on that are separated by diodes ( $D_g$  off and  $D_g$  on), enabling the gate resistances ( $R_g$  off and  $R_g$  on) and speed-up capacitances ( $C_g$  off and  $C_g$  on) to be optimized for turn-off and turn-on. The circuit in Figure 16.33 is proposed for eliciting the high-speed switching potential of SiC-MOSFETs [21]. The output terminals of the push–pull transistors are separated, enabling the gate resistances ( $R_g$  off and  $R_g$  on) and speed-up capacitances ( $C_g$  off and  $C_g$  on) to be optimized for turn-off and turn-on. In addition, the voltage drop at the diodes ( $D_g$  off and  $D_g$  on) can be eliminated and parasitic inductances in the gate current path can be suppressed compared with the circuit in Figure 16.32.

Figures 16.34 and 16.35 present experimental results obtained with the circuit in Figure 16.33 for turn-off and turn-on at  $V_{ds}$  of 200 V and  $I_d$  of 40 A. The relationship between turn-off loss and voltage surge is shown in Figure 16.34. The reference gate driver indicated by the dashed line in Figure 16.34 was adjusted only by  $R_g$  off. The proposed gate driver indicated by the solid line in the figure was adjusted only by  $C_g$  off with fixed  $R_g$  off of 20  $\Omega$ . The results indicate that the proposed gate driver can reduce turn-off loss by 65% at the same level of surge voltage compared with the loss obtained by adjusting only  $R_g$  off of the reference gate driver. The relationship between turn-on loss and current surge is shown in Figure 16.35. The reference gate driver indicated by the dashed line in Figure 16.35 was adjusted only by  $R_g$  on. The proposed gate driver indicated by the solid line in the figure was adjusted only by  $C_g$  on with fixed  $R_g$  on of 20  $\Omega$ . The results indicate that the proposed gate driver can reduce turn-on loss by 29% while maintaining surge current equal to that of the reference gate driver.

**Figure 16.34** Turn-off loss as a function of maximum  $V_{ds}$ .



**Figure 16.35** Turn-on loss as a function of maximum  $I_d$ .



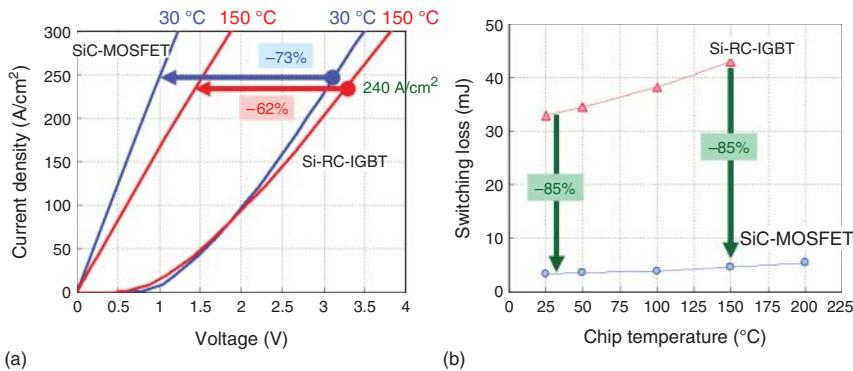
#### 16.5.4 Conclusion

As discussed here, these auxiliary technologies not only enable high-speed switching of SiC-MOSFETs but also solve the issues of EMI and voltage and current surges, which is essential for applying SiC-MOSFETs to EVs/HEVs.

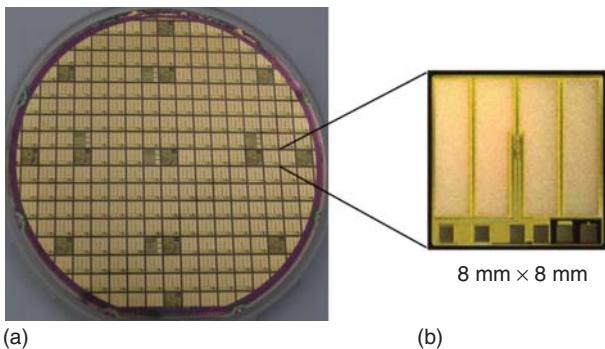
## 16.6 R&D of SiC Power Devices for Automotive Applications (DENSO CORPORATION)

### 16.6.1 Introduction

To prevent global warming, the regulation of CO<sub>2</sub> emissions has become stricter over the past several decades. Therefore, the electrification of automotive power train systems has become a global trend, and the popularization of environmentally friendly vehicles, such as HEVs, PHEVs, and EVs powered via batteries, among others has increased. For next-generation HEVs, PHEVs, and EVs, more compact, efficient, and low-cost inverter units are required. SiC power semiconductor devices are expected to be applicable in such units. In automotive inverter units with output powers of approximately 100 kW, MOSFET chips composed of SiC that possess a



**Figure 16.36** Device characteristics comparisons between the Si-IGBT and SiC-MOSFET.  
(a) Current–voltage characteristics and (b) switching loss.



**Figure 16.37** (a) An SiC-MOSFET wafer with  $\phi = 150$  mm and (b) an  $8\text{ mm} \times 8\text{ mm}$  SiC-MOSFET chip.

breakdown voltage of 600–1200 V and a rated current of 100–600 A are required. Such SiC-MOSFETs that are superior to the Si IGBTs used in conventional automotive inverter units have been realized, as shown in Figure 16.36. SiC-MOSFET chips with sizes of  $8\text{ mm} \times 8\text{ mm}$  on a 150-mm-diameter SiC wafer have also been fabricated as R&D samples, as shown in Figure 16.37. These SiC chips are equipped with current and temperature sensors, similar to conventional Si chips, to ensure their safe operation in automotive systems. Through experimentation involving the replacement of the inverter unit of a commercial HEV with SiC-MOSFETs, the mileage of these vehicles was effectively improved (<http://newsroom.toyota.co.jp/jp/detail/2657262>). SiC-MOSFETs were subsequently used in conjunction with boost converters and in the inverters of commercial vehicles such as FCVs and some EVs (<http://newsroom.toyota.co.jp/en/detail/5725437>; [http://www.honda.co.jp/factbook/auto/CLARITY\\_FUEL\\_CELL/201603/P14.pdf](http://www.honda.co.jp/factbook/auto/CLARITY_FUEL_CELL/201603/P14.pdf)).

To ensure a further increase in the use of SiC power devices in commercial vehicles, the reliabilities of these devices must be improved and their associated costs must be reduced. The evaluation and analysis of the influence of crystal dislocations

in SiC wafers is required to guarantee the long-term lives of these SiC devices in the severe operation environments in vehicles, as well as to ensure that accidental failure does not occur.

In addition, these SiC wafers with 150-mm diameters may be mass-produced via automated line processes, such as those used for Si devices. However, the cost of SiC devices is currently several times higher than that of Si devices. These costs must therefore be reduced to permit the application of SiC devices in automobiles.

In the following section, the R&D of SiC power devices in terms of their automotive applications from the DENSO CORPORATION is described.

### 16.6.2 Ultra-Low-Loss SiC-MOSFET for Cost Reduction

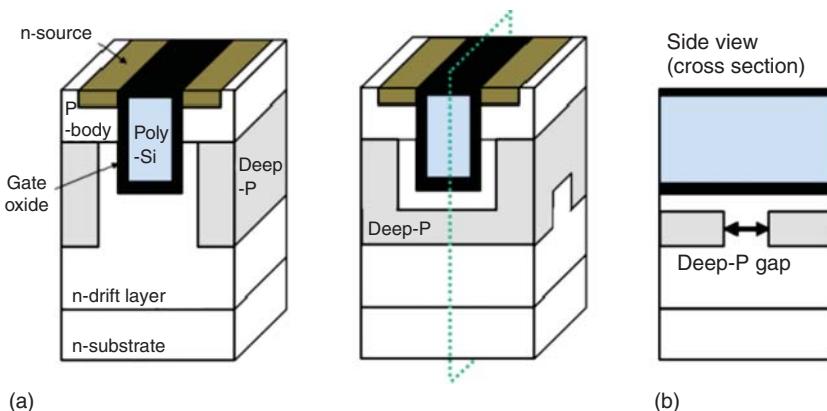
The realization of the required current capacity in a small-sized chip is important to achieve low-cost SiC-MOSFETs. Therefore, trench-gate-type MOSFETs was developed in this study. It is necessary to apply SiC-MOSFETs in the vehicles to further improve their on- and off-state characteristics, in addition to their long-term reliability. Compared with other Si devices, SiC has a high breakdown field (about 10 times higher than that of Si), and it is therefore important to reduce the gate oxide field. Although several groups have already reported original structures that may be used to decrease the gate oxide field, these structures may increase the junction gate field-effect transistor (JFET) resistance of these devices. SiC-MOSFETs that outperform the theoretical limits of Si unipolar devices have recently been demonstrated [22–24] (<http://global-sei.com/technology/tr/bn80/pdf/80-16.pdf>). However, there remains room for improvement in the trade-off between the on-resistance and the breakdown voltage.

In this study, we focus on improving the trade-offs between the on-resistance ( $R_{on}A$ ) and the gate oxide field ( $E_{OX}$ ). An original structure to suppress the gate oxide breakdown at the off-state is proposed. The remarkable on-state characteristics of the developed 4H-SiC trench MOSFETs with original structures will be demonstrated, while their high breakdown voltage will be maintained.

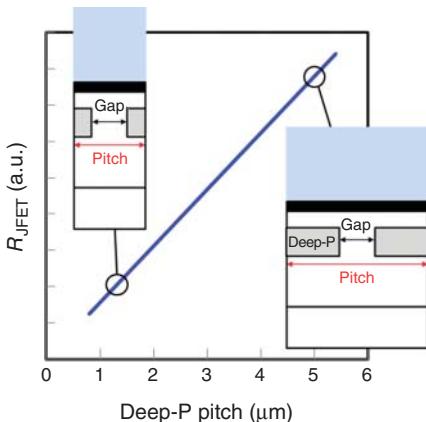
### 16.6.3 Proposed 4H-SiC Trench MOSFET Structure

Figure 16.38a,b show the 3D schematic views of the conventional 4H-SiC trench MOSFET (<https://www.denso.com/jp/ja/products-and-services/industrial-products/sic>) and the proposed Deep-P encapsulated 4H-SiC trench MOSFET, respectively. Both MOSFETs have a p-region, referred to as Deep-P, under the trench that serves to protect the gate oxide at the bottom of the trench from the high electric field in the off-state. The conventional MOSFET has a Deep-P structure (PDS) parallel to the trench gate, while the proposed MOSFET has an orthogonal Deep-P structure (ODS) [25].

For devices with a PDS, it is difficult to reduce the JFET resistance ( $R_{JFET}$ ) because the current paths of the JFET resistance depend on the cell pitch of the transistor. In contrast, the pitch of the Deep-P region in an ODS can be designed freely without depending on the cell pitch. The key area in an ODS is the space between the Deep-P



**Figure 16.38** 3D sketch of (a) the conventional structure and (b) the proposed structure (Deep-P encapsulated 4H-SiC trench MOSFET).



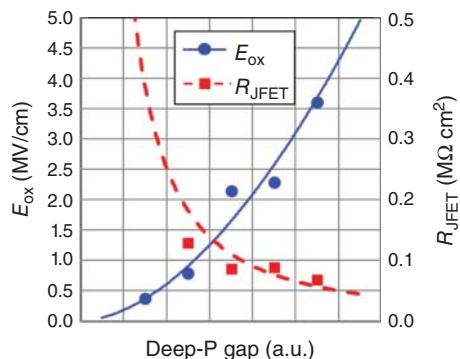
**Figure 16.39** Relationship between the on-resistance and the Deep-P pitch. The concentration and gap of the Deep-P are constant.

region and the trench that permits the distribution of electrons from the channel region. In the case of an ODS without such a space, the Deep-P region will contact the bottom of the trench, and the electrons from the channel region will not be well distributed because the electron path is limited by the Deep-P region. Thus, it is important to separate the Deep-P region from the bottom of trench to reduce the on-resistance.

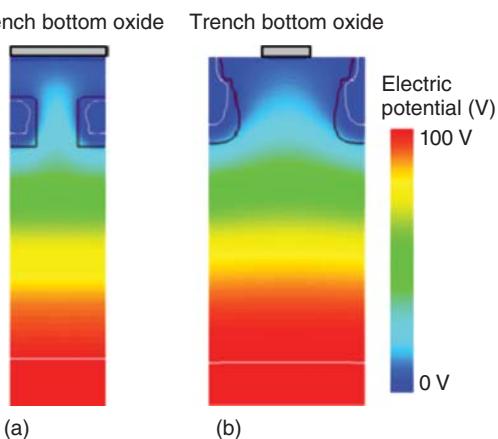
Figure 16.39 shows the simulated results of the relationship between the Deep-P pitch and the JFET resistance. The JFET resistance generally decreases as the Deep-P pitch is reduced because the density of the current paths increases (in the case of a constant Deep-P gap and concentration). Figure 16.40 shows the dependence of the JFET resistance and the gate oxide field on the gap between the Deep-P regions calculated by the device simulator. Selecting a suitable Deep-P gap results in a low JFET resistance without increasing the gate oxide field. Therefore, an adequate Deep-P gap and reduced Deep-P pitch result in a low JFET resistance.

In addition, to reduce the switching loss, it is important to reduce the gate-drain capacitance and gate-drain charge. The electric potentials and depletion regions

**Figure 16.40** Dependence of the JFET resistance and gate oxide field on the gap between the Deep-P regions. The concentration and width of the Deep-P region are constant.

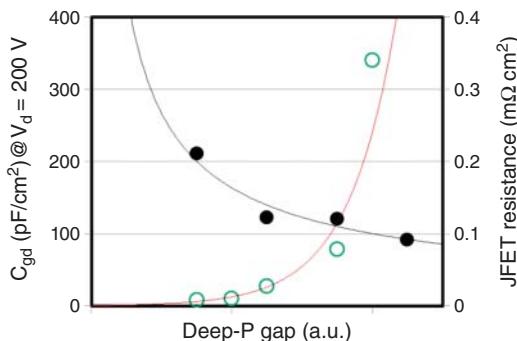


**Figure 16.41** Electric potentials of the (a) front view of the conventional structure and (b) side view of the presented structure at  $V_d = 100$  V and  $V_g = 0$  V.



of the conventional and presented MOSFETs were calculated using a device simulator [26]. Figure 16.41a,b show the electric potentials of the conventional and proposed structures, respectively, under a drain voltage of 100 V and a gate voltage of 0 V. The depletion region for each structure expands toward the drift region to almost the same depth. Compared with the conventional structure, the presented structure possesses a non-depleted Deep-P region under the trench gate oxide. The non-depleted region acts as the shield against the drain bias, which can reduce the effective gate-drain capacitance area. Therefore, a low gate-drain capacitance and low gate-drain charge are achieved in the proposed structure. This cell construction inherently has a small ratio of the gate-drain charge with respect to the gate-source charge. This feature is essential to suppress the parasitic turn-on phenomena that may cause the fatal failure of these devices in applications using the half bridges. In addition, the presented structure can avoid the switching delay of the Deep-P charge by connecting the Deep-P region closely to each P-base region [27].

The Deep-P gap should be selected to retain a low JFET resistance and a low gate-drain capacitance. Figure 16.42 shows the simulated results of the dependences of the gate-drain capacitance and the JFET resistance on the Deep-P gap. As can be seen in Figure 16.42, while the gate-drain capacitance increases by increasing the Deep-P gap, the JFET resistance, which directly affects the conduction loss,



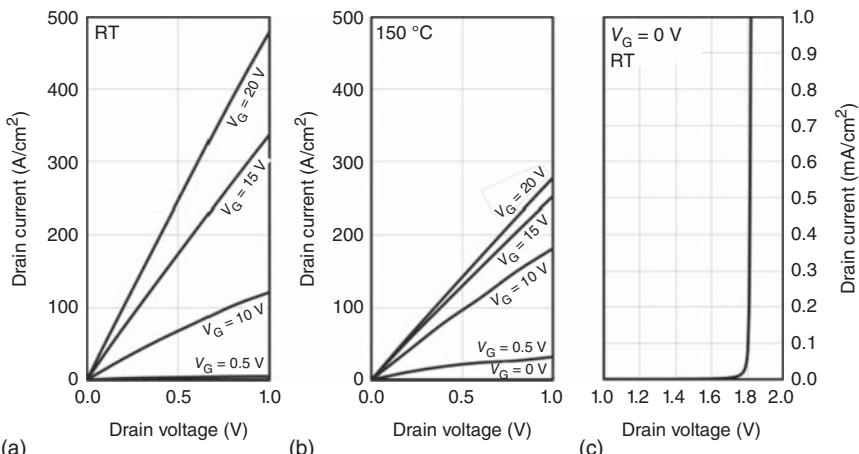
**Figure 16.42** Deep-P gap dependences of  $C_{gd}$  and JFET resistance.

decreases. For DC–DC converter or high-speed applications, it is more important to reduce the switching losses rather than the conduction losses, and a low gate–drain charge is generally the best choice for minimizing the switching losses. Therefore, it is considered that a narrow Deep-P gap is preferable. In contrast, a wide Deep-P gap is suitable for low-speed applications because the reduction of the conduction losses is more important than that of the switching losses. In that case, the Deep-P gap is limited up to the acceptable level of electric field crowding at the gate oxide. Therefore, the device design can be optimized by selecting an appropriate Deep-P gap for each specific application without the modification of the channel layout.

#### 16.6.4 Characteristics of the Developed MOSFET

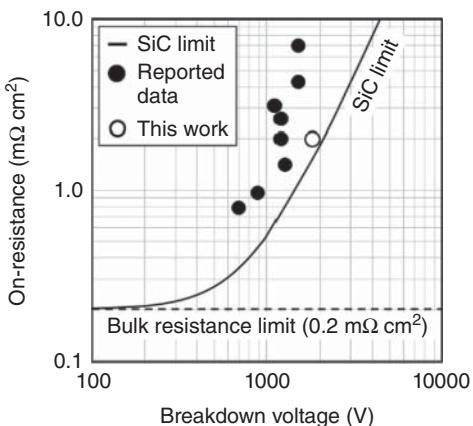
##### 16.6.4.1 Static Characteristics of the Optimized Structure

By utilizing the optimized conditions, 4H-SiC trench MOSFETs with an ODS were fabricated. Figure 16.43a,b show the on-state forward  $I_d$ – $V_{ds}$  characteristics at



**Figure 16.43** On- and off-state characteristics of the fabricated MOSFET with an optimized Deep-P gap at room temperature and 150°C. (a) On-state characteristics at room temperature. (b) On-state characteristics at 150°C. (c) Off-state characteristics at room temperature.

**Figure 16.44** Plot of the breakdown voltage vs. the on-resistance for 4H-SiC MOSFETs.



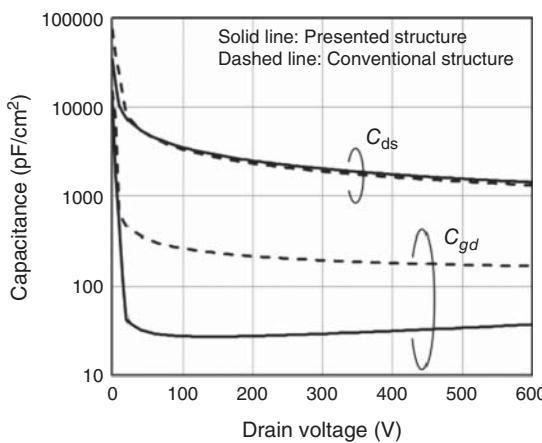
room temperatures and 150 °C for this device. The measured specific on-resistance was 2.04 mΩ cm<sup>2</sup> at room temperature and 3.47 mΩ cm<sup>2</sup> at 150 °C. The specific on-resistances were calculated at a gate voltage of 20 V and a drain current of 300 A/cm<sup>2</sup>. The breakdown voltage at room temperature was above 1800 V, as shown in Figure 16.43c. The specific on-resistance of the conventional structure was 3.5 mΩ cm<sup>2</sup> (not shown). A significantly low on-resistance could be achieved by applying an ODS with miniaturized patterns without deteriorating the off-state characteristics.

Figure 16.44 shows the plot of the breakdown voltage vs. the on-resistance for 4H-SiC MOSFETs. The plot shows the experimental results obtained in this work and the reported data for 4H-SiC MOSFETs in the literature. The SiC unipolar limit is also shown in Figure 16.44. Our results are shown to approach the SiC unipolar limit. MOSFETs with a superjunction structure would require further improvement in terms of the MOSFET performance.

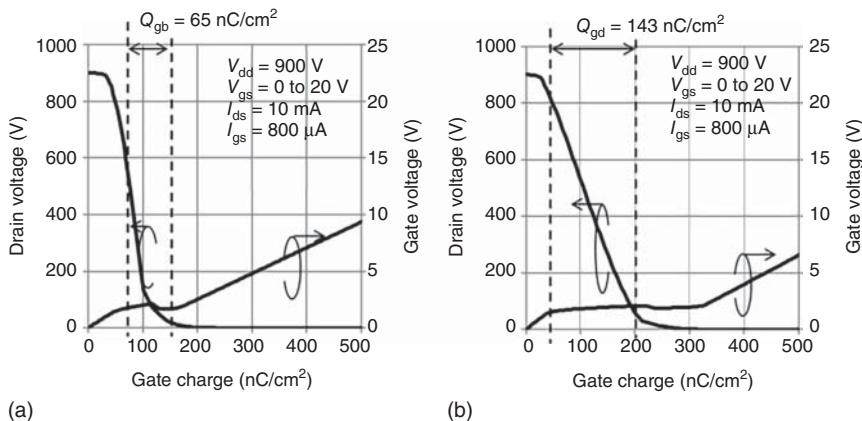
#### 16.6.4.2 Dynamic Behavior of the Optimized Structure

Capacitance–voltage measurements, gate charge tests, and double-pulse tests for the presented structure with an optimized Deep-P gap and the conventional structure were performed to confirm the shielding effect. Figure 16.45 shows the measured gate–drain capacitance and drain–source capacitance. The gate–drain capacitance of the presented structure at a drain voltage of 200 V was about 30 pF/cm<sup>2</sup>, while that of the conventional structure was about 200 pF/cm<sup>2</sup>.

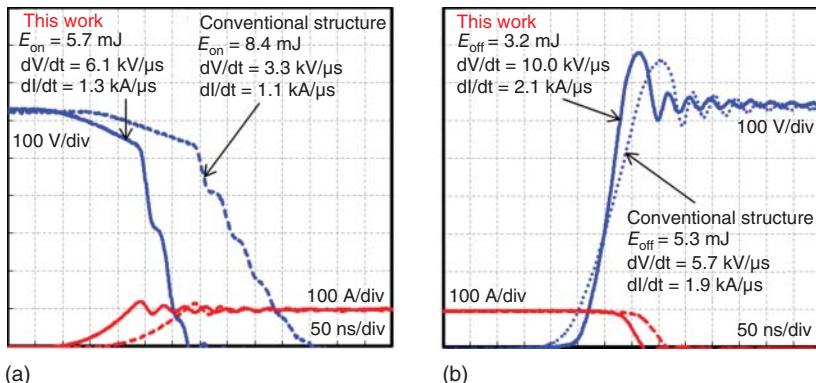
Figure 16.46a,b show the test results of the gate charge ( $Q_g$ ) for the presented structure and the conventional structure, respectively. The presented structure achieved a gate–drain charge of 65 nC/cm<sup>2</sup>, which is lower than that of the conventional structure (143 nC/cm<sup>2</sup>). Gate–drain charges were calculated within the 10–90% range of the drain voltage. To estimate only the gate–drain charge, measurements were performed at low load current. The turn-on and turn-off waveforms are depicted in Figure 16.47. Owing to the low gate–drain capacitance and charge, the presented structure could reduce  $E_{on}$  by 32% and  $E_{off}$  by 40% compared to the conventional structure. Figure 16.48a,b show the drain current dependence of  $E_{on} + E_{off}$  and the



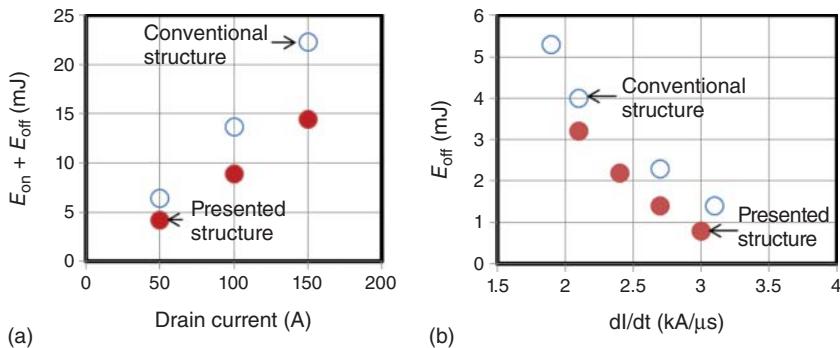
**Figure 16.45** Measured results for  $C_{gd}$  and  $C_{ds}$  of the conventional and presented structures.



**Figure 16.46** Measured gate charges of the (a) presented and (b) conventional structures.



**Figure 16.47** Double-pulse waveforms of the (a) turn-on and (b) turn-off of the conventional and presented structures ( $V_d = 650 \text{ V}$ ;  $V_g = -5/20 \text{ V}$ ;  $I_d = 100 \text{ A}$ ;  $R_g = 30 \Omega$ ; room temperature).



**Figure 16.48** (a) Drain current dependence of  $E_{on} + E_{off}$  ( $V_d = 650$  V;  $V_g = -5/20$  V;  $I_d = 50$ , 100, or 150 A;  $R_g = 30 \Omega$ ; room temperature) and (b)  $dI/dt$  dependence of  $E_{off}$  ( $V_d = 650$  V;  $V_g = -5/20$  V;  $I_d = 100$  A;  $R_g = 5, 10, 20$ , or  $30 \Omega$ ; room temperature) for the conventional and presented structures.

$dI/dt$  dependence of  $E_{off}$ , respectively, for the fabricated MOSFETs with an optimized Deep-P gap and the conventional structure. Compared with the conventional structure, the total losses were effectively reduced in the presented structure. The improvement of the trade-off between  $dI/dt$  and  $E_{off}$  must be considered to minimize  $E_{off}$ , given that the drain voltage surge is well suppressed during the turn-off period. As shown in Figure 16.48b,  $E_{off}$  was effectively reduced at the same  $dI/dt$ , indicating that the high  $dV/dt$  of the presented structure may be attributed to the improvement of this trade-off.

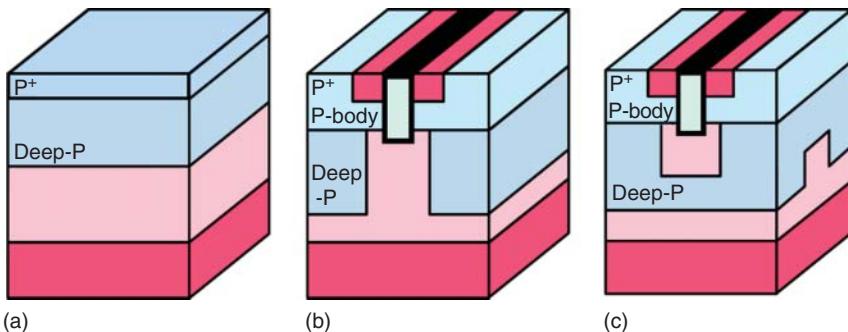
### 16.6.5 Measurements of Reliability

Important reliability issues for SiC-MOSFETs include (i) the dielectric breakdown lifetime of the gate oxide and (ii) the characteristic degradations caused by crystal dislocations in SiC devices. Considering the dielectric breakdown lifetime, adequate lifetimes were achieved using the above-mentioned presented structure. Therefore, in this section, the second issue is considered.

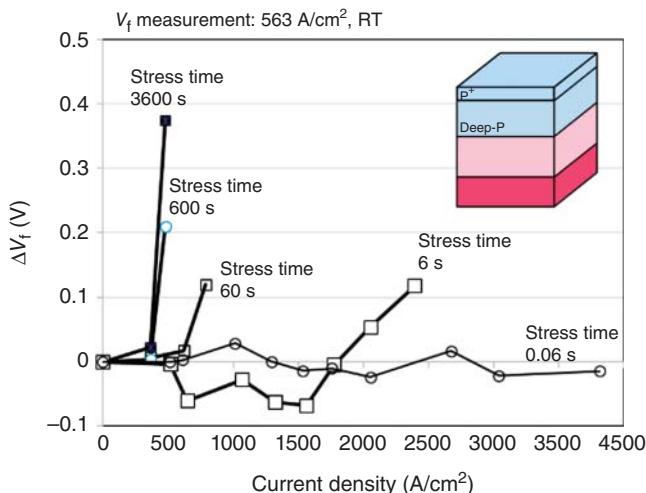
The major issue associated with the characteristic degradations in SiC-MOSFETs is the body diode current degradation [28, 29]. When the body diode is conducting, hole injection occurs from the top p-type layer into the n-type drift layer, which causes hole-electron recombination at various basal plane dislocations (BPDs). The BPD gains energy from this recombination process, and consequently, the stacking faults grow into the drift region. The stacking faults act as a resistance, which results in an increase in the conduction loss. Therefore, the bipolar degradation at the body diode conduction should be addressed.

### 16.6.6 Suppression of Bipolar Degradation in the Presented MOSFETs [30]

Figure 16.49a–c show the schematic cross-sectional illustrations of a PN diode, conventional MOSFET, and the presented Deep-P encapsulated MOSFET, respectively.



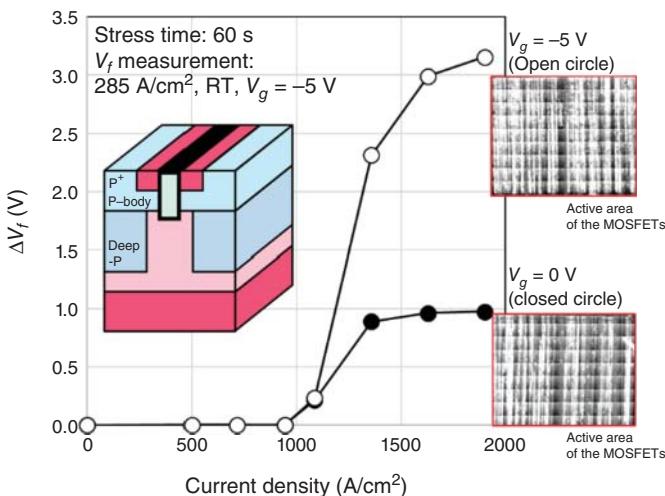
**Figure 16.49** Schematic cross-sectional illustrations of the (a) PN diode, (b) conventional MOSFET, and (c) Deep-P encapsulated MOSFET.



**Figure 16.50** Forward voltage degradation as a function of the current density and PL mapping images of the PN diodes.  $V_f$  was defined as a forward current of  $563 A/cm^2$  at room temperature.

The concentration and thickness of the drift layer are selected to achieve a blocking voltage of over 1200 V. All the structures used commercial wafers of the same specifications to focus on the structural differences.

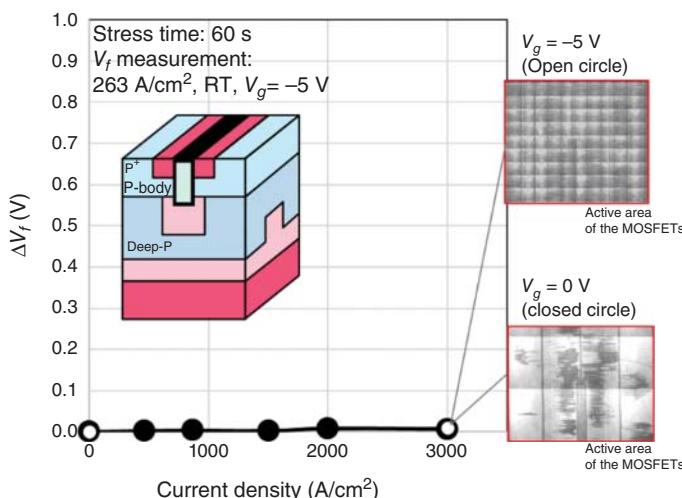
- (a) **PN diodes:** Over a stress time of 0.06 seconds, no degradation of the forward voltage up to a current density of  $4000 A/cm^2$  occurred, as shown in Figure 16.50. Consequently, the stacking faults were not observed in the photoluminescence (PL) image, which indicates that this stress time is insufficient to initiate the forward degradation process. In contrast, the forward voltages were degraded over stress times of 6, 60, 600, and 3600 seconds, and stacking faults were observed at each of these stress times. For the six-second case, the current density when forward degradation occurred was much larger than those at 60, 600, and 3600 seconds. As the stress time increases, the forward degradation appears to saturate. In previous studies [31, 32], it has been noted that the forward



**Figure 16.51** Forward voltage degradation of  $V_g = 0$  V and  $V_g = -5$  V as a function of the current density and PL mapping images of the conventional MOSFET.  $V_f$  was defined as a current of 285 A/cm<sup>2</sup> at room temperature and a gate voltage of  $-5$  V. The PL images of only the active areas are shown in this figure.

degradation has a threshold hole density depending on the temperature and concentration of the electron and hole densities, although the absolute values of these densities remain uncertain. The stress time was fixed at 60 seconds for subsequent tests to reduce the measurement time. The forward degradation strength of the PN diode was estimated to be around 500–800 A/cm<sup>2</sup>.

- (b) *Conventional MOSFETs:* Figure 16.51 shows the forward voltage degradation at gate voltages of 0 and  $-5$  V as a function of the current density. The corresponding PL mapping images are also shown. The forward voltage degraded at a current density of 1000–1100 A/cm<sup>2</sup> for both gate voltages, although the degree of forward voltage degradation at the gate voltage of  $-5$  V was about three times larger than that at 0 V. Since the forward voltage degradation threshold is determined by the hole concentration, this result suggests that the hole concentrations at both gate voltages do not differ at high current densities. As shown in the PL mapping image, the number of the stacking faults at a gate voltage of  $-5$  V is greater than that at 0 V. Because the forward voltage degradation values depend on the number of defects in the substrate and drift layer, it is assumed that the differences between these degradations are contributed to by the defect numbers in the drift layer and/or substrate.
- (c) *Deep-P encapsulated MOSFETs:* Figure 16.52 shows the forward voltage degradation at gate voltages of 0 and  $-5$  V as a function of the current density. The corresponding PL mapping images are also shown. In contrast to the results of the PN diodes and conventional MOSFETs, the forward voltage degradation did not occur up to a current density of 3000 A/cm<sup>2</sup> for the presented MOSFET, and stacking faults were not observed. These results indicate that the hole injections in the Deep-P encapsulated MOSFETs are much smaller than those of the PN diodes and conventional MOSFETs.



**Figure 16.52** Forward voltage degradation of  $V_g = 0$  V and  $V_g = -5$  V as a function of the current density and PL mapping images of the Deep-P encapsulated MOSFET.  $V_f$  was defined as a current of 263  $A/cm^2$  at room temperature and a gate voltage of  $-5$  V. The PL images of only the active area are shown in this figure.

Simulations of the devices were performed and the injected hole density was estimated for each structure. By accounting for the traps and geometrical effects, it was revealed that the injected hole density of the Deep-P encapsulated MOSFETs was much smaller than those of the PN diodes and conventional MOSFETs.

### 16.6.7 Summary

4H-SiC trench MOSFETs with an ODS were proposed and fabricated. The proposed SiC-MOSFETs demonstrated lower losses and higher reliabilities than the conventional SiC-MOSFETs. According to the superior results of the presented SiC-MOSFETs, the acceleration of the use of SiC power devices in commercial vehicles may be achieved.

### Acknowledgments

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## 17

### Point Defects in Silicon Carbide for Quantum Technology

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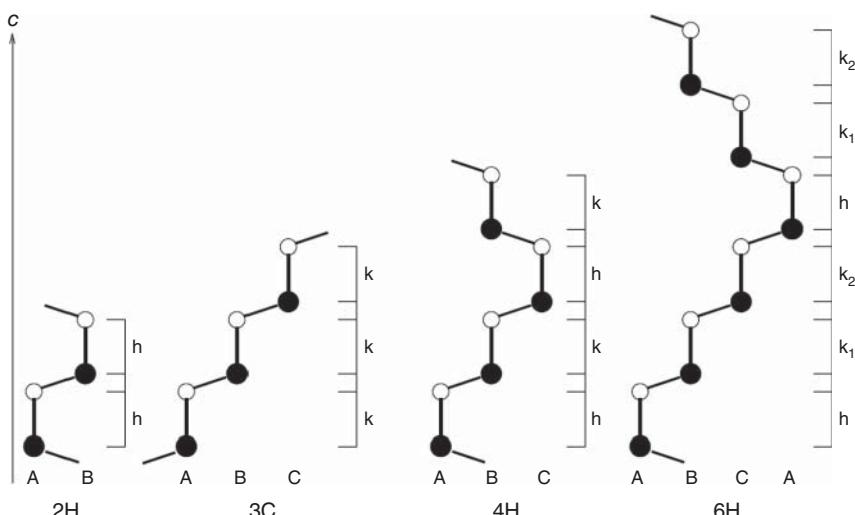
#### 17.1 Introduction

A new era in the fundamental and applied science on silicon carbide (SiC) has emerged in the field of quantum technology. This was inspired by the success of nitrogen-vacancy (NV) center in diamond [1–5] where the coherent control of single spin could be demonstrated at room temperature by means of optical readout and initialization that led to various sensor applications at the nanoscale. First principles calculations could identify the similarity between electronic structure of the NV center in diamond and divacancy in SiC in 2009 (see the conference proceedings of the International Conference of Silicon Carbide and Related Materials 2009 in Ref. [6] and a detailed publication in Ref. [7]). Indeed, the coherent control of the electron spin of divacancy defect in SiC was demonstrated in experiments in 2011 [8]. In addition, density functional theory (DFT) calculations combined with considerations of the presumed coherence time of the electron spin in various wide band gap materials identified SiC as a potential material to host optically addressable quantum bits [9]. Further experiments and theoretical studies have confirmed [10–13] that the electron spin coherence time can exceed 2 ms in SiC crystals with naturally abundant Si and C isotopes, including the single spin detection at room temperature of the silicon vacancy defect [11]. The big advantage of SiC is that this material can be grown at wafer scale with high purity and quality and acts as a wide band gap semiconductor. As a consequence, it can be envisioned that the combination of optical and electrical control of qubits in SiC is feasible, so the integration of semiconductor and quantum technologies can be realized within a single platform. Indeed, electrically driven single photon sources operating at room temperature have been realized in SiC diodes [14, 15]. The nature of these single photon sources was hinted from first principles calculations [15], as well as for the brightest solid-state single photon sources operating at room temperature [16].

Further advances in the SiC quantum technology have been flourished that are discussed in the other chapters in this book. The birth and development of SiC quantum technology relies on point defects with advantageous magneto-optical properties. In this review paper, we list the basic properties of these defects with short description of the most relevant ones. In particular, we will focus on the so-called divacancy, silicon vacancy, carbon antisite-vacancy (CAV) pair, and the NV pair defects, and other potential defects will be also considered.

## 17.2 Silicon Carbide: Polytypes and Types of Relevant Point Defects

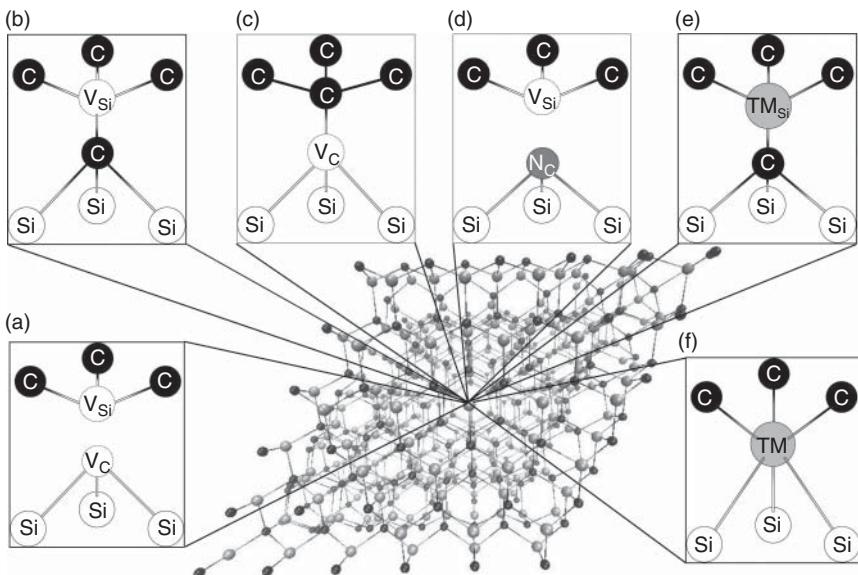
SiC has more than 250 known polymorphs in which they are common with the hexagonal lattice in the basal plane forming an Si–C bilayer. These bilayers can be stacked on top of each other either hexagonal close packed or face center cubic configurations which results in quasihexagonal (h) or quasicubic (k) Si–C bilayers in the sequence (see Figure 17.1). Because of the common basal plane structure, these different forms of SiC are also called polytypes. The chemical structure of these polytypes consists of tetrahedrons with  $sp^3$  fourfold coordinated C and Si atoms as usual in semiconductor structures. SiC did not form on Earth and should be produced. High-quality SiC can be grown by chemical vapor deposition (CVD) by using



**Figure 17.1** Important polytypes of SiC except for 2H. 2H SiC consists of only h Si–C bilayers and is shown only for didactic purposes. h and k labels refer to quasicubic and quasihexagonal bilayers where the indexes on k layers in 6H polytype distinguish the two quasicubic bilayers.

carbon and silicon precursors [17]. Depending on the conditions of CVD process or the substrate, the most common polytypes are the so-called 4H, 6H, and 3C SiC in Ramsdell notation, where H and C refer to hexagonal and cubic crystals, respectively. 4H and 6H SiC have four and six Si–C bilayers in their unit cell, respectively, in which sequences of  $hk$  and  $hk_1k_2$  Si–C bilayers follow each other (see Figure 17.1). Any Si or C atom in the quasihexagonal and quasicubic layers has the same fourfold coordination but the second neighbor environment differs. Although, the slightly polarized covalent Si–C bonds are common in these SiC polytypes, but the band gap of SiC varies significantly from 2.4 eV (3C) to 3.0 eV (6H) and 3.23 eV (4H) [17]. The absolute value of the top of the valence bands (VBM) is about the same position for these polytypes, but the position of the bottom of the conduction band (CBM) varies significantly. The reason behind this large variation has been recently explained by *ab initio* DFT calculations in which they showed that the CBM state is not a usual antibonding combination of the wave functions constituting the covalent bonds but rather “floating” states delocalized in the interstitial region of the crystal that are confined in the cage of quasihexagonal layers with pushing up the level of the CBMs with respect to that of 3C SiC [18]. We further note that the position of the CBM also affects the electrochemistry of these polytypes as has been recently explained by the so-called no-photon exciton generation (electro)chemistry (NPEGEC) process [19].

SiC can be doped n-type and p-type as well, so the Fermi level can be well varied by doping conditions [17]. Nitrogen and boron are often unwanted n-type and p-type contamination in SiC CVD layers but can be also used intentionally to control the conductivity of SiC. Nitrogen donor has a maximum limit of concentration ( $\approx 10^{19}$  1/cm<sup>3</sup>) because of the formation of a competing complex of four nitrogen around the silicon vacancy ( $V_{Si}$ ) at high nitrogen concentration but phosphorus can be also employed as a donor at higher concentration [20]. The resistance of the contaminated SiC layers can be either improved by introducing vanadium (we label it by Van in the context, in order not to confuse it with the vacancy label) (see Ref. [21] and references therein) or high temperature CVD growth with forming of vacancies and vacancy clusters (see Ref. [22] and references therein) which introduce deep acceptor and donor states that compensate the residual donor and acceptor states. The latter SiC samples are called high-purity semi-insulating (HPSI) SiC layers. Nitrogen and phosphorus donors are substitutional point defects. Nitrogen prefers to substitute carbon ( $N_C$ ) whereas phosphorus prefers to substitute silicon ( $P_{Si}$ ) in SiC (see Refs. [20, 23] and references therein). In general, an impurity atom may prefer to substitute C or Si atom in SiC. We further note that the h and k bilayers are inequivalent lattice sites in 4H and 6H SiC. These inequivalent lattice sites create different environment to the defects which affects their properties. For instance,  $N_C$  donor has an ionization energy at around 100 and 45 meV [24] at k and h site in 4H SiC, respectively. In general, a single substitutional defect or a single vacancy may have two and three inequivalent configurations in 4H and 6H SiC, respectively, whereas a pair defect has four and six inequivalent configurations in 4H and 6H SiC, respectively.



**Figure 17.2** The considered defects in SiC. TM stands for transition metal ion, whereas  $V_{Si}$  and  $V_C$  labels the Si-vacancy and C-vacancy, respectively.

For instance,  $V_C-V_{Si}$  divacancy defect exists in hh, kk, hk, and kh configurations in 4H SiC (see Figure 17.2a and Table 17.1). An impurity ion may reside at a single vacancy (Figure 17.2e) or divacancy. The latter can be realized by placing the ion either on-site (similar to Figure 17.2d) or at interstitial position (Figure 17.2f), where the latter is called asymmetric split-vacancy (ASV) configuration [37]. We further note that carbon may substitute silicon (or vice versa) in SiC that is called antisite defect. A special case is that during the diffusion of  $V_{Si}$  (Figure 17.2b) may transform to carbon antisite-vacancy (CAV) pair defect,  $C_{Si}-V_C$  defect (Figure 17.2c) that can be a stable configuration over  $V_{Si}$  depending on the position of the Fermi level in SiC (see Ref. [38] and references therein).

We note that the identification of inequivalent configurations of a defect is highly nontrivial, in particular, from experiments. As 4H and 6H SiC have only a single quasihexagonal site, a common practice was for identification of configurations in experiments to pickup two similar signals and a distinct signal in 6H SiC and then the two similar signals were associated with the two quasicubic sites and the remaining one to the quasihexagonal site. By following this logic, the similar signals as observed in 6H SiC and 4H SiC were used to identify the corresponding configurations in 4H SiC. However, it has been shown for nitrogen donors by combining experimental data and DFT calculations that this practice is misleading because the signals of h and  $k_2$  sites can be rather similar to each other and that of  $k_1$  site is distinct in 6H SiC [39]. In general, the interpretation of defect lattice sites from pure experimental data should be taken very cautiously from the literature and should be verified by first principles calculations.

**Table 17.1** Position of ZPLs and the ground state zero-field splittings (ZFS) of technologically important point defects in 3C and 4H SiC as obtained in experiments.

Polytype	Defect	Charge state	Spin state	Config. (PL signal)	ZPL (eV)	ZFS (GHz)
3C	$V_C V_{Si}$	0	1	kk	1.121 [25]	1.336 [25]
	$N_C V_{Si}$	1-	1	kk	0.845 [26]	1.303 [26]
4H	$V_{Si}$	1-	$\frac{3}{2}$	h(V1)	1.438 [27]	0.003 [28]
				k(V2)	1.352 [27]	0.035 [28]
4H	$V_C V_{Si}$	0	1	hh(PL1)	1.095 [29]	1.336 [29]
				kk(PL2)	1.096 [29]	1.305 [29]
				hk(PL3)	1.119 [29]	1.222 [29]
				kh(PL4)	1.150 [29]	1.334 [29]
4H	Unidentified	$\geq 1$		(PL5)	1.189 [29]	1.373 [29]
				(PL6)	1.194 [29]	1.365 [29]
4H	$V_C C_{Si}$ (CAV)	1+	$\frac{1}{2}$	hh( $A_{1,2}$ )	1.911, 1.902 [16]	
				hk ( $A_{3,4}$ )	1.864, 1.855 [16]	
				kk ( $B_{1,2}$ )	1.842, 1.846 [16]	
				kh ( $B_{3,4}$ )	1.832, 1.836 [16]	
4H	$N_C V_{Si}$	1-	1	hh(PLX1)	0.998 [30, 31]	1.282 [30]
				kk(PLX2)	0.999 [30, 31]	1.331 [30]
				hk(PLX3)	1.014 [30, 31]	1.193 [30]
				kh(PLX4)	1.051 [30, 31]	1.328 [30]
4H	$Van_{Si}$ <sup>a)</sup>	0	$\frac{1}{2}$	k( $\alpha$ )	0.969 [32]	540
				h( $\beta$ )	0.929 [32]	<40
4H	$Cr_{Si}$	0	1	k( $Cr_A$ )	1.158 [33, 34]	<1.2 [34]
				h( $Cr_C$ )	1.190 [33, 34]	6.46 [33, 34]
4H	$Mo_{Si}$	1+	$\frac{1}{2}$	h	1.152 [35]	?
				hh ( $Nb_0$ )	1.383 [36]	<72.54

a) Vanadium is denoted by Van in order to avoid confusing it with Si vacancy.  
Unknown data are labeled by question mark.

## 17.3 Point Defect Single Photon Sources and Quantum Bits

Quantum emission may be realized by a fluorescent isolated single point defect in solids. In the exemplary NV center in diamond, this has been realized by CVD growth of pure diamond and controlled creation of NV center by nitrogen implantation and annealing (see Ref. [5] and references therein). The implantation

dose was varied in order to produce the NV centers apart from each other so then illumination through an objective could photoexcite only a single defect in the confocal spot. Similar single photon emitters can be formed in SiC too. One of the most characteristic properties of these single photon emitters is the zero-phonon line (ZPL) in the corresponding photoluminescence (PL) spectrum in which phonons may also couple to the optical transition resulting in phonon sideband in the PL spectrum. The fraction of ZPL emission vs. the total emission, i.e. the Debye–Waller (DW) factor, is an important feature of these emitters as quantum information can be transmitted only from the ZPL emission. If the single photon emitter is paramagnetic, then the electron spin can be principally employed as a resource of quantum information. For NV center in diamond, the fluorescence is spin selective that can be employed to initialize its electron spin state by optical pumping and read out the spin state by the detected fluorescence intensity where driving of the electron spin can be achieved by microwave alternating magnetic field generated close to the sample [2], which is briefly called optically detected magnetic resonance (ODMR). An alternative readout method of the electron spin state is the electrical detection of magnetic resonance (EDMR) through spin-selective photoionization [40]. Typically, the spin levels in the ground state split even the absence of external magnetic field which is called zero-field-splitting (ZFS), thus ODMR and EDMR measurements can be carried out at zero constant magnetic field. Besides ZPL, ZFS is a characteristic parameter of solid-state defect quantum bits. First, we list the characteristic parameters of the observed single photon sources and quantum bits in the most studied 4H and 3C SiC polytypes. As explained above, stable inequivalent configurations of a defect may exist in 4H polytype that are labeled by k and h sites. We note that the PL5/6 centers have been recently associated with the neutral divacancy with  $S = 1$  spin state residing in the stacking fault of 4H SiC [41] but we keep the original claim of “unidentified” in Ref. [8] in Table 17.1.

Next, we list the defect quantum bits’ basic parameters in the less studied 6H SiC. The number of configurations of a defect can be the largest among the considered SiC polytypes.

In sections 17.3.1–17.3.5, we briefly summarize the recent results on the most prominent quantum bits and single photon sources in SiC.

### 17.3.1 Divacancy

The coherent manipulation of defect spins in SiC has been first demonstrated for the neutral divacancy defects [8] (see PL1-6 centers in Table 17.1). Neutral divacancies have  $S = 1$  ground state spin [42, 43] and near infrared optical transition at around 1100 nm of ZPL with broad emission in the phonon sideband with DW factor of about 0.03 that had been known as UD2 PL center in the literature [44]. It was previously predicted by combination of first principles calculations and group theory analysis of states [6, 7] that neutral divacancy is isovalent to NV center in diamond and the level structures (see Refs. [4, 5]) are also very similar which makes divacancy very promising quantum bits in SiC. The similarity between NV center in diamond and neutral divacancy in SiC has been later confirmed from photoluminescence

excitation (PLE) measurements [25] and highly accurate configuration interaction based first principles method [45], also in terms of Stark-tuning of the optical transition [46]. The typical coherence times are about 1.2 ms with ODMR readout contrast of about 15% [12, 25] in high-quality 4H SiC with optimized measurement conditions, whereas these parameters are about 0.9 ms and 3.5% in 3C SiC [25]. Simulations showed [13] that the nuclear spins of  $^{13}\text{C}$  and  $^{29}\text{Si}$  in natural abundant SiC crystals as the source of decoherence of the target divacancy electron spin results in about 2 ms coherence time for the divacancy spins, thus the low quality of crystals (possibly, too high concentration of residual nitrogen donors) may be responsible for the reduced coherence times in 3C SiC. Divacancy may exist in several charge states depending on the position of the Fermi level [30, 43, 47, 48]. The photoionization thresholds that have direct correspondence to the charge transition levels at low temperatures have been recently determined in experiments [48, 49] in which the correct and accurate first principles calculations imply [48] that  $(+|0)$  and  $(0| -)$  charge transitions levels are at  $\approx E_{\text{V}} + 1.0$  eV and  $\approx E_{\text{V}} + 2.0$  eV in 4H SiC, respectively. As a consequence, optical pumping with 960 nm laser results in the quenching of the PL1-4 centers into the “dark” negatively charged divacancy defect, in contrast to other interpretation [50, 51]. We note that the photoionization threshold should be polytype and temperature dependent as the band edges vary with polytypes and shift with temperature [52]. Divacancies may form in HPSI 4H SiC [8] but can be generated by, e.g. carbon implantation and annealing [29]. Most of the divacancy-related PL and ODMR centers can be observed at low temperatures in SiC, but room temperature signals can be also observed for some of the configurations (see a summary in Ref. [29]). The room temperature divacancy quantum bits are promising for quantum enhanced biosensing or hyperpolarization [53, 54]. The multiple divacancy quantum bits in 4H SiC [8] and 6H SiC [29] are challenging in terms of optimizing the measurement conditions for each configuration but can be used as a resource. Identification of the individual configurations was achieved by large-scale DFT calculations [55, 56]. For instance, the low symmetry of off-axis or basal divacancy configurations enables coherent optical and spin subsystems control and observation of Landau-Zener-Stuckelberg interference fringes in the resonant optical absorption spectrum [57]. In 3C SiC, a single divacancy center was found as expected [29, 58, 59]. We note that 3C SiC can be grown on Si substrate, and photonics crystals can be fabricated from SiC on a straightforward manner [59], but the in-built strain due to the mismatch between the Si substrate and SiC layers may reduce the potential of this heterostructure because the intrinsically good nonlinear optical properties of SiC cannot be fully harnessed. Strong optical nuclear spin polarization was found for divacancy configurations in 4H SiC [53] with applying a well-chosen constant, small magnetic fields, and illumination that were explained in details by combination of DFT and effective spin Hamiltonian simulations [53, 54]. Simulations predicted high-fidelity bidirectional nuclear quantum bit initialization with this technique for weakly coupled nuclear spins to the divacancy electron spin where this principles was confirmed in the experiments for stronger coupled nuclear spins [60]. The coupling of divacancy electron spin and nuclear spins was used as a resource to create solid-state spin ensembles

entanglement at ambient conditions with high fidelity [61]. Early measurements supported by DFT simulations shown an effective strain and electric field coupling to ground state divacancy spins [62] that lead to ODMR signals associated with “forbidden” electron spin resonance that can be driven by electrical fields [63]. The strain–spin coupling in the ground state was determined by DFT calculations and found significant coupling parameters connecting  $\Delta ms = \pm 1$  transitions [64, 65] that could be harnessed in mechanical driving of spin states [65]. Theory predicts that the stress–spin coupling parameters of divacancy spins are, at least, equal or even greater than that for NV center in diamond [64], which can be utilized to fabricate very sensitive pressure or piezo sensors at the nanoscale. Electric field and spin coupling could be used to realize electrically driven optical interferometry [57]. All-optical electrometry at ambient conditions could be realized by optical charge conversion of the defects between their fluorescent and dark charge states, with conversion rate dependent on the electric field [66]. Furthermore, spatial three-dimensional maps of surface acoustic wave modes in a mechanical resonator were demonstrated with using this effect and the piezo property of SiC [66]. The electric field-dependent optical charge conversion combined with heterodyne detection enabled electrometry at radio frequency range [67] with a predicted sensitivity of  $1.1 \text{ (V/cm)Hz}^{1/2}$ .

### 17.3.2 Si-vacancy

Silicon vacancy in hexagonal SiC has been known from decades (see a comprehensive review article in Ref. [68]). Early DFT calculations already identified that the negatively charged  $V_{\text{Si}}$  with  $S = 3/2$  spin is responsible for the Si-vacancy-related EPR centers [68] with nonzero but small zero-field splittings [69], despite the existing alternative interpretations [70], that were nullified by recent accurate DFT calculations [28, 56].  $V_{\text{Si}}(-)$  has an optical emission in the near infrared emission with ZPL at around 850 nm and a broad phonon sideband with a DW factor of about 0.15 [27] which are called  $V_{1,2}$  and  $V_{1-3}$  lines in 4H and 6H SiC, respectively. Time-dependent DFT calculations confirmed that the internal optical transitions of  $V_{\text{Si}}(-)$  are responsible for these signals [71]. For  $V_1$  center, a higher level excited state exists at about 4.5 meV ( $V'$ ) that no such a state was reported for the  $V_2$  or  $V_3$  configurations (e.g. Refs. [68, 72] and references therein).

Accurate DFT calculations identified the individual configurations (see Tables 17.1 and 17.2, and Refs. [28, 56, 76]) which is in contrast to previous interpretations based on the similarities of EPR signals in 4H and 6H SiC [77, 78]. The corresponding ODMR centers were labeled by  $\text{Tv1a}$ ,  $\text{Tv2a}$ , etc. in the literature [27]. After early group theory analysis reports [68], recent studies [79, 80] have proposed the fine electronic structure of  $V_{\text{Si}}(-)$  that has been recently verified by configurational interaction-based first principles method [81]. It was predicted by a phenomenological theoretical study that the  $V_1$  center could be used to realize spin–photon interface [82], whereas the spin–strain interaction and the optical spin polarization of the  $V_{\text{Si}}(-)$  electron spin have been recently analyzed based on group theory arguments [80, 83]. Si-vacancy is a highly energetic defect

**Table 17.2** Position of ZPLs and ground state zero-field splittings (ZFS) of technologically important point defects in 6H SiC as obtained in experiments.

Polytype	Defect	Charge state	Spin state	Config. (PL signal)	ZPL (eV)	ZFS (GHz)
V <sub>Si</sub>	1-	$\frac{3}{2}$		h(V1)	1.433 [27, 56]	0.028 [27, 56]
				k <sub>2</sub> (V2)	1.398 [27, 56]	0.128 [27, 56]
				k <sub>1</sub> (V3)	1.366 [27, 56]	0.028 [27, 56]
V <sub>C</sub> V <sub>Si</sub>	0	1		k <sub>1</sub> k <sub>1</sub> (QL1)	1.088 [29, 56]	1.3 [29, 56]
				hh(QL2)	1.092 [29, 56]	1.334 [29, 56]
				hk <sub>1</sub> (QL3)	1.103 [29, 56]	1.236 [29, 56]
				k <sub>1</sub> k <sub>2</sub> (QL4)	1.119 [29, 56]	1.317 [29, 56]
				k <sub>2</sub> h(QL5)	1.134 [29, 56]	?
				k <sub>2</sub> k <sub>2</sub> (QL6)	1.134 [29, 56]	1.347 [29, 56]
6H	N <sub>C</sub> V <sub>Si</sub>	0	1	hh	0.96[1] [73]	1.328 [73]
				k <sub>1</sub> k <sub>1</sub>	0.95[1] [73]	1.278 [73]
				k <sub>2</sub> k <sub>2</sub>	1.00[1] [73]	1.355 [73]
Van <sub>Si</sub> <sup>2</sup>	0	$\frac{1}{2}$		h( $\alpha$ )	$\approx$ 0.946 [74]	526.14 [75]
				k <sub>1/2</sub> ( $\beta$ ) <sup>3</sup>	$\approx$ 0.919 [74]	?
				k <sub>1/2</sub> ( $\gamma$ ) <sup>3</sup>	$\approx$ 0.893 [74]	?
Cr <sub>Si</sub>	0	1		k <sub>1/2</sub> (Cr <sub>A</sub> ) <sup>4</sup>	1.156 [34]	<1.2 [34]
				k <sub>1/2</sub> (Cr <sub>B</sub> ) <sup>4</sup>	1.180 [34]	<1.2 [34]
				h(Cr <sub>C</sub> )	1.189 [34]	5.396 [34]
Mo <sub>Si</sub>	1+	$\frac{1}{2}$		h	1.106 [35]	?
Nb <sub>Si</sub> V <sub>C</sub> (Nb-ASV)	0	$\frac{1}{2}$		hh (Nb <sub>0</sub> )	1.361 [36]	<72.54

- a) Calculated values.
- b) Vanadium is denoted by Van, in order to avoid confusing it with Si vacancy.
- c) Signals of  $\beta$  and  $\gamma$  belong to the quasicubic Van<sub>Si</sub> defects; however, they are not fully resolved so far.
- d) Signals of Cr<sub>A</sub> and Cr<sub>B</sub> belong to the cubic Cr<sub>Si</sub> defects; however, they are not fully resolved so far.

Unknown data are labeled by question mark.

which is stabilized in n-type 4H SiC when the defect is negatively charged (see latest accurate calculations from Refs. [9, 38, 84]). In p-type region, the carbon antisite-vacancy pair, a tautomer configuration of isolated Si-vacancy, is more stable (see Section 17.3.3 and references in Ref. [38]). For this reason, Si-vacancies are not formed in the growth of high-quality SiC but can be typically produced *a posteriori* by irradiation and implantation techniques [27, 85–94]. Implantation techniques were applied to engineer Si-vacancies into desired location in SiC samples, including mechanical resonators [95], photonic crystal structures [96–98] that can be used to significantly enhance the ZPL emission of Si-vacancies. We note that the electrically active carbon vacancies have much lower formation energies

than silicon vacancies [9, 38, 84, 99]; therefore, irradiation creates lots of unwanted defects. High-temperature annealing would remove the desired silicon vacancies; thus, those unwanted defects remain present together with silicon vacancies in SiC. This may compromise the quality of spin properties of  $V_{Si}(-)$  quantum bits. Recently, it has been found [94] that the spin-lattice relaxation time remains constant up to high irradiation fluences, independently of the irradiation type (electron, proton, or neutron). On the contrary, the spin coherence time is very sensitive to the irradiation type and fluence. The longest spin coherence time for the same emitter density is observed for electron irradiation. The shortest spin coherence time was observed in neutron-irradiated samples, which, however, can be partially recovered using annealing. Very recently, it has been demonstrated that Si-vacancies can be created at a given location within  $\approx 80$  nm accuracy by femtosecond laser writing [100] with a single pulse without annealing. This process also presumably create nearby carbon vacancies too that affect the charge state stability of  $V_{Si}(-)$  upon illumination [100]. Theory found that charge transition levels of the single, double, and triple acceptor state of Si-vacancies should be at  $\approx E_V + 1.3$  eV,  $\approx E_V + 2.5$  eV, and  $\approx E_V + 2.8$  eV in 4H SiC, respectively [84], where the latter two are associated with the S2 and S1 deep level transient spectroscopy (DLTS) centers in n-type irradiated 4H SiC [84, 101]. The photoionization [66] and/or controlled Fermi-level shifts in SiC diodes [81] can be applied to switch the  $V_{Si}(-)$  quantum bit on and off. The former process can be electric field dependent in given 4H SiC samples, thus can be used to realize all-optical electrometry [66]. Engineering of  $V_{Si}(-)$  into diodes was reported at ensemble level [14]. Tight control of charge state of single  $V_{Si}(-)$  (V2 center) quantum bit has been recently demonstrated in 4H SiC diode [81] which is a key step toward integrating the quantum technology with semiconductor technology. Off-resonant excitation of  $V_2$  ODMR center in 4H SiC results in  $\sim 1\%$  ODMR contrast at room temperature [102–104]. Resonant excitation of single  $V_1$  or  $V_2$  center at low temperatures in 4H SiC leads to high fidelity spin and optical control [105, 106]. The coherence time of the electron spin is at around 1 ms [10, 11, 72, 107–111]. These near-infrared color centers are relatively dim (around 10 kcount/s); thus, solid immersion lens was produced by etching of SiC, in order to observe single  $V_2$  centers in 4H SiC [11]. This defect may realize a maser [112], i.e. coherent emission of microwave photons, and subject for realizing a nanoscale vector magnetometer [113–117] and thermometer [113, 118]. The observed sensitivity of dc magnetometer is about  $100 \text{ nT}/\sqrt{\text{Hz}}$ , and it was proposed that engineering this magnetometer into an optimized light-trapping waveguide can improve the sensitivity to about  $100 \text{ fT}/\sqrt{\text{Hz}}$  [117]. By harnessing the giant 2.1 MHz/K shift of the zero-field splitting in the excited state of  $V_2$  center in 4H SiC, it was found that this effect results in an all-optical thermometry technique with temperature sensitivity of  $100 \text{ mK}/\sqrt{\text{Hz}}$  for a detection volume of approximately  $10^{-6} \text{ mm}^3$ .  $V_1$  center in 4H SiC has very promising properties for realizing quantum communication [82, 105, 119]: it shows a very stable zero-phonon-line emission against stray electric fields with nearby addressable nuclear spins for quantum memory. We note that  $V_{Si}(-)$  is less known in 3C SiC than in hexagonal polytypes. Itoh et al. observed in irradiated 3C SiC layers grown on Si substrate an isotropic

$S = 3/2$  T1 EPR center with tetrahedral symmetry that was associated with  $V_{Si}(-)$  [120]. A dominant PL line of 1.913 eV, also called E center, observed in this sample was found to disappear at annealing stages of  $\approx 100$  and  $700$  °C, similarly to the T1 EPR center [121]. Therefore, E center was assigned to  $V_{Si}(-)$  [121]; however, DFT calculations showed that this PL line can be rather associated with its tautomer configuration, the carbon antisite-vacancy pair [122] (see Section 17.3.3). Later, a 1.121-eV PL center was observed in 3C SiC with an ODMR signal too with tetrahedral symmetry that is also called L2 center [123, 124]. As DFT calculations imply [122] that CBM to in-gap level optical transition may occur at this energy for the excited state of  $V_{Si}(-)$ , the 1.121-eV ODMR center might originate from  $V_{Si}(-)$ . We note that the early analysis of the ODMR line indicated an  $S = 1/2$  effective spin which contradicts with the  $S = 3/2$  spin of  $V_{Si}(-)$  [123]. Further studies are necessary to resolve this issue. We note that multiconfigurational ab initio calculation predicted [125] that the neutral silicon vacancy has a singlet ground state with an  $S = 1$  metastable state above which was also supported by a constraint spin DFT calculations [126]. Later, photo-EPR studies confirmed this prediction [127]; thus,  $S = 1$  high spin state can be measured for neutral  $V_{Si}$  in 3C SiC.

### 17.3.3 Carbon Antisite–Vacancy Pair

The carbon antisite-vacancy (CAV) pair defect is a bistable conformation of the isolated silicon-vacancy defect [38, 99, 128, 129] which means that the relative stability of the two conformations depends on the position of the Fermi level. According to accurate calculations [38], the CAV defect is stable over  $V_{Si}$  for the range of the Fermi-level position between  $E_V$  and  $\approx E_V + 2.0$  eV in 4H SiC. In n-type conditions of 4H SiC, the  $V_{Si}$  is more stable than CAV defect but the metastable CAV defect might coexist with  $V_{Si}$  depending on the formation condition of point defects in the SiC sample (e.g. Ref. [16]). Ab initio calculations predicts that the negatively charged CAV may be observed with Fermi-level position at  $\approx E_V + 2.7$  eV with  $S = 1/2$  spin in 4H SiC which was associated with EPR centers in irradiated HPSI material [129]. The calculated  $(2+|+)$  and  $(+|0)$  charge transition levels are at  $\approx E_V + 1.3$  eV and  $\approx E_V + 2.1$  eV in 4H SiC [38], respectively. The positively charged CAV has  $S = 1/2$  spin and the HEI9/10 EPR centers were associated with this defect [130]. Steeds observed PL centers in electron irradiated 4H SiC samples called A–B lines [16] with ZPL energies at around 1.9 eV (see Table 17.1) that were tentatively assigned to the neutral CAV defect. However, accurate calculations showed [16, 38] that the neutral CAV defect is ionized to  $(+)$  state upon such illumination. Rather, split CBM level to in-gap deep defect level optical transition may be associated with this PL signal [16]. Indeed, well-engineered electron irradiation of HPSI 4H SiC resulted in the formation of ultrabright (million photons per second) single photon emitters associated with this defect [16]. To date, this is among the brightest solid-state single photon emitters. As mentioned earlier, this defect has  $S = 1/2$  ground state spin [130], but optical manipulation of its spin state has not yet been reported so far. Very recent photo-EPR measurements has confirmed, on the other hand, that the charge states of the ensemble of CAV defects can be switched by

photo-excitation [131], and the observed ionization thresholds are consistent with the ab initio results as given above. We note that the neutral CAV has  $S = 0$  ground state but a metastable  $S = 1$  state exists according to first principles simulations [38]. It was proposed that this defect may have a near-infrared optical transition in 4H SiC and optical pumping may lead to the population of the metastable triplet state [38]. Assuming a sufficiently long lifetime of this triplet state, quantum control of the electron spin and a nearby nuclear spin (either  $^{13}\text{C}$  or  $^{29}\text{Si}$ ) is doable. Group theory analysis implies that spin-selective non-radiative decay may occur from the triplet substates toward the singlet ground state; thus, the spin state may be read out optically [38] similar to the so-called ST1 defect in diamond [132]. Finally, we note that the so-called  $E$  PL center [121] in 3C SiC was observed in nanocrystallites which emits with ZPL at 648 nm (1.913 eV) and the corresponding defects in 3C SiC nanocrystals formed ultrabright single photon sources [122]. The  $E$  PL center was originally associated with  $\text{V}_{\text{Si}}$  [121]; however, ab initio calculations strongly imply [122] that the  $E$  PL center is the PL transition between the split VBM and the defect level in the gap for the (2+) charge state of the CAV defect in 3C SiC. Interestingly, the calculated (2 + |+) charge transition level is at  $\approx E_{\text{V}} + 1.95$  eV, whereas the neutral CAV defect is marginally stable at highly n-type conditions in 3C SiC [122]. The (2+) charge state has a singlet ground state. A metastable triplet excited state might exist for this defect but has not yet been reported.

### 17.3.4 Nitrogen-Vacancy Pair

Recently,  $\text{N}_\text{C}\text{V}_{\text{Si}}$  defects have been observed in the most common SiC polytypes (3C, 4H, 6H) in N-doped particle- and ion-irradiated SiC crystals [26, 30, 31, 73, 133–135].

The different configurations in hexagonal polytypes and the corresponding negative charge state in each polytype were identified by combination of ab initio simulations and experimental data (see Table 17.3). The single negative charge state of the  $\text{N}_\text{C}\text{V}_{\text{Si}}$  defects, i.e. the NV centers show near infrared emission as found in experiments [26, 31, 73, 133] arising from the transition between the  $^3E$  excited and  $^3A_2$  ground state both exhibiting  $S = 1$  spin state according to theory [9, 30, 47, 136, 137]. The observed PL spectra of  $\text{N}_\text{C}\text{V}_{\text{Si}}$  centers were broad even at cryogenic temperatures which implies relatively small DW factor similar to that of NV center in diamond. Optical spin polarization of the  $^3A_2$  ground state has been demonstrated in all three polytypes at room temperature [26, 73, 133]. The spin coherence times are assumed to be long based on the observed characteristics of the  $\text{N}_\text{C}\text{V}_{\text{Si}}$  EPR spectra. According to ab initio results [9, 30, 47, 136, 137] NV centers are stable within the ingap positions of the Fermi level of around  $\approx E_{\text{V}} + 1.5$  eV and  $\approx E_{\text{V}} + 2.6$  eV in the hexagonal polytypes, and above  $E_{\text{V}} + 1.5$  eV in 3C SiC, where  $E_{\text{V}}$  stands for the valence band edge. Nevertheless, by using particle irradiation and subsequent annealing, neutral divacancies always form besides NV center in a comparable amount as found by theory [30] and earlier PL experiments [73, 133]. Consequently, the spin- and optically active  $\text{V}_{\text{Si}}\text{V}_{\text{C}}(0)$  may be detrimental for the spectral and photostability of the NV center. Nevertheless, in a recent study [135], preferential formation of NV centers has been reported in ion-irradiated 4H SiC

**Table 17.3** Experimental (exp) and calculated (DFT) values of  $g$ ,  $D$  parameters in the ground state (see Ref. [73]) and ZPLs for axial NV center configurations in the most common polytypes of SiC.

Polytype	Config.	$g_{\perp}^{\text{exp}}$	$g_{\parallel}^{\text{exp}}$	$g_{\perp}^{\text{DFT}}$	$g_{\parallel}^{\text{DFT}}$	$D^{\text{exp}}$ (MHz)	$D^{\text{DFT}}$ (MHz)	$ZPL^{\text{exp}}$ (eV)	$ZPL^{\text{DFT}}$ (eV)
3C	kk	2.003	2.004	2.0029	2.0034	1303	1409	0.845 [26]	0.870 [30]
	hh	2.003	2.004	2.0029	2.0036	1313	1428	0.998 [30]	0.966 [30]
4H	kk	2.003	2.004	2.0029	2.0036	1270	1377	0.999 [30]	1.1018 [30]
	hh	2.003	2.004	2.0029	2.0036	1328	1404		0.96 [73]
6H	$k_1 k_1$	2.003	2.004	2.0029	2.0035	1278	1348		0.95 [73]
	$k_2 k_2$	2.003	2.004	2.0029	2.0036	1355	1431		1.00 [73]

samples by using annealing temperature of 1000 °C. Photoionization of NV centers might be detrimental for their photostability during single defect spectroscopy which is usually carried out by applying confocal microscope producing high excitation power. This might enhance two-photon absorption processes that may ionize NV centers to  $N_C V_{Si}(2^-)$  charge state. In order to avoid destructive effects on the photo- and spectral stability in hexagonal SiC, excitation energy lower than  $\approx 1.1$  eV has been proposed for the optimal readout process of the ground state spin along with efficient reionization of NV centers [30].

### 17.3.5 Other Defects

Besides vacancy-related intrinsic point defects, other defects have been observed as single photon sources or quantum bits, or have been proposed as quantum bit candidates in SiC. One class of such point defects is the transition metal defects which may be considered as atomic like states embedded into the crystal potential in which relatively high DW factor may be expected. Indeed, chromium defect in hexagonal SiC has about 0.73 DW factor and  $S = 1$  spin ground state spin that could be spin polarized upon illumination at ensemble level [33]. The spin state could be read-out by ODMR. Spin polarization is made possible by the narrow optical linewidths of these ensembles, which are similar in magnitude to the ground state zero-field spin splitting energies of the ions at cryogenic temperatures [33]. The wavelength of the emission is at around 1.16 eV (see Tables 17.1 and 17.2) with long optical decay rates ( $\sim 100 \mu s$ ) where the latter is due to the intraconfigurational spin-flip transition between the spin-singlet excited state and spin-triplet ground state [34]. The long optical decay rate may be not advantageous in many quantum protocols, but other optically active transition metal defects occur in SiC. For instance, molybdenum produces similar ZPL emission at around 1.15 eV in 4H SiC (see Table 17.1), but the observed optical lifetime is about 60 ns based on ensemble measurements [35]. On the other hand, the DW factor was estimated to only few percents [35]. The reason of the relatively small DW factor may be revealed by DFT simulations. The single

Mo configuration observed both in 4H and 6H SiC is associated with the  $\approx 0.3$  eV difference in the DFT formation energies favoring the quasihexagonal site over the quasicubic site(s) substituting the Si atom ( $\text{Mo}_{\text{Si}}$ ) [35, 138] which results in a significantly higher concentration of quasihexagonal configuration. In the PLE measurements, multiple electronic levels were observed in the ground and excited state that were associated with the spin sublevels [35]. The magnetic field dependence of these lines was consistent with an  $S = 1/2$  spin model which implied that the defect is in the single positive charge state [35]. By applying a small transverse magnetic field and well-chosen two-laser driving, a  $\Lambda$  system was established and coherent pair trapping of electron spins was realized for the ensemble of Mo defects [35]. The high-quality Mo-doped SiC resulted in a relatively long  $0.32$   $\mu\text{s}$  coherence time for the  $S = 1/2$  electron spin. We note that the observed g factor of the electron spin showed a large anisotropy and a large deviation from the value of the free electron [35]. This implies a contribution of the spin-orbit interaction to the g factor that also should result in a relatively large zero-field splitting that has not yet been reported so far. A promising candidate defect for quantum communication application is the neutral vanadium in 4H SiC (see Table 17.1) that have two configurations associated with the quasicubic and quasihexagonal sites substituting the Si atom, i.e.  $\text{Van}_{\text{Si}}$ , with optical emission at  $1280$  ( $\alpha$ ) and  $1330$  nm ( $\beta$ ) [139]. The latter is in the O-band of the optical fibers which is compatible with the existing telecommunication and World Wide Web infrastructure. We note that three  $\text{Van}_{\text{Si}}$  centers with similar near infrared emission were observed in 6H SiC (see Table 17.2) [75]. This defect has  $S = 1/2$  electron spin that was observed with showing linewidth smaller than  $2$  Gauss at  $77$  K in EPR measurements in old SiC samples [74]. This implies a sufficiently long coherence times of the electron spin at low temperatures. The ground-state orbital doublet together with  $S = 1/2$  split due to spin-orbit interaction at zero magnetic field which is manifested in the observed number of ZPL lines in  $\alpha$  and  $\beta$  emitters [74]. Recently, the optical properties of  $\text{Van}_{\text{Si}}$  have been revisited in pure, vanadium-doped 4H SiC samples mediated by DFT simulations [32]. Above band-gap excitation (at  $441$  nm) was applied in that study that created mobile excitons in SiC that recombined with  $\text{Van}_{\text{Si}}$  defect. This recombination is partially radiative that results in near-infrared fluorescence. After pulsed photoexcitation, the fluorescence decay signals were recorded [32]. The combination of results from DFT simulations and PL measurements indicates that the efficiency of emission is about  $23\%$  and  $15\%$  for  $\alpha$  and  $\beta$  emitters under this excitation wavelength. The observed PL lifetimes were  $163$  and  $43$  ns, respectively. The measured DW factor is around  $30\%$  for each emitter. DFT simulation strongly implies that  $\alpha$  and  $\beta$  emitters are the k and h configurations [32], respectively, that goes against previous assignments based on the spectral similarities of  $\text{Van}_{\text{Si}}$  defects in 4H and 6H SiC [139]. We note that very recently single  $\text{Van}_{\text{Si}}$  centers have been observed in 4H and 6H SiC [140]. The individual vanadium centers were created by vanadium implantation. Presumably, the other defects created in this process are responsible for the limited photostability of these single photon emitters which produces only  $100$ – $120$  counts per second under these conditions at close-to-resonant photoexcitation [140]. The observed coherence times were about  $1$   $\mu\text{s}$  at  $3.3$  K due to presumably fast dephasing between the two spin

sublevels caused by acoustic phonons [140]. Another likely quantum bit candidate could be the niobium defect in hexagonal SiC. Niobium produces a single line in the PL and EPR spectrum in hexagonal SiC [36, 37, 141] which is explained by DFT simulations [37]: the Mo creates an ASV configuration that is only stable in hh divacancy. This defect emits at  $\sim$ 1.36 eV (ZPL) and has  $S = 1/2$  spin state in its neutral charge state. Niobium is a contamination in the CVD growth of SiC but might be intentionally doped too. This magneto-optical system is similar to the neutral vanadium and positively charged molybdenum, thus is a subject of future quantum optics studies. Besides intentionally formed single photon sources, unintentional ones have been observed, in particular, at the interface of SiC/SiO<sub>2</sub>. Besides electrically driven strong visible emission from  $D_1$  PL center in 4H SiC [142], which is a common intrinsic defect in SiC (silicon antisite), was reported in a p-i-n junction [14]. Theory proposed [15] that this defect near stacking faults in 4H SiC diodes is responsible for the observed single defect electroluminescence with varying wavelengths where the variation depends on the distance of the  $D_1$  defect from the stacking fault. This model was questioned in a later study [143] which showed that thermal oxidation of SiC leads to several single photon emitters in the visible. It was also reported that at the C-face of SiC/SiO<sub>2</sub> interface of the metal-oxide-semiconductor field-effect semiconductor (MOSFET) devices contain single photon emitters [144]. The single photon emitters at the SiC/SiO<sub>2</sub> interface have not yet been identified but most likely they originate from carbon antisite - carbon interstitial clusters [145, 146]. We further note that similar ultrabright and stable single photon emitters were reported in the visible with unidentified microscopic structure in HPSI 4H SiC which was electron irradiated and annealed in forming gas at ambient pressure at 600 °C [147]. Furthermore, near infrared single photon emitters with stable  $\sim$ MHz count rates were observed in 3C SiC CVD layers that operate at room temperature [148]. The polarization degree of both excitation and emission of these emitters can reach up to around 97%. The emitters have very broad PL spectra even at cryogenic temperatures; thus, the DW factor should be low though not determined in this study [148]. They found that the most efficient excitation wavelength is around 975 nm (1.27 eV) for a single photon emitter whose PL centered at around 1275 nm (0.97 eV). The origin of these emitters has remained unidentified as well as the spin properties. We also mention that defect spins were observed by electrical detected magnetic resonance in 4H SiC diodes which could be principally employed as light-weight magnetometers operating at harsh conditions, e.g. in space missions [149]. The origin of this defect has not yet been identified. Similarly, electrically detected magnetic resonance of carbon dangling bonds was reported at the Si-face 4H SiC/SiO<sub>2</sub> interface [150, 151].

## 17.4 Conclusion

We presented a brief summary about the recent advances of quantum technology research and development based on SiC platform. The advantageous electron spin coherence times of defects, the existing readout protocols, and other favorable magneto-optical properties of point defects make this platform very promising

in several fields, in particular, quantum sensing and quantum communication, integrated with semiconductor technology. The tight control of SiC growth and defect engineering should be further improved as well as understanding the intricate details of divacancies, Si-vacancies, and transition metal defects is a key to advance the field toward formation of SiC quantum industry.

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## Part II

### Gallium Nitride (GaN), Diamond, and Ga<sub>2</sub>O<sub>3</sub>

## 18

### Ammonothermal and HVPE Bulk Growth of GaN

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#### 18.1 Introduction

For the last three decades, the nitride community has struggled with crystallization of bulk gallium nitride (GaN) and fabrication of native substrates. The most popular GaN-based devices, light-emitting diodes (LEDs), are built on foreign sapphire substrates. Silicon wafers are often used by academic facilities, but no spectacular improvement in LEDs fabricated on Si is observed. In the case of nitride-based electronic devices, high electron mobility transistors (HEMTs) are prepared today mainly on silicon substrates. A few kinds of devices have already been commercialized <https://www.infineon.com/cms/en/product/power/gan-hemt-gallium-nitride-transistor/>. It seems, however, that a long and bumpy road is ahead of the industry in order to achieve a full commercial success, comparable to that of LEDs. No doubt, the lack of native wafers, of high structural quality and appropriate size as well as properties, limits the development of all GaN-based electronic devices. Highly conductive native substrates are required for preparing high-power vertical transistors or diodes. Obviously, availability of semi-insulating gallium nitride (SI-GaN) substrates for making lateral devices (i.e. HEMT transistors) also remains an open issue. Therefore, the nitride community is still looking for the best technology to fabricate GaN substrates. For many years, work on developing bulk GaN has mainly been motivated by the laser diode market. Today, the main driving force for crystallizing bulk GaN seems to be the electronic industry. However, synthesizing GaN is quite a challenging process. The compound melts at extremely high temperature (exceeding 2200 °C), and the nitrogen pressure necessary for congruent melting of GaN is expected to be higher than 6 GPa [1–3]. Thus, today, it is impossible to crystallize GaN from the melt. This compound should be grown by other techniques requiring lower pressure and temperature. Crystallization from gas phase, solution, or any combination

thereof must be included. Three main technologies are applied for obtaining GaN: sodium flux, ammonothermal, and halide vapor phase epitaxy (HVPE). The first two represent crystallization from solution, the third one from vapor phase. There are also some modifications of these methods, especially for vapor phase, i.e. halide free vapor phase epitaxy or oxide vapor phase epitaxy (HFVPE [4–6] and OVPE [7], respectively). Recently, a growing interest in GaN substrates has been observed as well as an increase in their production volume. They are mainly fabricated in Japan. Companies like SCIOCS by Sumitomo Chemical ([https://www.sciocs.com/english/products/GaN\\_substrate.html](https://www.sciocs.com/english/products/GaN_substrate.html)), Sumitomo Electric Industries (SEI) ([https://global-sei.com/sc/products\\_e/gan](https://global-sei.com/sc/products_e/gan)), Mitsubishi Chemical Corporation (MCC) ([https://www.m-chemical.co.jp/en/products/departments/mcc/nes/product/1201029\\_9004.html](https://www.m-chemical.co.jp/en/products/departments/mcc/nes/product/1201029_9004.html)), or Furukawa (<https://www.furukawakk.co.jp/e/business/others>) can produce 2-in. and even 4-in. HVPE-GaN substrates. Mostly, highly conductive (n-type) substrates (GaN doped with silicon or/and germanium) are sold. SI-GaN doped with iron is available too. HVPE-GaN wafers are also offered by the Chinese company Nanowin (undoped, highly conductive doped with silicon, and SI wafers doped with iron) (<http://en.nanowin.com.cn/>) as well as by the French company Lumilog (undoped, highly conductive doped with silicon, and SI wafers doped with iron) (<https://www.ceramicmaterials.saint-gobain.com/lumilog>). The latter belongs to the Saint Gobain concern. Obviously, many companies work on fabricating bulk GaN without any special publicity. They develop not only HVPE method but also ammonothermal or sodium flux ones. Herein, MCC, working on ammonothermal crystallization of GaN, can be a good example ([https://www.m-chemical.co.jp/en/products/departments/mcc/nes/product/1201029\\_9004.html](https://www.m-chemical.co.jp/en/products/departments/mcc/nes/product/1201029_9004.html)) [8, 9]. Besides, MCC the ammonothermal method is advanced by such companies as SixPoint Materials Inc. (USA) [10] or (most probably) Kyocera (formerly a crystal growth division at Soraa, Inc., USA/Japan) [11]. However, ammonothermal GaN (Am-GaN) substrates produced by these mentioned companies are not yet available on a large scale on the market. Am-GaN wafers, highly conductive and SI, are mainly sold by the Institute of High Pressure Physics of the Polish Academy of Sciences (IHPP PAS) (<https://www.unipress.waw.pl/growth/index.php/ammono-gan-wafers-sales>). The Institute is the owner of, formerly, company Ammono S.A. In turn, the sodium flux method is developed at Osaka University, an academic institution [12]. Any guesses that some companies are working on this method can only come from a detailed patent analysis. Two-inch sodium flux crystals of high structural quality were demonstrated [13]. However, they are not available on the market. In the academic world, many institutes and universities work on bulk GaN growth. They include Tokyo University of Agriculture and Technology [14], Tohoku University [15], Yamaguchi University [16], and University of California Santa Barbara [17]. It should, however, be noted that up to now, no one has demonstrated a real bulk GaN crystal yielding several 10 of wafers per boule as well as a convenient technology for obtaining it. Reasons for lack of thick GaN will be discussed in this chapter in detail. It will be shown that due to anisotropy of the growth and crystallization occurring in the lateral directions during the growth

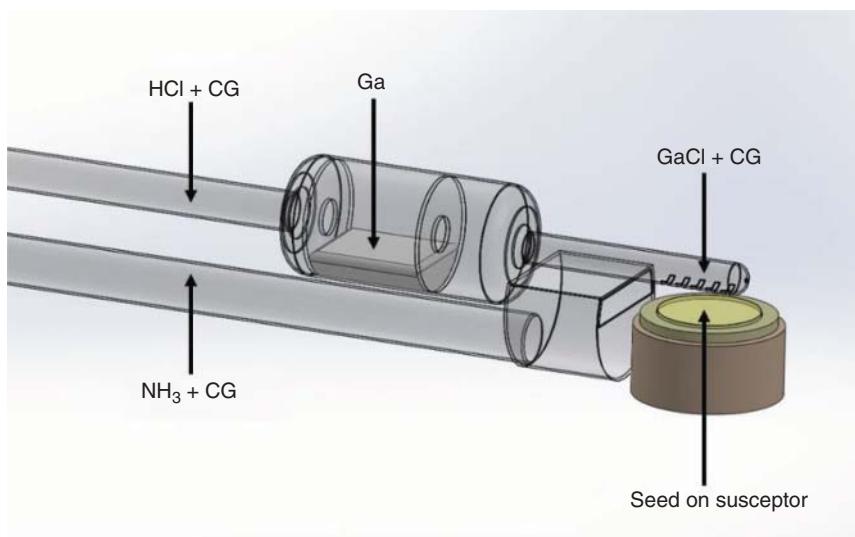
process in the chosen vertical direction, obtaining real bulk of GaN is difficult, even if native high structural quality seeds are used.

In this chapter, results of GaN bulk growth performed in Poland will be presented. Our description will be based only on crystals obtained by the team working at IHPP PAS, unofficially called Unipress. Two technologies will be described in detail: HVPE and basic ammonothermal. The processes and their results (crystals) will be demonstrated. Some information about wafering procedures, thus the way from as-grown crystal to an epi-ready substrate, will be shown. Results of other groups in the world will be briefly presented as the background for our work. The beginning of the chapter will focus on the history as well as state of the art of HVPE and ammonothermal methods. Then, HVPE deposited on native seeds (ammonothermally grown crystals) will be demonstrated. The crystallization results will be compared to those of basic ammonothermal method. The advantages, disadvantages, and challenges of both technologies will be discussed. A few solutions for further development of bulk GaN growth will be shown. Since the HVPE technology enables to obtain high-purity material (low concentration of unintentionally incorporated dopants and carrier concentration), the doping procedures for crystallizing highly conductive and highly resistive crystals will be analyzed. Doping bases on introducing silicon or germanium (for obtaining n-type material) and carbon, iron, and manganese (for SI-GaN). At the end of the chapter, all the described results will be summarized.

## 18.2 HVPE Method – History and State of the Art

As mentioned in the Introduction, the HVPE method is the crystallization from gas phase. Hydrochloride reacts with liquid gallium at relatively low temperature (800–900 °C) forming gallium chloride (GaCl). In this temperature range, the partial pressure of GaCl is much higher than that of GaCl<sub>3</sub>. Therefore, formation of GaCl is more favorable [14]. The latter is transported by the carrier gas (CG, mainly hydrogen or nitrogen) to the crystal growth zone (at temperature of 1000–1100 °C) where a seed is placed. Herein, GaCl reacts with ammonia (NH<sub>3</sub>) to synthesize GaN. The scheme of HVPE method is presented in Figure 18.1.

GaN was crystallized for the first time by HVPE in 1968. Maruska and Tietjen [18] used a sapphire wafer as a seed. They grew a GaN layer and determined the energy of the direct bandgap of 3.39 eV. A high free carrier concentration (above 10<sup>19</sup> cm<sup>-3</sup>) was reported. It was suggested that the reason of such a high value was the presence of nitrogen vacancies. Most probably, this statement was not true. At that time, commercially available ammonia contained 1000 ppm of water [19]. It was impossible, thus, to fabricate high-purity GaN. Unquestionably, GaN grown by Maruska was unintentionally doped with oxygen. Today, the highest purity GaN crystallized by HVPE contains less than 10<sup>14</sup> cm<sup>-3</sup> of unwanted impurities [20]. All reactant gasses as well as gallium are of high purity (6 N or higher). Also, some new special materials, as pyrolytic graphite, boron nitride, tantalum carbide, tungsten carbide, and similar, are applied in place of commonly used quartz for building the

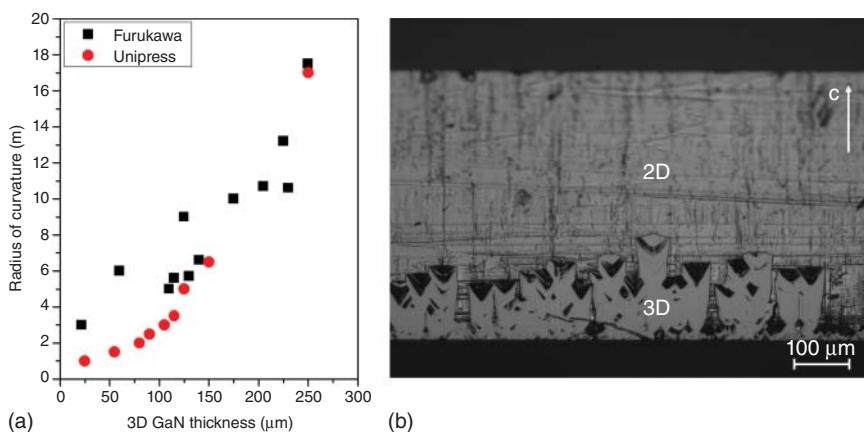


**Figure 18.1** Scheme of the HVPE method; horizontal configuration is presented; similar configuration based on quartz material is applied at Unipress; CG, carrier gas.

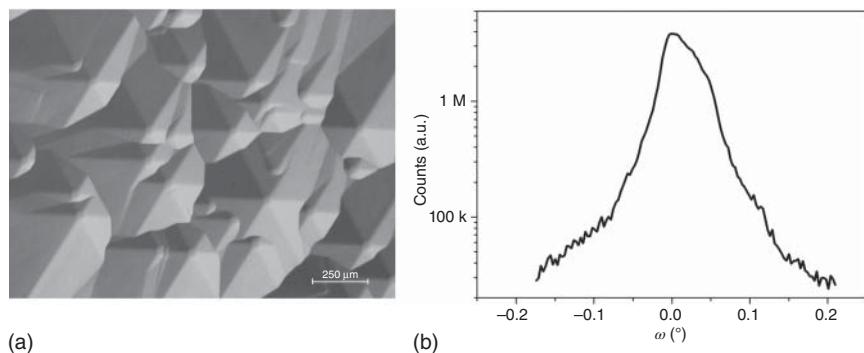
entire reactor or its crystal growth zone. Next to the purity, the second advantage of the HVPE method is the high growth rate. It is relatively easy to crystallize GaN in the  $\langle 0001 \rangle$  crystallographic direction (*c*-direction) with a rate of 100–200  $\mu\text{m}/\text{h}$ . A record value was reported by SCIOCS. Yoshida et al. [21] crystallized 800- $\mu\text{m}$ -thick GaN with a rate of 2 mm/h. The main problem in the HVPE technology is the kind of the used seed. As was already shown, the first “historical” candidate was sapphire. Since the 1990s, templates comprising a GaN layer grown by metal organic vapor-phase epitaxy (MOVPE) on sapphire have been used as seeds. Due to mismatch in both lattice constant and thermal expansion coefficient, GaN grown in the *c*-direction on sapphire templates was cracked. It was, however, observed that if a GaN layer was thick enough, it detached from the foreign seed. In order to obtain a regular habit of the separated crystal, it was necessary to control the lift-off process. One way of achieving that will be briefly described later. The next candidate for a foreign substrate in HVPE-GaN growth was gallium arsenide (GaAs). The value of its thermal expansion coefficient (at 1000 °C) is similar to the one of GaN. Gallium arsenide, unlike sapphire, can be easily removed by etching from the HVPE-GaN layer. Kumagai et al. [22] demonstrated a low-temperature GaN buffer layer on the GaAs(111)A surface. This accomplishment was a real breakthrough in HVPE-GaN growth. SEI developed dislocation elimination by the epitaxial growth with inverse pyramidal pits (DEEP) and advance-dislocation elimination by the epitaxial growth with inverse pyramidal pits (A-DEEP) technologies and fabricated quasi-bulk GaN. The substrates consisted of areas (e.g. arranged in stripes) of high ( $10^8 \text{ cm}^{-2}$ ) and low ( $10^4 \text{ cm}^{-2}$ ) dislocation density [23–25]. DEEP and A-DEEP approaches will not be described in detail in this chapter. It should be, however, noted that laser diodes applied in BluRay are built on the A-DEEP SEI GaN substrates [23]. In spite

of all, more companies and academic institutions prefer MOVPE-GaN/sapphire templates as seeds for HVPE-GaN growth. As mentioned above, some tricks to obtain the lift-off of the new-grown GaN from sapphire were needed. One of the proposed methods was void assisted separation (VAS) [26–28]. It involved the formation of voids between the template and the new-grown HVPE-GaN. A thin titanium layer was deposited on the surface of an MOVPE-GaN/sapphire template. The layer was annealed in ammonia atmosphere to form a TiN nanonet. Due to GaN, decomposition voids were formed under the nanonet. Next, during HVPE growth, the GaN layer nucleated through the openings in TiN and the voids remained on the GaN-sapphire interface. Stress induced by the difference in thermal expansion coefficients of HVPE-GaN and sapphire resulted in a well-controlled self-separation of GaN during the cooling process in HVPE. Free-standing (FS) crystals and then, after proper wafering procedures: grinding, lapping, mechanical, and chemo-mechanical polishing, GaN substrates were obtained. As mentioned in the Introduction, 2- and 4-in. GaN wafers, with their (0001) plane (c-plane) prepared to the epi-ready state, are offered by a few companies. They apply VAS or its derivatives for growing GaN. The main problem of such substrates is the bending of their crystallographic planes. The wafer is macroscopically flat and has two parallel surfaces. However, the angle between the crystallographic planes and the surface of the substrate (misorientation angle) changes. Therefore, a uniform misorientation of the wafer is difficult or often simply impossible. The main trick used to reduce the bending of the crystallographic planes is to start the crystallization process in a three-dimensional (3D) growth mode and change it in time (by changing the supersaturation) into a two-dimensional (2D) one. This solution was demonstrated by Geng et al. [29]. The intrinsic strain, the driving force of the wafer bending, can be reduced by the introduction of a 3D growth in the initial crystallization stage. Bending is, thus, controlled by the thickness of the 3D GaN layer. It is clearly shown in Figure 18.2a where the radius of curvature (bending of crystallographic planes) is presented as a function of the thickness of the 3D GaN layer. Figure 18.2b represents images of a cross section (m-plane) of GaN grown on a sapphire template at Unipress. The sample was photo-etched. In this technique, the etching rate depends on the free carrier concentration in the material and crystal sectors with different electrical properties can be visualized. The 3D and 2D growth modes can be well distinguished.

Figure 18.3a presents a typical morphology of 1-mm-thick GaN deposited on an MOVPE-GaN/sapphire template. Many hillocks are visible. Figure 18.3b shows a rocking curve of a FS GaN crystal (as-grown) obtained after crystallization on such a seed. The full width at half maximum (FWHM) for (00.2) reflection is close to 150 arcsec. The X-ray beam size was 1 mm × 10 mm. The etch pit density (EPD) and, correlated with it, threading dislocation density (TDD) in FS HVPE-GaN are on the order of  $1\text{--}5 \times 10^6 \text{ cm}^{-2}$ . Generally, GaN crystals grown on foreign seeds have a thickness of 1–2 mm and one well-developed facet, c-plane. From a sapphire seed, one GaN crystal and, after wafering, one substrate are fabricated. Therefore, it usually is a wafer to wafer technology. Fujito et al. [30] succeeded, however, in presenting 2-in. in diameter and 5.8-mm-thick bulk GaN. It allowed to fabricate a few wafers from one HVPE process.



**Figure 18.2** (a) Radius of curvature (bending of crystallographic planes) as a function of 3D GaN layer thickness; data from Unipress and Furukawa [29] are presented; (b) optical microscopy image of cross section of GaN grown on MOVPE-GaN/sapphire; sample was photo-etched; 3D and 2D growth modes are well visible. Source: Data from Geng et al. [29]



**Figure 18.3** (a) Morphology of 1-mm-thick GaN grown by HVPE on MOVPE-GaN/sapphire; view on the c-plane; (b) X-ray rocking curve for FS HVPE-GaN (as-grown) crystallized before on MOVPE-GaN/sapphire; FWHM for (00.2) reflection is close to 150 arcsec.

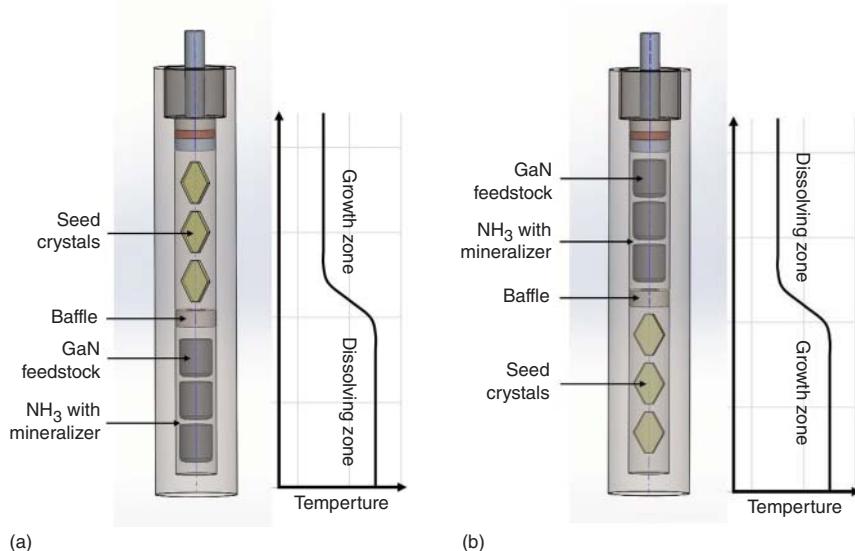
Typical unintentionally doped (UID) GaN grown on a foreign (sapphire) seed by the HVPE method is n-type with the free carrier concentration on the order of  $10^{16} \text{ cm}^{-3}$ . Doping with silicon and/or germanium to obtain n-type crystals and iron or carbon for fabricating SI-GaN is commonly used and described in detail in the literature (e.g. [31–34]).

### 18.3 Ammonothermal Method – History and State of the Art

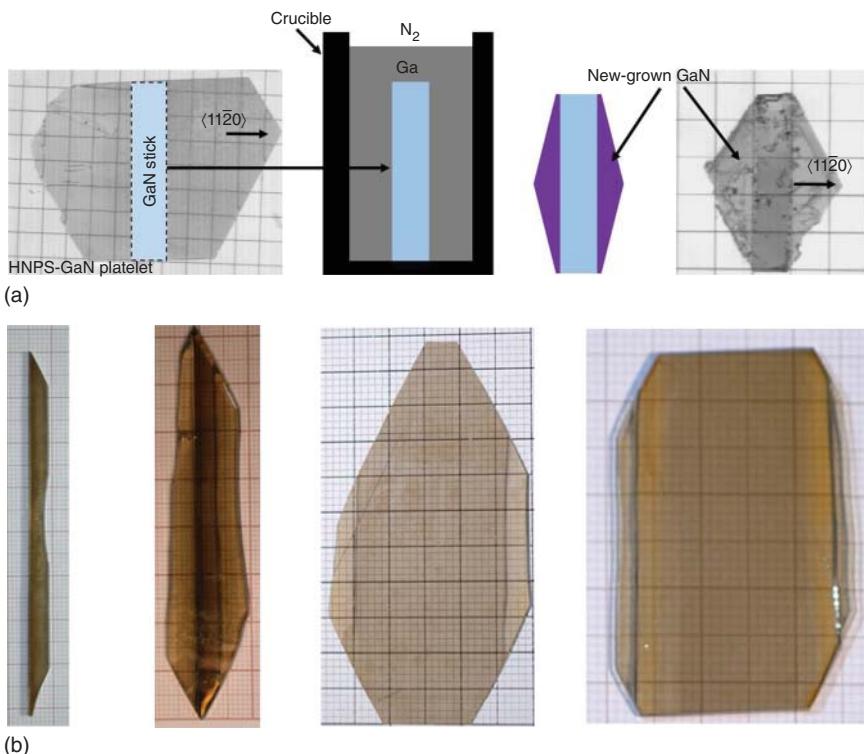
Ammonothermal crystallization is analogous to hydrothermal growth used for the production of quartz [35]. The difference lies in using supercritical ammonia instead of water. In an ammonothermal process, GaN feedstock is dissolved in supercritical

ammonia in one zone of a high-pressure autoclave. The dissolved material is transported to the second zone, in which the solution is supersaturated and GaN crystallization on native seeds takes place. The convection mass transport is enabled by an appropriate temperature gradient between the two zones. Different mineralizers can be added to ammonia in order to accelerate its dissociation and enhance the solubility of GaN. The choice of applied mineralizers determines the type of environment: acidic or basic. In ammonoacidic growth, halide compounds (with  $\text{NH}_4^+$  ions) are introduced into the supercritical solution. Alkali metals or their amides (with  $\text{NH}_2^-$  ions) are used in the case of ammonobasic crystallization. In the latter approach, a negative temperature coefficient of solubility is observed (<https://www.linkedin.com/pulse/mystery-solubility-retrograde-temperature-inverse-why-mukherjee>). This results in the direction of the chemical transport of GaN from the low-temperature solubility zone (with feedstock) to the high-temperature crystallization one (with seeds). Figure 18.4 shows schemes of acidic and basic ammonothermal process. Typical pressures and temperatures during ammonothermal crystallization vary from 1000 to 6000 atm and 300–750 °C, respectively.

As mentioned, native seeds, usually FS HVPE-GaN, are used in the ammonothermal process. They are mainly up to 1-mm-thick crystals with well-developed c-planes. This results from a habit of HVPE-GaN deposited before on a foreign foundation (MOVPE-GaN/sapphire; see 18.2). Thus, the main growth directions in the ammonothermal method are  $\langle 0001 \rangle$  or  $\langle 000\bar{1} \rangle$  (the  $-c$ -direction). Obviously, using FS HVPE-GaN as seeds does not allow to obtain high structural quality of Am-GaN since the crystallographic quality of the seed is low and can only be duplicated, but not improved. However, many results of such research were published (e.g. [36–38]). A breakthrough in the structural quality of Am-GaN was achieved by the Polish company Ammono (today IHPP PAS). Their solution involved seeded growth



**Figure 18.4** Scheme of the ammonothermal method (a) acidic; (b) basic.

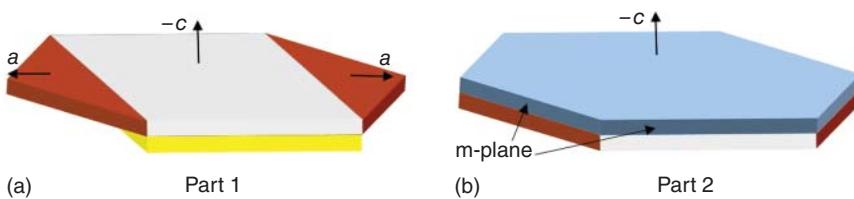


**Figure 18.5** (a) Scheme of HNPS growth presented by Grzegory et al. [39]; the idea as well as resulting HNPS-GaN crystal are presented; GaN stick was overgrown in the  $a$ -directions; new-grown material was nucleated from the edges of the seed and was defect-free; grid 1 mm; (b) same growth method applied at Ammono Company; results of GaN stick overgrowth during many crystal growth processes; grid 1 mm. Source: Grzegory et al. [39].

and was based on an idea which had been presented in the high nitrogen pressure solution (HNPS) method [39]. Grzegory used a GaN stick, previously sliced from a bigger HNPS-GaN platelet crystal. Such a seed was vertically placed in a crucible with liquid gallium. The high nitrogen pressure crystallization process occurred mainly in the fastest growth directions  $\langle 11\bar{2}0 \rangle$ , the  $a$ -directions. The new-grown material was nucleated on the edges of the stick, and, therefore, it was defect-free. The scheme of the method applied by Grzegory is presented in Figure 18.5a. In turn, Figure 18.5b shows the approach of Ammono Company. A long HVPE-GaN stick was overgrown in the  $a$ -directions until the  $\langle 11\bar{2}0 \rangle$  facets disappeared and the  $\langle 10\bar{1}0 \rangle$  facets (m-facets) appeared. After many ammonothermal runs, a crystal with a big lateral surface could be obtained from a thin seed.

Today, the basic Am-GaN growth developed at IHPP PAS consists of two parts described below and schematically shown in Figure 18.6:

**Part 1 – Enlargement of seeds:** The seeds can be enlarged by taking advantage of lateral crystallization in the  $a$ -direction (the red part of the crystal in Figure 18.6a), and their diameter can reach more than 2 in.



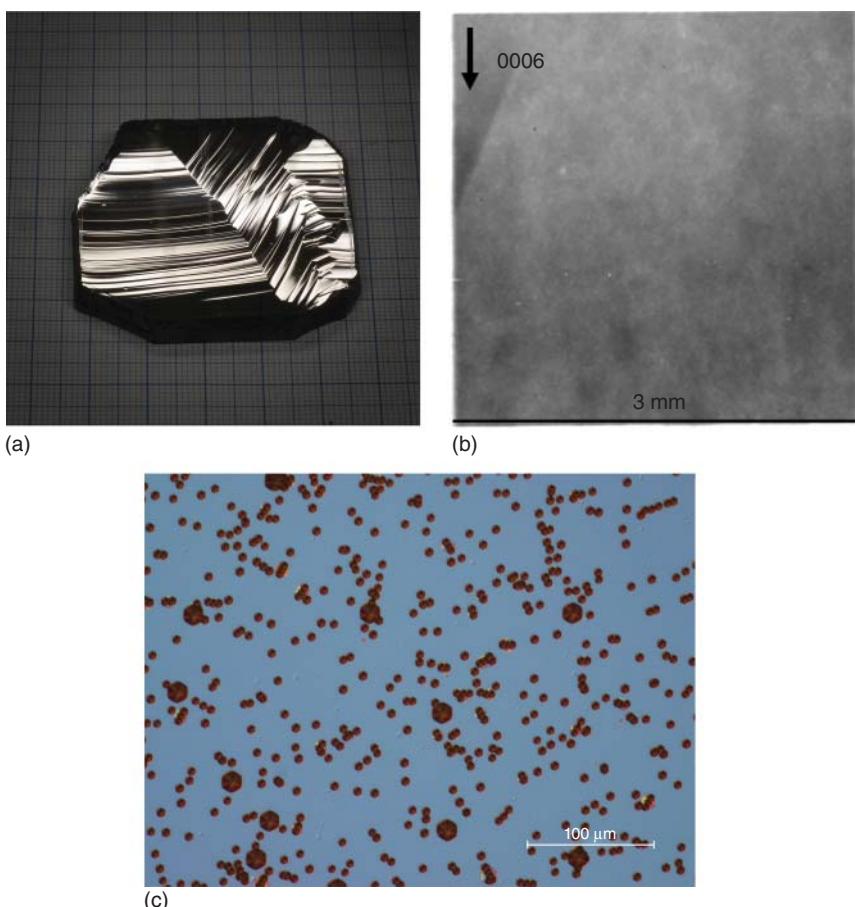
**Figure 18.6** Basic ammonothermal growth method (two processes); (a) part 1 – the seed is enlarged in lateral directions; (b) part 2 – the seed is only grown in  $-c$ -direction; the  $(10\bar{1}0)$  facets (m-planes) are visible.

**Part 2 – Multiplication of seeds:** Growth is performed mainly in vertical direction, along  $c$ -axis (the blue part of the crystal in Figure 18.6b). The crystal is sliced perpendicularly to the  $c$ -direction. Population of the seeds used for subsequent ammonothermal or/and wafering process (GaN substrate fabrication) is increased. The crystals are structurally flat, and the EPD is on the order of  $5 \times 10^4 \text{ cm}^{-2}$ .

Figure 18.7a shows a typical growth morphology of basic ammonothermal grown crystal. Hillocks and huge macrosteps are well visible. Results of synchrotron white-beam X-ray topography (SWXRT) for Am-GaN are depicted in Figure 18.7b. It can be seen that the crystal is of extremely high structural quality and crystallographic uniformity. Figure 18.7c presents the etch pits created after defect selective etching (DSE, etching in KOH/NaOH solution at  $500^\circ\text{C}$ ) in the material grown in the  $-c$ -direction (the blue part of the crystal in Figure 18.6b). Value of EPD was  $5 \times 10^4 \text{ cm}^{-2}$ .

Today, IHPP PAS crystallizes three kinds of Am-GaN. Their main electrical properties are presented in Table 18.1. Figure 18.8 shows substrates obtained by wafering procedures (slicing, grinding, lapping, mechanical polishing, and chemo-mechanical polishing) from material of properties analyzed in Table 18.1. The main dopant in Am-GaN crystals is oxygen. The free carrier concentration is usually equal to the concentration of this element. Using some getters, one can decrease the oxygen content to  $1 \times 10^{18} \text{ cm}^{-3}$ . For growing semi-insulating material, the donors are compensated by manganese acceptors. A lot of information about ammonothermal process and properties of Am-GaN crystals and substrates can be found in Refs [40–42].

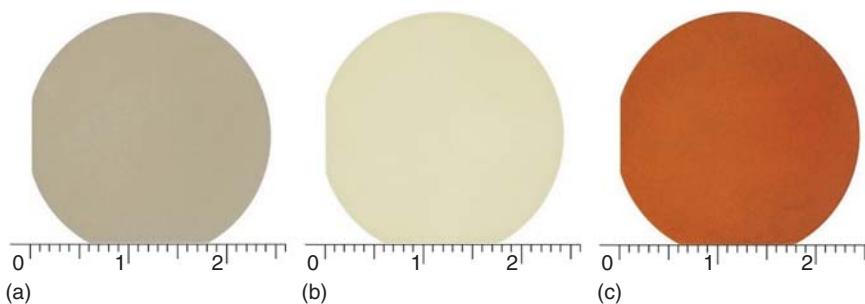
An interesting feature of Am-GaN with the highest carrier concentration is the formation of star-like defects after annealing at temperature on the order of the  $1000^\circ\text{C}$ . After this process (or epitaxial growth on an Am-GaN wafer), some defects can appear in the volume of the ammonothermal material. They are clearly shown in Figure 18.9a which presents an image from an optical microscope focused in the volume of the crystal. Horibuchi et al. [43] explained the process of their formation. As was reported [44, 45], ammonothermally grown crystals with a high oxygen (and free carrier) concentration contain a significant number of gallium vacancies ( $10^{19} \text{ cm}^{-3}$ ) or their complexes with oxygen or hydrogen. At high temperature, the vacancies migrate to dislocation lines forming helical dislocations. It is interesting that these helical dislocations cannot propagate into the overgrown epitaxial



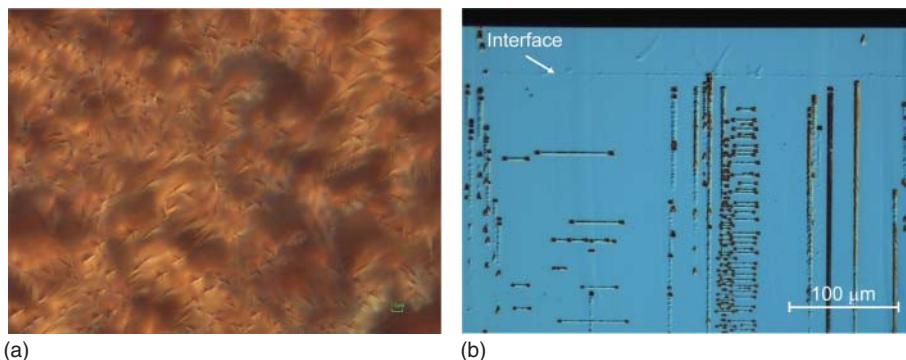
**Figure 18.7** (a) Morphology of Am-GaN grown in the  $-c$ -direction; (b) synchrotron white-beam X-ray topography (SWXRT) for a 1-in. Am-GaN crystal; uniform gray contrast indicates a low defect density. Source: Courtesy of L. Kirste; grid 1 mm; (c) EPD in the material grown in the  $-c$ -direction (the blue part of the crystal grown in Figure 18.6b); EPD =  $5 \times 10^4 \text{ cm}^{-2}$ .

**Table 18.1** Electrical properties (measured at room temperature using a home-built Hall effect system in van der Pauw configuration) of three types of ammonothermal GaN.

Material type	Conductivity type	Carrier concentration ( $\text{cm}^{-3}$ )	Carrier mobility ( $\text{cm}^2/\text{V s}$ )	Resistivity ( $\Omega \text{ cm}$ )
High carrier concentration	n-type	$\sim 10^{19}$	$\sim 150$	$10^{-3}$
Low carrier concentration	n-type	$\sim 10^{18}$	$\sim 250$	$10^{-2}$
High resistivity (Mn-doped)	Semi-insulating	—	—	$\geq 10^8$



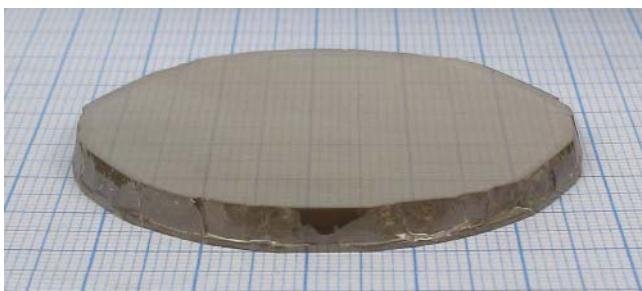
**Figure 18.8** Am-GaN substrates prepared by IHPP PAS (a) n-type with a carrier concentration of  $10^{19} \text{ cm}^{-3}$ ; (b) n-type with a carrier concentration of  $10^{18} \text{ cm}^{-3}$ ; (c) semi-insulating doped with Mn; diameter in cm.



**Figure 18.9** Star-like defects in highly conductive Am-GaN: (a) image from an optical microscope focused in the volume of the Am-GaN substrate after epitaxy process at  $1100^\circ\text{C}$ ; star-like defects are well visible; (b) cross section, m-plane, of HVPE-GaN grown on highly conducting Am-GaN after DSE; helical defects are well visible in the Am-GaN crystal; they do not propagate into the HVPE-GaN layer.

layer. The defects are stopped at the interface or just before it. It is clearly seen in Figure 18.9b. A differential interference contrast (DIC) microscopy image of an m-plane cross section of HVPE-GaN grown on highly conducting Am-GaN is shown after DSE. The helical defects are well visible in the Am-GaN crystal, but they do not propagate into the HVPE-GaN layer.

One of the most important factors limiting the Am-GaN crystallization in the  $-c$ -direction is associated with the anisotropy of the growth. Apart from the  $\langle 0001 \rangle$  direction, crystallization also occurs in the lateral directions at the edges of the crystal, on the m-facets (see Figure 18.6b). This phenomenon was well described by Zajac et al. [42]. It was shown that kinds and concentrations of impurities incorporated into non-polar  $(10\bar{1}0)$  facets as well as on the  $(000\bar{1})$  plane are vastly different. This causes stress and finally leads to plastic deformation of the growing Am-GaN crystals. The donors' concentrations are higher on the  $-c$ -plane and much lower on the side facets. Additionally, higher concentrations of acceptors (C, Fe, Mn, Mg, and others) are detected in the laterally grown GaN.

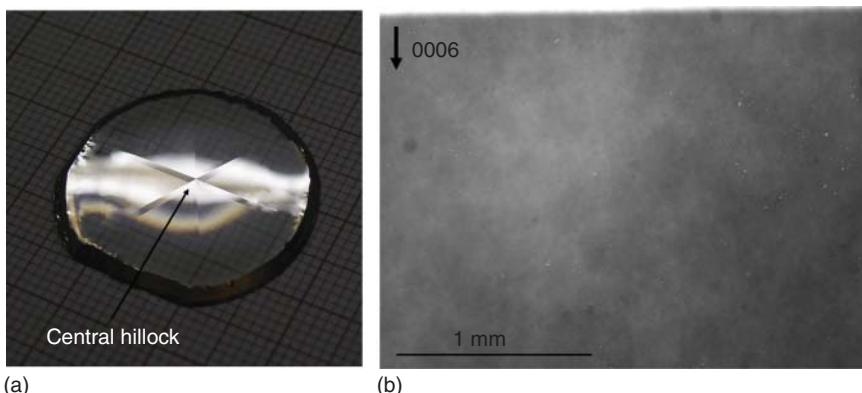


**Figure 18.10** Am-GaN crystal grown in one crystallization run: 6-mm-thick and with a 2.1-in. diameter; grid 1 mm.

In the basic ammonothermal method, the growth in the  $\langle 0001 \rangle$  direction is treated as parasitic. As a result, the  $(000\bar{1})$  surface is exposed, while the opposite  $(0001)$  face is completely masked. Similar approach can be used for blocking the crystallization on the side facets. In this case, mechanical blocking seems to be the best idea to hinder growth in directions other than the desired one. Figure 18.10 presents a 2.1-in. in diameter and 6-mm-thick GaN crystal obtained in one ammonothermal process with mechanically blocked side facets.

## 18.4 HVPE-GaN-on-Ammono-GaN – State of the Art

HVPE-GaN growth on native ammonothermal seeds seems to be a very perspective technology. First official communications about the combination of the two GaN crystallization methods came from Unipress [46, 47]. Using 1-in. Am-GaN substrates with their c-planes prepared to the epi-ready state, HVPE-GaN crystallization with high growth rate, up to  $350 \mu\text{m/h}$ , was reported [48]. Up to 2-mm-thick HVPE-GaN was grown. In order to obtain FS material, the layer was sliced from the seed [49]. The observed morphology was one hillock on the entire crystal's growing surface (see Figure 18.11a). The almost perfect structural quality of ammonothermal seed was reflected by the HVPE layer (see Figure 18.11b) [49–51]. EPD on the c-plane was on the order of  $5 \times 10^4 \text{ cm}^{-2}$  [52]. The main impurities in UID HVPE-GaN were silicon and oxygen, at the level not higher than  $1 \times 10^{17} \text{ cm}^{-3}$ . Concentration of oxygen was often below the secondary ion mass spectrometry (SIMS) detection limit [53, 54]. Some traces of iron ( $1 \times 10^{16} \text{ cm}^{-3}$ ) were found. In the photoluminescence (PL) spectra, weak signals from magnesium were also observed [53]. In general, PL displayed multiple bound and free exciton peaks. The spectra were dominated by two sharp donor-bound exciton emission lines with extremely low values of FWHM. Acceptor-bound exciton and free exciton emissions were also present [47]. A weak signal in the yellow luminescence (YL) range was detected. It could be correlated with the gallium vacancies or their complexes with silicon or oxygen. HVPE-GaN is usually carbon-free; thus, YL cannot be connected to the presence of this element. No structure close to the band edge was observed in the absorption spectra [47]. Optical-isothermal capacitance transient spectroscopy (OICTS) and deep level

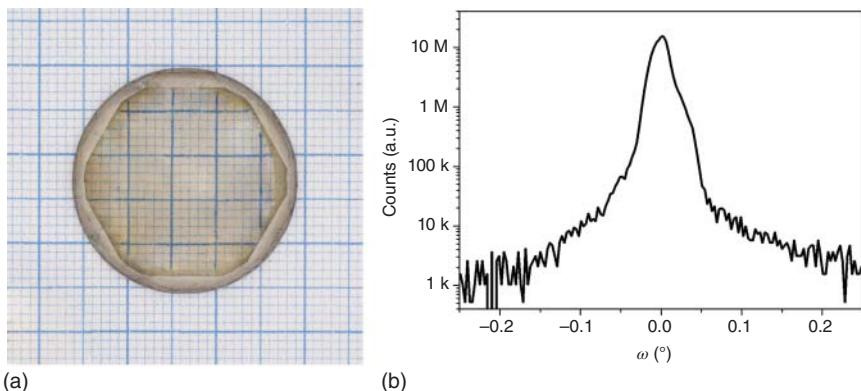


**Figure 18.11** (a) Typical morphology of HVPE-GaN grown on Am-GaN seed; one hillock is formed on the surface of the growing crystal; grid 1 mm; (b) SWXRT for FS 1-in.-HVPE-GaN grown before on Am-GaN seed; uniform gray contrasts indicate a high degree of crystalline perfection. Source: Courtesy of L. Kirste.

transient spectroscopy (DLTS) were carried out at Kyoto and Nagoya Universities to investigate hole (OICTS) and electron (DLTS) traps. The main trap detected with OICTS was H1 (0.85 eV above the valence band maximum) with a concentration below 1% of the net carrier concentration. This trap can be connected to the presence of carbon in GaN, and the low concentration is due to no contamination with carbon in HVPE-GaN. However, concentration of the main electron trap detected, E3, comprises 24% of the net carrier concentration (K. Kanegae, M. Horita, J. Suda, private communication). This trap, placed 0.56 eV below the conduction band minimum, could be correlated with substitutional defects or iron impurity. As mentioned above, some traces of iron were found in our HVPE-GaN samples.

#### 18.4.1 Bulk Growth – Challenges

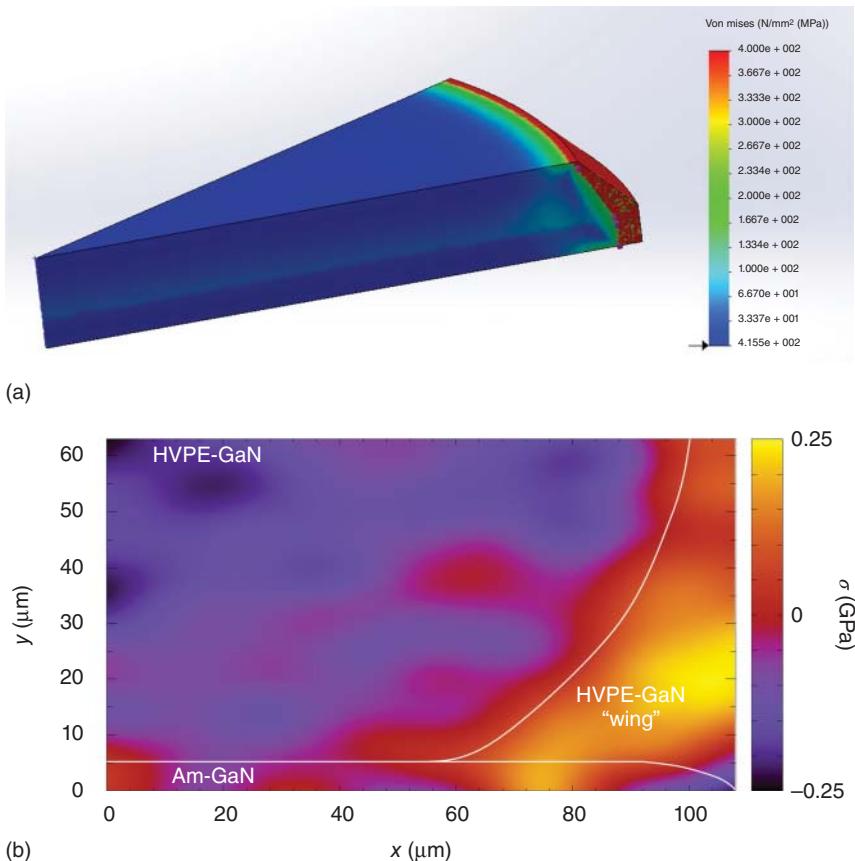
It was presented that thick HVPE-GaN layers can be grown on native ammonothermal seeds. MCC demonstrated 5.8-mm-thick HVPE-GaN crystallized in the  $\langle 10\bar{1}0 \rangle$  direction [9]. They used their own Am-GaN from the supercritical acidic ammonia technology (SCAAT) as a seed [8]. The technology was based on the already demonstrated result of growth of 5.8-mm-thick GaN on sapphire in the c-direction [30]. However, the results of MCC seem unique. In most research facilities and companies, despite the high growth rate and purity, HVPE still remains a wafer-to-wafer technology. According to our knowledge, crystallization of thick boules even on perfect ammonothermal seeds is limited by two factors: (i) parasitic deposition occurring in the growth zone and (ii) anisotropy of the crystallization. Since bulk GaN should be grown over a long period of time, the parasitic deposition needs to be completely eliminated. It seems to be a purely technical issue. However, it is a very serious problem. From the scientific point of view, the supersaturation driving the GaN growth should exist only at the surface of the crystal. In all other areas of the reactor as well as close to the HVPE layer, the supersaturation for GaN



**Figure 18.12** (a) Three-mm-thick HVPE-GaN grown on Am-GaN; equilibrium hexagonal crystal habit is well visible; c-plane is reduced; grid 1 mm; (b) rocking curve for (0002) reflection of the same crystal with FWHM of 77 arcsec and bowing radius of 18.6 m; X-ray beam size: 1 mm  $\times$  10 mm.

formation should be close to zero or even negative. This is the first issue that should be addressed in order to obtain bulk GaN. The second important factor limiting depositing HVPE-GaN in the c-direction is associated with the anisotropy of the growth and crystallization occurring in lateral directions. During deposition in the  $\langle 0001 \rangle$  direction, even if it starts from a round shape of a seed, the natural hexagonal shape of GaN finally appears. As already mentioned, Fujito et al. [30] published a detailed discussion on the formation of a dodecagon shape of a crystal if a round substrate is used as a seed. For HVPE-GaN, the  $\langle 11\bar{2}0 \rangle$  is the fastest growth direction and the  $\langle 10\bar{1}0 \rangle$  direction is the slowest one. Therefore, during a crystallization process at first, all  $(11\bar{2}0)$  facets disappear and all  $(10\bar{1}0)$  facets appear and start to dominate. The inclined facets  $(10\bar{1}1)$  and  $(10\bar{2}2)$  on m-plane sides and  $(11\bar{2}2)$  facets on a-plane sides are formed [30]. The formation of this equilibrium shape through the collapse of the growth facet reduces the size of the c-plane. It is clearly shown in Figure 18.12a where 3-mm-thick HVPE-GaN from an Am-GaN seed is presented. The dodecagon shape changes into a hexagonal one. The size of the c-plane is reduced. Figure 18.12b shows a rocking curve for the presented as-grown crystal.

The next problem concerning thick GaN deposited in the c-direction is growth in the lateral directions. It was shown that the kinds and concentrations of impurities incorporated on non-polar and semi-polar facets and on the c-plane are different [77, 78]. This causes stress and finally leads to plastic deformation of the HVPE-GaN layer [49, 52]. SIMS measurements showed that the concentration of oxygen in GaN grown in the c-direction was extremely low, at the level of  $10^{16}$  cm $^{-3}$ . In turn, oxygen concentration in the laterally crystallized material (called wings) always reached  $10^{19}$  cm $^{-3}$ . The large content of dopants and high free carrier concentration lead to an increase of the lattice constants in GaN [55]. It was shown that both  $a$  and  $c$  lattice constants increased in the laterally grown GaN [56]. The experimental data of lattice constants were used for numerical simulations in order to determine and examine the stress in HVPE-GaN and the seed [57]. Figure 18.13a



**Figure 18.13** (a) Calculated Von Mises stress distribution in HVPE-GaN deposited on 1-in. Am-GaN seed; (b) Raman map of the stress distribution at the edge of the growing crystal (on 1-in. Am-GaN seed); the highest stress was detected in the material grown in lateral directions (wings).

shows the stress distribution in a 1.5-mm-thick layer crystallized on 600-μm-thick Am-GaN. The value of Von Mises stress in HVPE-GaN close to its center was very low, close to 2 MPa. At the interface between the crystal and laterally overgrown GaN, the stress reached 200 MPa. The highest value of maximum equivalent stress was obtained in the side area, and it exceeded 1200 MPa. The strain in HVPE-GaN grown in the c-direction on a native seed was also studied by Raman spectroscopy [58]. The stress of 200 MPa in the wing area was determined (see Figure 18.13b). Again, it was concluded that the non-polar and semi-polar growth of GaN leads to the formation of large stress in the crystal, close to its edges. This stress is much more significant than that generated by the lattice mismatch between the seed and the deposited layer. It should herein be noted that this is a common problem of GaN bulk growth. At the end of 18.3, a similar phenomenon was described for basic ammonothermal method. The situation, however, is opposite to the one described for HVPE. Concentrations of donors are higher on the -c-plane and much lower on the side facets. In the case of Am-GaN, it is difficult to control the conditions on

the particular surface of each crystal. There are too many seeds in the growth zone. Nevertheless, it seems possible in the HVPE technology. Herein, the supersaturation on the surface of the crystal can be strictly controlled. It can be drastically reduced on the edges and sidewalls. Only one growth facet (*c*-facet) can be stabilized and grown out for an arbitrary time period. According to a hypothesis by Professor Zlatko Sitar, this condition may be achieved by controlling the thermal field around the crystal. It has to reach its final shape by adapting to the thermal field rather than taking the equilibrium hexagonal habit. This was demonstrated for aluminum nitride (AlN) growth by physical transport deposition (PVT) and presented on HexaTech web page (<http://www.hexatechinc.com/company.html>). An AlN crystal assumes the round shape from the seed and expand as forced by the designed thermal field. Once the crystal reaches a constant thermal field, it resumes the equilibrium shape as dictated by the surface energetics, forming various facets. This clearly shows that the equilibrium shape can be overpowered by a proper thermal field design. In this case, the crystal will follow the thermal field and grow in a direction perpendicular to the isotherms. Obviously, there is a big difference in the formation of supersaturation in PVT and HVPE methods. The supersaturation is the difference of thermodynamic potentials at the interface between a crystal and its environment. In the case of PVT, it is almost unambiguous with the temperature distribution on the growing surface. In the case of HVPE, reactions of all vapor species should be considered.

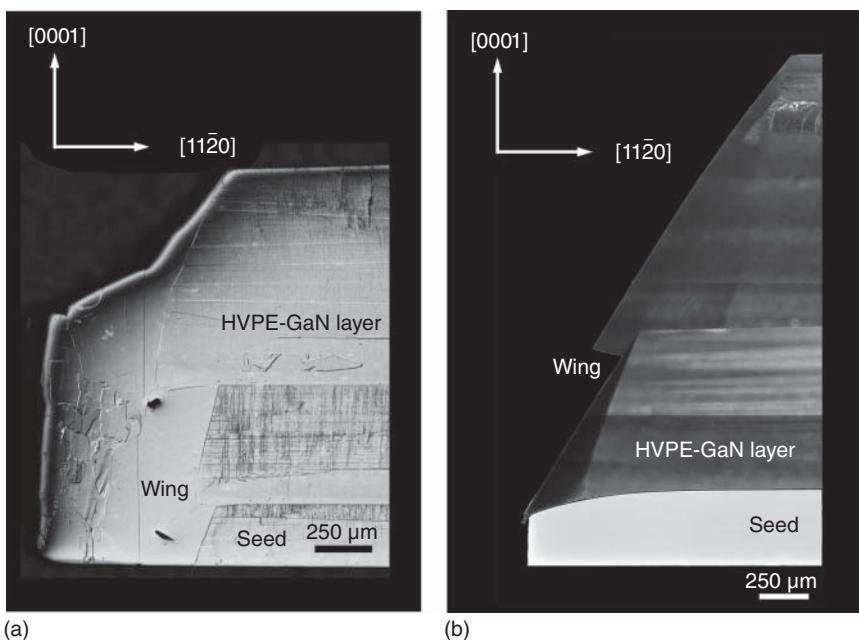
First attempts to change the environment of deposited HVPE-GaN have already been made. Some metal (molybdenum, Mo) elements were added around the crystal. Molybdenum can switch the thermal field as well as catalyze ammonia decomposition in the growth zone. A large reduction in crystallization in lateral directions was observed. It is clearly seen in Figure 18.14. The edges of HVPE-GaN deposited without and with Mo are presented. The lateral growth was almost totally reduced when the HVPE process was additionally performed at a lower temperature, close to 1000 °C (in place of always applied 1045 °C). All these results allow to look optimistically into the future of bulk GaN growth. Still, the highest pressure must be put on obtaining the right temperature gradient on the crystal's growing surface.

### 18.4.2 Doping

As mentioned before, doping in HVPE method allows to fabricate highly conductive and semi-insulating GaN crystals and then substrates. Usually, growth is performed on foreign seeds, mainly MOVPE-GaN sapphire templates. Therefore, the stress in the layer is completely different than that in HVPE-GaN grown on native seeds. Below, the latter case will be described in detail for GaN doped with silicon, germanium, carbon, iron, and manganese. Some discrepancies with crystallization on foreign substrates will be pointed out.

#### 18.4.2.1 Doping with Donors

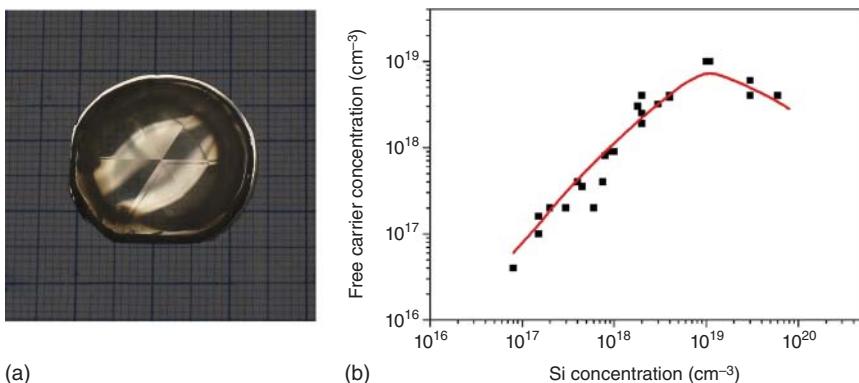
The most common n-type dopant for GaN is silicon. However, it is observed that with increasing Si concentration in GaN grown on a foreign seed, the tensile strain in deposited layers increases. It was published (see e.g. [59, 60]) that the use of Ge



**Figure 18.14** Edges of HVPE-GaN crystals grown (a) without Mo elements in the crystal growth zone; (b) with Mo elements in the crystal growth zone; reduction of the growth in the lateral directions is visible.

instead of Si as an n-type dopant can be helpful for solving this problem. The lattice distortion caused by Ge atoms substituting into Ga sites is very small due to their similar ionic radii [61]. Germanium is also a shallow donor in GaN, with an activation energy of 20 meV, which is similar to Si (17 meV) [62, 63]. Germanium can be introduced, thus, as a highly favorable n-type dopant in GaN. It leads to a smoother surface, lower film stress, and less TDD [64]. It should be noted that it was not observed in the case of GaN-on-GaN growth.

Dichlorosilane ( $\text{H}_2\text{SiCl}_2$ ) was used as a precursor of Si in HVPE processes. The precursor was supplied to the gallium source zone of the HVPE reactor. Adding  $\text{H}_2\text{SiCl}_2$  to the reactant gases caused no changes in the morphology of deposited crystals. The growth mode was governed by hillocks (see Figure 18.15a). The structural quality of the doped material was not deteriorated in comparison to the Am-GaN seed or UID HVPE-GaN. The EPD remained at the same low value. Opposite results were obtained for HVPE-GaN:Ge. In this case, the applied precursor was germanium tetrachloride ( $\text{GeCl}_4$ ). Crystallization in hydrogen carrier gas resulted in formation of pits on the surface. A morphologically stable growth, with hillocks visible on the c-plane, was enabled by using nitrogen as the carrier gas. The significant difference in morphology of HVPE-GaN:Ge deposited in different carrier gas was explained with the use of thermodynamic calculations [65]. In hydrogen, the equilibrium partial pressure of Ge was higher than the saturated vapor pressure of Ge. This led to the formation of Ge droplets on the surface of the growing crystal and, consequently, to the formation of pits on these droplets. The pits were not observed when nitrogen



**Figure 18.15** (a) Morphology of HVPE-GaN:Si; hillock growth mode; grid 1 mm; (b) free carrier concentration as a function of Si concentration in HVPE-GaN:Si; a knee of compensation is well visible.

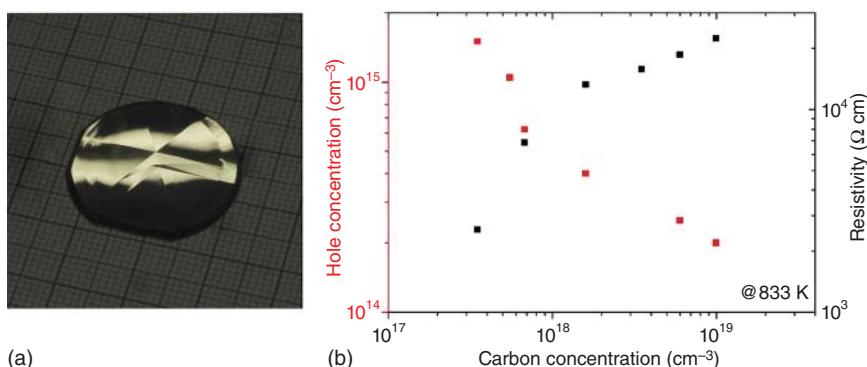
was the carrier gas. In this case, the equilibrium partial pressure of Ge was lower than the saturated vapor pressure of Ge. Thus, germanium droplets could not be formed and disturb the crystallization run. Growth with nitrogen as the carrier gas resulted in high-quality HVPE-GaN:Ge layers. However, they were not thicker than 500  $\mu\text{m}$ . When this value was exceeded, cracks appeared in the seed. The reason for this was the lattice mismatch between Am-GaN and HVPE-GaN:Ge. The  $a$  lattice parameter in HVPE-GaN:Ge was bigger than the  $a$  lattice parameter in Am-GaN. Therefore, the new-grown layer was always under compressive stress, and seed was under tensile stress. The stress force in GaN:Ge acted in an opposite direction than in the seed. Such phenomenon was never observed in the case of HVPE-GaN:Si. Herein, like in the case of UID-GaN, deterioration always started from the edges, due to the formation of wings (see Figures 18.13 and 18.14). Herein, it should be remarked that the role of wings has never been analyzed for HVPE-GaN:Ge.

The lattice parameters of GaN:Si were not strongly different from those of Am-GaN. In HVPE-GaN:Si, the free carrier concentration was on the order of  $1\text{--}6 \times 10^{18} \text{ cm}^{-3}$  with mobility  $300\text{--}170 \text{ cm}^2/\text{Vs}$  for different Si contents in the crystals. SIMS measurements performed on the c-plane showed that the Si concentration exceeded  $1 \times 10^{19} \text{ cm}^{-3}$ . The free carrier concentration was 1 order of magnitude lower than that of silicon. Most probably, a large fraction of electrons from silicon was compensated by some acceptor state. A possible explanation is that gallium vacancies and their complexes with Si were responsible for this effect. Low-temperature (15 K) photoluminescence spectra measured for Si-doped samples showed that the intensity of the YL signal increased with Si content. As mentioned, the HVPE technology is carbon-free. Thus, gallium vacancies and/or their complexes could be responsible for the YL. The second fact that indicated the existence of gallium vacancies complexes was the behavior of the free carrier concentration as a function of Si incorporated in the crystals. This dependence is presented in Figure 18.15b. When more Si atoms are detected by SIMS, the free carrier concentration (determined by Raman spectroscopy) increases reaching its

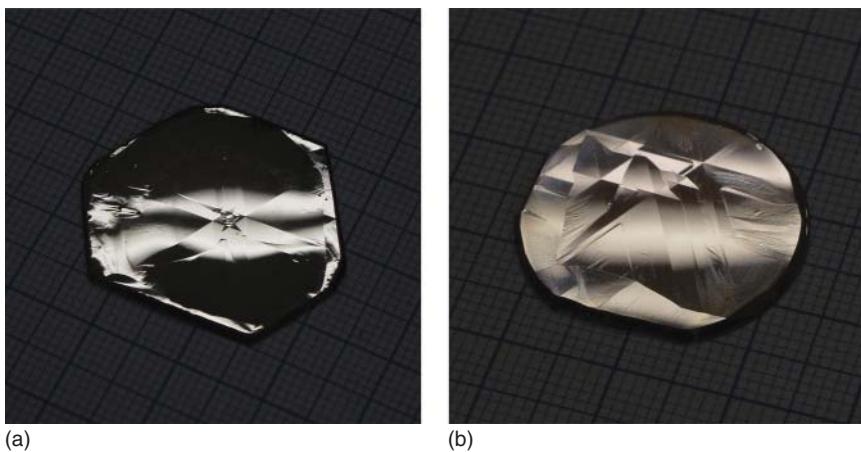
maximum value and then starts to decrease. No doubt, the silicon donors were compensated by some point defects. A similar behavior was observed for AlGaN doped with Si and theoretically explained by the formation of Ga vacancies – Si complexes [66]. It is interesting that the YL has never been observed in the case of GaN:Ge crystals. Additionally, the free carrier concentration measured by different methods (Hall, capacitance–voltage, Raman) was always equal to the Ge content in GaN.

#### 18.4.2.2 Doping with Acceptors

Methane ( $\text{CH}_4$ ) was used as a carbon precursor for crystallizing HVPE-GaN:C on Am-GaN seeds. The layers were up to 1 mm thick with C concentration varying from  $10^{17}$  to  $10^{19} \text{ cm}^{-3}$ . The morphology of the crystals was not changed; one or a few hillocks on the entire surface were always observed (see Figure 18.16a). The structural quality of the Am-GaN seeds was reflected by the layers. A dominating YL signal, much stronger than the near band edge luminescence, appeared in low-temperature PL spectra of GaN:C [67, 68]. Additionally, a small shift of the YL to higher energy (from 2.23 to 2.3 eV) was observed for highly doped ( $10^{19} \text{ cm}^{-3}$ ) material [68]. The crystals were highly resistive [69]. The value of resistivity at room temperature was too high to be measured, and it had to be extrapolated. HVPE-GaN:C showed p-type conductivity at high temperature. The hole concentration changed from  $\sim 10^{12} \text{ cm}^{-3}$  at 600 K to  $\sim 10^{15} \text{ cm}^{-3}$  at 1000 K. Hall method allowed to determine the activation energy of an acceptor level at around 1 eV [67]. This result was in good agreement with electron paramagnetic resonance (EPR) measurements [68, 70, 71]. They revealed the presence of a carbon-related defect in all samples which were photo-ionized with 1 eV light, thus, consistent with the presence of carbon at nitrogen site- $\text{C}_\text{N}$ . These results were also in good agreement with theoretical predictions for  $\text{C}_\text{N}$  in GaN [72, 73]. An interesting experimental observation is presented in Figure 18.16b. The resistivity and hole concentration in HVPE-GaN:C are shown as a function of carbon content for a chosen temperature value (833 K). One can see that for more carbon, the resistivity increases but the hole concentration decreases. Content of other impurities remained at the same



**Figure 18.16** (a) Morphology of HVPE-GaN:C; (b) resistivity and hole concentration as a function of carbon concentration [C] in HVPE-GaN:C; results prove the existence of additional point defects compensating deep carbon acceptors.



**Figure 18.17** Morphologies of (a) HVPE-GaN:Fe; (b) HVPE-GaN:Mn.

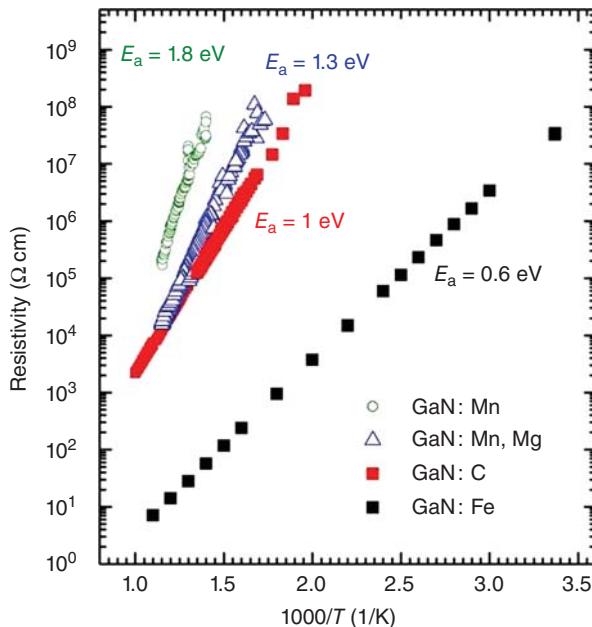
level. It can be assumed that in the crystals with higher carbon doping, additional defects can be formed and they compensate the  $C_N$  deep acceptors. There are some indications that carbon is amphoteric in GaN [74]. Thus, it can also be a donor. This results in the self-compensation phenomenon in HVPE-GaN:C.

Semi-insulating HVPE-GaN can also be crystallized on native seeds by doping with iron or manganese [75, 76]. Hydrochloride was flown over solid metals used as sources for these elements. A typical morphology of HVPE-GaN:Fe and HVPE-GaN:Mn is shown in Figure 18.17a,b, respectively. The high structural quality was kept (it did not differ from UID HVPE-GaN grown on a native seed) if the concentration of dopant did not exceed  $10^{18}$  and  $10^{19} \text{ cm}^{-3}$  for Fe and Mn, respectively. Doping with Fe allowed for a decrease of free carrier (electron) concentration in GaN and increase of the resistivity. At 300 K, its value reached  $10^8 \Omega \text{ cm}$  and the activation energy was 0.6 eV. All Mn-doped samples were very highly resistive at 300 K, and it was not possible to measure their resistivity. Electrical characterization was possible for temperatures higher than 550 K when the resistivity decreased to  $10^8 \Omega \text{ cm}$  and the material exhibited n-type conductivity. Activation energy in the case of GaN:Mn was close to 1.8 eV. Figure 18.18 summarizes the temperature-dependent resistivity measurements for all presented above acceptor dopants. There are also data of HVPE-GaN co-doped with Mn and Mg. Magnesium was added unintentionally. The activation energy was changed and took a lower value: 1.2–1.3 eV. The GaN:Mn,Mg samples were p-type at high temperature.

## 18.5 Summary

Results of HVPE and basic ammonothermal GaN crystallization, performed in Poland, were presented and discussed. Both methods seem to be very perspective for obtaining bulk GaN and fabricating high-quality GaN substrates. No doubt, the ammonothermally grown GaN crystals demonstrate perfect structural quality. It can be transferred to HVPE-GaN when Am-GaN seeds are used for vapor phase crystallization. Both methods allow to obtain n-type and semi-insulating crystals.

**Figure 18.18** Resistivity as a function of inverse of temperature for HVPE-GaN:Mn, HVPE-GaN:Mn,Mg, HVPE-GaN:C, and HVPE-GaN:Fe; values of determined activation energies are shown.



Time will show which material is more beneficial for making GaN substrates for specific applications. Since the future will belong to GaN-on-GaN technology, crystallization of this nitride becomes a crucial problem for further development of high-power high-frequency electronic as well as optoelectronic devices. Bulk GaN crystals are needed. The main goal is to design a process that will overcome the equilibrium crystal shape in GaN growth. This will allow to demonstrate true bulk GaN, eventually yielding several 10 of wafers per boule. Both described crystal growth technologies are, today, ready for this breakthrough achievement.

## Acknowledgments

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# 19

## GaN on Si: Epitaxy and Devices

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### 19.1 Introduction

The history of GaN research fights against GaN crystal growth. Thanks to the pioneers' technical breakthroughs, GaN optoelectric devices such as light-emitting diodes (LEDs) have been bringing great benefits in our life as in lighting bulb, backlight of smartphones, and thin flat panel displays [1–8].

In addition to the GaN optoelectronic devices, GaN-based materials are very attractive for various electron devices taking advantages of its excellent electron transport properties such as high breakdown field, high thermal conductivity, and high carrier saturation velocity. AlGaN/GaN heterojunction generates two-dimensional electron gas (2DEG) at the interface induced by spontaneous and piezoelectric polarization effects without any intentional impurity doping. The 2DEG has high sheet-carrier density around  $10^{13} \text{ cm}^{-2}$  and high mobility of  $1200\text{--}2000 \text{ cm}^2/\text{Vs}$ , enabling extremely low on-state resistance ( $R_{\text{on}}$ ) and gate charge ( $Q_g$ ). The figure of merit  $R_{\text{on}} Q_g$  for low conduction and low switching losses can be smaller than one to the tenth of that by conventional Si-based power devices, improving conversion efficiencies of power electronics systems. Converters and inverters with the efficiencies over 99% have been already demonstrated with the GaN devices, and some of them have been commercially available on the market such as power supplies and chargers for smartphones. These notable progresses of GaN power devices and converters have been led by significant progresses of GaN crystal growth especially on hetero-material substrates due to the lack of native GaN bulk substrates for a long time.

This chapter describes entire technology related to GaN power devices; GaN epitaxial growth, technical approaches of GaN lateral devices, device semiconductor processing, practical power applications, and device integrations utilizing advantages of GaN lateral devices.

## 19.2 GaN Epitaxy on Si Substrate

### 19.2.1 GaN Epitaxial Method and Doping

#### 19.2.1.1 Metal–Organic Chemical Vapor Deposition (MOCVD)

For III-N epitaxial growth, both metal–organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) have been standard methods. So far, MOCVD has been mostly used for GaN-based optoelectric and electron devices and utilizes metalorganic precursors for group-III elements (Ga, Al, and In) and nitrogen precursor, typically ammonia ( $\text{NH}_3$ ), which are transported with  $\text{H}_2$ ,  $\text{N}_2$ , or those mixed gas as carrier gas into a growth chamber. The metal–organic precursors are trimethylgallium (TMG), trimethylaluminium (TMA), and trimethylindium (TMI) for gallium, aluminum, and indium elements, where they react with  $\text{NH}_3$  on the surface of a substrate for formations of GaN, AlN, and InN as described by following chemical equations.

- $\text{Ga}(\text{CH}_3)_3 + \text{NH}_3 \rightarrow \text{GaN} + 3\text{CH}_4$
- $\text{Al}(\text{CH}_3)_3 + \text{NH}_3 \rightarrow \text{AlN} + 3\text{CH}_4$
- $\text{In}(\text{CH}_3)_3 + \text{NH}_3 \rightarrow \text{InN} + 3\text{CH}_4$

$\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$  ternary or quaternary crystal ( $x$ ,  $y$ , and  $x+y$  are between 0 and 1) can be grown by adjusting the ratio of TMG, TMA, and TMI for the desired material composition. Practically, there is some composite limitation especially for high indium-composition AlInGaN due to material phase separation. The AlInGaN material system has a direct band gap from 0.7 eV (InN) to 6.2 eV (AlN) for any material composition. Typical growth temperature for GaN and AlN is 1000–1200 °C [3, 9] and that for Indium contained compounds such as InGaN can be lower around 700 °C [10]. The crystal growth on heterogeneous substrate such as sapphire requires low-temperature grown layer usually used as nucleation layer [3, 4]. The growth pressure in the growth chamber is lower than 760 Torr in order to avoid gas-phase pre-reaction at the upstream of the growth chamber

#### 19.2.1.2 N, P-Type Doping

In general, n-type doping into III-N layers is achieved to replace the group III elements (Ga, Al, and In) with group IV elements, typically silicon, by using silane as a doping gas added in the gas source. Silicon acts as a shallow donor in the III-N layer, achieving high electron density of  $10^{19} \text{ cm}^{-3}$  [11, 12]. For p-type doping, magnesium (Mg) is the most common dopant provided from the metal–organic precursor of cyclopentadienyl magnesium ( $\text{C}_5\text{H}_5\text{}_2\text{Mg}$ ) replacing the group III elements. During the MOCVD growth of p-type GaN, Mg is inactivated by hydrogen of the carrier gas which can be eliminated during post-annealing process in nitrogen gas at 700–800 °C [6]. The acceptor level of magnesium in GaN is relatively high around 110–160 meV [13], so that the resultant hole density in p-GaN is limited around  $10^{17} \text{ cm}^{-3}$  at room temperature regardless of high Mg concentration of  $10^{19}$ – $10^{20} \text{ cm}^{-3}$  [14]. The higher Mg doping over  $10^{20} \text{ cm}^{-3}$  results in decrease of hole density due to the formation of Mg cluster or inversion domain of crystal polarity [15, 16].

### 19.2.1.3 Doping for Semi-insulation Layer

In lateral GaN power devices, semi-insulation (SI) layers act as an important role of highly resistive buffer layer to achieve high breakdown voltage and low leakage current, which are introduced under the active layer of AlGaN/GaN. In general, the highly insulated semiconductor layer can be obtained by purifying the semiconductor layer without any intentional doping. However, in the MOCVD process, residual impurities, typically oxygen and carbon, exist in the growth chamber, originating from the metal-organic precursors, carrier gases, and air leakage. The oxygen impurity acts as shallow donor locating the group III sites [17, 18], while the carbon impurity mainly occupies N sites as a deep acceptor with the activation energy of 0.9 eV in GaN [19]. In addition to the residual impurities, the atomic vacancies of the group III elements and that of nitrogen also affect the conductivity, where the vacancies of the group III elements and that of nitrogen can be a deep acceptor and a shallow donor, respectively [20, 21]. Therefore, the unintentional doping of GaN can bring about unstable conductivity control. Thus, doping of carbon or iron (Fe) is used for the growth of the semi-insulated layers compensating residual carriers in GaN. The concentration of carbon contained in the group III precursor can be controlled to be  $10^{16}$ – $10^{19}$  cm $^{-3}$  by adjusting growth parameters such as growth rate, V/III ratio, growth temperature, and pressure [22]. Fe can be doped in GaN by using ferrocene ( $\text{Fe}(\text{C}_5\text{H}_5)_2$ ) as a precursor and can generate plural electrical states in the energy midgap of GaN which traps the residual carriers [23]. Memory effect of Fe doping, in which the Fe doping profile has a tail even to upcoming grow layers, has to be taken into account [24].

## 19.2.2 Substrates for GaN Epitaxy

In general, the III-N epitaxial layers have been fabricated on hetero-material substrates such as sapphire, SiC, and Si by using hetero-epitaxial growth because of the difficulty to obtain large-diameter GaN bulk substrates. Table 19.1 summarizes material characteristics of the substrates for the III-N epitaxial growth. The choice of the substrate significantly affects the quality of III-N epitaxial layers, device structures (lateral or vertical), those performance, and cost depending on related applications. GaN substrates enable to fabricate vertical GaN power devices as same as Si- and SiC-based vertical power devices, while a Si and a SiC can be used to fabricate the lateral GaN power devices taking advantage of superior electrical characteristics of the AlGaN/GaN hetero structure. The detailed features of each substrate are described below.

### 19.2.2.1 GaN

The GaN substrate is an ideal substrate due to the perfect matching of mechanical characteristics with the GaN epitaxial layers. However, GaN does not melt at ambient pressure due to its quite high vapor pressure as high as 6 GPa [25], and GaN has been difficult to be applied conventional melt-based crystal growth used for Si, GaAs, and InP such as Czochralski method and Bridgman method. Therefore, as of today, commercially available GaN substrates are mainly prepared by using hydride vapor

**Table 19.1** Material properties of substrates for GaN epitaxy.

	Sapphire ( $\alpha\text{-Al}_2\text{O}_3$ )	6H-SiC	Si	GaN
Crystal structure	Hexagonal	Hexagonal	Diamond	Wurtzite
Lattice mismatch (%)	16	3.1	17	—
Linear thermal expansion coefficient (TEC) ( $\times 10^{-6}\text{ K}^{-1}$ )	7.5	4.4	2.6	5.6
CTE mismatch (%)	—26	25	56	—
Thermal conductivity (mW/cm/K)	25	230–490	150	210
Energy gap (eV)	9.9	3.03	1.12	3.4
Substrate diameter (mm)	150	150	400	50–100
Substrate relative cost	Low	High	Very low	Very high

phase epitaxy (HVPE) with low dislocation density of  $10^4\text{ cm}^{-2}$  [26], but the available diameter is limited up to 4 in. Recently, GaN power devices on the GaN substrate are reported with superior performances to those on heterogeneous substrates such as Si [27]. For a review on bulk growth of GaN, please see Chapter 18.

### 19.2.2.2 Sapphire

Historically, the initial technical breakthroughs of GaN epitaxial growth were achieved on sapphire substrates in 1980s through 1990s in order to overcome technical challenges of the large mismatches of the lattice constant (16%) and thermal expansion between GaN(0001) and c-plane sapphire due to the absence of GaN bulk substrate on those days [3, 4]. After that, GaN optoelectric devices such as green, blue, and white LEDs are main drivers for the sapphire substrate taking advantage of its transparency for wide-range wavelength up to ultraviolet, and the technical approaches of GaN crystal growth on sapphire have been also applied to fabricate GaN high electron mobility transistors (HEMTs) on sapphire of which diameter is up to 4–6 in. Although the sapphire substrate got an interest at the early stage of GaN HEMT development, the low thermal conductivity of sapphire has limited to extract the full potential of the extremely high power density of GaN HFETs. Therefore, the recent interest for the substrate has shifted to the cost-effective Si for wide-range applications and highly thermal-conductive SiC for high-frequency and military applications.

### 19.2.2.3 SiC

Since SiC substrates have superior thermal conductivity of around  $300\text{ W/mK}$  as high as that of Copper and are available to obtain the semi-insulation (SI)

characteristic, GaN HEMTs on Si-SiC have been widely used for high-frequency applications with high power density, high efficiency, and high operating temperature which cannot be achieved by GaAs-based HEMT devices [28, 29]. 6H-SiC is a suitable polytype of SiC for GaN epitaxial growth due to the closer mechanical properties to GaN, which differs from 4H-SiC mainly used for the fabrication of SiC vertical power devices. Although the mechanical characteristics of 6H-SiC are relatively close to those of GaN, the price of the 6H-SiC substrate has been still more expensive than sapphire and Si. Furthermore, the number of SiC-substrate suppliers has been quite limited now.

#### 19.2.2.4 Si

Si is one of the most abundant materials on the earth, and the Si substrates are commercially available with the large diameter of up to 12 in. and various resistivities thanks to matured technologies for bulk crystal growth and wafer production. The GaN-on-Si technology is very promising to reduce the cost of GaN HFETs so as to widely spread for commercial use. Si has a good thermal conductivity as high as GaN, but which is lower than that of SiC. In addition to the substrate features, the advantage of GaN-on-Si technology is to utilize well-established Si complementary metal-oxide-semiconductor (CMOS) processes such as metallization, via-hole formation, and wafer grinding. This is the background that GaN-on-Si has been researched extensively regardless of its material challenges such as large mismatch of lattice constant and thermal expansion coefficient (TEC) between GaN and Si. So far, several technical approaches have been introduced to overcome challenges originated from these mismatches and achieved high-quality epitaxial layers with less wafer curvature which can be acceptable for processing equipment.

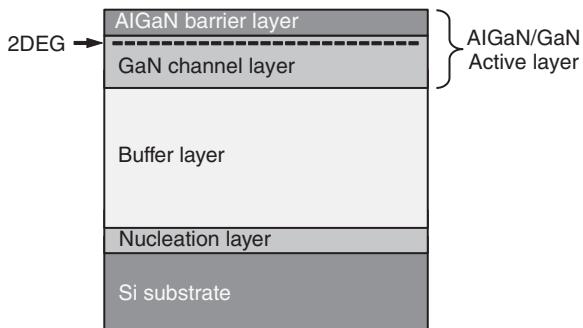
### 19.2.3 Epitaxial Growth Technology on Si Substrate

#### 19.2.3.1 Crystal Orientation of Si Substrate

Typically, Si(111) is used for the growth of wurtzite GaN(0001), which is the most stable crystal structure of GaN. The epitaxial technologies to manage mechanical stress in GaN on Si is a key technology to suppress wafer curvature and cracks originated from the large mismatches of the lattice constant and the coefficient of thermal expansion (CTE) between Si(111) and GaN(0001). As shown in Figure 19.1, the GaN epitaxial layers on Si consist of the following parts: (i) nucleation layer to initiate the epitaxial growth on the heterogeneous substrate of Si, (ii) buffer layer to manage the internal stress to obtain a thick epitaxial layer for higher breakdown voltage, and (iii) active layer for the lateral electrical channel with the 2DEG. Each part is described in detail below.

#### 19.2.3.2 Nucleation Layer

The past approaches to grow GaN directly onto Si resulted in insufficient crystal quality with three-dimensional GaN growth for the device fabrication. During the crystal growth, Ga species can easily diffuse into the Si substrate and roughen the surface of Si substrate, which is so-called Ga melt-back [30]. AlN is introduced as a

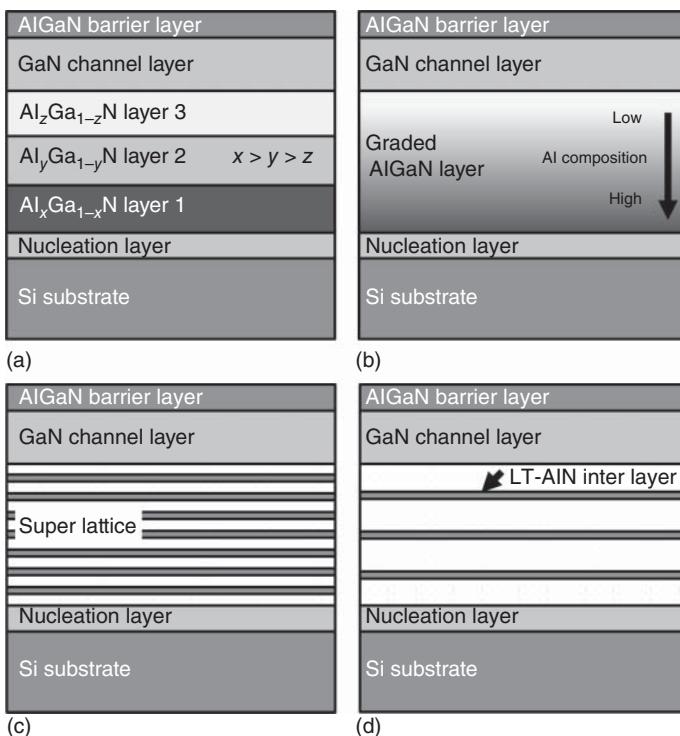


**Figure 19.1** Epitaxial structure of GaN on Si substrate.

nucleation layer for GaN on Si to solve the Ga melt-back [31]. Aluminum reacts with nitrogen actively and has low diffusion velocity of the adatom on Si substrates. In result, lots of AlN nucleation occur simultaneously and coalesce each other including large amount of small AlN islands. Even though the initial AlN layer includes high-density dislocations of  $10^{10} \text{ cm}^{-2}$ , the AlN initial layer can transfer the crystal orientation to upcoming grown layers. The thickness of AlN layer is typically 20–200 nm. AlN/Si material system has been researched actively in the crystallographic and electrical points of view, since the characteristics of the AlN initial layer can affect the crystal quality of GaN on Si in total [32].

### 19.2.3.3 Buffer Layer

The buffer layer is grown on the AlN nucleation layer in order to manage the mechanical stress to obtain the thick epitaxial layer for higher breakdown voltages. For 600-V rating devices, 3–5  $\mu\text{m}$  thick epitaxial layers have been used for GaN on Si. During cooling-down process after the crystal growth, the GaN layer shrinks more than the Si substrate due to the larger CTE mismatch of 54% between GaN and Si, inducing high tensile stress in the GaN layer to lead cracks in GaN layer, wafer bowing, and break at the worst case. The magnitude of the tensile stress increases in proportion to the thickness of the epitaxial layers. The essential technology is to design the structure of the buffer layers to introduce compressive stress to cancel the tensile stress originated from the CTE mismatch between GaN and Si. So far, several buffer layers have been reported as shown in Figure 19.2. The step-graded AlGaN layers consist of several AlGaN layers with different Al compositions, starting from the first AlGaN layer on the AlN nucleation layer. The second AlGaN layer is grown on the first AlGaN layer, having lower Al composition than that of the first one to have larger lattice constant for the compressive stress [33]. Repeating the same way to reduce Al composition even more to be finally GaN, the next graded AlGaN and GaN layers can generate the compressive stress as well. Instead of the step-graded approach, the AlGaN buffer layer with continuously reduced Al composition is also reported [34]. The AlN/GaN superlattice structure, in which thin GaN and AlN layers are repeatedly grown with several tens of GaN/AlN layers, is practically demonstrated to obtain thick buffer layer [35]. The stress management by using low-temperature AlN interlayers between thick GaN layers is also reported [36]. Semi-insulated buffer layers doped with C or Fe can be used to achieve higher

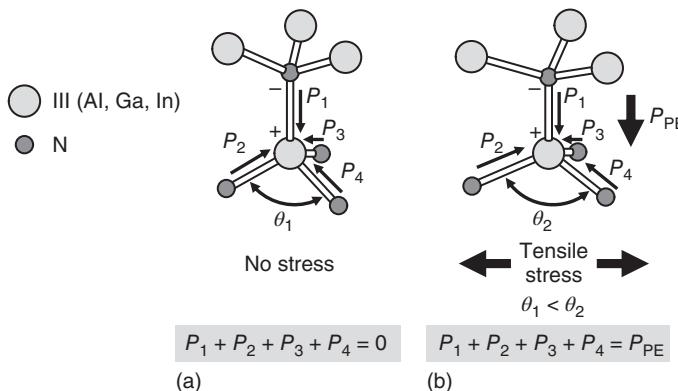


**Figure 19.2** Structures of buffer layers for GaN on Si substrate. (a) Step-graded AlGaN, (b) graded AlGaN, (c) superlattice, and (d) low temperature AlN interlayers.

breakdown voltage and lower leakage current [37, 38]. A drawback of C and Fe doping into the buffer layer is carrier trapping by C- and Fe-related electrical states, where trapped electron acts as negative charge and lifts up the electrical potential in the vicinity of the 2DEG, reducing drain current of the GaN HFET [39, 40]. Therefore, the C- or Fe-doped layer is recommended to have certain distance from the AlGaN/GaN active layer.

#### 19.2.3.4 AlGaN/GaN Active Layer with Polarization Effect

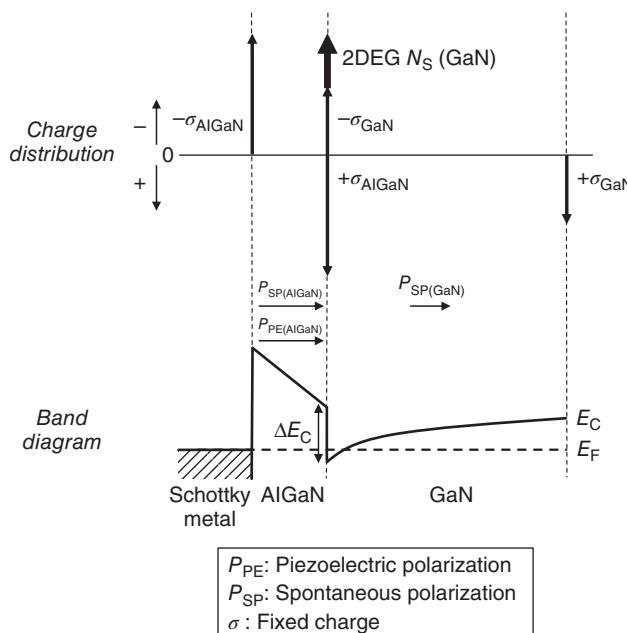
Wurtzite-type GaN, AlN, and InN have a hexagonal crystal structure, where the axis direction of the hexagonal column is called as *c*-axis. Wurtzite-type GaN has different faces perpendicular to *c*-axis which are Ga-face and N-face leading to different electrical characteristics. The Ga-faces is usually obtained by MOCVD, while the N-face can be grown by MBE. Since nitrogen has higher electronegativity than gallium, Ga and N atoms act as anion (+) and cation (-), respectively, causing electrical polarization. In the wurtzite crystal structure, the electrical polarization called as spontaneous polarization occurs along the *c*-axis, of which values are 0.081, 0.029, and  $0.032 \text{ C/m}^2$  for AlN, GaN, and InN, respectively. In addition to the spontaneous polarization, internal mechanical stress between epitaxial layers with difference lattice constants generates piezo electric polarization. In wurtzite crystal structure as shown in Figure 19.3, the composition of polarization vectors  $P_1 + P_2 + P_3 + P_4$



**Figure 19.3** Polarization vectors of III-N semiconductor in the tetrahedron shape. The balanced polarization (a) and the unbalanced one with the piezoelectric polarization (b). (a) No stress and (b) tensile stress.

becomes zero because of crystal symmetry. However, mechanical stress due to the lattice mismatch between the epitaxial layers deforms the crystal symmetry and the balance of the composition vector. Thus, the piezo polarization  $P_{\text{PE}}$  appears as  $P_{\text{PE}} = P_1 + P_2 + P_3 + P_4$ . The detailed theoretical investigation on the piezoelectric polarization was done by Ambacher et al. [41].

Figure 19.4 shows charge distribution and band diagram of AlGaN/GaN hetero structure. Free carriers are generated at AlGaN/GaN interface to neutralize charges induced by the spontaneous and piezoelectric polarizations. In general, although semiconductor requires impurity doping to generate free carriers, the AlGaN/GaN material system can obtain high-density and high mobility 2DEG without any intentional impurity doping. Typically, AlGaN layer with the thickness of 20 nm, Al composition of 25% can yield the 2DEG density of  $1 \times 10^{19} \text{ cm}^{-2}$ , of which mobility can reach around  $2000 \text{ cm}^2/\text{V s}$  depending on the smoothness at the AlGaN/GaN interface and the crystal quality of the epitaxial layers. Thanks to the superior electrical characteristics of AlGaN/GaN with any intentional doping, GaN power devices can achieve high current, low on-state resistance, and high breakdown voltage. The 2DEG density can be increased by increasing either the thickness or the Al composition of the AlGaN barrier. However, the critical thickness of the compressed AlGaN barrier can limit the 2DEG density. There are several approaches for higher 2DEG density taking the other barrier layers. The introduction of a thin AlN interlayer between the AlGaN barrier and GaN channel layers can increase both the 2DEG density and mobility [42]. The AlN layer has larger polarization than the AlGaN and can suppress alloy scattering of the 2DEG caused by the AlGaN alloy at the AlGaN/GaN interface. The thickness of the AlN interlayer is limited up to 2 nm due to the large lattice mismatch between AlN and GaN. The other approaches for barrier layers are to utilize highly Al-composition InAlN or InAlGaN replaced Ga with In to increase Al composition keeping lattice constants as long as AlGaN, which can have the lattice-matched growth on GaN as  $\text{In}_{0.18}\text{Al}_{0.82}\text{N}/\text{GaN}$  which generates quite



**Figure 19.4** Charge distribution and band diagram of AlGaN/GaN structure.

high-density 2DEG of around  $2 \times 10^{19} \text{ cm}^{-2}$  induced by high spontaneous polarization of Al [43, 44].

In addition to the top barrier layers on the GaN channel layer, a back barrier layer under the GaN channel layer can be used as AlGaN/GaN/AlGaN double hetero structure to improve the carrier confinement into the GaN channel layer to improve pinch-off characteristics especially for short gate devices, preventing so-called “short channel effect” [45]. In addition to the band offset at the lower GaN/AlGaN interface, polarization-induced negative charge can lift up the potential around the AlGaN back barrier layer which helps suppress carrier transport via the AlGaN back barrier layer as leakage current.

There is another approach to cover the AlGaN/GaN top barrier layer with GaN, InGaN, and InAlGaN capping layers for several purposes. First, the GaN cap layer can improve surface ununiformity of the sensitive AlGaN top barrier to avoid “current collapse” caused by carrier trapping of surface states [46]. Second, the InGaN cap layers on the AlGaN barrier layer generate negative polarization-induced charge at the interface between the cap layer and the AlGaN top barrier, which increase the effective Schottky barrier height resulting in the reduction of reverse leakage current and normally-off operation [47]. Third, n-type layers such as n-type AlGaN/GaN super lattice [48] and n-type InAlGaN cap layers [49] can decrease the ohmic contact resistance due to lower barrier height against the electrodes.

In addition to above III-N cap layers, surface passivation by in situ SiN thin layer can be grown with MOCVD continuously after III-N growth. The in situ SiN has a

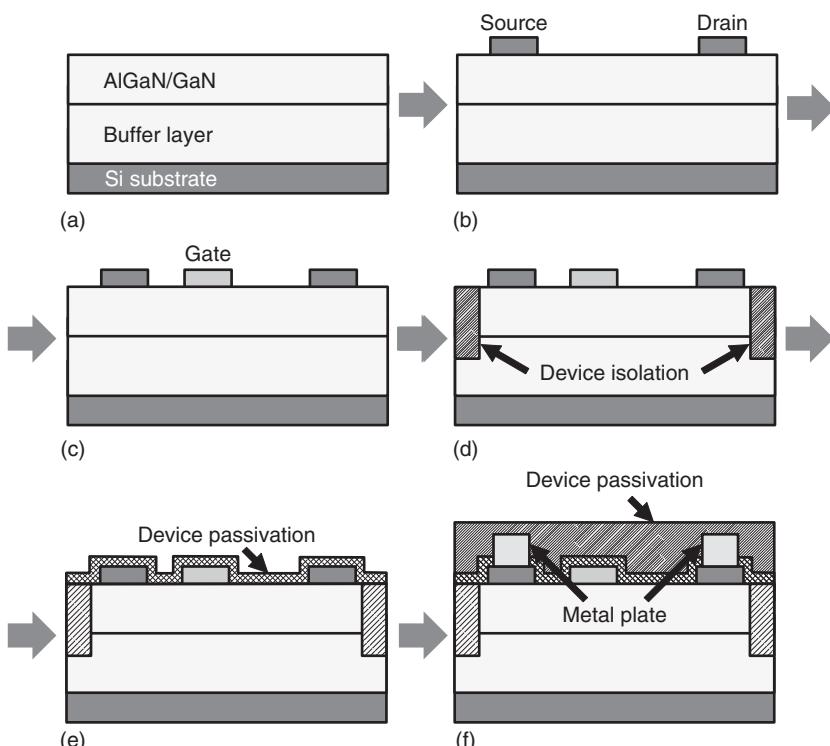
crystalline structure [50] which increases 2DEG density and suppresses the current collapse by neutralizing surface states on the AlGaN top barrier layer [51].

## 19.3 Lateral GaN Devices on Si Substrate

### 19.3.1 Device Structure and Fabrication Process

As shown in Figure 19.5, GaN HFETs with 2DEG have a lateral structure. The device processing of GaN HFETs is similar to that of GaAs HEMTs which consists of (i) metallization of ohmic contact for source and drain, (ii) that of Schottky contact for gate, (iii) electrical isolation, (iv) device passivation, (v) metal plating, and (vi) final device passivation.

The ohmic contact for GaN HFET is Ti/Al-based material system which requires high-temperature post annealing typically around 800 °C for 30 seconds in nitrogen ambient to reduce ohmic contact resistance down to  $10^{-6} \Omega/\text{cm}^2$  [52]. For further reduction of contact resistance, selective Si ion implantation into source and drain regions is used to fabricate n<sup>+</sup>-type region. Although post-implant high-temperature



**Figure 19.5** Sequence of GaN-HFET device process showing (a), (b) ohmic metalization, (c) gate metalization, (d) device isolation with ion implantation, (e) surface passivation, and (f) metal plating and final passivation.

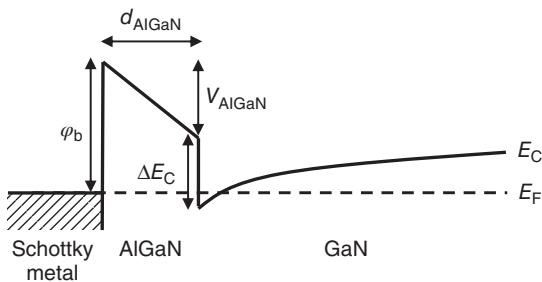
annealing over 1200 °C is necessary to recover crystal damage for Si activation as n-type donor, the contact resistance with order of  $10^{-7} \Omega/\text{cm}^2$  is reported [53].

Schottky contact as gate contact is preferred to consist of high work-function metal such as Ni, Pd, and Pt for high Schottky barrier height to suppress reverse gate leakage current [54, 55]. Practically, Ni/Au electrode has been used for gate metal due to its better adhesion to the AlGaN surface than that of Pd and Pt. The condition of the AlGaN surface such as nitrogen vacancy [56] can affect reverse electrical characteristics of the Schottky contact, and the introduction of insulate gate structures with  $\text{SiO}_2$  and  $\text{Al}_2\text{O}_3$  as alternative solutions has been reported [57, 58].

The device isolation is employed to define the active HFET region and electrically isolate the HFETs each other to avoid operational interferences among the HEMTs. There are mainly two approaches for the isolation, dry etching and ion implantation. Dry etching processes such as reactive ion etching (RIE) with chlorine-based gas have been used to etch GaN in order to eliminate the 2DEG, because GaN-based materials are quite chemically stable and cannot be etched by conventional acid-based wet etching processes as in Si- and GaAs devices. However, dry etching induces crystal damage that can degrade the HFET performance such as increasing of leakage current which results in inferior breakdown characteristics and worsens flatness of the device surface that affects coverage of metallization and passivation on the sidewall of the etched GaN layers.

Ion implantation technique has been also employed to isolate the HEMT with the device flatness kept. Implanted ions generate crystal damage of which energy states trap electrons and holes, which leads highly resistive regions with the resistance over  $10^9 \Omega/\text{square}$ . The ion-implanted isolation has been demonstrated by using various ion species from light element to heavy one such as H, He, N, O, F, P, Fe, and Zn [59–63]. Distribution of implanted ions and induced damage can be simulated by using Monte Carlo simulation [64] to select ion doses and acceleration energies for desired distribution of implanted ions and induced lattice damage. The simulated density of the induced damage becomes two orders of magnitude higher than that of implanted ion density. Practically, plural implantation steps with different doses and acceleration energies are employed to produce so-called box profile keeping constant ion density until certain depth of GaN layers. The resistance of the implanted region can be decreased by post-implanted annealing over 600 °C due to damage recovery. Therefore, temperatures of post processing after the ion implantation have to be selected carefully to maintain the high resistivity of the implanted regions.

Finally, the surface of GaN HFET is passivated with dielectric film, typically SiN, to protect the device surface from water and oxidation. The other purpose of the passivation is to deactivate surface states of the AlGaN barrier layer. The surface states can trap electrons accelerated by high electric field during the HEMT operation and then lift up the electrical potential in the vicinity of the 2DEG, resulting in decrease of drain current which is called as “current collapse” [65]. In addition to the surface passivation, another solution for the current collapse caused by high electric field has been proposed to form metal plates called as field plate to lower the electric field. The field plate is connected to source (source field plate, SFP) or gate (gate field plate,



**Figure 19.6** Band diagram of AlGaN/GaN structure with Schottky gate.

GFP) electrodes to reduce the peak electric field between gate and drain to avoid the electron trapping by the surface states, suppressing the current collapse [66].

### 19.3.2 Structures for E-Mode Operation

AlGaN/GaN HFETs usually show depletion-mode (D-mode, normally-on) characteristic which has negative gate threshold voltage and requires negative gate bias to deplete 2DEG under the gate. Figure 19.6 shows an energy band diagram of AlGaN/GaN with Schottky gate, and the threshold voltage of AlGaN/GaN HFET with Schottky gate can be described with the following equation.

$$V_T = \varphi_b - \Delta E_C - V_{\text{AlGaN}} = \varphi_b - \Delta E_C - \frac{q N_s d_{\text{AlGaN}}}{\epsilon_0 \epsilon_{\text{AlGaN}}} \quad (19.1)$$

where,  $\varphi_b$ ,  $\Delta E_C$ ,  $N_s$ ,  $d_{\text{AlGaN}}$ ,  $\epsilon_0$ ,  $\epsilon_{\text{AlGaN}}$ , and  $q$  are Schottky barrier height, conduction band offset between AlGaN and GaN, 2DEG density, AlGaN thickness, permittivity of vacuum, relative permittivity of AlGaN and electron charge, respectively. For power electronics application, enhancement-mode (E-mode, normally-off) characteristic with positive gate threshold voltage is required to keep power electronics systems safe even if gate driving circuit is failed. Referring to the above equation, following approaches are effective to obtain the E-mode characteristic.

1. Decreasing 2DEG density
  - Thinning AlGaN barrier layer
  - Reducing Al composition in AlGaN layer
2. Introducing negative charge into gate area
3. Increasing work function of gate material

Decreasing of 2DEG density by either thinning AlGaN barrier layer or reducing Al composition in AlGaN barrier is an effective way to obtain the normally-off operation [67]. However, the reduced 2DEG density can bring drawbacks to increase on-state resistance and decrease drain current of AlGaN/GaN HFETs. One of the methods to introduce negative charge to gate is fluorine treatment typically by carbon tetrafluoride ( $\text{CF}_4$ ) plasma to introduce fluorine atom to interstitial sites of AlGaN barrier layer [68]. Due to the highest electronegativity of fluorine among all elements, an introduced fluorine atom can capture a free electron and act as a negative fixed charge which lifts up the gate potential and depletes the 2DEG. Addition to the abovementioned approaches, the method to increase work

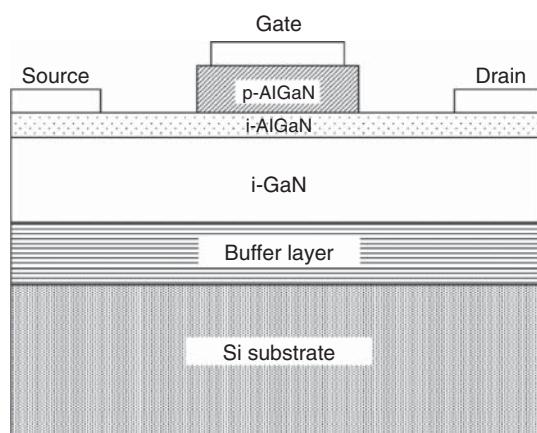
function of gate material can lead to normally-off characteristic. Even though the highest work function metal of platinum (Pt, 5.12–5.93 eV) is insufficient to obtain E-mode operation of AlGaN/GaN HFET, using p-type wide-bandgap semiconductor such as p-GaN or p-AlGaN for gate material provides high built-in potential between p-type gate and AlGaN/GaN [69]. Since the gate threshold voltage of p-(Al)GaN/AlGaN/GaN can be determined with the thickness and Al composition of AlGaN barrier layer controlled by epitaxial growth technique, the device process has high controllability and high reproducibility which are preferred for device mass production. The next subsection of 19.3.3 and the session of 19.4 describe the p-type gate AlGaN/GaN HFET and related applications in detail, respectively.

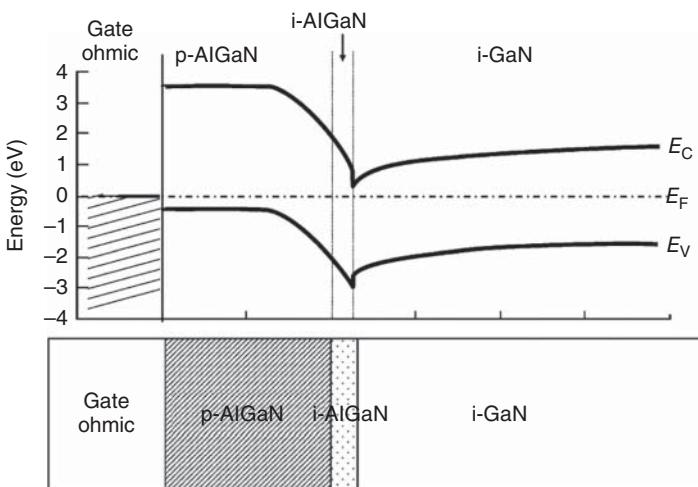
### 19.3.3 E-Mode GaN Gate-Injection Transistor (GIT) on Si Substrate

#### 19.3.3.1 Device Structure and Operational Principle

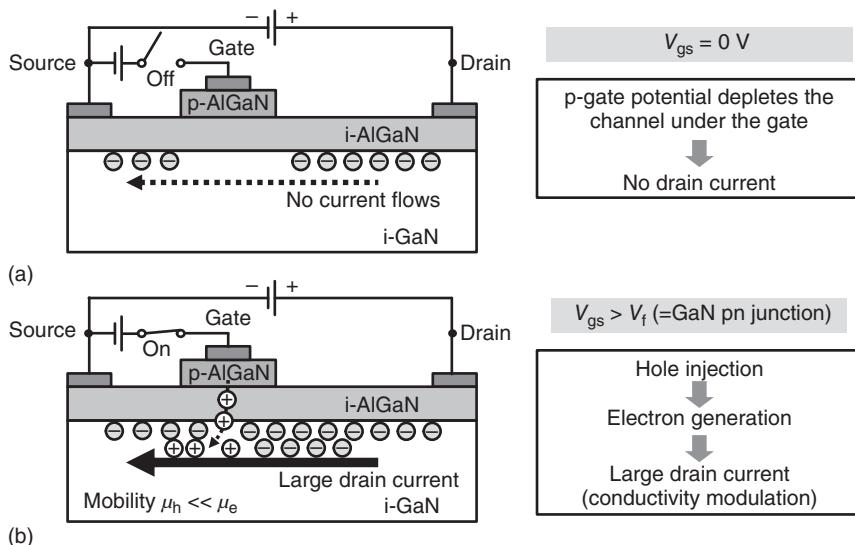
As shown in Figures 19.7 and 19.8, the E-mode gate-injection transistor (GIT) has a p-type gate onto the AlGaN/GaN HFET structure which lifts up the potential of the 2DEG under the gate and depletes the 2DEG there at the zero gate voltage. Figure 19.9 summarizes the basic operational principle of GIT. At the zero gate voltage, the electron channel under the gate is fully depleted to enable the E-mode operation. By increasing the gate voltage up to the forward voltage of the gate pn junction, the drain current starts to flow, which is based on the phenomena in conventional unipolar field effect transistors. When the gate voltage becomes higher than the forward voltage of around 3.5 V, holes can be injected from the p-type gate into the 2DEG, which is called conductivity modulation observed in Si-insulated gate bipolar transistor (IGBT) operation. Then the injected holes induce the same amount of electrons at the 2DEG to keep the charge neutrality. The induced electrons move to the drain side and contribute for increasing drain current while the injected holes stay underneath the gate due to the two order magnitude lower mobility of holes than that of the electrons. Figure 19.10 shows the  $I_{ds}$ - $V_{gs}$  characteristics of a fabricated GIT in which the second peak of the transconductance  $g_m$  at higher

**Figure 19.7** Schematic cross-section of GaN-GIT [69].





**Figure 19.8** Band diagram of GaN-GIT at the gate bias of 0 V [69].

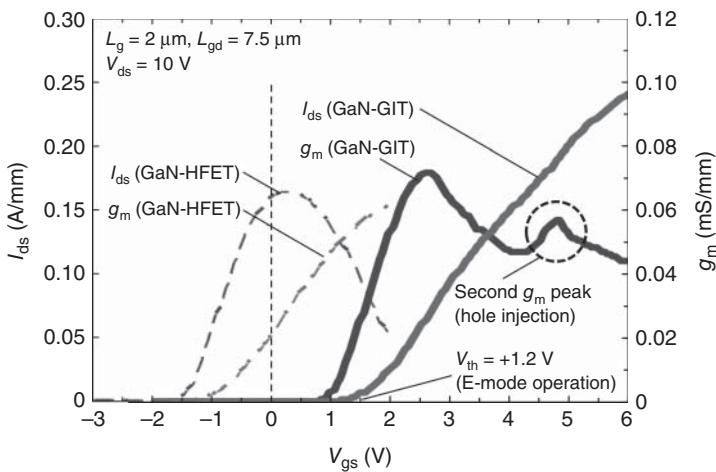


**Figure 19.9** Cross-sectional structure of GaN-GIT showing operational principle at (a) off-state and (b) on-state.

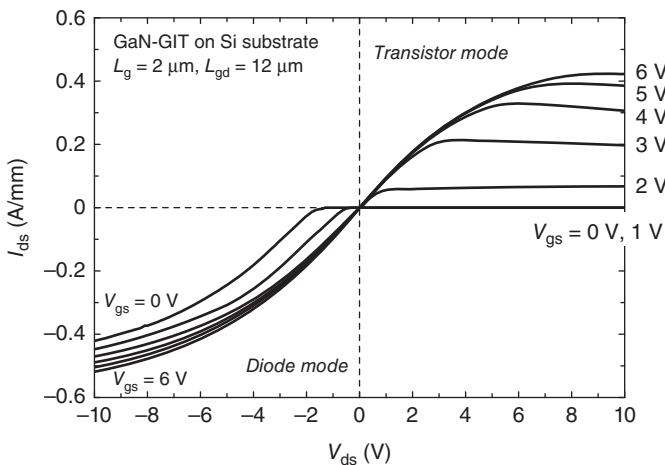
gate voltage indicates the abovementioned conductivity modulation. The electroluminescence (EL) of the GIT around the p-type gate is also a proof of the operational principle [70], where the EL indicates the recombination of the injected holes and the electrons at the higher gate voltage.

### 19.3.3.2 DC Performance of GIT

One of features of GIT is the device fabrication on cost-effective Si substrate. A p-AlGaN/i-AlGaN/GaN heteroepitaxial structure for the GIT is grown on 6-in.

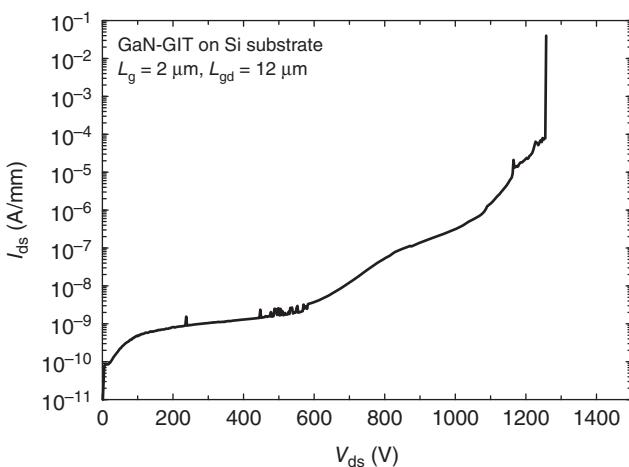


**Figure 19.10** Measured  $I_{ds}$ - $V_{gs}$  characteristics of fabricated GaN-GIT on Si substrate.



**Figure 19.11** Measured on-state  $I_{ds}$ - $V_{ds}$  characteristics of fabricated GaN-GIT on Si substrate.

Si(111) substrate with buffer layers consisting of the GaN/AlN multilayers on top of the AlGaN/AlN initial layers. The p-gate is selectively formed by dry etching. GaN lateral HFETs have two conduction modes of “transistor mode” and “diode mode”. The transistor mode has the drain current which flows from drain to source as conventional transistor operation, while the diode mode has the reverse conduction from source to drain through the 2DEG with drain offset voltage like diode even without any intrinsic body diode as in Si-metal oxide semiconductor field-effect transistors (MOSFETs). As shown in Figure 19.11, the transistor mode shows no drain offset voltage with the measured specific on-state resistance  $R_{on}A$  of  $2.3\text{ m}\Omega\text{ cm}^2$ . On the other hand, the diode mode has the drain threshold voltage of  $+1.5$  V corresponding to the gate threshold voltage. By applying the gate voltage in

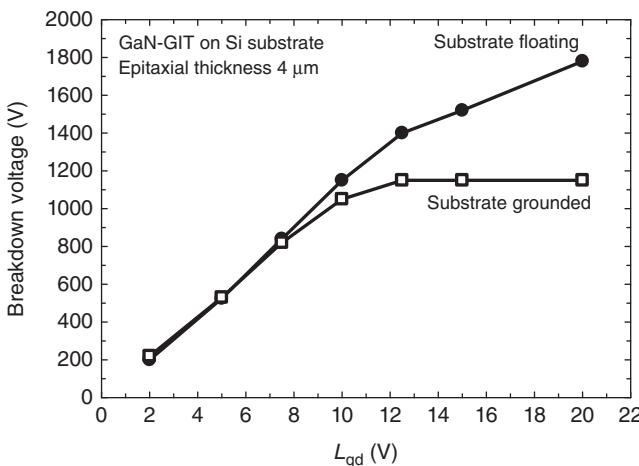


**Figure 19.12** Measured off-state  $I_{ds}$ – $V_{ds}$  characteristics of fabricated GaN-GIT on Si substrate.

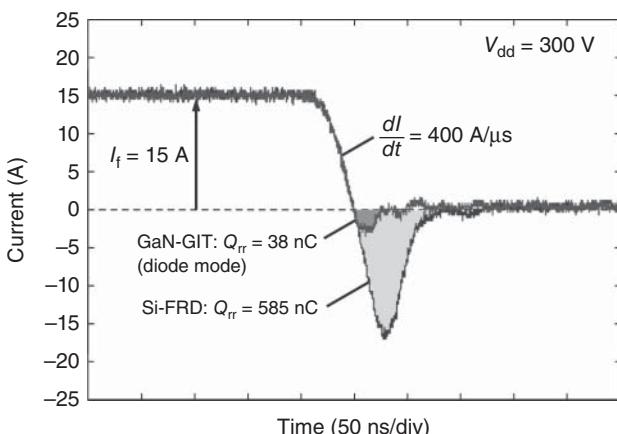
the diode mode, the GIT has no  $V_{ds}$  offset-voltage enabling low conduction loss. The 600-V-rating GIT shows a breakdown voltage of 1260 V at  $L_{gd}$  of 12  $\mu\text{m}$  as shown in Figure 19.12. As shown in Figure 19.13, the breakdown voltage increases with extending  $L_{gd}$  and then saturates a certain value determined by the thickness of GaN epitaxial layers on Si, where the vertical electrical field in the device dominates the breakdown characteristics of GaN HFETs on Si. A 600-V rating GaN-GIT with wider gate width shows the on-state resistance  $R_{on}$  of 65 m $\Omega$ , the rating continuous current of 15 A and the gate charge  $Q_g$  of 11 nC. The figure of merit  $R_{on}Q_g$  for low conduction and low switching losses is calculated to be 700 m $\Omega$  nC which is one thirteenth of that by state-of-art super junction Si-MOSFETs.

### 19.3.3.3 Switching Performance of GIT

In addition to the device performance, package and assembling technologies with low parasitic inductances are also important to extract full potential of the high-speed switching of GaN devices. Conventional packages such as TO-220 have long lead terminals of which parasitic inductances slow down switching speed of GaN devices. The flip-chip assembly can significantly reduce the parasitic inductance down to 2 nH in comparison with 25 nH obtained by TO-220 package. The flip-chip assembly enables the fast switching speed  $dV_{ds}/dt$  of 170 V/ns leading to low switching loss [71]. In addition to the conduction and switching losses, recovery losses of the diode mode induced by turning-off of diode operations are also taken into account for achieving higher conversion efficiency. Figure 19.14 shows a recovery characteristic of the GaN-GIT compared with that of an Si-based fast recovery diode (Si-FRD) [72]. The GaN-GIT has much smaller recovery charge than that of the Si-FRD because of unipolar characteristic in the GaN-GIT diode mode. In summary, the GIT has quite high potential for highly efficient and high-frequency power applications.



**Figure 19.13** Breakdown voltages of fabricated GaN-GITs on Si substrate for various  $L_{gd}$ , comparing electrical potential of Si substrate.

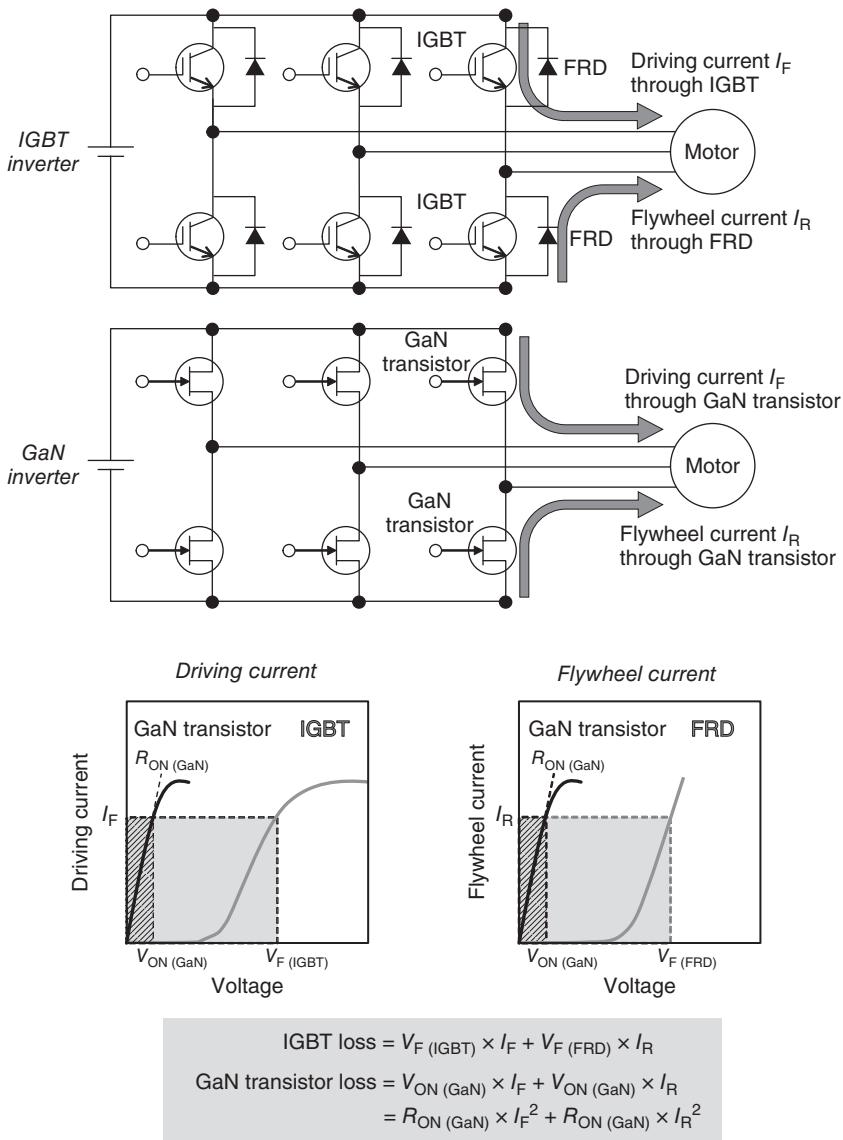


**Figure 19.14** Measured recovery characteristics of GaN-GIT in diode-mode operation compared with that of a Si-based FRD.

## 19.4 Application of GaN HFET

GaN HFETs enable to make power conversion systems such as inverters and power supplies higher efficient and smaller size taking advantage of the superior device characteristics.

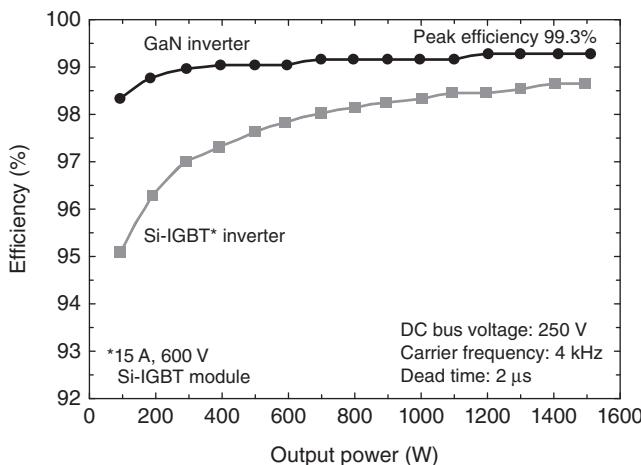
In the inverter application as shown in Figure 19.15, GaN HFETs can achieve low conduction loss by no drain-voltage offset and synchronous rectification utilizing the diode mode of the GaN-GIT. Furthermore, the GaN inverter requires no external diode such as Si-FRD as seen in the Si-based inverter, which can reduce the number of components, assembling area, and system cost. Figure 19.16 shows conversion efficiencies and loss analysis of GaN inverter with GaN-GITs compared with those



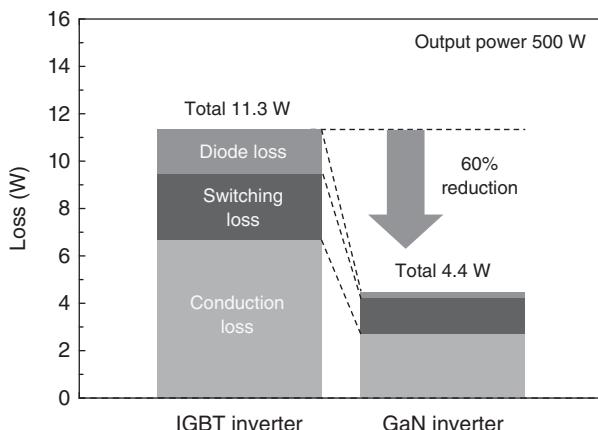
**Figure 19.15** Operations of a IGBT-based inverter and GaN-based one showing forward and flywheel conduction losses.

by the Si-based inverter. The GaN inverter achieves the high conversion efficiency over 99% at 1.5 kW and significantly improves the efficiency in lower output region in comparison with that by Si-IGBTs due to the lower conduction loss of GaN-GITs. The reduction of the total loss in the GaN inverter by 60% at 500 W contributes to achieve the higher efficiency as analyzed in Figure 19.17 [72].

Power supplies such as DC/DC and AC/DC are also suitable applications for GaN HFETs, since high-frequency operation can reduce the system size by using smaller components such as capacitors, inductors, and transformers. So far, GaN DC/DCs



**Figure 19.16** Measured power-conversion efficiency of three-phase inverter with GaN-GITs compared with that with Si-IGBTs.

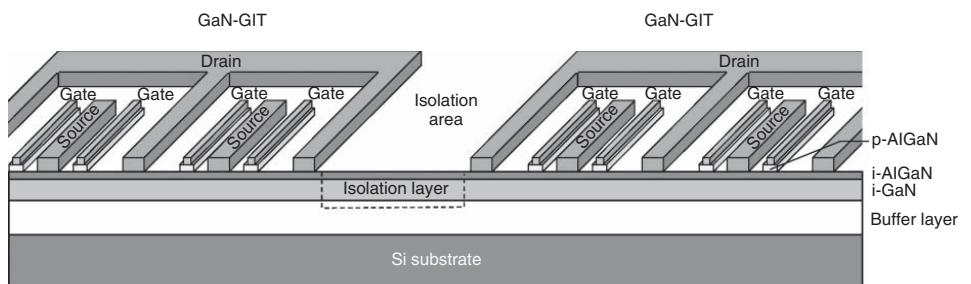


**Figure 19.17** The analysis of operating losses in the GaN inverter system compared with that in the Si inverter system.

with 1–5 MHz operation [73] and with integrated small transformer into printed circuit board (PCB) are demonstrated [74].

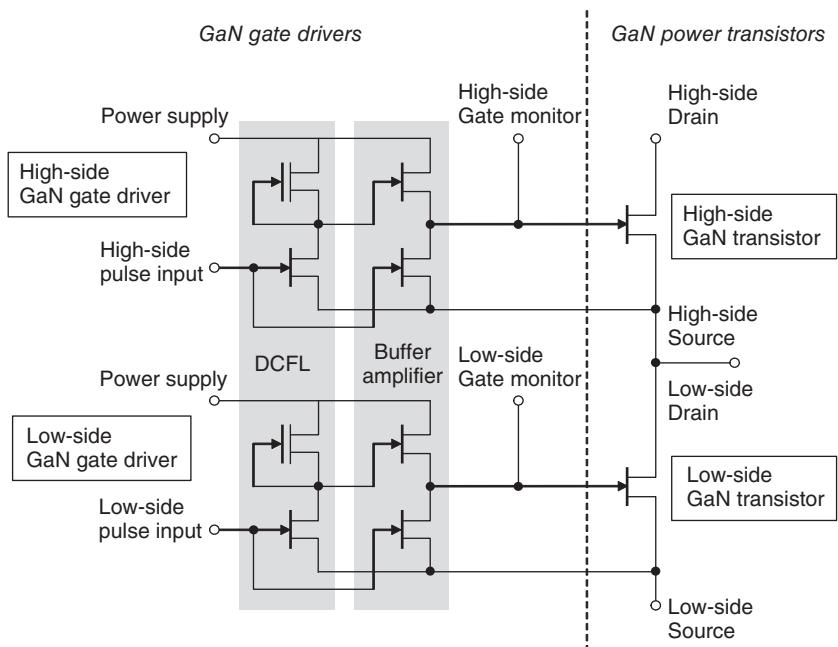
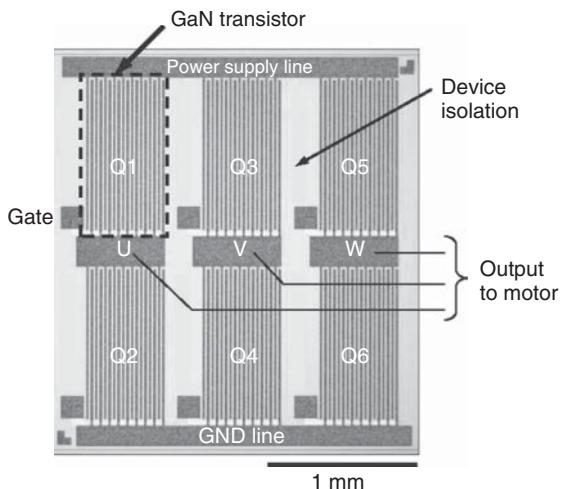
## 19.5 Integration of Lateral GaN Devices

One of the biggest advantages of GaN lateral devices is integration of GaN devices and gate drivers onto the same substrate to build highly functional integrated circuits (ICs) which is technically difficult for other vertical power devices. Lateral GaN devices can be integrated into one chip with planer device isolation typically fabricated by ion implantation as shown in Figure 19.18. The integration eliminates wirings between the devices and minimizes parasitic inductances which are good to extract high potential of GaN devices for high-frequency operations. Figure 19.19



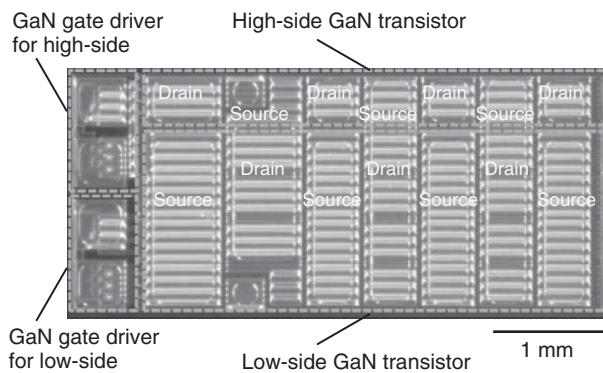
**Figure 19.18** Schematic cross-section of GaN-GITs integrated into one chip with planer isolation.

**Figure 19.19** Photograph of the fabricated 6-in-1 GaN three-phase inverter IC.

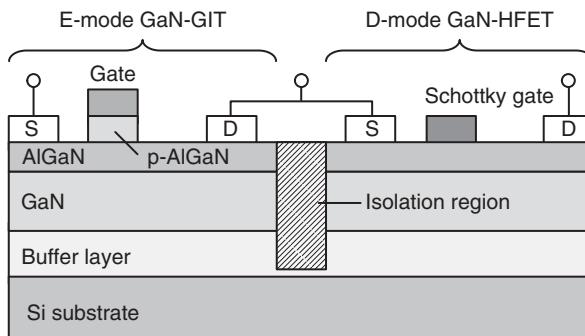


**Figure 19.20** Circuit diagram of the DC/DC converter IC with integrated GaN gate drivers.

shows a GaN three-phase inverter IC consisting of six GaN-GITs integrated onto Si substrate [75]. Highly resistant region prepared by ion implantation achieves high-voltage electrical isolation between the devices, and the demonstrated conversion efficiency is higher than that obtained by conventional Si-IGBT inverters. Another example is low voltage GaN DC/DC integrated with GaN-based gate drivers [76]. The GaN gate drivers utilize direct coupled field-effect transistor logic (DCFL) circuit instead of CMOS circuit due to the extremely low hole mobility in GaN as shown in Figure 19.20. In addition, buffer amplifiers are also integrated to



**Figure 19.21** Photograph of the fabricated DC/DC IC in which two GaN power transistors and two GaN gate drivers are integrated into one chip.



**Figure 19.22** Schematic cross-section of E-mode and D-mode GaN HFETs integrated in GaN DC/DC IC.

enable lower power consumption for the gate driving. Figures 19.21 and 19.22 show the photograph and the cross-sectional schematic of the GaN DC/DC IC, where both E-mode and D-mode GaN devices are fabricated by a part of the entire device processing. One to three megahertz operations and peak conversion efficiency of 88.2% at 2 MHz are demonstrated. In summary, abovementioned integration of GaN devices is an essential solution to enable higher device performances and expands application potential of GaN devices.

## 19.6 Summary

This chapter summarizes entire technology related to GaN power devices from GaN epitaxial growth to the related power applications. The first part of the chapter summarizes GaN epitaxy on Si substrate including impurity doping, choice of substrates, detailed epitaxial structures to initiate epitaxial growth, manage mechanical stress, and generate 2DEG for GaN lateral power devices. In the second part of the chapter, the technologies on GaN lateral power devices are summarized, especially focusing on E-mode GaN-GIT device, which is suitable for practical power applications. The third part of the chapter shows power application

examples of GaN lateral power devices achieving higher conversion efficiency than that by conventional Si power devices. Finally, the fourth part of the chapter introduces integrations of GaN lateral devices on one chip which could expand applications of GaN devices furthermore. In summary, GaN-based power devices are very promising devices for power electronics applications due to the superior device performance surpassing conventional Si-based power devices. The technical breakthroughs of GaN epitaxial growth and device technologies by the pioneers in the early days have opened the door to expand the application of GaN optoelectric and power devices giving us lots of obvious benefits in our life. The maturity level of GaN power devices has been improving in the past years. Even though GaN market is still at the early stage so far, the author looks forward to big contribution of GaN power devices for future highly efficient energy society.

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## 20

# Growth of Single Crystal Diamond Wafers for Future Device Applications

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### 20.1 Introduction

Diamond as a mineral is known for several thousand years. It was found in nature and was valued most of the time for its appearance and for its mechanical properties. Ultimate values of stiffness and hardness still form the base for many industrial applications, e.g., as material for cutting tools.

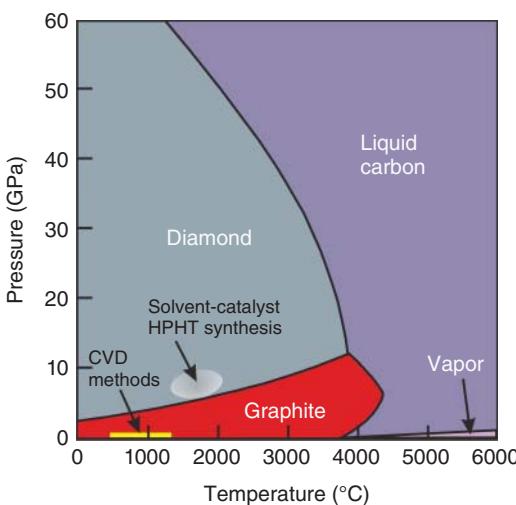
Later, it turned out that diamond excels in further characteristics comprising optical, thermal, and electronic properties. For electronic applications, carrier mobility  $\mu$ , saturation drift velocity  $v_s$ , the breakdown field strength  $E_m$ , and the thermal conductivity  $\lambda$  are relevant quantities. In power electronics, the opposing requirements of minimum losses in ON state and highest blocking voltages in OFF state are summarized in Baliga's figure of merit (BFM) given by

$$\text{BFM} = \frac{1}{4} \mu \epsilon_r \epsilon_0 E_m^3 \quad (20.1)$$

with  $\epsilon_r$  and  $\epsilon_0$  the relative permittivity of diamond and the vacuum permittivity, respectively [1]. Normalized to the value of silicon, diamond's BFM is by more than 4 orders of magnitude higher and even compared to 4H-SiC there is a factor of 40. Thus, diamond's high breakdown field of  $\approx 10$  MV/cm and the cubic dependence in Eq. (20.1) form the base for its qualification as the *ultimate semiconductor material*, at least in the field of high-power devices.

Their realization first of all calls for techniques to grow single crystals with excellent structural quality and purity. Furthermore, appropriate dopants preferentially with low activation energy and adequate methods for a controlled insertion of defined quantities of the dopants are necessary. Here, it turns out that thermodynamic stability and the extreme properties of diamond pose specific restrictions as compared to standard semiconductor materials.

Diamond and graphite are two crystalline allotropes of pure carbon. The enthalpy of formation under standard conditions is 1.9 kJ/mol higher for diamond than for graphite. As a consequence, graphite is thermodynamically the stable modification



**Figure 20.1** The phase diagram of carbon (restricted to the two solid allotropes diamond and graphite). The gray ellipse and the yellow bar indicate schematically the regions of the HPHT and CVD synthesis, respectively.

of carbon. The phase diagram of carbon in Figure 20.1 shows that the stability region of graphite extends at ambient pressure over the whole temperature region up to  $\approx 4000\text{ }^{\circ}\text{C}$  and up to pressures of several gigapascals.

According to the phase diagram, diamond is not stable at normal pressures. Nevertheless, spontaneous transformation does not occur due to the high kinetic barrier, e.g. an activation energy of 730 kJ/mol for the graphitization of the {110} surface [2]. This metastability explains that diamonds can have an age of several billion years, and it facilitates stable operation of diamond tools and devices even at elevated temperatures of several hundred degrees Celsius.

For the synthesis of diamond, two completely different concepts have successfully been developed. In the first one, the high-pressure high-temperature (HPHT) method, growth conditions are established under which diamond is the stable phase of carbon, while in the second one, the chemical vapor deposition (CVD) technique, diamond is metastable and growth is controlled by kinetics. The typical parameter regions are schematically indicated in Figure 20.1. In the following, both methods are described in detail, and their individual strengths and limitations are discussed with respect to the supply of the base material for power devices.

## 20.2 High-Pressure High-Temperature (HPHT) Synthesis

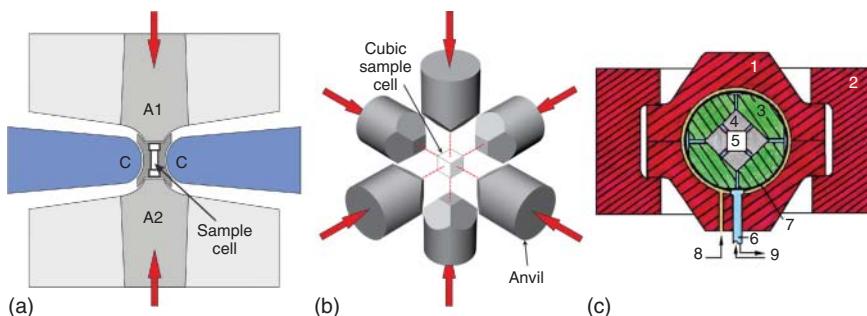
### 20.2.1 Basic Concepts and Technical Realizations

In the HPHT process, carbon material like graphite is filled into a growth capsule to transform it to diamond. According to the calculated Berman–Simon equilibrium line between graphite and diamond (see phase diagram), pressures of  $\approx 2\text{ GPa}$  are sufficient to reach the stability region of diamond at room temperature [3].

However, due to the slow kinetics, temperatures well above 1000 °C are needed to obtain acceptable transformation velocities which in turn call for even higher pressures. For the direct conversion of pure graphite to diamond pressures >10 GPa and temperatures >2000 °C are required and the produced material is typically polycrystalline [4–6]. During the original elaboration of the HPHT process at the General Electric (GE) Research Laboratory, it already turned out that the presence of molten metals can drastically mitigate the necessary conditions [7]. For mass production of diamond nowadays, metal alloys like Fe–Ni, Fe–Co, Ni–Mn are added to grow diamond out of a metal–carbon solution at pressures of 5–6 GPa and temperatures of 1300–1600 °C [8, 9].

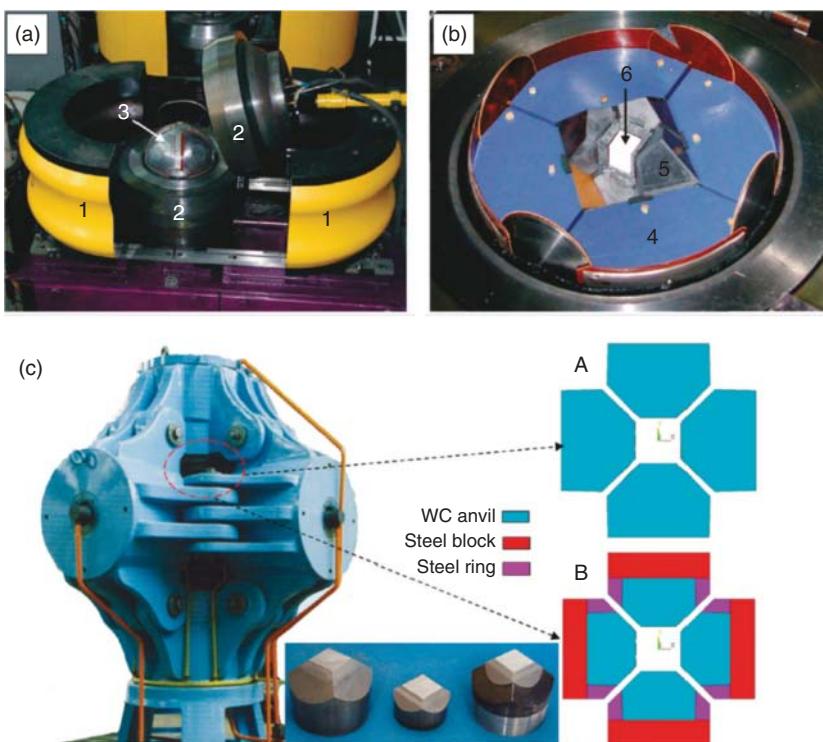
Concerning the specific role of the metal additives, two alternative models, i.e., the action as pure solvents for the carbon atoms and the action as catalyst were under debate for a long time [10]. While some authors claim that the metals serve purely as solvents [11], the term solvent catalyst is still common in literature [9, 12].

Development of technical setups that can produce and sustain the required pressures and temperatures in a sufficiently large volume for 50–100 hours or more was in the focus of R&D on the HPHT technology. The original high-pressure belt apparatus used for the first successful diamond synthesis [13]<sup>1</sup> at GE labs in 1954 consisted of two opposing pistons tipped with anvils for the transfer of the pressure [11, 14] (see Figure 20.2a). The belt-type concept was further refined by companies like Element Six or Sumitomo for the commercial production of synthetic diamond



**Figure 20.2** Schematic representations of three common HPHT growth setups: (a) In the belt-type apparatus, two anvils A1 and A2 compress the sample cell in the center in two opposing directions. These anvils and the belt C are made of WC-Co. (b) In the standard cubic apparatus, six anvils act along three perpendicular axes (adapted from [9]). (c) In the split sphere (BARS) arrangement, the pressure chamber (1) consisting of two half spheres is pressurized with oil (8). The eight large anvils (3) transfer the pressure via six pyramid-shaped WC-Co anvils (4) to the growth cell (5). (2) safety clamps, (6) power inlet, (7) rubber membrane, (9) cooling water. Source: (a) Adapted with permission from Nassau and Nassau [11]. © 1979 Elsevier. (c) Reprinted with permission from Abbaschian et al. [15]. © 2005 Elsevier.

<sup>1</sup> Historically, the first diamond synthesis by man was achieved already one year earlier in 1953 by E. Lundblad and his team at Allmänna Svenska Elektriska Aktiebolaget (ASEA) in Sweden – since these results were kept secret for several years the credit for the first successful diamond synthesis went to the GE team (see Ref. [13]).



**Figure 20.3** Photos of typical growth setups. (a, b) BARS setup with (1) clamps, (2) assembly with semi-sphere cavities, (3) multi-anvil block with a diameter of 300 mm, (4) steel anvils, (5) tungsten carbide anvils, and (6) high-pressure growth cell. (c) Photo of cubic high-pressure apparatus with schematic cross section of the multi-anvil assembly consisting of anvils with (A) traditional and (B) hybrid design. The inset shows an optical photo of different anvils. The overall height of the setup is  $>3$  m [17]. Source: (a, b) Reprinted with permission from Palyanov et al. [18]. © 2010 American Chemical Society. (c) Reprinted with permission from Han et al. [19]. © 2011 American Chemical Society.

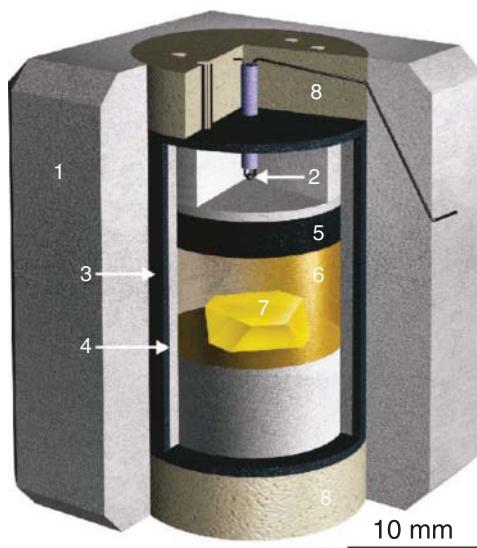
[4]. A modified version with uniaxial compression is the toroid anvil setup [4, 16]. Development of alternative multi-anvil geometries started already in the 1950s first with the invention of a tetrahedral press with four anvils [11]. Further technologically relevant multi-anvil-type setups are the standard cubic press that uses six anvils [9] (see Figure 20.2b) and its modification, the split sphere (also known by the Russian abbreviation BARS) setup [15], shown in Figure 20.3c.

Typical growth setups are shown in Figure 20.3.

### 20.2.2 The Temperature Gradient Method

Spontaneous nucleation of diamond from the supersaturated metal–carbon solution can be used to produce small grit for grinding and polishing applications. It should be avoided for the synthesis of large crystals with high structural quality. Instead,

**Figure 20.4** Schema of a high-pressure growth cell used in a BARS setup. (1)  $\text{ZrO}_2$  container, (2) thermocouple, (3) graphite heater, (4)  $\text{MgO}$  sleeve, (5) graphite as carbon source, (6) metal melt, (7) diamond seed, (8) talc ceramics. Source: Reprinted with permission from Palyanov et al. [18]. © 2010 American Chemical Society.



a single crystal or an arrangement of sacrificial diamonds is used as seeds, and a well-defined temperature profile is realized within the pressure cell (temperature gradient method). This guarantees that the carbon is dissolved in the metal solution in the hot region and precipitates on the seed crystals located in the colder region in a kind of homoepitaxial growth process. The design of a typical high-pressure growth cell is shown in Figure 20.4.

### 20.2.3 Chemical Purity and Classification

The HPHT growth environment contains various chemical elements besides the indispensable carbon. Their relevance for the final crystal quality strongly depends on (i) the incorporation coefficient and (ii) their impact on the physical properties of the crystals.

The elements that form the solvent catalyst are present in stoichiometric concentrations at the liquid–solid interface of the growing diamonds. Their incorporation is, however, rather limited which is usually attributed to the low solubility in the dense crystal lattice, i.e. the extraordinary small covalent radius of  $\text{sp}^3$ -carbon which results in the highest atom number density of all solid materials ( $1.77 \times 10^{23} \text{ cm}^{-3}$ ) [20]. Nevertheless, traces of Ni, Co, and various other elements are found in dispersed form in HPHT grown diamond giving rise to a huge number of color centers [21], some of them having attracted the interest of the quantum optics community [22].

Light elements like H, B, N are easily inserted into the diamond crystal lattice. Specifically, nitrogen incorporates over a large range of concentrations either as isolated substitutional point defect (called “C” center) or aggregated forming different complex centers (like “A” and “B” centers) [23, 24]. Both, absolute

**Table 20.1** Classification of diamond.

Type	I			II	
	IaA	IaB	Ib	IIa	IIb
[N] in ppm	>1			<1	
N center	A	B	C		
[B]	Low	Low	Low	Low	Dominant
Electrical resistance	Very high	Very high	Very high	Very high	Low
Color			Yellow		Blue

The identification of the different types of centers in type I crystals is done via their signature in IR spectra. In type II crystals, nitrogen is below the detection threshold in IR. In IIb crystals, the concentration of uncompensated boron is high enough to turn them semiconducting.

concentration and type of involved complexes are classification criteria to assign the crystals to different types. The distinguishing criterion between type I and II is a critical nitrogen concentration of about 1 ppm which represents the detection threshold for nitrogen related defects by infrared (IR) spectroscopy [25]. For a classification of different types of diamond see Table 20.1.

Substitutional nitrogen gives rise to a yellow color (pale yellow for 5–10 ppm, golden yellow for 50–100 ppm, increasingly greener for high concentrations). In the case of boron, 1 ppm of B produce a light blue, 10 ppm a deep blue color [3]. Doping with concentrations approaching the metal-to-insulator transition ( $\approx 2500$  ppm) [26] turns the crystals increasingly black.

Sources responsible for nitrogen incorporation during HPHT synthesis are nitrogen impurities in the solvent–catalyst metals and the carbon source material as well as gas inclusions in the growth cell [27]. Thus, the usual industrial diamond crystals are yellow as shown in Figure 20.5 (photos in upper row). To synthesize colorless high-purity crystals nitrogen getters like Al, Ti, and Zr are added. For the minimization of the boron content high-purity carbon sources are required. Finally, for the avoidance of Ni incorporation, high-purity Fe–Co provides a viable strategy. Examples of colorless IIa-type HPHT diamond crystals with impurity concentrations [N], [B], [Ni] < 0.1 ppm obtained in this way are shown Figure 20.5 (photos in the bottom row).

#### 20.2.4 Morphology and Structural Quality

Crystal growth under HPHT conditions is generally a three-dimensional process that can involve several different families of crystallographic planes. For usual process parameters, the crystal habit is dominated by {111} and {100} facets. It can vary from purely cubic over cubo-octahedral to octahedral shape. With lower probability {110}, {113}, {117}, and even higher indexed planes can occur [29, 30]. Their appearance is controlled by the *P*–*T* conditions and the composition of the solvent–catalyst. Higher temperatures generally favor the formation of octahedral crystals [30]. Examples



**Figure 20.5** Cubo-octahedral-shaped diamond crystals grown by the temperature gradient method at different temperatures. Substitutional nitrogen ( $\approx 100$  ppm) causes the yellow color of the Ib-type crystals in the upper row. In the type IIa crystals in the lower row, the nitrogen concentration is  $< 0.1$  ppm. Source: Reprinted with permission from Sumiya and Tamasaku [28]. © 2012 The Japan Society of Applied Physics.

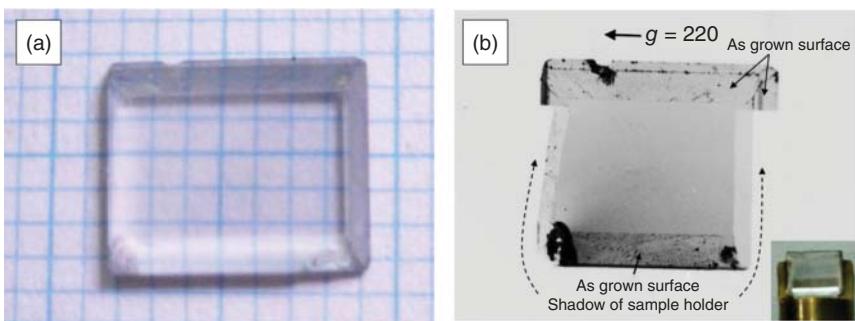
of various cubo-octahedral-shaped crystals which confirm this trend are shown in Figure 20.5.

The schema in the bottom of Figure 20.5 describes the development of the crystal shape starting from (001)-oriented seeds. With higher temperatures the ratio  $v_{001}/v_{111}$  between growth rates along the crystallographic  $\langle 100 \rangle$  and  $\langle 111 \rangle$  directions increases thus causing a relative decrease in size of the  $\{100\}$  cube facets as compared to  $\{111\}$  faces. The crystal habit changes toward octahedron shape.

The growth sectors do not only differ in growth velocity but also in the uptake of impurities and the incorporation of structural defects. This has the important consequence that plates cut out of HPHT crystals typically show clearly distinguishable regions with different color (in the case of Ib-type samples) and structural defects (like dislocation densities) which reflect the former growth sectors.  $\{100\}$  growth sectors typically show the highest structural quality facilitating under optimum conditions virtually extended dislocation-free regions (see Figure 20.6).

## 20.2.5 State of the Art in Crystal Size

Large synthetic single crystals like the yellow 9 ct crystal manufactured by Sumitomo around 1990 [31] and the yellow 34.8 ct crystal produced by De Beers in a 600 hours process and first presented 1992 at the Japan International Machine Tool



**Figure 20.6** Diamond plate cut in (001) orientation from a IIa-type HPHT crystal.  
 (a) Optical image and (b) transmission X-ray topograph. Crystal size:  $7.5 \times 6 \times 0.7 \text{ mm}^3$ .  
 Source: Reprinted with permission from Sumiya and Tamasaku [28]. © 2012 The Japan Society of Applied Physics.

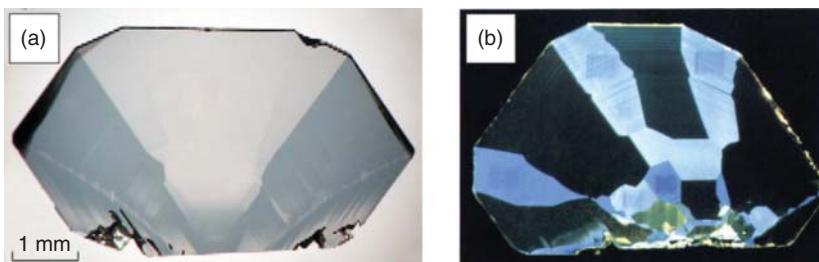
Fair in Tokyo [32] were rare objects manufactured in laboratory scale experiments. In 2012, Sumitomo described 8–10 ct large crystals of type IIa which facilitated the cutting of (001)-oriented slices with an edge length of 12 mm [28]. In the subsequent years, the St. Petersburg-based company New Diamond Technology (NDT) pushed the limit for IIa-type crystals to ever-larger size using the Chinese technology shown in Figure 20.3c. At the ICDCM diamond conference 2017 in Gothenburg [17], crystals with a size up to 61 ct (as-grown) were presented in the talk given by A. Katrusha and plates of  $15 \times 15 \text{ mm}^2$  are commercially available on the company website (01/2020) ([http://ndtcompany.com/products/single\\_crystal\\_diamond\\_plates](http://ndtcompany.com/products/single_crystal_diamond_plates)). Evaluation of the dislocation densities revealed moderate values on the order of  $10^3 \text{ cm}^{-2}$  [33].

### 20.2.6 Boron Doping

Boron doping to turn the crystals p-type semiconducting was successfully achieved already in the early days of HPHT research [34]. In contrast, the reliable realization of n-type conductivity, which is nowadays routinely done by in situ phosphorous doping during CVD diamond growth [35], is still a challenge for HPHT synthesis [36].

For the synthesis of boron-doped diamond, boron or boron-containing compounds are added to the HPHT growth system. Since substitutional nitrogen acts as a 1.7 eV deep donor, nitrogen getters like for the synthesis of colorless IIa crystals are needed to avoid a compensation of the B acceptors. In this way, boron-doped diamond with B concentrations ranging from few ppb to several thousand parts per million [37] have been synthesized. In heavily boron-doped diamond samples from the HPHT technique, superconductivity has been observed in 2004 [38].

Boron incorporation is highly growth sector dependent. Blank et al. report 6–8 times higher concentrations of uncompensated acceptors in {111} than in {100} growth sectors [39]. As a consequence, electronic properties will drastically vary



**Figure 20.7** Boron-doped diamond crystals grown by the HPHT technique. The variations are due to drastic differences in incorporation efficiency for different growth sectors.  
 (a) Transmission optical micrograph of a 397- $\mu\text{m}$ -thick slab cut parallel to (110).  
 (b) Cathodoluminescence topograph of a sample taken at room temperature looking along [110]. Source: (a) Reprinted with permission from Blank et al. [39]. © 2007 Elsevier.  
 (b) Reprinted with permission from Burns et al. [40]. © 1990 Elsevier.

laterally when substrates are employed which were grown on different sectors as for the examples shown in Figure 20.7.

In the context of high-power electronics, boron-doped substrates are of interest as growth substrates for the fabrication of vertical Schottky barrier [41] or p-i-n diodes [42] by subsequent CVD growth on top.

## 20.3 Chemical Vapor Deposition (CVD)

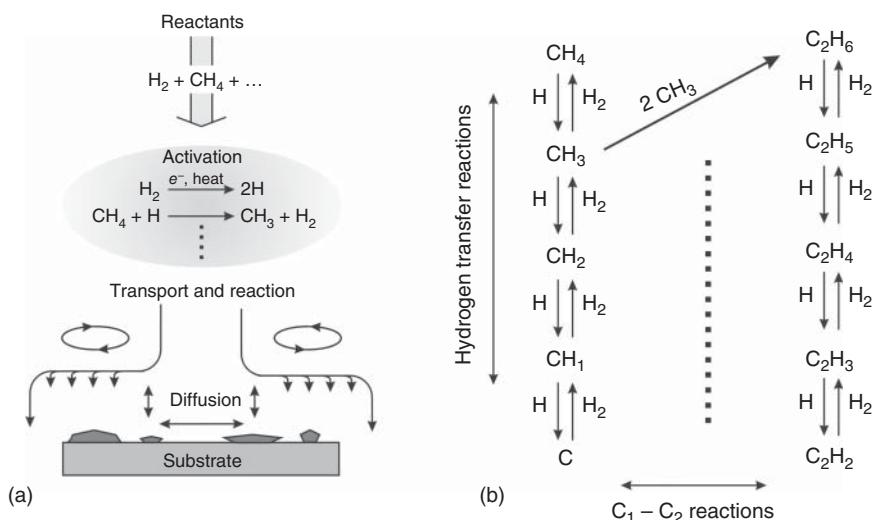
### 20.3.1 Basic Principles

#### 20.3.1.1 The Mechanism of Diamond Growth by CVD

In contrast to the HPHT method, growth by CVD takes place at pressures of few to several hundred millibars and temperatures of 500–1200 °C. Under these conditions, graphite is the stable allotrope of carbon. Diamond formation is therefore controlled by kinetics instead of thermodynamics.

Atomic hydrogen plays the central role in CVD diamond growth, and the major technological challenge consists in its efficient generation and transport to the growth surface. Within the standard model, atomic hydrogen participates in the following crucial processes:

- (a) Hydrogen atoms terminate the surface  $\text{sp}^3$  bonds, thus stabilizing the diamond lattice and preventing a rearrangement to graphitic  $\text{sp}^2$  carbon.
- (b) Molecular hydrogen is dissociated into atoms that react with the carbon-containing molecules creating a complex mixture of hydrocarbon species. These include also the reactive hydrocarbon radicals that are required for the surface growth processes. So the whole gas phase chemistry is driven and controlled by the atomic hydrogen.
- (c) At the diamond surface, the H radicals abstract adsorbed surface H-atoms, thus creating dangling bonds which can act as sites for the adsorption of  $\text{C}_x\text{H}_y$  growth species.



**Figure 20.8** (a) A simple schema showing the principal elements of CVD diamond growth: process gases flowing into the reactor, activation of the reactants by thermal or plasma processes which induces the complex gas phase processes, transport of the activated species to the growth surface by convection and diffusion, and finally the surface growth processes. Source: Butler and Woodin [43, 44]. © 2017, Royal Society. (b) The principal gas phase reactions in a  $\text{CH}_4/\text{H}_2$  feed gas mixture involve “H-shifting” reactions [45] amongst different  $\text{C}_1$  or  $\text{C}_2$  species and the bimolecular hydrocarbon reactions forming  $\text{C}_2$  and higher species [43].

- (d) Finally, to integrate the new carbon atom into the crystal lattice, the adsorbed hydrocarbon species (e.g.  $\text{CH}_3$ ) have to be dehydrogenated in several consecutive hydrogen abstraction steps.

The general features of CVD diamond processes, as schematically summarized in Figure 20.8, comprise the flow of gaseous reactants typically containing 90–99% of hydrogen and 1–10% of a hydrocarbon gas like methane into a reactor where they are activated thermally or via a plasma to generate atomic hydrogen and  $\text{C}_x\text{H}_y$  species. These are transported via convection and diffusion to the growing diamond surface where they participate in the diamond growth processes and deliver the required carbon.

The gas activation processes dissociate the molecular hydrogen into atoms. These react with the inert hydrocarbon feed gas molecules like  $\text{CH}_4$  and transform them into a complex mixture of other hydrocarbon species including reactive carbon-containing radicals which can act as growth species. The schema in Figure 20.8b shows the fast H-shifting reactions with  $\text{C}_x\text{H}_y$  ( $x = 1, 2$ ) species which cause abstraction or addition of atomic hydrogen and indicates various transfer reactions between  $\text{C}_1$  and  $\text{C}_2$ . Even for the simple  $\text{CH}_4/\text{H}_2$  gas composition, 20–30 species and more than 100 reactions have to be considered to describe the chemistry adequately [46]. At high pressures and gas temperatures,  $\text{C}_2\text{H}_2$  is the dominating species in the gas volume [45, 47].

A large number of studies have been devoted to the identification of the growth species [48] by evaluating correlations between growth rate and the concentrations of reactive species in direct vicinity to the crystal surface. Furthermore, the absolute arrival rates have to be high enough to deliver sufficient carbon, and the reactivity of the species has to be taken into account (which directly rules out CH<sub>4</sub>). Most studies revealed a major role of CH<sub>3</sub>. Under certain process and excitation conditions, C<sub>2</sub>H<sub>2</sub> can yield relevant contributions.

Using the model proposed by Harris and Goodwin [49] in a simplified version which considers only two gas phase species involved in the growth processes (atomic hydrogen H and CH<sub>3</sub>) and few surface reactions [50], it was possible to simulate the experimentally obtained growth rates consistently over more than 2 orders of magnitude [50, 51]. This result strongly supports CH<sub>3</sub> as dominating growth species under typical process conditions.

### 20.3.1.2 Gas Mixtures for Diamond CVD

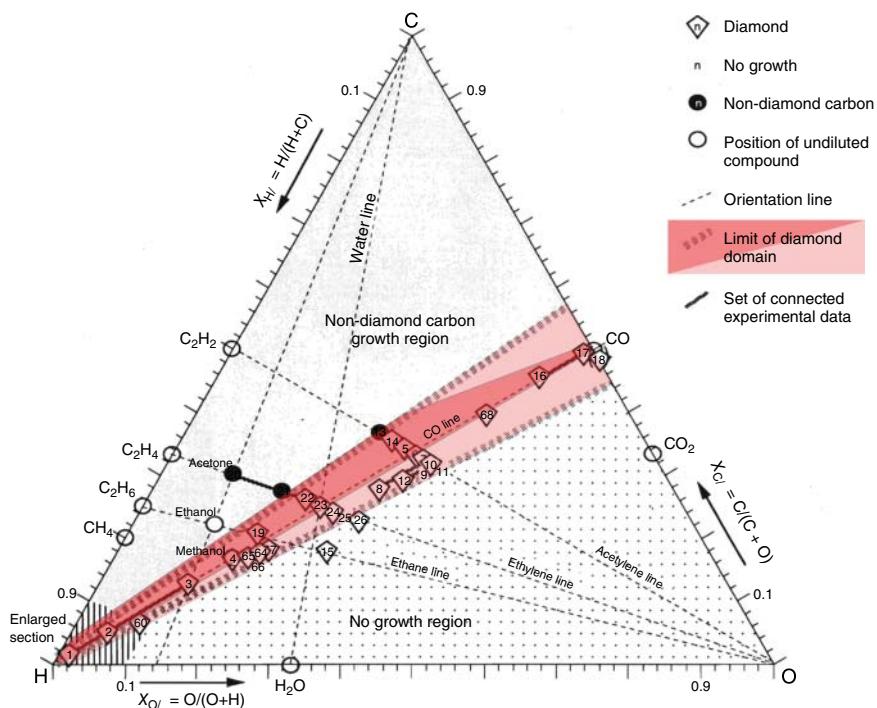
A couple of variations and alternatives to the simple CH<sub>4</sub>/H<sub>2</sub> gas mixtures have been explored. These included other carbon sources (larger hydrocarbon molecules, fullerenes), alternative chemistries based on halogens instead of hydrogen [52], the addition of oxygen containing molecules, and finally noble gases (Ar).

For the deposition of nanocrystalline diamond (NCD) and ultrananocrystalline diamond (UNCD) films, argon has been added [53] or pure Ar/CH<sub>4</sub> gas mixtures have been used [54]. In the context of high-quality single crystal growth, addition of Ar reduces the thermal conductivity of the gas mixture in plasma-activated processes thus increasing gas temperature, hydrogen dissociation, and as a consequence the growth rate [55].

Technologically most relevant is the addition of stoichiometric quantities of oxygen. With their C–H–O diagram, Bachmann et al. have introduced a general concept for the selection of gas mixtures appropriate for the growth of diamond (see Figure 20.9) [56].

Each point in the C–H–O triangle corresponds to a defined stoichiometric ratio [C]:[H]:[O]. The corners define the pure elements (100%), along the edges there is a continuous variation in the composition of only two elements. The middle of the C–O edge corresponds to CO. Only within a narrow region around the CO line, diamond growth is possible. Above this range, the excess of carbon causes the deposition of non-diamond graphitic phases, below etching prevails. The applicability of this diagram is based on the fact that the chemistry is independent of the specific precursors supplied into the growth reactor.

Based on the first data set, the authors predicted the wedge-shaped region (bright red in Figure 20.9). Subsequent refinement yielded the lens-shaped area (dark red in Figure 20.9). Posterior experiments by other authors at high gas pressures, high substrate temperatures, and especially during homoepitaxial deposition revealed that high-quality diamond can be grown with CH<sub>4</sub> concentrations up to 20% [58], proving that the diamond domain can be significantly wider around the H corner under specific conditions. As a consequence, the C–H–O diagram should only be taken as a useful but rough guideline.



**Figure 20.9** C-H-O diagram for the deposition of diamond. Highlighted in red are the regions of gas compositions appropriate for diamond growth. Bright red: original wedge-shaped region [56]. Dark red: refined data [57]. Source: Reprinted with permission from Bachmann et al. [56] and Bachmann et al. [57]. © 1991 Elsevier.

### 20.3.1.3 The Role of Trace Gases

To avoid impurities that can modify the optical properties or induce electronically active defect states, ultra-pure gases (99.9999% and better) are used in the synthesis of electronic-grade diamond material, and all reactor components are selected carefully. Prominent examples of detrimental impurities are nitrogen that acts as a 1.7 eV deep donor and boron that forms a 0.37 eV deep acceptor level in diamond. Besides this, their presence in trace concentrations in the gas phase can modify the growth velocity.

Nitrogen addition at ppm level can drastically accelerate diamond growth. For polycrystalline diamond, an increase by a factor of 6 was reported by addition of 25 ppm nitrogen [59]. For homoepitaxial growth on (001)-oriented crystals, recent experiments in the author's lab revealed factors of up to 13 for 400 ppm nitrogen in the process gas [60]. The effect is growth sector dependent and strongest on {100} faces [61]. This has a pronounced impact on the granularity and promotes the formation of textures with ⟨100⟩ fiber axis in polycrystalline films [62]. Furthermore, addition of nitrogen represents an efficient and widely used strategy to stabilize homoepitaxial growth on (001) substrates by suppressing non-epitaxial crystallites like twins.

The strength of the nitrogen effect is quite sensitive to the method used for the activation of the gas phase: While low ppm levels are sufficient in CVD reactors with plasma activation of the gas phase, hot filament (HF) methods require significantly higher concentrations (500–4000 ppm at 1% CH<sub>4</sub> in H<sub>2</sub>) [63].

Concerning the responsible mechanisms, the low absolute concentrations that are sufficient to induce measurable effects exclude gas phase processes as a relevant explanation. Instead, catalytic effects directly at the growth surface yield a reasonable explanation [64].

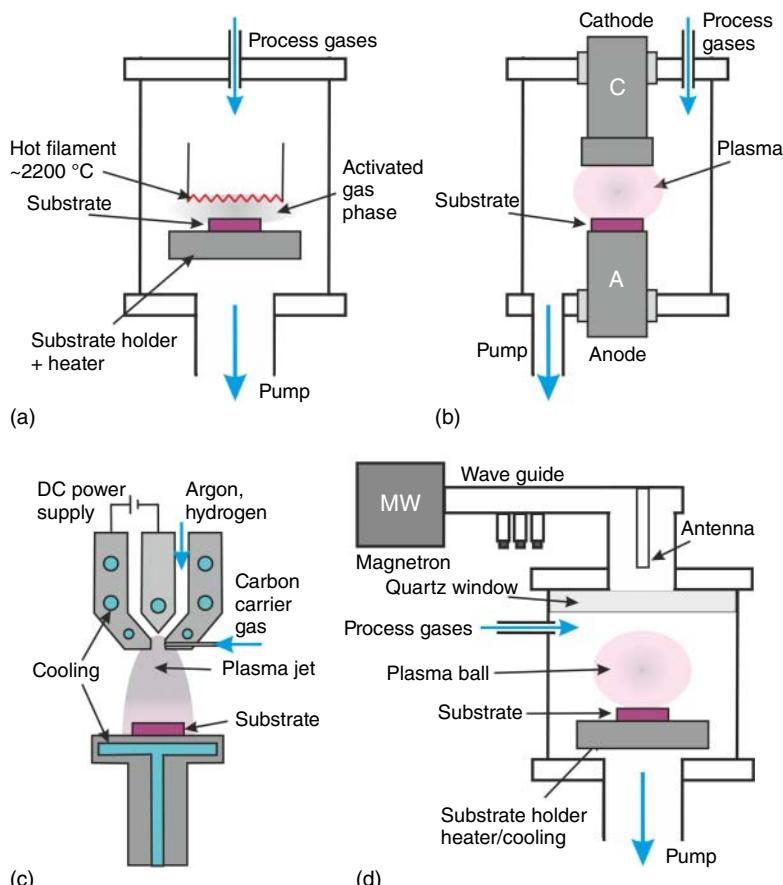
Growth acceleration by nitrogen is extremely sensitive to the presence of even lower concentrations of boron [65]. In microwave (MW) reactors, below a critical threshold of [N]/[B] ≈ 10<sup>3</sup>, the effect of nitrogen is completely canceled by boron which acts as a kind of catalyst poison.

#### 20.3.1.4 Experimental Setups

A crucial step toward technologically relevant growth rates in diamond CVD was the awareness that substrate surface temperature and gas phase temperature have to be decoupled so that the latter can be significantly higher [66]. Thereupon, various diamond CVD techniques have been developed which mainly differ in the method of gas phase activation with strong implications on the scalability to larger areas and growth rates. Four of the technologically most relevant techniques are schematically shown in Figure 20.10.

**Hot Filament (HF) CVD** In the hot filament method, the source gases interact with a hot surface which is usually a thin wire of refractory metals like Ta, W, or Re. The gases are decomposed into hydrocarbon radicals and atomic hydrogen which are transported by diffusion and convection to the substrate surface. Typical operating conditions are a pressure in the range of 1–100 mbar, a substrate temperature of 600–1200 °C, filament temperatures of 2000–2600 °C, a distance filament–substrate of 1–20 mm, and feed gas mixtures of 0.1–7% hydrocarbons in H<sub>2</sub> [67]. Oxygen can be added optionally (typically in the range of 0–3%). For very high filament temperatures and methane concentrations, growth rates of 10 µm/h are feasible [68]. However, these conditions limit filament lifetime and enhance incorporation of metal atoms from the filament into the films. Concentrations in the 0.1 at% range have been measured even for moderate filament temperatures [69]. Thus, in production setups, lower filament temperatures and growth rates in the 1 µm/h range are common. The huge advantage of the method is its comparatively easy scalability via extended arrays of parallel wires to large areas of up to 50 × 100 cm<sup>2</sup> [70] and the feasibility to coat 3D bodies. Modifications of the technique are forced convection of the gas to accelerate the transport of the reactive species to the growth surface as well as bias assistance to accelerate the electrons emitted from the filament and to ignite a plasma thus enhancing the activation of the gas phase and increasing the growth rate to 3–5 µm/h [71].

**DC-Plasma CVD** The direct current (DC) plasma technique is a rather simple method to generate an electrical discharge and to ignite a plasma. The schema in



**Figure 20.10** Schemata of different reactors: (a) hot filament CVD, (b) DC plasma CVD, (c) DC plasma jet CVD, (d) microwave plasma CVD.

Figure 20.10b shows the cylindrical cathode and anode with the DC power supply. The substrate is placed on the anode. If placed on the cathode, amorphous carbon is deposited [72] due to the intense bombardment with positive ions. The technique shows its greatest potential at high gas pressures: for 200 mbar and current densities of  $>10 \text{ A/cm}^2$ , gas temperatures of  $\approx 6000^\circ\text{C}$  with growth rates of  $250 \mu\text{m/h}$  were reported. However, with increasing pressure, the deposition area shrinks severely ( $1\text{--}2 \text{ cm}^2$ ) [73]. In the meantime, scaling to 8-in. wafer size with growth rates of  $9 \mu\text{m/h}$  for the deposition of polycrystalline diamond has been reported [74].

**DC-Plasma Jet CVD** A further increase in the pressure in a DC-plasma system can be achieved by separating the activation region from the diamond growth region as for the plasma torch [73]. In the DC-plasma jet (see schema in Figure 20.10c) that can operate up to atmospheric pressure a gas mixture of argon and hydrogen is ionized and heated to temperatures of  $>5000^\circ\text{C}$  by a DC arc discharge before it leaves the plasma generator through a nozzle and expands into the reactor vessel which

can be at significantly lower pressure. The carbon carrier gas is typically introduced into the gas mixture close to the gas exit. Growth rates of up to 930 µm/h have been reported for this technique [75]. The restriction to small deposition areas has been overcome by application of magnetic fields that induce a rotation of the arc root and by an appropriate design of the gas flow facilitating growth rates of 40–50 µm/h over an area of 110 mm in diameter [76]. Modifications of the plasma jet operate with inductively coupled radio-frequency (RF) or microwave (MW) excitation [77]. Both are electrodeless which means a lower risk of contamination by electrode material.

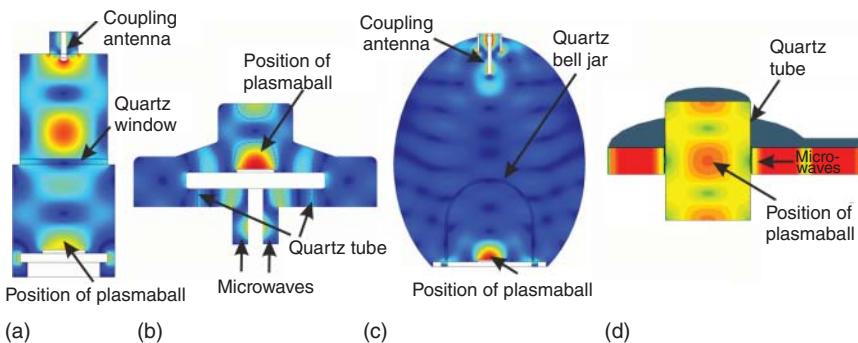
**Microwave Plasma Chemical Vapor Deposition (MWPCVD)** In microwave plasma chemical vapor deposition (MWPCVD), microwaves are fed into a reactor vessel through a dielectric window (typically quartz). Inside the reactor, at reduced pressure, an electrical breakdown occurs, and a plasma is ignited in the region of maximum electric field strength. The substrate is placed close to this position. After ignition of the discharge, the pressure can be increased and growth typically occurs at pressures of 20–400 mbar.

The first MWPCVD experiments were reported by Japanese researchers at the National Institute for Research in Inorganic Materials (NIRIM) in 1983 [78]. The used frequency of 2.45 GHz was identical to the operating frequency of the standard microwave oven present in virtually every kitchen. The original NIRIM-type reactor consisted of a quartz tube that was fed through the broad side of a fundamental mode rectangular metal wave guide. Inside the tube in the waveguide, a plasma was ignited. The setup is still used in the research area, but the schema shown in Figure 20.10d is more common: here, the microwaves generated by the magnetron propagate in the waveguide to the reactor where they are coupled into the chamber through a dielectric window (quartz). The inner chamber diameter was chosen so that it can sustain only one microwave radial mode at this frequency. The TE<sub>10</sub> mode, which is the fundamental propagation mode in the waveguide, is converted into the cylindrical TM<sub>01</sub> mode inside the reactor [79].

This reactor type originally developed and commercialized by Applied Science and Technology, Inc. (ASTeX, USA), now continued by Seki Diamond Systems (Cernes Technologies Ltd., Japan), has been used extensively in the research area. Substrates with a diameter up to 100 mm can be inserted and coated at low pressure (several 10 mbar). The setup has also successfully been applied to grow single crystals at pressures of 300 Torr with growth rates of 165 µm/h and final thicknesses of up to 18 mm [80].

Several alternative reactor designs based on the 2.45 GHz microwave frequency have been developed in the following. These comprise the overmoded cavity plasma reactor by ASTeX (“clamshell design”) [79], the ellipsoidal plasma reactor developed by the Fraunhofer Institute [81] and the cylindrical resonator with annular slots (CYRANNUS) design commercialized by the Innovative Plasma Systems GmbH ([www.iplas.de](http://www.iplas.de)). The concepts for the coupling of the microwaves of the different reactors are shown in Figure 20.11.

Due to its  $\approx 2.7$  times larger wavelength, 915 MHz was chosen to scale the three reactor types (Figure 20.11b–d) to larger areas and higher absolute power. In



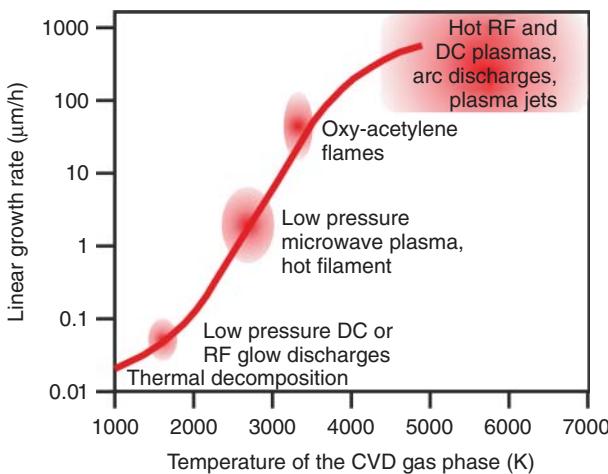
**Figure 20.11** Simulations of the electric field distribution for different microwave reactor geometries. Depending on the design, the quartz windows through which the microwaves enter the reactors have the shape of a plate, a bell jar, or a tube. The field maxima (yellow-red) inside the reactors indicate where the dielectric breakdown will occur and the plasma ball will form. Ideal pressure conditions for the ignition are on the order of 10 mbar. Atmospheric pressure outside the reactor vessel prevents discharge formation in the waveguide or at the antenna. (a) The classical ASTeX reactor as schematically indicated in Figure 20.10d, (b) the overmoded ASTeX reactor, (c) the ellipsoidal reactor, and (d) the CYRANNUS reactor (simulated without substrate holder which is inserted from the bottom of the quartz tube). Source: Adapted with permission from Silva et al. [82]. © 2009 Institute of Physics IOP Publishing.

the opposite direction, i.e. toward higher frequency, millimeter waves of 30 GHz gyrotrons have been used to generate a plasma above the substrate by four or two crossing beams [83, 84]. The specific benefit of 30 GHz radiation is the higher penetration depth of the microwave field which facilitates high plasma densities (electron densities  $>10^{13} \text{ cm}^{-3}$ ).

Besides the described technologically most relevant techniques, further approaches have been explored like the combustion flame growth (oxygen–acetylene torch) [85] or the photon plasmatron that uses CO<sub>2</sub> laser radiation to ignite an atmospheric plasma working even in air without reactor chamber [86, 87].

### 20.3.1.5 Growth Rate and Gas Temperature

A comparison between all the different deposition techniques yields the first conclusion that high growth rates require high gas temperatures in the activation zone (see Figure 20.12). In the case of MW activation, an increase in pressure at constant input power automatically results in a shrinking plasma ball and an increasing plasma temperature. For the transition from  $\approx 50 \text{ mbar}$  to  $\approx 400 \text{ mbar}$ , the absorbed power density changes from  $\approx 5\text{--}10 \text{ W/cm}^3$  to  $1000 \text{ W/cm}^3$  accompanied by a rise in H and CH<sub>3</sub> radical density by factors of 1000 and 10, respectively [51, 88]. This stronger activation of the gas phase, specifically the increase in atomic hydrogen, widens the range of useful methane concentrations up to 20% and facilitates growth well above 1000 °C where the density of dangling bonds which are adsorption sites for growth species is higher [44]. The combined action of all these effects explains the huge benefit of high pressures beyond the simple gas kinetic increase in arrival



**Figure 20.12** Correlation between temperature of the gas phase in the activation zone and typical growth rates for different activation methods. Source: Redrawn with permission from Bachmann et al. [56]. © 1991 Elsevier.

rate of particles at the surface [89]. To keep the size of the deposition area constant, the input power has to be increased appropriately.

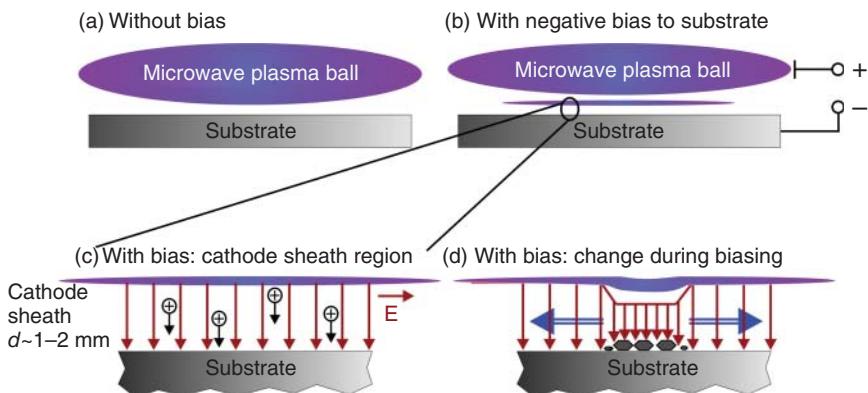
In the field of semiconductor materials, purity is a further aspect of major relevance. Here the activation with the hot filament, besides its limited growth rates, shows major disadvantages. Among the plasma techniques, contactless concepts like MW activation are preferred. In the meantime, high-power 915 MHz reactors facilitate scaling of the deposition area to several 10 cm in diameter in combination with growth rates  $>10 \mu\text{m}/\text{h}$  so that they offer an attractive technical solution for the commercial production of high-quality diamond wafers.

### 20.3.1.6 Nucleation by Seeding

Diamond growth can immediately start on existing diamond surfaces. This also works on c-BN with diamond grains growing immediately with an epitaxial alignment [90]. On surfaces of other materials, the density of grains is usually very low. Nucleation occurs only sparsely and in an uncontrolled way at irregularities. This behavior is attributed to a high nucleation barrier as a consequence of a high surface energy [91]. For technical purposes like the coating of technical parts to form a protective layer, scratching with diamond powder is a well-established method. Many different variations of this concept have been explored, but in the end, diamond debris was always left on the surface that provided seeds for the subsequent homoepitaxial growth [92]. By the use of nanodiamonds, e.g., from the detonation synthesis, maximum nucleation densities  $>10^{11} \text{ cm}^{-2}$  have been obtained [93].

### 20.3.1.7 Bias-Enhanced Nucleation (BEN)

Real nucleation of a new phase is achieved by the bias-enhanced nucleation (BEN) procedure [94]. It works on different materials like elemental semiconductors



**Figure 20.13** Schema of (a) a microwave plasma discharge above a substrate and (b) its modification during BEN. (c) The high electrical field in the cathode region accelerates positive ions toward the surface. (d) The local field enhancement above diamond-coated regions as typically observed for nucleation on Si (not on Ir). Source: Reprinted with permission from Schreck [106] © 2014 Elsevier.

(Si [94, 95]) and composite semiconductors (SiC [96]), metal carbides (TiC [97]), and pure metals (Mo [98], Ni [99, 100], Re [101], Ir [102]). In most cases, a carbide is formed at the surface during the BEN treatment, and the real nucleation finally occurs on this interlayer. For Ir, this scenario can definitely be ruled out.

The basic principle of the BEN procedure consists in the application of a negative bias voltage of 100–300 V to the substrate in MW plasma, in HF [103] or in DC plasma setups [102]. Under these conditions, the surface in contact with the plasma will be bombarded with positive ions. Few studies have been performed with positive bias. Some enhancement in nucleation density was found [104], but the effect was much weaker and nearly all the subsequent work was focused on negative bias.

In an MW plasma reactor, as shown schematically in Figure 20.10d, a negative bias voltage is applied to the substrate holder while the metallic chamber walls define the grounded reference. Alternatively, the substrate may stay at ground potential, and a positive voltage is applied to the plasma ball via an electrode, for example, a metal ring [105].

Figure 20.13 schematically shows the changes in the visible shape of the discharge that occur after application of a negative bias voltage to the substrate holder. Few millimeters above the cathode, a thin luminous layer separated by a dark space appears (Figure 20.13b). It resembles the negative glow in a classical glow discharge [107]. Measurements of the Stark splitting for the hydrogen Balmer lines directly above the biased substrate by optical emission spectroscopy (OES) reveal a field strength of several kilovolts per centimeter thus confirming that most of the applied voltage drops in this narrow region [108]. As a consequence, positive ions are accelerated (Figure 20.13c). In spite of a gas kinetic mean free path on the order of 10 μm, they can reach kinetic energies up to >100 eV as determined experimentally [109].

The hyperthermal particles hit the surface and induce several effects: first, they cause electron emission. Second, they can activate surface processes, and third, they can be deposited on the surface or implanted shallowly below the surface. This “subplantation” is typically the key process for the majority of models explaining the diamond nucleation by BEN which will be discussed later in context with the heteroepitaxy of diamond on iridium.

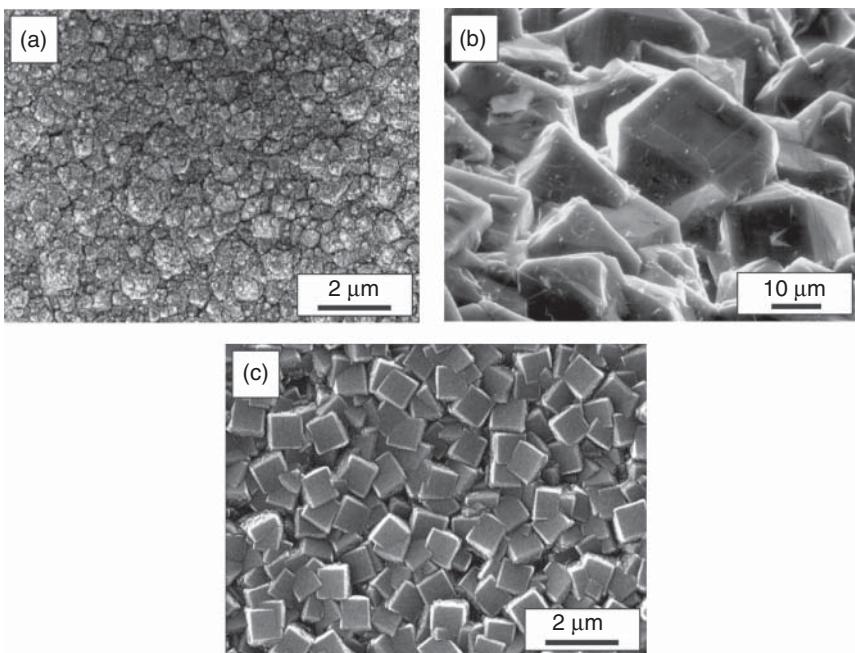
During BEN, small diamond grains can be found on the substrate surface after a short incubation time [110]. On nearly all substrate materials (except iridium), these tiny crystals immediately start to grow during BEN gradually covering the surface with a closed layer of diamond. This change can be noticed by a drastic rise in the biasing current by up to an order of magnitude [108]. The current increase is attributed to the significantly higher electron emission coefficient of hydrogen terminated diamond with its negative electron affinity as compared to other common substrate materials. As a consequence, the space charge density, the electric field strength, and the ion bombardment above diamond-coated regions increase as highlighted in Figure 20.13d.

While this feedback on the current provides a sensitive indicator for the status of the nucleation process, it also has severe negative implications: the field enhancement at the rim of a diamond covered area accelerates the nucleation in the immediate neighborhood. Thus, nucleation typically occurs first either in the center or at the edge of the substrate (the latter when the substrate holder is coated with diamond). This spot will then work as a starting point for a growth front that rapidly moves across the whole substrate inducing quite some inhomogeneity. Furthermore, the harsh ion bombardment is detrimental for the crystal quality. It can gradually change the crystal orientation, progressively increases the mosaic spread or nucleate crystals with completely new orientation [111–113]. Continuous renucleation can be desirable in the case of nano- or ultrananocrystalline diamond layers [114]. However, for the synthesis of homogeneous heteroepitaxial diamond wafers, all these phenomena are absolutely undesirable. The great success of Ir is therefore based not only on the significantly better alignment but also on the very weak feedback process (see below).

### 20.3.2 Examples of Polycrystalline CVD Diamond Layers

Figure 20.14 shows the surface of various polycrystalline diamond films grown by MWPCVD. The grain size of sample Figure 20.14a is well below 1 μm, while the other two samples consist of micrometer size crystals. The planar {100} facets in Figure 20.14c indicate a pronounced ⟨100⟩ fiber texture [115]. For microcrystalline layers with a surface morphology similar to Figure 20.14b, usually a ⟨110⟩ fiber texture is found [116, 117]. This also holds for nanocrystalline films [117].

The formation of textures with different fiber axes starting from randomly oriented seeds or nuclei can conclusively be explained by the principle of evolutionary selection of specific crystallite orientations. This concept, first proposed by Van der Drift [118], was successfully transferred to the growth of polycrystalline diamond by the definition of a growth parameter  $\alpha = \sqrt{3} v_{100}/v_{111}$



**Figure 20.14** Scanning electron micrographs of the surface of polycrystalline diamond layers grown by MWPCVD. (a) Nanocrystalline, (b) polycrystalline, and (c) polycrystalline diamond film with pronounced  $\langle 100 \rangle$  fiber texture.

with  $v_{100}$  and  $v_{111}$  the vertical growth rates on the  $\{100\}$  and  $\{111\}$  facets, respectively [115]. For cubo-octahedral-shaped crystals bounded only by  $\{100\}$  and  $\{111\}$  faces, it varies between 1 (cube) and 3 (octahedron). The parameter is also very useful to define regimes of stability toward twinning for homoepitaxial growth on these two growth sectors [119].

Besides these two low-Miller-index planes, in homoepitaxial growth on single crystal seeds stable  $\{113\}$  and  $\{110\}$  faces have been observed. For a correct modeling of the temporal development in 3D shape, it was therefore necessary to introduce two additional parameters  $\beta = \sqrt{2}v_{100}/v_{110}$  and  $\gamma = \sqrt{11}v_{100}/v_{113}$  [120, 121].

### 20.3.3 CVD Growth of Single Crystals

Polycrystalline diamond has been established in a range of high-tech applications such as wear-resistant coatings, cutting tools, heat spreaders, as well as optical components like windows for infrared, optical, UV, microwave, and X-ray radiation. However, in some fields, the polycrystalline nature prevents the devices from reaching the ultimate performance. This holds specifically for electronic devices which suffer from reduced charge carrier mobility [122] and detectors which show incomplete charge collection [123].

On the other hand, diamond single crystals synthesized by CVD methods have already demonstrated their unique potential in an impressive way by mobility

values of holes and electrons close to the theoretical limit [124, 125] and charge collection efficiencies close to unity [126]. As a consequence, strong efforts were directed toward a reproducible synthesis of high-quality single crystals in technologically relevant wafer size. Two fundamentally different approaches are currently being explored. The first one is based on homoepitaxial growth on high-quality crystals originally from the HPHT synthesis. It comprises typically the reuse of the substrates, the application of the CVD-grown crystals as new seeds, and various attempts to increase the lateral size. The second one uses heteroepitaxy on foreign substrates. Both concepts and their current state of the art will be described in the following.

### 20.3.4 Homoepitaxy

#### 20.3.4.1 Homoepitaxial Growth on Different Crystals Faces

The initial seed for homoepitaxial growth is usually a HPHT crystal. It is cut as a plate with parallel faces and polished to provide a defined crystallographic plane for the CVD growth process. Already in the earliest experiment of homoepitaxial growth by MWPCVD on (001)-, (110)-, and (111)-oriented single crystals, it turned out that the different growth sectors behave completely different [127]. In subsequent studies, it was found that (110) growth surfaces show a trend to develop {111} microfacets [128] and (111) surfaces are prone to stacking faults and twinning [129]. The  $\alpha$ -parameter concept described before provides a useful guide to identify growth conditions which suppress all twins on {100} faces and other conditions which facilitate the avoidance of penetration twins on {111} faces [119]. However, the contact twins for which the twin plane coincides with the growth surface cannot be avoided so easily.

In the meantime, dedicated growth strategies have been developed for (001), (110), (111), and (113) surfaces [130]. While growth on (001)-oriented crystals yields the highest crystal quality, incorporation of dopants is easier on the alternative crystal faces. Specifically, n-type doping by phosphorous is most efficient on (111). This face also offers the opportunity to incorporate nitrogen-vacancy (NV) centers with one preferential orientation, while (001) growth does not distinguish between four symmetry equivalent orientation variants.

An alternative strategy for an efficient avoidance of twins and other non-epitaxial crystallites consists in the deposition on vicinal faces which are tilted by few degrees away from the low Miller index crystal plane [131]. At a pressure of 200 mbar and 10% CH<sub>4</sub> in H<sub>2</sub> without any nitrogen a change of the off-axis angle from 0° to 6° increased the growth rate by a factor of 5 to  $\approx$ 28  $\mu\text{m}/\text{h}$  and completely suppressed non-epitaxial crystallites [58, 132]. This acceleration was attributed to the step flow growth mode, i.e., the lateral continuation of existing terrace edges without the necessity of nucleating new lattice planes as a rate-limiting step. The parameter space for the selection of growth conditions is widened, and there is no need for nitrogen as a measure to stabilize (001) growth. However, for small samples, the steps are consumed after a certain thickness and the surface gradually changes to lower off-axis angles closer to on-axis growth [58]. With larger wafer diameter, this restriction gets increasingly irrelevant.

### 20.3.4.2 Single Crystal Seed Recovery

HPHT single crystals of the type Ib with  $\approx$ 100 ppm of substitutional nitrogen are still quite common as seeds for homoepitaxy. Colorless IIa crystals as shown in Figure 20.6 are also attractive growth substrates. In the meantime, CVD grown material itself is often used as new seeds for homoepitaxial deposition processes. In all these cases, reuse of the seeds is compulsory for an economically viable synthesis of diamond by homoepitaxy. It may also become relevant in the future for the duplication of crystals produced by heteroepitaxy. Currently, there exist two established methods and one novel technique.

**Seed Recovery by Laser Cutting** The standard procedure is based on horizontal slicing of the sample after the growth process with a laser to separate the grown part from the seed. The latter will be re-polished before it is applied as new seed in the next deposition run [133]. Nd:YAG pulse lasers working with the infrared fundamental line at 1064 nm or with the frequency doubled line at 532 nm are frequently used ([www.bettontville.com](http://www.bettontville.com)). With larger lateral size a higher cutting depth is necessary and material loss due to the kerf increases. To cope with this problem, refined tools based on the guidance of a laser beam in a water jet have been developed ([www.synova.ch](http://www.synova.ch)) [134]. Limits for this new technique in terms of cutting depth are still under exploration.

**Liftoff and Cloning of Seeds by Ion Implantation** In an alternative approach, high-energy ion implantation is used to form a highly damaged sacrificial layer inside the sample that will later serve as predetermined breaking point. The method profits from the fact that the energy loss of ionized particles peaks at low energy (Bragg peak) causing maximum damage close to the end of the range. By careful choice of the implantation dose, amorphization can be achieved in the buried layer while the surface is still largely intact. In the original work, the top layer was split off after annealing to obtain a free standing few-micron-thick membrane [135]. Other researchers performed extended homoepitaxial growth before they induced the splitting and repeated the procedure to generate a set of nearly identical CVD crystals from one seed crystal [136]. Since the defect structure (specifically the density and distribution of threading dislocations) of all the grown crystals is quite similar and largely determined by the defect structure of the original seed, the term “cloning” has been introduced by the authors [137].

**Liftoff by Epitaxial Lateral Overgrowth (ELO) Using SiO<sub>2</sub> Masks** Recently, a new liftoff concept has been introduced [138]. It exploits the extremely low coefficient of thermal expansion (CTE) of SiO<sub>2</sub> which is even smaller than that of diamond. In a first step, a thin layer of SiO<sub>2</sub> is deposited on the surface of a seed crystal. This layer is then patterned by photolithography using a photoresist and reactive ion etching (RIE) to obtain an oxide mask with open windows and covered areas. In the subsequent epitaxial lateral overgrowth (ELO) process, diamond is grown homoepitaxially through the open windows and laterally across the SiO<sub>2</sub> regions until the mask is completely embedded in diamond. During cool down from deposition temperature

tensile stress develops in the diamond bridges, i.e., the diamond material that grew through the open windows of the mask. For small fill factor (FF), which is the fraction of surface area uncovered by mask material, the tensile stress is high enough to directly induce a cracking of the diamond bridges and a simple liftoff.

The ion implantation induced liftoff and the ELO process with  $\text{SiO}_2$  masks are intrinsically scalable to wafer size.

#### 20.3.4.3 Size Increase and Mosaic Growth

The quality of the homoepitaxial layer is usually not limited by small inclusions or point defects like chemical impurities in the seed crystals (provided that CVD growth is performed with ultrahigh purity gases). This rule does not apply to threading dislocations that end at the growth surface. They cannot simply stop at this interface but will be continued in the crystal lattice of the deposited material. Thus, HPHT crystals with ultralow dislocation density (down to zero) are the optimum starting point for the synthesis of CVD crystals. The intrinsic size limitations of the HPHT grown seeds stimulated activities to increase the sample size by the CVD processes. The three major concepts that have been explored comprise (i) the lateral expansion of the growth surface area by sophisticated growth protocols, (ii) the three dimensional enlargement by a sequence of growth steps on the {100} side faces [139], and (iii) the mosaic crystal wafer fabrication [137] (see Figure 20.15).

#### 20.3.5 Heteroepitaxy

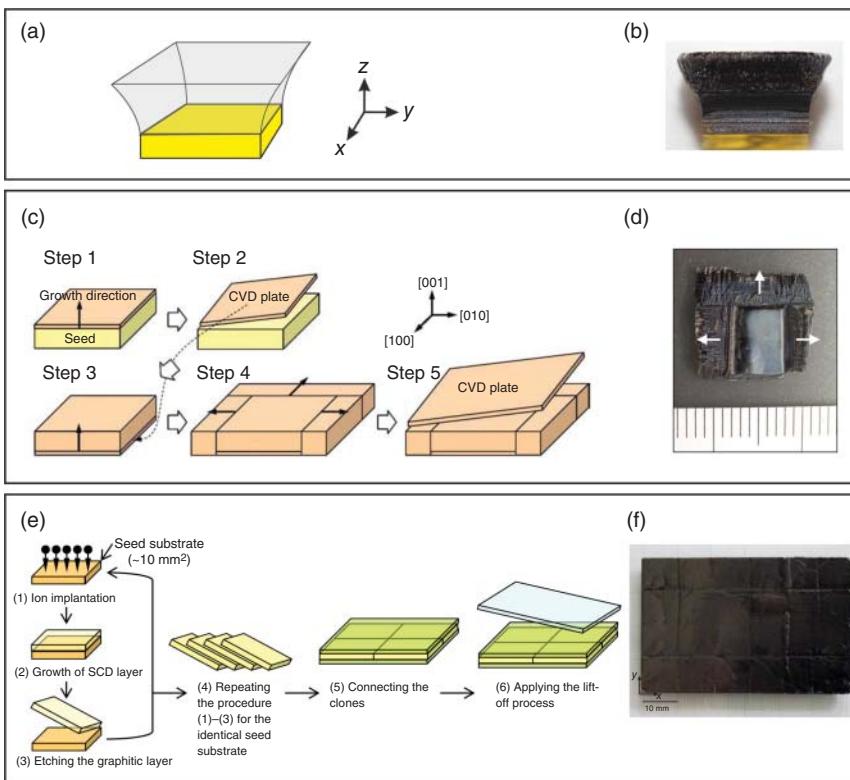
Heteroepitaxial deposition of a material on the surface of a foreign single crystal is a common approach when the synthesis of bulk crystals of the desired quality and size is not possible. Though some progress has been made during the last years, 3- or 4-in. size single crystal wafers synthesized by the HPHT technique do not appear feasible in the foreseeable future.

A viable heteroepitaxy system for diamond has to fulfill various requirements:

- a growth surface that facilitates the deposition of oriented diamond crystals, that withstands the harsh plasma environment and the required temperatures, and that finally guarantees a good adhesion
- a procedure for the generation of oriented diamond nuclei
- scalability of both, i.e., surface and nucleation procedure, to wafer size

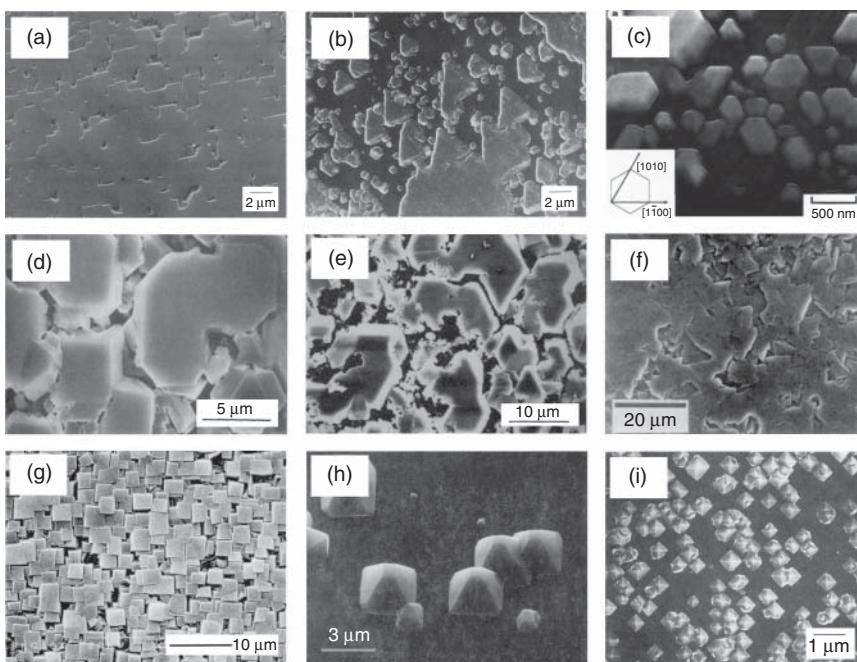
##### 20.3.5.1 Growth Substrates for Heteroepitaxy

The search for appropriate single crystal surfaces suitable for heteroepitaxial diamond growth started in the early 1990s. Figure 20.16 shows a selection of investigated substrates on which deposition of oriented diamond crystals has been achieved. The first three worked without any special treatment (a–c c-BN [90, 145] and  $\text{Al}_2\text{O}_3$  [146]). The second group required a kind of seeding (d–f Ni [147] and Pt [148]). On the final three substrates, BEN was used to obtain epitaxial nucleation (g–i Si [91], 3C-SiC [96], and Ir [102]).



**Figure 20.15** Different approaches for the lateral increase in crystal size by CVD growth. (a) Schema of lateral enlargement in xy-direction during growth in z-direction, (b) photo of a crystal with the growth surface enlarged by a factor of 2 (area of initial Ib crystal:  $13.69 \text{ mm}^2$ ), (c) schema of sequential growth steps on {100} side faces, (d) photo of enlarged crystal ( $12.6 \times 13.3 \times 3.7 \text{ mm}^3$ ), (e) concept of lift-off and cloning by ion implantation followed by overgrowth of clones, (f) photo of a 2-in. mosaic wafer produced by overgrowth of a tiled arrangement of cloned crystals. Source: (b) Reprinted with permission from Nad et al. [140]. © 2016 AIP Publishing. (c, d) Reprinted with permission from Mokuno et al. [141]. © 2009 Elsevier. (e) Reprinted with permission from Yamada et al. [142]. © 2012 Elsevier. (f) Reprinted with permission from Yamada et al. [143]. © AIP Publishing.

While major activities were focused for several years on Si (and 3C-SiC), it finally turned out that this does not offer a viable route to real single crystals for the following reasons: high nucleation densities up to  $\approx 10^{11} \text{ cm}^{-2}$  could be obtained by BEN on Si, but typically only  $10^8\text{--}10^9 \text{ cm}^{-2}$  were epitaxially aligned. The initial mosaic spread of the oriented layers was on the order of  $\Delta\omega \approx 10^\circ$  (tilt) and  $\Delta\varphi \approx 5\text{--}6^\circ$  (twist). While appropriate growth steps facilitated the formation of closed layers consisting exclusively of aligned crystals and caused a significant decrease of  $\Delta\omega$  down to few degrees, the azimuthal spread in orientation remained nearly unchanged [113]. Thus, small-angle grain boundaries persisted and prevented the transition to real single crystals. In addition, the immediate commencement of crystal growth after nucleation during BEN induced the feedback described in Figure 20.13d with all its



**Figure 20.16** Heteroepitaxial diamond growth on different substrate materials: (a) c-BN(001), (b) c-BN(111), (c)  $\text{Al}_2\text{O}_3$ (0001), (d) Ni(001), (e) Ni(111), (f) Pt(111), (g) Si(001), (h) 3C-SiC(001), (i) Ir/MgO(001). Source: Reprinted with permission from Schreck [144]. © 2009 Wiley.

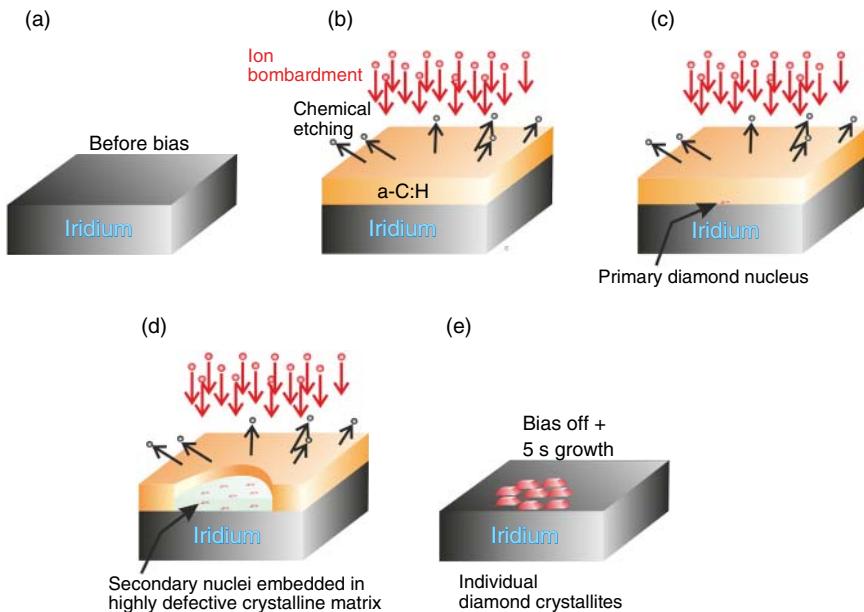
negative implications for the homogeneity. Furthermore, the harsh bombardment of the small grains caused that epitaxial orientation was only obtained within a defined process time window [149].

Iridium does not suffer from these drawbacks. The density of oriented grains shortly after BEN is up to  $3 \times 10^{11} \text{ cm}^{-2}$ , the initial mosaic spread (600 nm thick layer) is  $\Delta\omega$ ,  $\Delta\varphi \approx 1^\circ$ , and the feedback is avoided since the grains cannot grow in  $z$ -direction due to the harsh ion bombardment (see next chapter).

### 20.3.5.2 Bias-Enhanced Nucleation on Iridium: Phenomenology and Mechanism

The most intriguing observations during a successful BEN process on Ir surfaces in contrast to all the materials studied before are the minimal changes in biasing current and surface morphology. Actually, scanning electron microscopy (SEM) facilitates clear identification of regions which contain diamond nuclei only by the in-lens detector which is specifically sensitive to work function contrasts. These regions were called “domains” [150].

The standard scenario for the processes occurring during BEN is summarized in Figure 20.17. Due to the harsh ion bombardment, the initially clean Ir surface (a) is quickly covered by a closed amorphous a-C:H layer with a thickness of 1–2 nm (b). This precursor layer is permanently etched by the atomic hydrogen



**Figure 20.17** Schema describing the typical phenomenology of BEN on Ir. Source: Schreck et al. [151]. Licensed under CC BY 4.0. (a) Ir surface exposed to plasma before biasing. (b) An a-C:H layer is quickly formed after start of the BEN process. Dynamic equilibrium between deposition of hyperthermal particles and etching by atomic hydrogen limits layer thickness to a constant value of 1–2 nm. (c) Spontaneous formation of a primary diamond nucleus. (d) Lateral expansion of the domain and formation of secondary nuclei embedded in a highly defective crystalline matrix (domain), which is thinner than the surrounding a-C:H film. (e) During the first 5 s after termination of BEN, the atomic hydrogen etches completely the a-C:H precursor phase as well as the defective matrix in the domains. Simultaneously crystalline diamond grains with a height of 2 nm at a distance of 15–20 nm are formed.

leading to a dynamic equilibrium of deposition and etching. After some time, primary nuclei are spontaneously formed (c) and in their immediate neighborhood further nucleation events (secondary nuclei) occur (d). They are embedded in a highly defective crystalline matrix which is  $\approx 1$  nm thinner and denser than the surrounding precursor matrix. At this stage, the presence of carbon arranged in diamond crystal structure (i.e. the nuclei) can be detected by X-ray photo-electron diffraction (XPD) [152], by X-ray absorption near edge structure (XANES) spectroscopy [153], but not by high-resolution transmission electron microscopy (HRTEM). When the bias voltage is switched off (while the MW discharge is still on), the atomic hydrogen etches the whole a-C:H precursor layer completely within five seconds and the nuclei grow to 2-nm-high diamond grains (e) easily detectable by HRTEM [154].

The observations summarized in Figure 20.17 raise the crucial questions how nuclei are formed, why they are gathered in well-defined areas, and why growth of larger grains during BEN on Ir is prohibited in contrast to other substrate materials. The model of ion bombardment induced buried lateral growth (IBI-BLG) can

conclusively explain all the peculiarities that have been reported for BEN on Ir. The first step, i.e., the formation of the primary nucleus as indicated in Figure 20.17c, is a real nucleation event. It can be described, as recently proposed, in terms of a spontaneous precipitation of pure  $sp^3$  clusters. These events occur in the dense a-C:H matrix with few of the clusters ( $1 \text{ in } 10^4\text{--}10^6$ ) being perfect diamond [155]. The nucleation is energetically favored directly at the interface to the iridium film in accordance with the observation that virtually all the nuclei are epitaxially oriented.

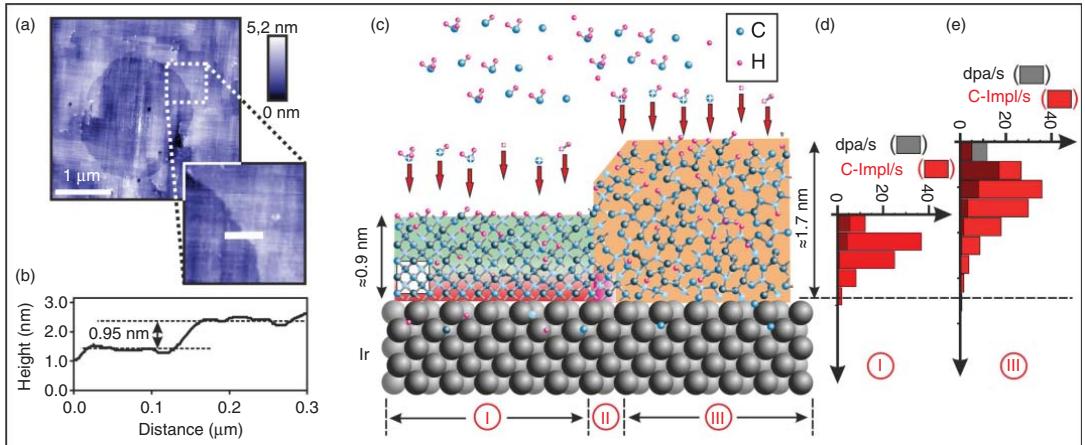
The atomic displacements and implantation of carbon atoms due to the ion bombardment does not only nucleate diamond, but it can also induce crystal growth. The basic effect of growth of tiny diamond crystals inside of carbon onions had been observed in former irradiation experiments with high-energy electrons [156] and ions [157]. Subsequent experiments revealed that this transformation is also possible for planar graphitic structures [158], and a model was developed to describe the kinetics of the involved processes quantitatively [159]. Extrapolation of this model suggests that the ion bombardment conditions during BEN on iridium facilitate an analogous growth now laterally over distances of several microns (see Figure 20.18).

Buried growth at the interface to the iridium – instead of the film surface where CVD growth usually takes place – is necessary to preserve the crystallinity and the perfect heteroepitaxial alignment. The particularly strong ion bombardment on Ir (higher bias voltages) as compared to other substrates suppresses any crystal growth perpendicular to the surface. Only very rarely, a continuous epitaxial layer is observed. Usually, a splitting into individual crystallites occurs with the consequence that >99% of the tiny grains in a micron-size domain (distance  $\approx 15\text{--}20 \text{ nm}$ ) result from secondary nuclei formed by lateral growth and splitting instead of real independent nucleation events [151].

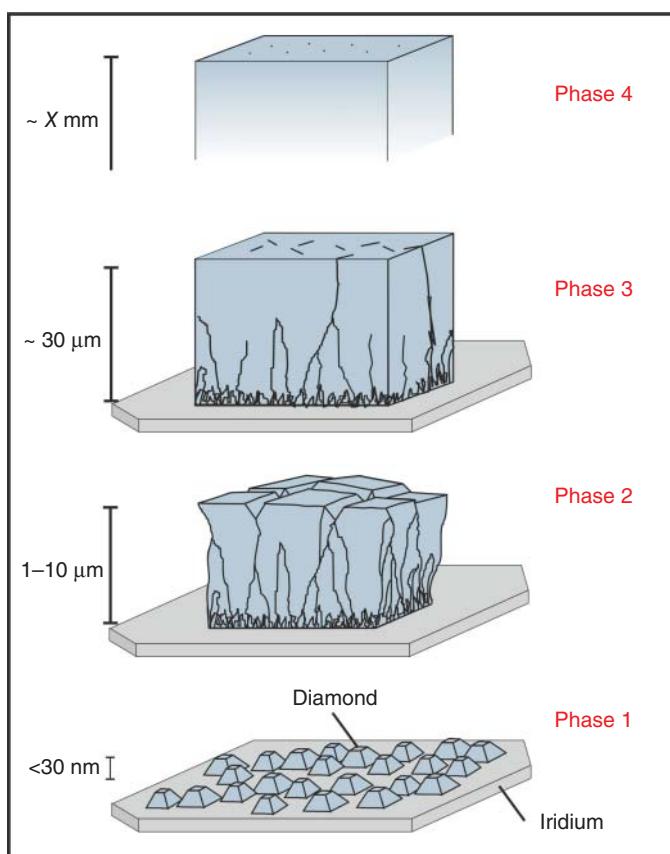
#### 20.3.5.3 Structural Improvement with Film Thickness

After nucleation, diamond films on iridium pass through different phases until they reach the stage of single crystals (Figure 20.19). The nucleation density of  $3 \times 10^{11} \text{ cm}^{-2}$  within domain regions usually guarantees that formation of a closed layer happens below a thickness of 50 nm (incomplete coverage of the surface with domains may delay this process). During the subsequent phase 2, the deposit resembles a perfect mosaic crystal, i.e., nearly dislocation-free regions are separated by a polygonized network of grain boundaries. The mosaic blocks increase in size until the network disintegrates after several  $10 \mu\text{m}$  into individual or bands of dislocations (phase 3). Afterward, growth proceeds as single crystal (phase 4). Under appropriate growth conditions, growth can continue for many millimeters continuously improving the crystal quality.

Powerful methods to monitor the improvement in structural quality of heteroepitaxial diamond layers are  $\mu$ -Raman spectroscopy with high spectral resolution, quantification of the dislocation density (by transmission electron microscopy TEM and etch pit counting), and X-ray diffraction (XRD rocking curves and azimuthal scans). Figure 20.20 summarizes the corresponding results for two  $\approx 1\text{-mm-thick}$



**Figure 20.18** Detailed description of the IBI-BLG mechanism. (a) Atomic force microscopy (AFM) image and (b) surface line profile of a sample after BEN taken around a circular domain (comparable to stage (d) in Figure 20.17). (c) The model shows the Ir crystal covered in region (III) by the a-C:H precursor layer (orange), in region (I) by the domain area with the highly damaged diamond nuclei and in region (II) by the thin boundary between both. (d, e) Results of simulations by the SRIM code (Stopping and range of ions in matter) for implanted carbon atoms and displacements per atom (dpa) in the two regions I and III. Source: Schreck et al. [151]. Licensed under CC BY 4.0.



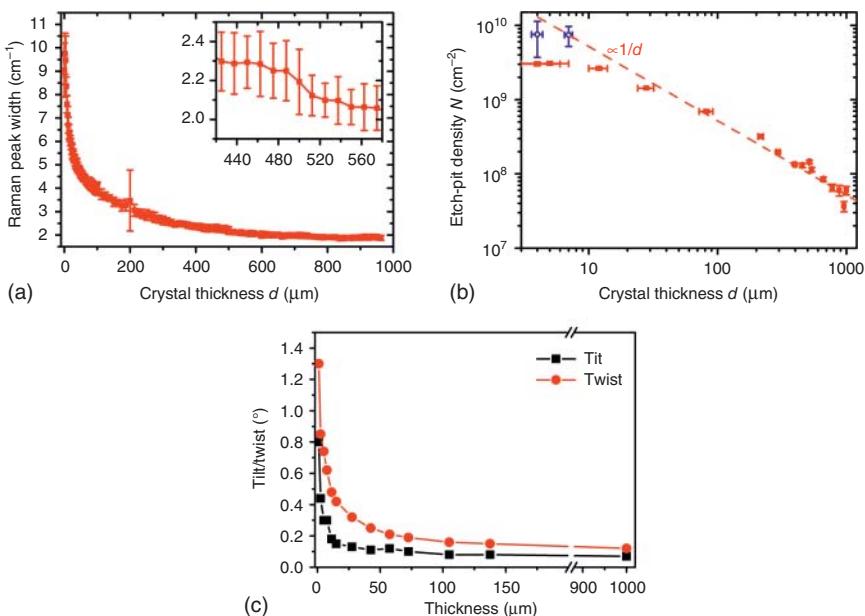
**Figure 20.19** Schema of the different stages of epitaxial diamond growth on Ir.

samples. In sample #1, the Raman line width decreased from  $>10$  to  $1.86\text{ cm}^{-1}$  and the dislocation density from  $\approx 10^{10}\text{ cm}^{-2}$  to  $\approx 5 \times 10^7\text{ cm}^{-2}$  following a  $1/d$  relationship ( $d$  = film thickness) [160]. In sample #2, full width at half maximum (FWHM) of tilt and twist decreased from  $\approx 1^\circ$  to  $\approx 0.1^\circ$ .

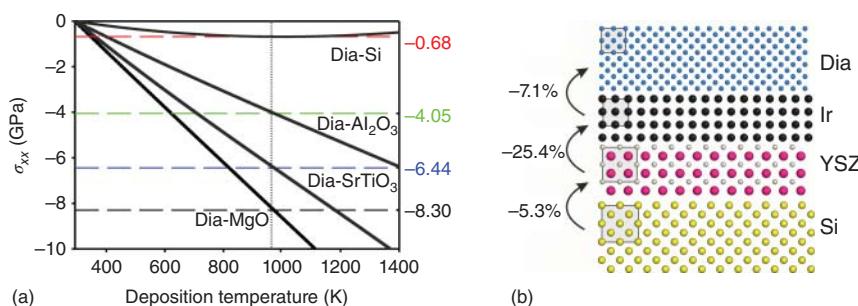
Merging of neighboring grains by disclination formation was identified as a crucial mechanism for grain coarsening and structural improvement during the initial stage of film growth (phases 2–3 in Figure 20.19) [161]. The subsequent continuous decrease in dislocation density over millimeters of film thickness is attributed to the mutual interaction between dislocations resulting in annihilation or fusion reactions [162].

#### 20.3.5.4 Multilayer Substrates for Scaling to Wafer Size

For all research experiments, thin iridium layers deposited by e-beam evaporation predominantly on oxide single crystals were used instead of bulk single crystals. These comprised  $\text{MgO}$  [102],  $\text{SrTiO}_3$  [163], and  $\text{Al}_2\text{O}_3$  [164]. Compared with diamond, oxides are characterized by high CTE values which results in high compressive stress in the diamond films grown on top. Figure 20.21 shows the



**Figure 20.20** Variation of (a) Raman line width and (b) etch pit density (EPD) with thickness for a heteroepitaxial diamond film grown on Ir/YSZ/Si(001). The off-axis angle of the Si(001) wafer was 6° toward [110]. At a thickness of  $\approx 500 \mu\text{m}$ , the initial nitrogen addition in the gas phase was reduced to zero (see step-like decrease in Raman line width in the inset). For the lowest thickness two data points (blue) of dislocation density measurements derived alternatively by TEM were added to the graph. (c) Mosaic spread of a heteroepitaxial diamond sample which was grown in a sequence of deposition steps without any nitrogen using a Si(001) substrate with an off-angle of 4°. Source: (a, b) Reprinted with permission from [160]. © 2013 AIP Publishing. (c) Graph courtesy of Dr. Martin Fischer, Augsburg Diamond Technology GmbH.



**Figure 20.21** (a) Thermal stress  $\sigma_{xx}$  in diamond layers on different substrates vs. deposition temperature (the iridium interlayer can be ignored due to its low thickness). (b) Schematic representation of the epitaxial multilayer structure Dia/Ir/YSZ/Si(001).

compressive thermal stress that develops during cool down from deposition to room temperature for various multilayer substrates. Even for moderate temperatures of 700 °C, the values are very high, e.g. –8.3 GPa for diamond on MgO (the thin iridium interlayer is neglected in these considerations). Delamination and uncontrolled crack formation are usually a consequence. In contrast, silicon shows a minor misfit and the stress even decreases for higher deposition temperature. Silicon would also be a preferred option in terms of wafer quality, size, and price.

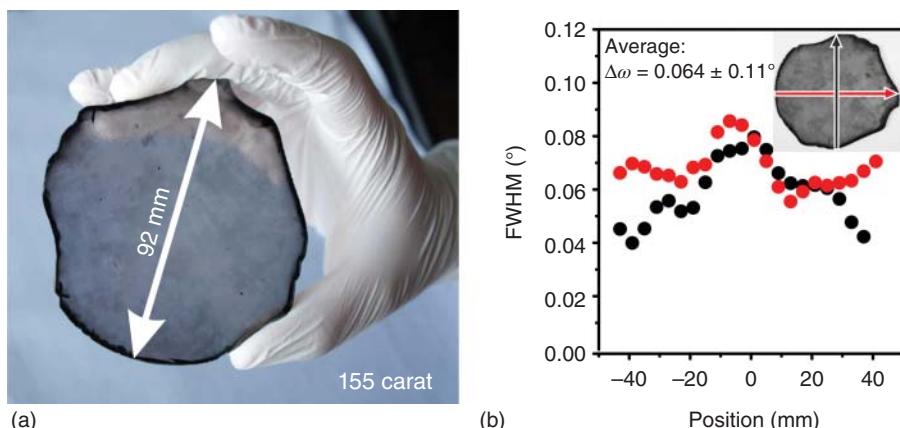
Since chemical reactivity and the formation of silicides with low melting point prevent direct growth of Ir on Si, a further inert interlayer between Ir and Si was necessary to facilitate growth of Ir on silicon wafers. Figure 20.21b shows the multilayer structure diamond/Ir/YSZ/Si(001) with YSZ = yttria stabilized zirconia [165]. Basically, YSZ of different stoichiometry resulting in tetragonal or cubic crystal structure can be chosen to grow oxide buffer layers by pulsed laser deposition (PLD) for the subsequent deposition of single crystal iridium [166]. With SrTiO<sub>3</sub> buffer layers grown by molecular beam epitaxy (MBE), the multilayer system diamond/Ir/SrTiO<sub>3</sub>/Si(001) has been established as a promising alternative [167, 168].

A peculiarity of the heteroepitaxy of iridium on oxide buffers should be highlighted: as indicated in Figure 20.21b, the lattice misfit between YSZ and Ir is huge (25.4%). Moreover, the oxide layers grown by PLD have a typical mosaic spread of  $\approx 1\text{--}2^\circ$ . Both aspects are normally considered highly counterproductive for the growth of high-quality single crystal layers. However, this general rule is void for Ir on oxide buffer layers when an appropriate two-step deposition process with an ultralow rate in the first step is applied so that iridium with a mosaic spread of  $\approx 0.1^\circ$  can be realized on oxides with a mosaic spread of 1–2°. In the crucial first step, the metal islands reorient each other mutually during coalescence so that an angular spread lower than the growth substrate can be obtained [169]. This mechanism also works for various other metals [170]. In addition, the concept can be transferred to oxide layers with even higher mosaic spread like biaxially textured MgO produced by ion beam-assisted deposition (IBAD). Since biaxially textured oxide films can virtually be deposited on every substrate including amorphous or polycrystalline solids, the approach provides an additional degree of freedom for the selection of appropriate substrates [169].

### 20.3.5.5 The State of the Art in Scaling and Mosaic Spread

Scaling of the single crystal iridium wafers to a diameter of 4 in. [171] and in the following also of the diamond layers (see Figure 20.22a) [151] was achieved in the past years.

Wafers, as shown in Figure 20.22, can routinely be grown in the meantime. The mosaic spread has been further improved to  $\Delta\omega = 0.03^\circ$  and  $\Delta\varphi = 0.05^\circ$  with minimum dislocations densities of  $7 \times 10^6 \text{ cm}^{-2}$  at a thickness of 2.2 mm [172].



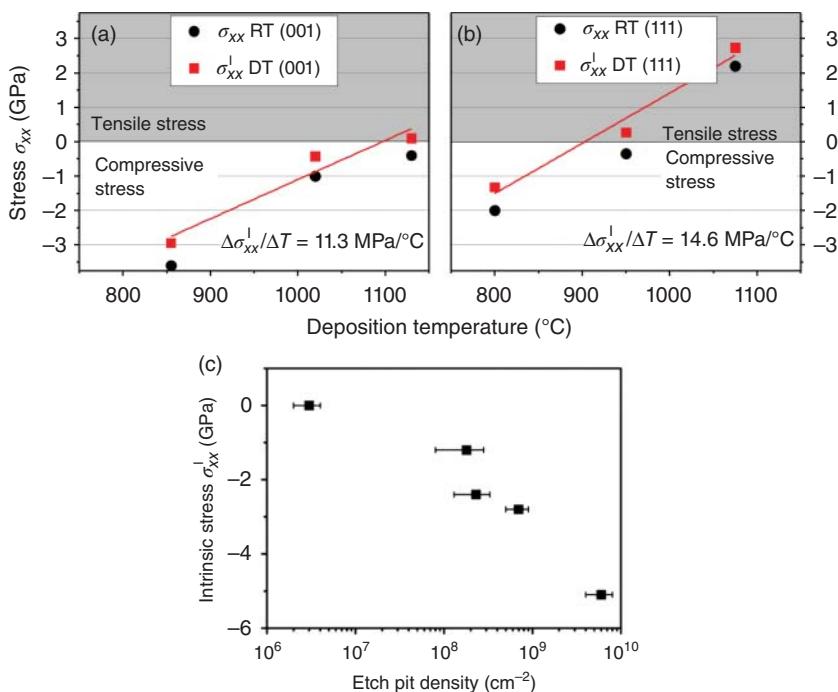
**Figure 20.22** (a) Free-standing unpolished single crystal diamond wafer with a thickness of  $1.6 \pm 0.25$  mm grown heteroepitaxially on Ir/YSZ/Si(001). (b) Width of rocking curve measured along two perpendicular lines across the wafer. The corresponding average azimuthal width (dia(311) reflection) was  $0.12 \pm 0.04^\circ$  and the Raman line width  $1.75 \pm 0.07 \text{ cm}^{-1}$ . Source: Schreck et al. [151].

#### 20.3.5.6 Intrinsic Stress and Its Correlation with Dislocations

While extrinsic stress due to differences in CTEs between substrate and layer develops at the end of the deposition process during cool down to room temperature, intrinsic (growth) stress already appears during the deposition at constant temperature. Various former homoepitaxy experiments had already revealed that intrinsic stress can be a major problem for the growth of structurally intact films. Specifically on (111) surfaces tensile stress and pronounced crack formation in homoepitaxial layers were observed [173]. During heteroepitaxial diamond growth, these problems appeared even more drastically. It was finally found that the appearance of intrinsic stress is intimately related to the presence of dislocations and “effective climb of dislocations” was identified as the relevant mechanism [174]. The pronounced temperature dependence of stress formation is different for {001} and {111} growth sectors and varies from compressive at low to tensile at high deposition temperatures (see Figure 20.23). High dislocation densities promote stress formation and drastically narrow the temperature window for the growth of crack-free layers [162].

#### 20.3.5.7 Heteroepitaxy on (111)-Oriented Substrates

The benefits of the (111)-orientation for in situ doping or for the incorporation of aligned NV centers are strong arguments for heteroepitaxial wafers with this orientation. After demonstration of the basic proof of concept [175], heteroepitaxial growth on Ir/YSZ/Si(111) has been studied in detail. It turned out that the structural improvement progresses even faster with increasing film thickness than for (001) samples. As a consequence, minimum values of  $0.08^\circ$  for the azimuthal mosaic spread,  $4 \times 10^7 \text{ cm}^{-2}$  for the dislocation density, and  $1.8 \text{ cm}^{-1}$  for the Raman line

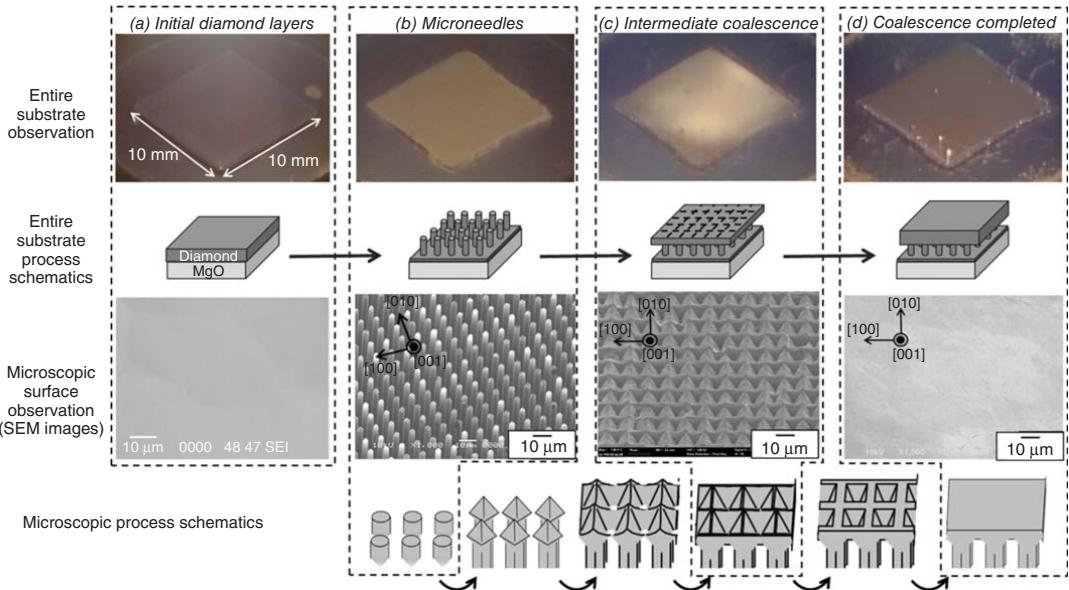


**Figure 20.23** Variation of in-plane stress with deposition temperature for growth on (a) (001)- and (b) (111)-oriented substrates [174]. The RT values were measured by XRD at room temperature. The DT values at deposition temperature, which represent the intrinsic stress, were then calculated using the corresponding CTE values. (c) Variation of intrinsic stress with dislocation density for epitaxial growth on a series of (001)-oriented substrates which contained different dislocation densities [162]. The lowest density was obtained by a short bias-assisted growth treatment on an HPHT crystal before the homoepitaxial layer was grown. All samples were grown at 850  $^{\circ}$ C, 200 mbar, with 8%  $\text{CH}_4/\text{H}_2$ , i.e., under conditions which favor the development of compressive stress. Source: (a, b) Reprinted with permission from Fischer et al. [174]. © 2012 AIP Publishing. (c) Reprinted with permission from Schreck et al. [162]. © 2016 Wiley-VCH.

width have been obtained at comparatively low thickness [176]. All types of twins could be avoided by the use of off-axis substrates. However, growth rates were limited to  $\approx 1 \mu\text{m/h}$  so that layers up to 330  $\mu\text{m}$  in thickness required technologically unacceptable process times. One reason are the complex stress formation processes [177, 178] that drastically narrow the parameter window of useful deposition temperatures.

#### 20.3.5.8 The Microneedle Approach

To cope with the thermal incompatibility of diamond on Ir/oxide substrates, Japanese groups developed the microneedle approach [179–181] (see Figure 20.24). It comprises first the standard procedures for heteroepitaxial growth of diamond on Ir/MgO substrates followed by patterning of the thin diamond film to form microneedles which are finally overgrown with a thick bulk layer. This bulk



**Figure 20.24** Sequence of process steps of the microneedle concept. (a) Thin heteroepitaxial diamond on Ir/MgO(001). (b) Formation of diamond microneedles via Ni masks using the thermochemical reaction of diamond with Ni in a high temperature hydrogen environment. (c, d) Two different stages of overgrowth of the needle structure with final formation of a closed bulk diamond layer after removal of the Ni. Source: Reprinted with permission from Aida et al. [180]. © 2017 Elsevier.

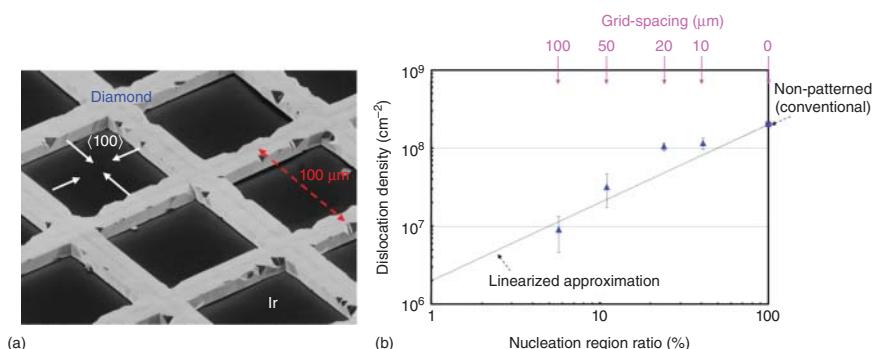
diamond layer splits off due to the thermal stress and bending of the whole multilayer structure during cool down from deposition temperature. The microneedle layer forms the weak link that initiates a well-defined separation. Up to 2-in. diamond wafers manufactured with this technique have recently been reported [182].

### 20.3.6 Advanced Concepts for Structural Improvement

The observation of the dislocation density decreasing inversely to the thickness  $d$  means that every additional order of magnitude in defect reduction requires an identical increase in thickness provided the correlation continues to be valid. Thus, refined approaches are necessary instead of simply growing thicker layers.

#### 20.3.6.1 Epitaxial Lateral Overgrowth

ELO is a common technique for dislocation density reduction, e.g. in group-III nitride layers [183]. Several attempts have also been made in the field of diamond heteroepitaxy either by patterning directly the BEN layer [184, 185] or by the use of gold masks [186]. A very detailed study with a systematic variation of the grid spacing and fill factor (FF) has been published recently (see Figure 20.25). In this work, first BEN was performed on Ir/MgO(001) substrates. The thin carbon layer containing the nuclei was then covered by a photoresist which was patterned by photolithography. In the next step, the pattern with a defined grid spacing was transferred to the nucleation layer by Ar ion bombardment. Outside the 3- $\mu\text{m}$ -wide lines, all the nuclei were destroyed. After removal of the photoresist, the pattern was overgrown (partial overgrowth is shown in Figure 20.25a) until a closed diamond layer was formed. At 60- $\mu\text{m}$  thickness, etch pits were generated, and the dislocation density was derived. As shown in Figure 20.25b, the patterned overgrowth with various grid spacings reduced the dislocation density from  $2 \times 10^8 \text{ cm}^{-2}$  for standard growth without patterning to a surface averaged value of  $9 \times 10^6 \text{ cm}^{-2}$  (locally  $5 \times 10^6 \text{ cm}^{-2}$ ) for the 100- $\mu\text{m}$  spacing. At the same time, the FWHM values for tilt



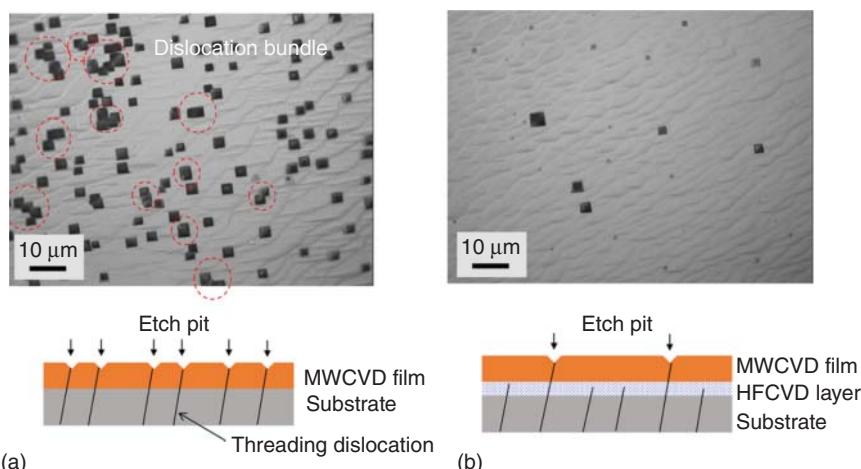
**Figure 20.25** (a) Heteroepitaxial diamond layer after 2-hour growth (partial overgrowth) on an Ir/MgO(001) sample patterned with 100- $\mu\text{m}$  grid spacing after BEN. (b) Average dislocation density after complete overgrowth vs. the ratio of the nucleation region in which the diamond nuclei were not destroyed by the patterning procedure. Source: Reprinted with permission from Ichikawa et al. [187]. © 2019 Elsevier.

and twist decreased from  $0.17^\circ$  and  $0.51^\circ$  (value measured at  $60\text{-}\mu\text{m}$  thickness) to  $0.064^\circ$  and  $0.043^\circ$  (at  $100\text{-}\mu\text{m}$  thickness), respectively.

The ELO technique described before is based on the destruction of diamond nuclei. Classically, a mask material is used as a stopping layer like for the liftoff concept with  $\text{SiO}_2$  masks described in Chapter 20.3.4.2 or the gold masks in [186]. Besides this, the microneedle approach in Chapter 20.3.5.8 or the lateral growth over a macroscopic hole as reported by Tallaire et al. [188] represent a kind of air-bridged [189] or maskless [190] ELO. Both are known from GaN growth. Bridging the gap between neighboring needles or the macroscopic hole by lateral growth without generation of new dislocations can reduce the local dislocation density in the former gap regions and the average value after film closure. Actually, growth over the macroscopic hole manufactured in a Ib substrate (with a typical dislocation density of  $10^4\text{--}10^6 \text{ cm}^{-2}$ ) resulted in a local value of  $2 \times 10^3 \text{ cm}^{-2}$  [188].

### 20.3.6.2 Dislocation Stopping by W or Ta Atoms

A novel approach for a very efficient reduction in dislocation density has recently been reported. It is based on the metal-assisted termination (MAT) of dislocations by W or Ta atoms which are incorporated into the diamond crystal during a short hot filament growth step with high filament temperature  $>2400\text{ K}$  [191, 192]. Typical W concentrations are  $\approx 10$  ppm. Afterward, growth is continued metal free by MWPCVD. On single crystal substrates, incorporation of W atoms reduced the dislocation density from  $2 \times 10^6 \text{ cm}^{-2}$  to  $3 \times 10^4 \text{ cm}^{-2}$  (Figure 20.26) and also on heteroepitaxial substrates impressive improvements in crystal quality have been obtained. In both cases, the structural changes also translated into improved device characteristics of Schottky barrier diodes fabricated with these substrates.



**Figure 20.26** Etch pits generated to reveal densities of threading dislocations for MWPCVD layers grown (a) without and (b) with a few-micron-thick HFCVD interlayer on single crystal substrates with initial dislocation densities of  $\approx 2 \times 10^6 \text{ cm}^{-2}$ .  
Source: Reprinted with permission from Ohmagari et al. [191]. © 2018 AIP Publishing.

## 20.4 State of the Art and Outlook

During the last few years, appreciable progress has been achieved in the field of HPHT as well as CVD growth. Most prominent is the increase in single crystal size of HPHT crystals making available  $15 \times 15 \text{ mm}^2$  single crystal plates and the 92-mm-wafer grown by CVD on the heteroepitaxy substrate Ir/YSZ/Si. HPHT crystals free of dislocations in limited regions have been shown. These would provide the ideal substrates for exploring the limits of diamond-based electronic devices. Systematically increasing the size of low dislocation density seeds is one approach toward electronic-grade wafer material. On the other hand, the heteroepitaxy concepts profit from the simultaneous nucleation over a large area. The coalescence of  $\approx 2 \times 10^{13}$  nuclei that are typically formed during BEN on a 4-in. diameter wafer surface results in initial dislocation densities  $> 10^{10} \text{ cm}^{-2}$ . By simple growth of several millimeter thick crystals or by ELO, this value can be reduced to  $< 10^7 \text{ cm}^{-2}$ . Future work has to show whether the different ELO concepts have the potential for significant further improvement. The intriguing novel MAT approach provides a simple and very efficient method to reduce dislocation densities. Exploring its potential, limits, and the underlying mechanisms deserve increased interest of the scientific community.

In conclusion, the progress in crystal growth is increasingly removing one former bottleneck in the development of diamond electronics by establishing a base for the supply of wafer-size high-quality substrates to manufacture competitive electronic devices.

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## 21

# Diamond Wafer Technology, Epitaxial Growth, and Device Processing

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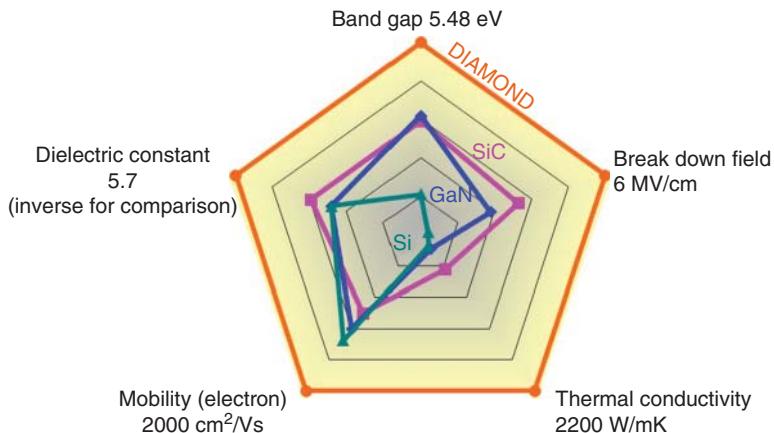
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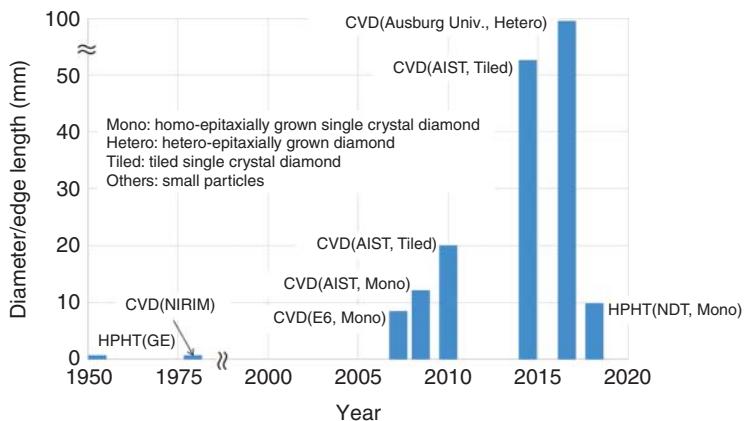
## 21.1 Diamond Epitaxial Growth and Wafers

Several material constants of diamond are superior to those of other materials [1–3]. Owing to its high reflectivity and variety of light absorption characteristics, which are attributed to the many types of color centers, diamond is one of the most famous gemstones. Diamond has also been commercialized in industry in mechanical tools and heat spreaders [4]. In addition, the electrical and thermal characteristics of diamond are superior to those of other materials, as summarized in Figure 21.1 [1]. These characteristics are considered attractive for realization of high-performance power devices.

Although most commercialized diamond is obtained by mining, recently, some artificial diamond has been commercialized [4–11]. The production of artificial diamond using the high-pressure high-temperature (HPHT) method was first reported in the 1950s [5]. Since then, this method has been adopted worldwide to produce mechanical tools, heat spreaders, and dies in industry. In this method, diamond crystals are grown in its stable phase in a finite region inside the apparatus [12]. This method produces bulk crystal with the highest crystal quality, meaning the lowest dislocation density and lowest impurity content [13]. Currently, diamond substrates produced using the HPHT method, with edge lengths that are typically 2–3 and 10 mm at most, are available for use in experiments in electronics and spintronics. Recently, a diamond “block” with an almost 1-in. diameter was reported by a Russian company; however, its internal features were unclear [14]. Using this method, it is extremely difficult to realize a several-inch-size wafer because of practical difficulties. Chemical vapor deposition (CVD) is another technique used to grow diamond crystal artificially [15]. Artificial diamond grown using microwave (MW) plasma CVD was first reported as CVD-grown diamond in the 1980s [15]. Since then, several CVD methods have been used to grow diamond, including



**Figure 21.1** Electrical and thermal characteristics of diamond and other semiconductor materials. Source: Koizumi et al. [1]. © 2008, John Wiley & Sons.



**Figure 21.2** Progress made in the development of artificial diamond. Source: Element six [6]; Light Box Jewelry Inc [10]; Haruta et al. [17]; Ohtake and Yoshikawa [18]; Matsui et al. [19]; SP3 diamond technologies [20]; Ohmagari et al. [21] and Mokuno et al. [22]. GE, NIRIM, E6, AIST, and NDT represent General Electric Company in the US, the National Institute for Research in Inorganic Materials in Japan, Element Six in the UK, National Institute of Advanced Industrial Science and Technology in Japan, and New Diamond Technology in Russia, respectively.

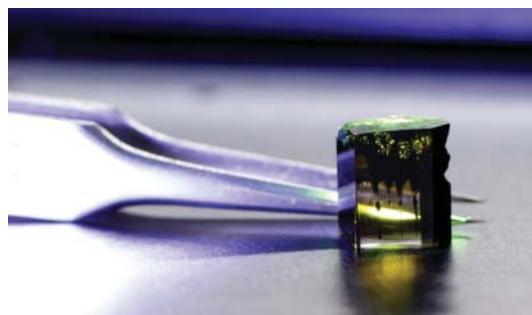
(pulse-) direct current (DC) plasma, inductively coupled plasma (ICP), plasma-jet, flame, and hot-filament (HF) CVD [16–21]. In these methods, the vapor phase for the crystal growth is filled with the source gas mixture, which typically consists of hydrogen and methane. Then, this source gas mixture is dissociated into radicals; this process is promoted by plasma or highly heated filaments. These radicals react, and diamond crystals grow on the substrate. Figure 21.2 summarizes the progress made in the sizes of reported and commercialized artificial diamond.

As described above, the HPHT method can be used to synthesize crystals with the highest quality because the growth mode, in which the crystal grows three

dimensionally, is well established [13]. Because the dislocations extend from the seed crystal almost vertically to the top surface of the seed substrate, one may extract crystal from extended regions where dislocations are suppressed. This high-quality region is then re-used as the seed crystal to obtain a reduced dislocation density. However, such a three-dimensional growth mode is not well established for CVD [22–24]. An HPHT-made single-crystal diamond is typically adopted as the seed substrate for CVD growth. Therefore, the size and quality of CVD-made diamond is limited by the characteristics of the HPHT-made diamond, which is one of the major issues for the preparation of wafers with large area and sufficient quality. This issue must be solved for realization of industrial use, especially for electronics.

To increase the size of the seed substrate, one may attempt to repeat the growth on several {001} surfaces [25]. Using a substrate with 7–8-mm edge lengths, a half-inch-size substrate was demonstrated. However, it is not easy to grow diamond with thicknesses larger than several millimeters [22, 25, 26] because of the generation of undesired miscellaneous crystals and the thermally non-equilibrium environment of the growth [26–29]. In addition to the growth on the substrate, undesired miscellaneous crystals grow on the holder as well as the edges of the substrate. Such miscellaneous crystals act as antennas, leading to undesired concentration of the plasma for plasma CVD; therefore, the growth may need to be stopped to prevent drifting of the growth condition before the generation of these undesired miscellaneous crystals. To prepare a millimeter-thick crystal, one may thus repeat the growth with thicknesses of 0.1 mm or less [30]. The introduction of oxygen has been shown to reduce the appearance of these miscellaneous crystals [31]. Although the growth rate is also reduced in this case, the total growth thickness for a batch is increased. The thermally non-equilibrium environment is attributed to the locally concentrated plasma distribution with high temperature (approximately 3000 K) [27–29]. The hottest region is approximately 10 mm above the top substrate, where the temperature is maintained at approximately 1000–1300 K. Therefore, a steep temperature gradient of several 1000 K exists around the substrate, which may induce the generation of large internal stress inside the substrate. The use of pulse-mode discharge has been shown to reduce the gas temperature to some extent [32]. Optimization of the substrate holder shape is also effective for reducing the temperature gradation inside the substrate. These techniques enable several-millimeter-thick bulk crystal to be obtained, as shown in Figure 21.3.

**Figure 21.3** Example of bulk crystal with 10-mm thickness grown on  $10\text{ mm}^2$  square seed substrate using microwave plasma CVD.





**Figure 21.4** Tiled clone with 20-mm edge, where four single-crystal diamond substrates with 10-mm edges were connected with each other.

Other approaches to obtain a diamond substrate with large area are tiling and hetero-epitaxial growth [33–36]. The concept of tiling was proposed in the 1990s for diamond; however, it is difficult to obtain a smooth boundary without cracking and/or non-epitaxial components [37]. It was observed that freestanding substrates made from identical seed substrate could be connected with each other smoothly [38]. In this case, although dislocations and stressed regions are still present near the boundaries, the boundaries could be made very smoothly, and such so-called “tiled-clones” could also be used for the seed substrate to obtain wafers with the same area and even to connect them to enlarge the area. Figure 21.4 shows an example of a tiled clone, where four single-crystalline diamond substrates with 10-mm edges were connected.

Another approach is to use hetero-epitaxial diamond. In this case, diamond is grown on another material, such as yttrium-stabilized zirconia (YSZ) or iridium [35]. Bias-enhanced nucleation (BEN) is used to promote nucleation before the growth. The dislocation density is therefore higher than that of homo-epitaxial single-crystalline diamond. This value can be reduced if a diamond layer of several 100  $\mu\text{m}$  is grown [39].

Several attempts to improve the crystal quality of CVD-made diamond have been made [40–42]. Dislocations, which are present in the seed crystal, extend into the CVD-grown layers grown on the seed. The direction of the dislocations can be controlled by the off-angle of the top surface of the substrate [40]. However, the direction is limited to almost the same angle with the off-angle, and therefore, it is almost impossible to eliminate the dislocations. Lateral growth is a promising method to avoid the extension of the dislocations [41]. One may fabricate a specific structure to promote the lateral growth in a limited area on the top surface of the substrate. Furthermore, metal nanoparticles can be placed just above the locations of dislocations [42]. In these two cases, the regions just above the structure and nanoparticles can act as the origins of the dislocations. Another option to improve the crystal quality is growth into several {001} surfaces [25, 43].

For CVD, oxygen and nitrogen are sometimes introduced into the source gas mixture in addition to hydrogen and methane [18, 38, 43–48]. In the beginning of the study of the CVD growth of diamond, the “Bachmann diagram” was proposed,

where the fractions of hydrogen, methane, and oxygen are indicated for diamond growth [46]. Oxygen is known to have the effects of etching and improvement of the crystal quality [18, 45]. Therefore, this gas is sometimes adopted for pre-processing of the growth and even introduced during the growth [49]. Nitrogen is known to enhance the growth rate and promote preferential growth in  $\langle 001 \rangle$  directions [38, 47, 48]. Frequently, substrates with  $\{001\}$  surfaces are adopted to grow diamond crystals because twin crystals are easily generated on  $\{111\}$  surfaces and the growth rate of  $\{111\}$  is usually lower than that of  $\{001\}$  surfaces. Therefore, especially to obtain bulk crystals using CVD, a small amount, on the order of ppm, of nitrogen is introduced. Nitrogen generates deep-level impurities ( $\approx 1.7$  eV), which makes the crystal semi-insulating. Other impurities, such as boron and phosphine are also introduced to yield p- and n-type conductivity, whose impurity levels are 0.37 eV above the valence band maximum and 0.57 eV below the conduction band minimum, respectively [50–52]. Increasing these impurities is known to reduce the resistivity and generate soot inside the vacuum vessel for microwave plasma CVD [50]. Recently, HFCVD has been used to grow single-crystal diamond films with high-density boron without soot formation; however, metals of the wire were also incorporated. In addition to the low resistivity, some effects that reduce killer defects have been observed with the use of HFCVD [51]. For HPHT, carbon sources are supplied throughout catalytic metals, such as Ni, onto a seed crystal, because of the temperature gradient inside the apparatus, where an environment for achieving a diamond stable phase is realized. Therefore, catalytic metals can be incorporated into the crystals.

The growth mechanism of CVD diamond crystals has been studied from the viewpoint of gas phase analyses as well as surface reactions [53, 54].  $\text{CH}_3$  is considered one of the most important precursors that directly contributes to the crystal growth [53–56]. The models proposed in these preceding works suggest that the growth rate is proportional to the concentration of  $\text{CH}_3$  near the top surface of the substrate. Some agreement with experimentally obtained growth rates was observed; however, the agreement was limited to the central region of the substrate [57]. Usually, the growth rate has a convex profile in the horizontal direction in experiments [57, 58]. However, the distribution of  $\text{CH}_3$  near the top surface of the substrate has concave profiles [18, 27, 29]. To understand this gap between theoretical predictions and experimental results in terms of the distribution of the growth rate, the contributions from other radicals with large numbers of lone pair electrons and the non-uniformity of the substrate temperature may need to be considered [29, 57]. Understanding of the fundamental reaction processes of the impurities mentioned above in addition to those of hydrocarbon radicals require rather extensive work [53, 54].

Once a diamond crystal is obtained, further processing may be required, for example, to prepare freestanding wafers and/or a specific structure. One promising processing technique is laser irradiation. A pulsed laser with nano-second frequency is utilized, in which the transformation from the diamond structure into graphite is realized by local absorption of the incident laser and its thermal activation [59]. Use of a pico- and femto-second pulsed laser is considered to result in a gentler cutting process because its transformation mechanism is based on electronic excitation

[60, 61]. Using this method, one may be able to separate the CVD-grown layers from the seed substrate. However, because of the incident angle and finite diameter of the beam waist, the separation process from the substrate with larger size requires larger kerf loss. It is also possible to separate the CVD-grown layers by preparing patterned notches between the substrate and CVD layers before the growth [36, 62]. Use of high-speed ion implantation is another option to prepare freestanding wafers [25, 63]. This method can be applied for inch-size wafers [33, 38]. In addition to cutting and slicing, polishing is also necessary; diamond is one of the hardest and most fragile materials. One of the most conventional polishing techniques is scaif polishing [64–67]. This mechanical polishing process, in which iron plates with diamond particles are used as polishing plates, is known to damage the surfaces.  $\text{SiO}_2$  plates are also adopted as polishing plates, and the redox reaction is expected to contribute to polishing of the surface [68]. Chemical reactions, ultra violet (UV) light, and plasma are also known to promote polishing of diamond surfaces [69–71]. Atomically flat surfaces have been achieved using photon–phonon etching [72]. A method to process the as-grown surface into such a super fine structure within a realistic time for inch-size substrates remains to be established.

The current state of the art of diamond epitaxial-growth and wafers has been summarized. In this decade, substrates with several millimeters in edge length and even inch-size substrates have become commercially available. To realize this achievement, techniques to prepare bulk crystals, including both growth techniques and processing techniques, have been developed. Many works studying the internal plasma chemical reactions both numerically and experimentally have elucidated part of the mechanism of the crystal growth. However, the fundamental concepts of growth apparatuses that are currently commercially available were proposed more than 10 years ago. A detailed understanding of the growth mechanisms may result in further development to help overcome the current status. This apparatus development would also enable the preparation of seed substrates of larger size and sufficient quality.

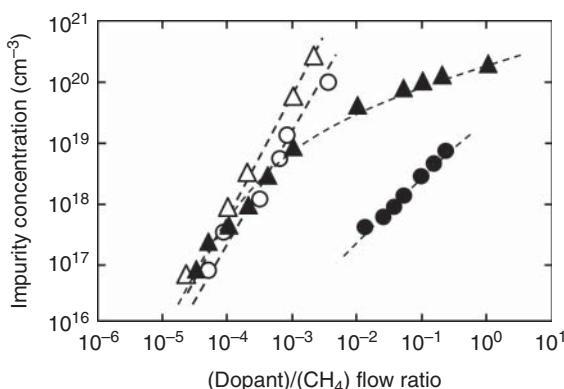
## 21.2 n-Type Doping and Processing

n-Type conductivity control by impurity doping has been one of the great challenges for CVD diamond, which tends to be an essentially p-type semiconductor, such as the natural gemstone “Blue Diamond.” The introduction of n-type conductivity is theoretically possible by doping with group V impurities as well as silicon, whereas the incorporation of impurity atoms into substitutional sites of the diamond lattice is limited because of the toughness and dense covalent bond length of carbons. Nitrogen is one potential candidate owing to its similar covalent bond length ( $0.77\text{ \AA}$ ) to diamond ( $0.74\text{ \AA}$ ). However, the donor level of substitutional nitrogen is extremely deep at  $\sim 1.7\text{ eV}$ , below the bottom of the conduction band minimum, because of its structural distortion from the substitutional site. Therefore, improvement of the electrical conductivity at room temperature cannot be expected with nitrogen doping. However, the covalent bond length of phosphorus is approximately

1.1 Å, which is approximately 1.5 times larger than that of carbon. Phosphorus can be experimentally incorporated into the substitutional sites of the diamond lattice and forms a donor level at  $\sim 0.57$  eV, which is currently the shallowest donor level in diamond semiconductors.

Phosphorus-doped diamond films have been homo-epitaxially grown by plasma-enhanced chemical vapor deposition (PECVD) using microwaves of 2.45 GHz [73, 74]. The source gas used is a mixture of pure hydrogen and methane, and n-type doping is achieved by introducing a phosphorus-based gas into the gas mixture. Phosphine, PH<sub>3</sub>, used in general semiconductor processes is mainly used as a phosphorus dopant; phosphorus doping can also be achieved using an organic phosphorus-based gas, e.g. trimethyl-phosphine or tertiary-butyl-phosphine [75]. Typical gas flow rates of CH<sub>4</sub>/H<sub>2</sub> are approximately 0.05–1%, and the ratio of PH<sub>3</sub>/CH<sub>4</sub> varies from 1 ppm to 50% to cover wider phosphorus doping levels from 10<sup>15</sup> to 10<sup>20</sup> cm<sup>-3</sup>. The total gas flow, substrate temperature, pressure, and microwave power are 1000 sccm,  $\sim 900$  °C, 150 Torr, and 3600 W, respectively. Figure 21.5 shows typical process windows for phosphorus and boron doping of CVD diamond. For boron doping, the concentrations given by the open circles and triangles monotonically increase with increasing B<sub>2</sub>H<sub>5</sub>/CH<sub>4</sub> gas flow ratio during CVD growth without any restriction of (001) and (111) crystal orientations. For (111) phosphorus doping, marked by closed triangles, a similar tendency is observed in the low-concentration region; however, saturation starts in the region with concentrations exceeding 10<sup>19</sup> cm<sup>-3</sup>. For the (001) phosphorus doping, indicated by closed circles, the incorporation itself is extremely difficult compared with that for (111) doping, and the incorporation efficiency is two orders of magnitude lower than that for (111) phosphorus doping. This strong orientational dependence and the saturation tendency in the heavily doped region are typical for phosphorus doping and are caused by the steric barrier resulting from the large difference in the covalent bond length between phosphorus and carbon atoms. According to first-principles calculation, the formation energy of phosphorus atoms on the diamond surface is much lower than that in the bulk, indicating that phosphorus tends to segregate on the diamond surface during growth. This trend is stronger for phosphorus than for boron and stronger on (001)-oriented surfaces than on (111)-oriented surfaces [76].

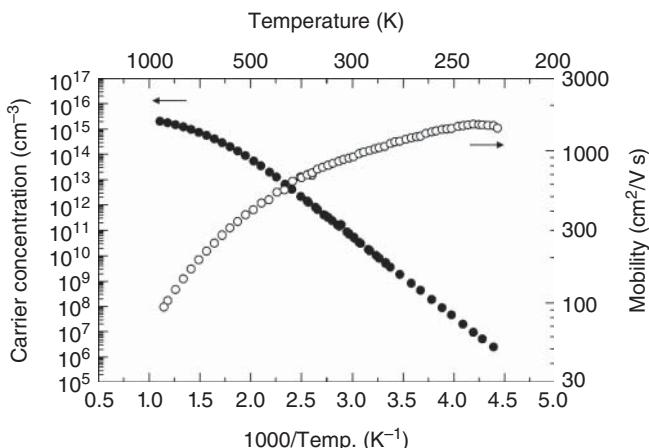
Conductivity control by impurity doping is a fundamental component of the device fabrication process. From the viewpoint of the device active layer, higher carrier mobility achieved through light doping is preferable, whereas heavy doping is preferable for lower resistance including ohmic contact. In a general compensated semiconductor, the p-type or n-type character is determined by the relationship between the donor and acceptor densities ( $N_D$  and  $N_A$ , respectively) in the semiconductor.  $N_D > N_A$  indicates n-type conductivity, and vice versa. Therefore, suppression of  $N_A$  is essential for light n-type doping as well as  $N_D$  control.  $N_A$  is the density of electron capture states, including boron acceptors, vacancy defects, and their complexes. To realize light n-type control, a metal CVD reactor compatible with ultra-high vacuum equipped with a load-lock system was developed to suppress the unintentional incorporation of other impurities. The plasma condition was modified for efficient dissociation of source gas mixtures



**Figure 21.5** Typical process windows for phosphorus and boron doping of CVD diamond. The open and closed markers are data for boron and phosphorus doping, respectively. The circles and triangles represent (001) and (111) crystal orientations, respectively.

and radical generation for growth precursor. The off angle and direction of the initial substrate were also optimized to enhance the step-flow growth. These comprehensive parameter controls have enabled stable n-type doping even for lower phosphorus concentrations down to  $10^{15} \text{ cm}^{-3}$  [52].

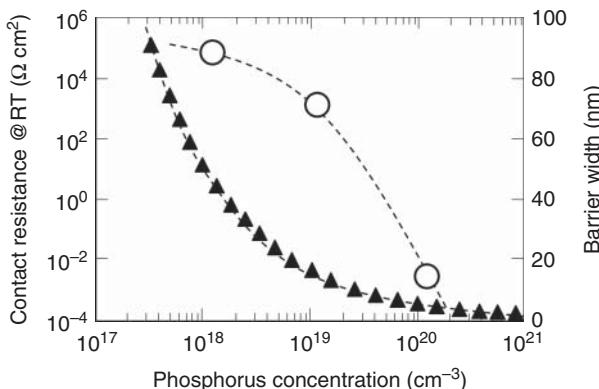
Figure 21.6 shows the typical temperature dependence of the carrier concentration and mobility for a lightly n-type diamond film with phosphorus concentration of  $3 \times 10^{15} \text{ cm}^{-3}$ . A negative Hall coefficient was measured in the entire temperature range, indicating thermally activated band conduction due to donor electrons. Through least-squares fitting using the theoretical formula accounting for carrier compensation, a donor level of  $\sim 0.57 \text{ eV}$  due to the substitutional phosphorus was clearly achieved with  $N_D$  of approximately  $3 \times 10^{15} \text{ cm}^{-3}$ , which is almost equal to the phosphorus concentration estimated by secondary ion mass spectrometry (SIMS). Most of the phosphorus atoms were incorporated into diamond substitutional sites and acted as donors. The electron mobility depends on the measurement temperature with a combination of electron scattering mechanisms, including those



**Figure 21.6** Typical temperature dependence of carrier concentration and mobility for lightly n-type diamond film with phosphorus concentration of  $3 \times 10^{15} \text{ cm}^{-3}$ .

of acoustic phonons, valley phonons, ionized impurities, and neutral impurities [77]. For a phosphorus concentration of approximately  $10^{18} \text{ cm}^{-3}$ , electron scattering due to ionization and/or neutral impurities is dominant, whereas for light phosphorus doping of approximately  $10^{15} \text{ cm}^{-3}$ , the effect of these impurities is suppressed and acoustic phonon scattering is dominant. As observed in Figure 21.6, the electron mobility monotonically increases with decreasing measurement temperature with a  $T^{-3/2}$  relationship, with the highest electron mobilities recorded at room temperature and 220 K of 1060 and  $1500 \text{ cm}^2/(\text{V s})$ , respectively.

Heavy phosphorus doping is also important for device fabrication processes. Because of its deep dopant level of approximately 0.57 eV, only a low free-carrier concentration of approximately  $10^9\text{--}10^{11} \text{ cm}^{-3}$  is thermally generated from the dopants at room temperature, resulting in a high specific resistance of approximately  $10^6 \Omega \text{ cm}$ . For a deep dopant such as diamond, when the doping concentration increases, the carrier transport mechanism changes from band conduction to hopping conduction through dense donor states, and this hopping conduction can easily result in lower resistivity. The specific resistance at room temperature becomes lower than  $10^2 \Omega \text{ cm}$  through nearest-neighborhood-hopping conduction when the phosphorus concentration exceeds  $10^{20} \text{ cm}^{-3}$ . In addition, another issue for n-type diamond is that ideal Ohmic contact has not yet been realized because of a deep pinning level around  $E_C\text{-}4.3 \text{ eV}$  at the phosphorus-doped diamond/metal interface [78]. A realistic solution is to improve the injection efficiency by narrowing the barrier width through heavy doping [79]. Figure 21.7 shows changes of the barrier width of a semiconductor/metal interface and the contact resistance as a function of phosphorus concentration. The barrier width was calculated from the space-charge-layer width assuming a Schottky barrier height of 4.3 eV. The contact resistance was estimated using the transfer-length method based on circular-type transfer length method (TLM) pattern electrodes. With increasing phosphorus concentration, the barrier width drastically decreases down to the order of a few nanometers, and the contact resistance decreases accordingly by orders of



**Figure 21.7** Changes of the barrier width of semiconductor/metal interface and the contact resistance as a function of phosphorus concentration. The open circles and closed triangles represent data for contact resistance and barrier width, respectively.

magnitude. The barrier width would be narrow enough for tunneling through the barrier to occur with heavy phosphorus doping.

The control of n-type conduction is an important subject for diamond semiconductors. Although issues remain to be solved, such as lower resistance and ideal ohmic contact, n-type control has finally been realized through phosphorus doping using microwave plasma CVD. This technical innovation based on n-type doping has led to the development of diamond electronic devices, such as high-blocking-voltage PIN diodes [80, 81], inversion channel metal oxide semiconductor field-effect transistors (MOSFETs) [82], and quantum applications based on nitrogen-vacancy complexes [83, 84].

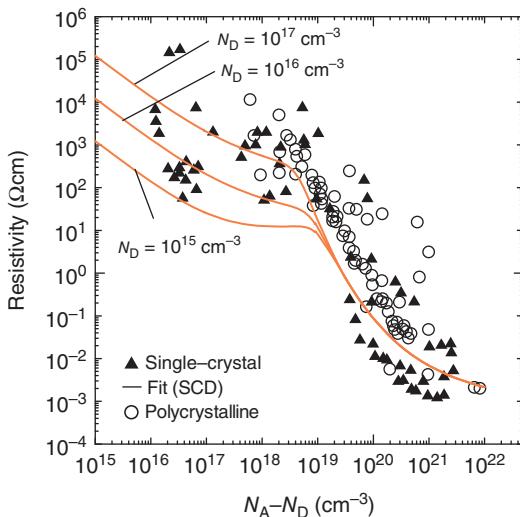
### 21.3 p-Type Doping and Processing

Boron (B) is the most reliable and widely used element for controlling p-type conduction in diamond. Substitutionally incorporating B atoms into the diamond lattice produces the shallowest known acceptor level of 0.37 eV above the valence-band maximum. As compared with other semiconducting materials (e.g. Si, SiC, GaN, and  $\text{Ga}_2\text{O}_3$ ), the activation energy is rather high, limiting the hole ionization at room temperature: the carrier concentration is limited to  $\sim 1\%$  of the doping concentration. Full ionization of B for a lightly doped epilayer can be realized above 450 K [85]. High-temperature operation is one effective solution to exploit the full potential of diamond electronics. Superior device performance at elevated temperature has been demonstrated for Schottky barrier diodes (SBDs) [86] and metal–semiconductor field-effect transistors [87].

To control the doping concentration, *in situ* doping can be applied. Neither the thermal diffusion process nor the ion-implantation technique are well established for diamond. The former process is limited by the negligible diffusion coefficient in a realistic temperature range, and the latter technique is hampered by the lattice damage introduced by the highly energetic ions. Ion implantation is only applicable for the  $\text{p}^+$  contact region and junction termination extension (JTE) structure, which requires a high doping concentration  $> 10^{19} \text{ cm}^{-3}$  in a selective area. To realize an optimum doping profile with p-type conduction, a B-containing source gas (diborane:  $\text{B}_2\text{H}_6$  or trimethylboron:  $\text{B}(\text{CH}_3)_3$ ) is introduced during CVD growth.

Figure 21.8 shows the relationship between the film resistivity ( $\rho$ ) and effective doping concentration ( $N_{\text{A}} - N_{\text{D}}$ ) at room temperature [88].  $\rho$  is modified widely from  $10^5$  to  $10^{-3} \Omega \text{ cm}$  by controlling the doping concentration from  $10^{15}$  to  $10^{21} \text{ cm}^{-3}$ . In the low-doping-concentration regime,  $\rho$  is largely affected by donor-like impurities ( $N_{\text{D}}$ ). Reduction of background impurities, e.g. H, Si, N, O, is important to realize an optimum resistivity. Hole mobilities exceeding  $2000 \text{ cm}^2/(\text{V s})$  were confirmed by Hall effect measurements at room temperature; these values are larger than those of typical semiconducting materials. Polycrystalline films exhibit rather high  $\rho$  compared with that of single-crystal films because of the reduced mobility, which is mainly caused by carrier scattering by the grain boundaries. With increasing  $N_{\text{A}} - N_{\text{D}}$ , the carrier transport properties change from band

**Figure 21.8** Resistivity as a function of effective B doping concentration ( $N_A - N_D$ ). Source: The original version of this figure is presented in Werner et al. [88].



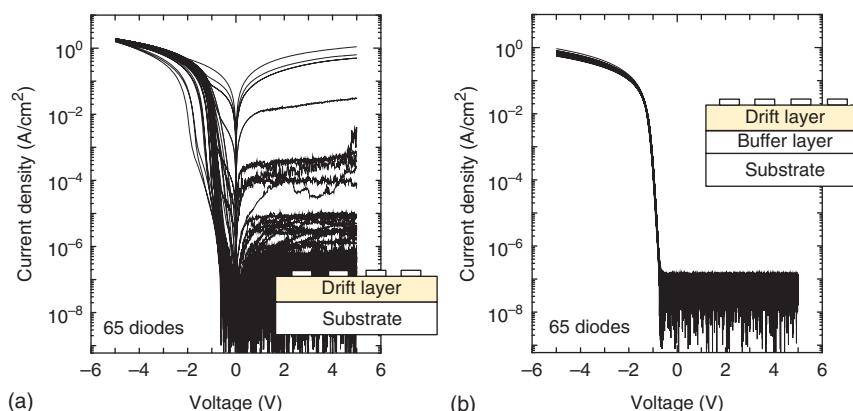
transport to nearest-neighbor-hopping conduction, which effectively decreases the apparent activation energy. This phenomenon is apparently observable for  $N_A - N_D > 10^{19} \text{ cm}^{-3}$ . Above the metal-insulator-transition doping level ( $3 \times 10^{20} \text{ cm}^{-3}$ ), the apparent activation energy becomes zero (degenerate semiconductors). Superconducting properties have been reported from such films [89].

To realize high-performance diamond electronics, reduction of electrically active killer defects is crucial. Threading dislocations (TDs) are major defects in CVD-grown diamond, and they are generally taken over from a substrate to an epitaxial layer or even proliferated from its interface [63]. Therefore, sophisticated surface treatment is a prerequisite [90]. UV-assisted ultra-flattening surface polishing can effectively suppress the dislocation emergence at the interface; however, existing dislocations in the substrate are all propagated during epitaxial growth. For III-V semiconductors such as gallium nitride (GaN), dislocation-reduction techniques, as represented by epitaxial lateral overgrowth (ELO), have been widely adopted [91]. This process requires a stripe mask pattern, which effectively terminates dislocations below the mask and only allows their propagation from opening windows. Their effectiveness has also been verified in heteroepitaxial diamond growth [92]. However, this method is only applicable for high dislocation densities ranging from  $10^{10}$  to  $10^6 \text{ cm}^{-2}$ , and achieving further reduction of the dislocation density remains challenging.

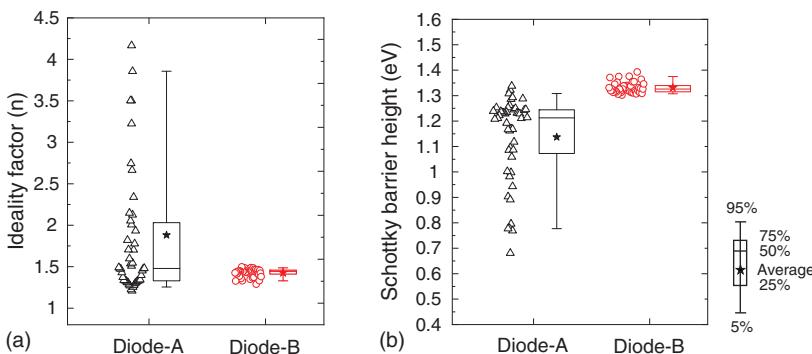
Naamoun et al. proposed a technique to prevent TDs from propagating from the substrate to the CVD epitaxial layer using metal nanoparticles [42]. This concept is based on the selective revealing of dislocations by  $\text{H}_2/\text{O}_2$  plasma etching followed by Pt nanoparticle self-assembly (island growth) in the etch-pit positions. After the subsequent CVD overgrowth, some of the TDs are annihilated by the metal nanoparticles. However, the overall dislocation density remains high ( $\sim 10^6 \text{ cm}^{-2}$ ). Optimization of metal incorporation without introducing self-defects is therefore crucial. New dislocations emerging from the metal nanoparticles is another

problem that remains to be overcome. Ohmagari et al. proposed a technique called metal-assisted termination (MAT) to annihilate TD propagation through the incorporation of atomic-scale metal impurities [93]. In MAT, metal impurities that possess larger covalent radii than that of carbon atoms are randomly incorporated during epitaxial growth by CVD, suppressing TD propagation. This strategy was accomplished using hot-filament (HF) CVD with heated *W* wires. *W* ( $\sim 10^{18} \text{ cm}^{-3}$ ) was incorporated as an impurity during epitaxial growth. After growth of a film with a thickness of several micrometers, the dislocation density decreased substantially from  $10^6 \text{ cm}^{-2}$  in the substrate to  $10^4 \text{ cm}^{-2}$  in the epilayer.

To investigate the effect of dislocation reduction, SBDs were fabricated. The thickness and *B* concentration of the drift layer were  $3 \mu\text{m}$  and  $1 \times 10^{16} \text{ cm}^{-3}$ , respectively. Two different device configurations were compared: Diode A (conventional SBDs without buffer layer) and Diode B (with MAT buffer layer). Mo/Au Schottky and Ti/Mo/Au Ohmic electrodes were prepared on an oxygen-terminated diamond surface. A total of 65 diodes (Schottky diameters of  $100 \mu\text{m}$ ) were fabricated on identical substrates, and the electrical characteristics were measured using a semiconductor parameter analyzer (Agilent Technologies Inc., B1505A). Figure 21.9a shows the typical *J*-*V* characteristics of Diode A. The diode properties were categorized into three groups depending on the leakage-current level at a reverse voltage of 5 V: (i) low leakage (below the detection limit), (ii) high leakage, or (iii) Ohmic-like (rectification ratio less than 10). The following results were reported for Diode A: 23 low-leakage diodes (35%), 39 high-leakage diodes (60%), and 3 Ohmic-like diodes (5%). The large leakage current may have originated from the high dislocation density of  $\sim 10^6 \text{ cm}^{-2}$ . Breakdown behavior was observed at a reverse voltage of 50 V. In contrast, for Diode B, all 65 diodes exhibited low leakage, as observed in Figure 21.9b. The *J*-*V* curves of the examined diodes are superimposed, revealing their high uniformity. Breakdown was not observed up to 750 V, which was the limit of the apparatus.



**Figure 21.9** Electrical properties of diamond Schottky barrier diodes: (a) Diode A (normal epitaxy) and (b) Diode B (after insertion of buffer layer). A total of 65 Schottky contacts with diameters of  $100 \mu\text{m}$  were fabricated on identical substrates, and their in-plane uniformity was evaluated.



**Figure 21.10** Distribution of SBD parameters of Diode A (normal epitaxy) and Diode B (after insertion of buffer layer): (a) Ideality factor and (b) Schottky barrier height.

Figure 21.10 presents the histogram analysis of the  $n$  and  $\phi_B$  plots. Diode A showed discrete  $n$  and  $\phi_B$  values:  $n = 1.88$  (standard deviation 0.93) and  $\phi_B = 1.14$  eV (standard deviation 0.17 eV). This tendency is often observed for diamond SBDs. The metal–semiconductor interface (i.e. oxygen termination) may have degraded because of the presence of defects [94]. Device B exhibited uniform forward characteristics:  $n = 1.43$  (standard deviation 0.05) and  $\phi_B = 1.33$  eV (standard deviation 0.02 eV). It was considered that highly uniform and stable oxygen termination was realized after the dislocation reduction.

The growth and physical properties of B-doped p-type diamond epilayers were briefly summarized. The film resistivity is widely controllable from  $10^5$  to  $10^{-3}$   $\Omega$  cm with increasing B concentration from  $10^{15}$  to  $10^{21}$   $\text{cm}^{-3}$ . To realize high-performance diamond electronics, a low-dislocation-density high-quality B-doped epilayer is indispensable. The electrical properties of a SBD with a p-type drift layer were non-uniform: good rectifying actions were observable; however, some diodes exhibited high leakage current. Highly uniform electrical properties were recently demonstrated after the insertion of a metal-containing buffer layer. Crystalline uniformity of the epilayer is important for handling high current with a large electrode.

## 21.4 Devices

Owing to its excellent material properties, diamond is the so-called “ultimate semiconductor” and is expected to reduce the power consumption and increase the operation frequency of circuits. A figure of merit (FOM) is a measure used to compare materials and how much devices can be improved. For power devices, Baliga introduced the following two important FOMs, Baliga’s FOM (BFOM) and Baliga’s high frequency FOM (BHFOM) [95]:

$$\text{BFOM} = \epsilon \mu E_G^3 \cong V_{\max}^2 / R_{onA}$$

$$\text{BHFOM} = \mu E_B^2$$

here,  $\epsilon$ ,  $\mu$ ,  $E_G$ ,  $V_{\max}$ ,  $R_{\text{on}}A$ , and  $E_B$  are the dielectric constant, carrier mobility, bandgap energy, breakdown voltage, specific on-resistance, and avalanche breakdown field, respectively. The BFOM estimates the trade-off limit between conduction loss and the breakdown voltage of a unipolar device, and the BHFM includes the switching loss of the gate capacitance of field-effect transistors (FETs). For both FOMs, diamond has advantages [96]. Huang also introduced FOMs such as the high-temperature FOM (HTFOM) and chip-area FOM (HCAFOM), which consider the actual switching behavior and estimated high temperature operation capability and reduction of chip area [97] (further details are provided in [96, 98]). As the FOMs of diamond are higher than those of other wide-bandgap semiconductors, the reported performance of experimentally fabricated diamond devices is not as high as that expected from the FOMs [98].

One of the major issues facing diamond is its low conductivity at room temperature, especially in the channel region and drift layer [96]. Only less than 5% of boron acceptors are activated at room temperature because of the large activation energies of impurity boron; accordingly, the resistivity becomes high. On the other hand,  $R_{\text{on}}A$  of diamond becomes lower than that of SiC and GaN, and the advantage of using diamond is obvious when the operation temperature is higher than 100 °C. Another challenge is the poor device processing. Processing technology established for silicon devices, especially ion implantation and oxidation, are not applicable to diamond. Accordingly, edge-termination techniques, such as JTE, which can reduce the high electrical field peak at the edge of the electrode, cannot currently be applied for diamond [96]. The small size of a single-crystal diamond wafer (<4 mm) results in low reproducibility of the fabrication process. New device processing techniques need to be developed to increase the device performance up to the material limit.

To date, both unipolar and bipolar diodes, including p-type-intrinsic-n-type diodes (PiNDs), SBDs, junction barrier Schottky diodes (JBSDs), metal-intrinsic-p-type diodes (MiPDs), and Schottky pn diodes (SPNDs), have been experimentally reported. The cross-sectional structures and a summary of the device performances are presented in Table 21.1. The highest  $V_{\max}$  (>11.5 kV) was achieved for a PiND without a mesa structure. The breakdown voltage decreased because the leakage current increased when a mesa structure was utilized. The decrease in the breakdown voltage is considered to result from structural effects at the mesa edges. The forward current density for bipolar diamond devices is low because of the short minority carrier lifetime.

The pseudo-vertical SBD (pVSBD) structure is well utilized for diamond diodes because of the high crystal quality and the ability to use a low-cost semi-insulating substrate. A heavily boron-doped p<sup>+</sup> type layer with 1–3 μm thickness is first grown on the semi-insulating substrate before the deposition of a lightly boron-doped p<sup>-</sup> layer. Ohmic contacts are directly formed on the p<sup>+</sup> layer after selective etching of the p<sup>-</sup> drift layer. In this structure, the depletion layer expands vertically through the drift layer and the forward current flows laterally in the p<sup>+</sup> layer [98]. The highest

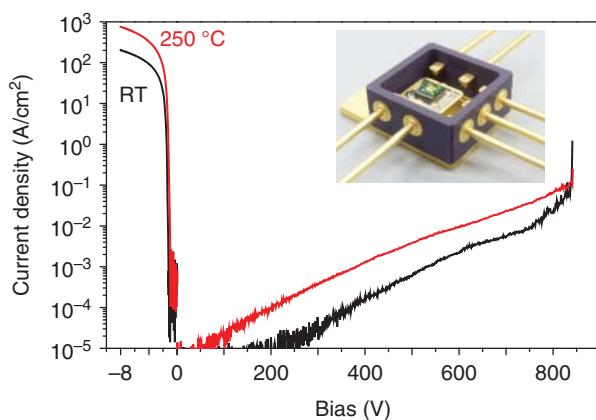
**Table 21.1** Diamond diodes.

Type	Unipolar				Bipolar
Device	pVSBD	VSBD	SPND	MiPD	PiN
Structure					
$V_{max}$	2.5 kV	1.8 kV	<100 V	2.5 kV	>10 kV
$E_{max}$	<i>&gt;7 MV/cm</i>	<i>2.7 MV/cm</i>	<i>3.4 MV/cm</i>	<i>4.2 MV/cm</i>	<i>3.4 MV/cm</i>
$I_{max}$	0.5 A	20 A	<100 mA	<100 mA	<100 mA
$J_{max}$	<i>&gt;4.5 kA/cm<sup>2</sup></i>	<i>&gt;1 kA/cm<sup>2</sup></i>	<i>&gt;60 kA/cm<sup>2</sup></i>	<i>7.5 kA/cm<sup>2</sup></i>	
Remarks	Stable interface @ 400 °C and X-ray	Fast turn-off @ 250 °C $t_{rr} < 20$ ns	No trade-off between $R_{on}S$ vs. $V_{br}$	Small temperature coefficient of $R_{on}$	Highest $V_{max}$
Challenge	Edge-termination current capability	Edge-termination defects	Low n-doping with low compensation	High current capability	Long lifetime of electron high n+ doping

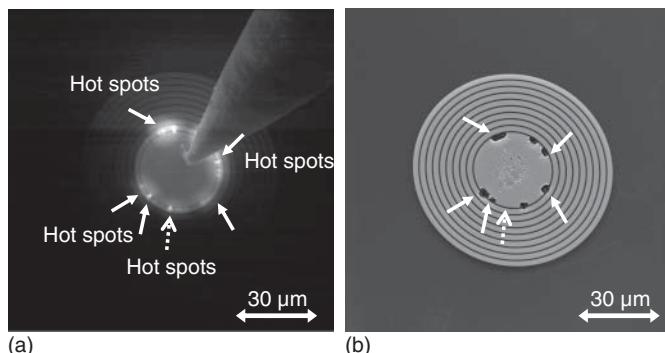
Values of  $E_{max}$  and  $J_{max}$  are italic.

reported BFOM is 244 MW/cm<sup>2</sup> on pVSBD using ozone surface oxidation [99]. For this device, no breakdown behavior was confirmed because of the measurement limit of the test equipment. A maximum breakdown field of 7.7 MV/cm was estimated from the doping concentrations in the p<sup>-</sup> layer.  $R_{on}A$  of pVSBD increased with increasing contact area because the lateral resistance of the p<sup>+</sup> layer limits the maximum current. Accordingly, VSBD is needed for high-current (>5 A) applications. Figure 21.11 shows the typical forward and reverse current–voltage characteristics of a VSBD [98]. The maximum reverse electrical field was 2.1 MV/cm, which is poorer than the ideal value of diamond, >10 MV/cm. The leakage current of diamond SBDs can be explained using a thermionic-field emission model considering the barrier lowering effect. This model agrees well with the measured leakage current even at elevated temperatures [99, 100].

One of the reasons for the premature breakdown at low electrical field is the breakdown at the edge of the electrode where the potential distribution becomes steep [98]. Field enhancement at the edge of the electrode can be experimentally visualized using electron-beam-induced current (EBIC) (for more details on the measurement mechanisms, refer to [101]). Figure 21.12a shows an EBIC image under biased



**Figure 21.11** IV characteristics of diamond Schottky barrier diode and packaged device.



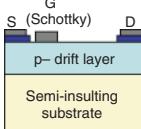
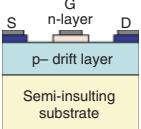
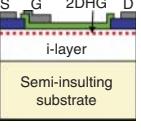
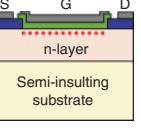
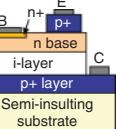
**Figure 21.12** (a) EBIC image of diamond pVSBD with floating metal guard rings under biased condition, and (B) top view of the pVSBD after hard breakdown [102].

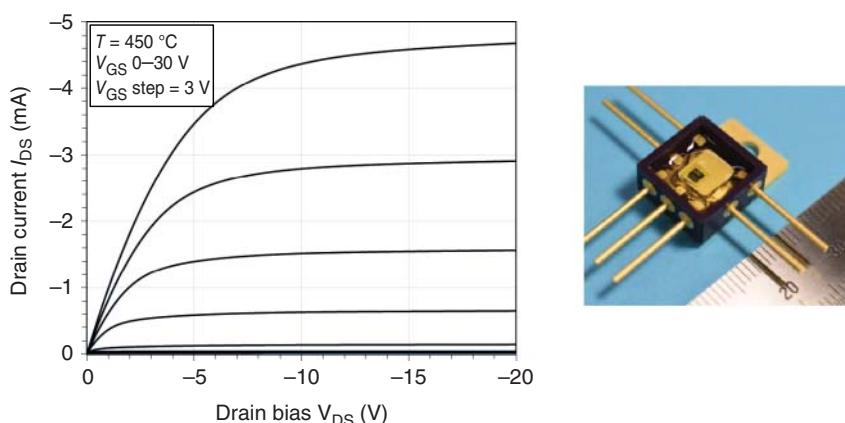
condition, and Figure 21.12b shows a top view after the hard breakdown of pVSBD with floating metal guard rings. As observed in these figures, hot spots appeared at the periphery of the main contact, and hard breakdown occurred at the spots [103]. One possible source of the hot spots is structural defects originating from the fabrication process, particularly the lithography and lift-off processes [101].

For switching devices, metal–semiconductor field-effect transistors (MESFETs), metal–insulator–semiconductor FETs (MISFETs) [104], junction FETs (JFETs) [105], hydrogen-terminated surface channel FETs (H-FETs), inversion-channel metal–oxide–semiconductor (MOS) FETs [82], and bipolar transistors have been realized. The typical device structures and a summary of the performances reported to date are provided in Table 21.2.

The first kV-class diamond FETs were realized on MESFETs [87]. Figure 21.13 shows the typical current–voltage characteristics of a MESFET operated at 450 °C

**Table 21.2** Diamond switching devices.

Type	Unipolar			Bipolar	
Device	MESFET	JFET	H-FET	MOSFET	
Structure					
$V_{max}$	2.2 kV	>600 V	2 kV	<50 V	<50 V
$E_{max}$	2.1 MV/cm	>6 MV/cm	3.6 MV/cm		
$I_{max}$	1 A@250°C	450 A/cm²	12 kA/cm²	<1 mA	<1 mA
$J_{max}$	<3 mA/mm@250°C	(bipolar mode)			
Remarks	Stable operation @ 500 °C & after 10 MGy X-rays	Normally off high T Bipolar mode	Shallow channel $f_{max} > 100$ GHz Normally-on/off vertical structure	Inversion channel (normally-off)	
Challenge	Vertical structure	Vertical structure High n+ doping	Reliability Doping control	High V <sub>r</sub> Vertical structure Mobility	Long lifetime of electron low n+ layer resistivity

**Figure 21.13** IDS-VDS characteristics of diamond MESFET operated at 450 °C and packaged device. Source: Koizumi et al., [96]. copyright 2018, Elsevier.

[87] and of a discrete FET mounted on a metal–ceramics package. Increasing the gate–drain distance ( $L_{GD}$ ) allows wide expansion of the depletion layer from the gate to the drain; accordingly,  $V_{max}$  can be increased from 700 to 1500 V when  $L_{GD}$  is increased from 5 to 30  $\mu\text{m}$ . Without considering field spikes at the drain edge of the gate electrode,  $E_{max}$  was estimated to be 2.15 MV/cm. The MESFET works with low gate leakage current even at high temperature owing to its high Schottky barrier height.

The highest current density of diamond FETs ( $>12 \text{ kA/cm}^2$ ) was achieved on a surface channel diamond FET [106] using vertical configuration. The FET uses a p-type 2D channel formed by surface hydrogen termination [107]. Similar to a MESFET,  $V_{max}$  of hydrogen-terminated surface channel FETs can be increased to 2 kV by increasing  $L_{GD}$  to 24  $\mu\text{m}$ .

An inversion-type p-MOSFET has been realized utilizing OH termination on (111) diamond [82]. A phosphorous-doped n-type layer was used for the body, and  $\text{Al}_2\text{O}_3$  deposited by atomic layer deposition was used as the gate insulator. The inversion mobility was limited to  $20 \text{ cm}^2/(\text{V s})$  because of the high interface state density ( $1 \times 10^{13}/[\text{cm}^2 \text{ eV}]$ ).

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## 22

# Gallium Oxide: Material Properties and Devices

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### 22.1 Introduction

At present, the majority of power switching devices are made by Si. However, it is difficult to keep continuous improvements of Si device performance for a long time in the future from the viewpoint of its intrinsic material properties ruled by a small bandgap energy ( $E_g$ ) of 1.1 eV. Given these circumstances, silicon carbide (SiC) and gallium nitride (GaN) are expected to be principal candidates for next-generation power devices from their physical properties such as larger  $E_g$  of 3.3–3.4 eV, greater breakdown electric fields ( $E_{br}$ ), and larger Baliga's figures of merit (FOMs) than those of Si [1, 2]. However, these materials have the same fundamental drawback that melt-grown bulk single crystals are hardly available.

Gallium oxide ( $\text{Ga}_2\text{O}_3$ ) is one of the oxide semiconductors having an extremely large  $E_g$  of over 4.5 eV [3–5] and an expected  $E_{br}$  of larger than 7 MV/cm. Availability of melt-grown bulk single crystals is another important feature, especially for future industrialization and mass production of  $\text{Ga}_2\text{O}_3$  power devices. From these advantages over the competitors,  $\text{Ga}_2\text{O}_3$  has recently been attracting much attention as a promising material for next-generation power electronics. Furthermore,  $\text{Ga}_2\text{O}_3$  is recognized as a representative among emerging ultrawide bandgap semiconductors, which correspond to semiconductor materials with  $E_g$  significantly exceeding those of SiC and GaN [6].

First, this chapter introduces material properties, and melt bulk and epitaxial thin-film growth techniques of  $\text{Ga}_2\text{O}_3$  based on the comprehensive survey of published literatures. Primitive developments of  $\text{Ga}_2\text{O}_3$  Schottky barrier diodes (SBDs) and field-effect transistors (FETs) are then discussed, with a particular focus on devices developed in the author's group.

## 22.2 Physical Properties of $\text{Ga}_2\text{O}_3$

### 22.2.1 Polymorphs

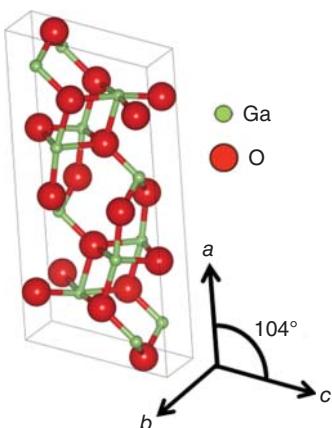
From the first report in 1952, it has been believed that  $\text{Ga}_2\text{O}_3$  has five types of polymorphs that are labeled as  $\alpha$ ,  $\beta$ ,  $\gamma$ ,  $\delta$ , and  $\epsilon$  [7]. In addition to the five polymorphs, a new phase of  $\kappa\text{-}\text{Ga}_2\text{O}_3$ , which has a very similar crystal structure to  $\epsilon\text{-}\text{Ga}_2\text{O}_3$ , was recently discovered [8, 9]. Research efforts have mostly been devoted to  $\beta\text{-}\text{Ga}_2\text{O}_3$  until now because its bulk single crystals can be synthesized by melt growth methods.  $\beta\text{-}\text{Ga}_2\text{O}_3$  has a unique crystal structure called “ $\beta$ -gallia structure,” which is the thermodynamically stable form that belongs to the  $\text{C}2/\text{m}$  space group with lattice constants of  $a = 12.2 \text{ \AA}$ ,  $b = 3.0 \text{ \AA}$ , and  $c = 5.8 \text{ \AA}$ , as illustrated in Figure 22.1. It is a monoclinic structure with an angle between the  $a$  and  $c$  axes of  $104^\circ$ . The unit cell of  $\beta\text{-}\text{Ga}_2\text{O}_3$  contains two inequivalent Ga sites and three inequivalent O sites. Ga(I) and Ga(II) are tetrahedrally and octahedrally coordinated with O, respectively. O(I) and O(II) have threefold Ga coordination, while O(III) has fourfold one.

The other polymorphs ( $\alpha$ ,  $\gamma$ ,  $\delta$ ,  $\epsilon$ , and  $\kappa$ ) correspond to metastable phases. It is impossible to synthesize bulk single crystals of the metastable phases from melt; only thin films are available by low-temperature heteroepitaxial growth on foreign substrates. Corundum  $\alpha\text{-}\text{Ga}_2\text{O}_3$  is the second most investigated phase behind  $\beta\text{-}\text{Ga}_2\text{O}_3$  because of its ease of epitaxial growth on sapphire substrates having the same corundum structure.  $\gamma$ -,  $\delta$ -,  $\epsilon$ -, and  $\kappa\text{-}\text{Ga}_2\text{O}_3$  crystallize into defective spinel, cubic bixbyite-like, hexagonal, and orthorhombic structures, respectively.  $\epsilon$ - and  $\kappa\text{-}\text{Ga}_2\text{O}_3$  are expected to exhibit large spontaneous polarization and ferroelectric properties. Note that the metastable  $\text{Ga}_2\text{O}_3$  thin films change into the most stable  $\beta\text{-}\text{Ga}_2\text{O}_3$  by high-temperature annealing processes and that device process temperature is restricted to be relatively low to avoid the transformation. Throughout this chapter, most of the topics will be focused on  $\beta\text{-}\text{Ga}_2\text{O}_3$ .

### 22.2.2 Material Properties of $\beta\text{-}\text{Ga}_2\text{O}_3$

Table 22.1 summarizes important material properties of major semiconductors and  $\beta\text{-}\text{Ga}_2\text{O}_3$  for power switching devices. The  $E_g$  of  $\beta\text{-}\text{Ga}_2\text{O}_3$  was estimated to be

**Figure 22.1** Atomic unit cell of  $\beta\text{-}\text{Ga}_2\text{O}_3$ .



**Table 22.1** Comparison of material properties between Si, SiC, GaN, and  $\beta\text{-Ga}_2\text{O}_3$ .

	<b>Si</b>	<b>4H-SiC</b>	<b>GaN</b>	<b><math>\beta\text{-Ga}_2\text{O}_3</math></b>
Bandgap (eV)	1.1	3.3	3.4	4.5
Mobility ( $\mu$ ) (cm <sup>2</sup> /Vs)	1400	1000	1200	~200
Breakdown electric field ( $E_{\text{br}}$ ) (MV/cm)	0.3	2.5	3.3	7–8
Dielectric constant ( $\epsilon$ )	11.8	9.7	9.0	10–12
Baliga's FOM ( $\epsilon\mu E_{\text{br}}^3$ )	1	340	870	>1500
Thermal conductivity (W/cm K)	1.5	2.7	2.1	0.27

4.4–4.9 eV from optical absorption spectra [3–5]. Furthermore, there have been arguments about whether  $\beta\text{-Ga}_2\text{O}_3$  is a direct or an indirect bandgap semiconductor. Onuma et al. investigated polarized transmittance and reflectance spectra of  $\beta\text{-Ga}_2\text{O}_3$  bulk single crystals and found out that  $\beta\text{-Ga}_2\text{O}_3$  is an indirect semiconductor with an  $E_g$  of 4.43 eV at room temperature [5]. On the other hand, the direct  $E_g$  corresponding to band-to-band transition at the  $\Gamma$  point was estimated to be 4.48 eV, which is larger than the indirect  $E_g$  by only 50 meV. The optical  $E_g$  of  $\alpha\text{-Ga}_2\text{O}_3$  was extracted to be 5.3 eV from the optical transmittance spectrum [10]. It can be considered that the large  $E_g$  leads to the expected high  $E_{\text{br}}$ . In fact, the peak  $E_{\text{br}}$  of  $\beta\text{-Ga}_2\text{O}_3$  at catastrophic breakdown event happening at a gate dielectric of an FET or an anode electrode edge of a SBD has been simulated to be >5 MV/cm [11–13], which is approximately double those of SiC and GaN and leads to the Baliga's FOM much larger than those of SiC and GaN as shown in Table 22.1.

Si, germanium, and tin (Sn) are often used as donor dopants of  $\beta\text{-Ga}_2\text{O}_3$ . These group IV elements form shallow donor states in  $\text{Ga}_2\text{O}_3$ . The electron density ( $n$ ) in  $\beta\text{-Ga}_2\text{O}_3$  can be controlled in the wide range of  $10^{15}$ – $10^{20}$  cm<sup>-3</sup> by using the donor dopants. The electron effective mass was calculated to be 0.23–0.34  $m_0$  ( $m_0$ : the free electron mass) [14–16], which agree well with experimental data [17–19] and are nearly equal to those of SiC and GaN.  $\beta\text{-Ga}_2\text{O}_3$  has multiple phonon modes in the low-energy range due to its unique band structure determined by the low-symmetric crystal structure [20, 21], and the room-temperature electron mobility in  $\beta\text{-Ga}_2\text{O}_3$  is expected to be up to 200 cm<sup>2</sup>/Vs due to the polar optical phonon scatterings in the lowest energy branch [22, 23]. The saturation electron velocity was theoretically calculated to be about  $2 \times 10^7$  cm/s [24], which is comparable with the values for other compound semiconductors such as GaAs and GaN and thus sufficiently high for various radio-frequency (RF) device applications.

Two fundamental properties of  $\text{Ga}_2\text{O}_3$  are often pointed out as serious drawbacks for power device applications. One is a lack of p-type material, and the other is poor heat dissipation capacity due to its low thermal conductivity.

In contrast to the n-type doping, there has been no report on successful p-type doping with effective hole conduction. In general, it is difficult for single-crystal oxide semiconductors to realize shallow acceptor doping because their valence band states are derived mainly from the O 2p orbitals with strong bonding. There are

some proposed candidates for deep acceptors of  $\text{Ga}_2\text{O}_3$  such as magnesium (Mg), zinc, beryllium, and nitrogen (N); however, theoretical studies have predicted that all these impurities would exhibit extremely large activation energies of over 1 eV [25–27]. Another expected factor that limits hole conductivity in  $\text{Ga}_2\text{O}_3$  is the very low mobility owing to the heavy hole effective mass originated from the valence band structure with small energy dispersion [14, 15, 28]. Furthermore, it has also been predicted by first-principles calculations that holes tend to form localized small polarons by the self-trapping effect due to local lattice distortions and that this phenomenon prohibits effective hole conduction under low electric field or by diffusion [27, 29]. From the three factors, hole-conductive p- $\text{Ga}_2\text{O}_3$  seems to be hardly realized. However, the deep acceptor p- $\text{Ga}_2\text{O}_3$  is sufficiently useful to form a large energy barrier ( $>3$  eV) in n- $\text{Ga}_2\text{O}_3$  by utilizing the built-in potential of the p–n junction.

Performance of  $\text{Ga}_2\text{O}_3$  devices operated at high-voltage and large current conditions is limited by its low thermal conductivity because self-heating under high-power operation is inevitable even in high-efficiency power devices, and the resistance of the drift layer increases with rising operation temperature due to the decrease in electron mobility [30–34]. Therefore, the low thermal conductivity of  $\text{Ga}_2\text{O}_3$  in the range of 0.1–0.3 W/cm K at room temperature [35–39], which is more than an order of magnitude smaller than those of Si, SiC, and GaN, is a serious potential weakness of  $\text{Ga}_2\text{O}_3$  power devices. The thermal management will be one of the important and challenging research topics for  $\text{Ga}_2\text{O}_3$  device technologies. Direct wafer bonding to a foreign substrate with good thermal and electrical conductivities is considered to be one of the effective methods to improve the heat dissipation [40, 41].

## 22.3 Melt Bulk Growth

The most important feature of  $\beta$ - $\text{Ga}_2\text{O}_3$  from the viewpoint of device commercialization is that bulk single crystals can be synthesized by melt growth methods. Various techniques such as floating zone [42, 43], Czochralski [44, 45], vertical Bridgman [46], and edge-defined film-fed growth (EFG) [47, 48] have been utilized for  $\text{Ga}_2\text{O}_3$  bulk growth. High-quality, large-size wafers can be produced from melt-grown bulk ingots as is the case with Si, GaAs, and sapphire. This merit can offer  $\text{Ga}_2\text{O}_3$  a significant advantage in material quality and production cost over SiC and GaN, whose bulk crystals can be produced only by alternative techniques requiring high pressure and/or temperature. Six-inch-diameter single-crystal  $\text{Ga}_2\text{O}_3$  wafers have already been fabricated from an EFG bulk. n-type conductivity of  $\text{Ga}_2\text{O}_3$  bulk crystals has been controlled by shallow donor doping of Si or Sn, and semi-insulating bulk crystals are also available by deep acceptor/trap doping with iron (Fe) or Mg [48].

## 22.4 Epitaxial Growth

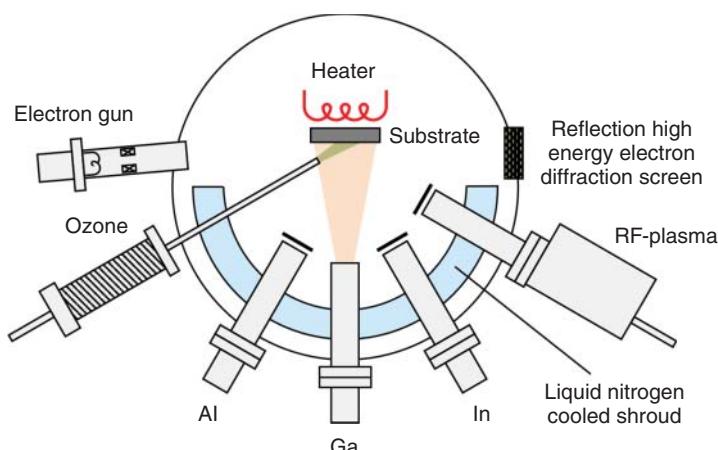
As is the case with other compound semiconductors, various epitaxial growth technologies have been developed for  $\text{Ga}_2\text{O}_3$ , such as molecular beam epitaxy (MBE),

halide vapor phase epitaxy (HVPE), and metalorganic chemical vapor deposition (MOCVD). For  $\text{Ga}_2\text{O}_3$ , there is another unique and popular technique called mist chemical vapor deposition (CVD), which was mainly designed for oxide semiconductors and has often been utilized for growth of the metastable phases.

### 22.4.1 MBE

In the early stage of development, epitaxial growth of  $\text{Ga}_2\text{O}_3$  thin films was mostly explored by MBE. A conventional gas source MBE machine is used for  $\text{Ga}_2\text{O}_3$  growth, as schematically illustrated in Figure 22.2. There are two types of oxygen sources used for  $\text{Ga}_2\text{O}_3$  MBE. One is ozone, and the other is oxygen ( $\text{O}$ ) radicals that are produced by decomposing  $\text{O}_2$  gas with an RF plasma cell. Purity of  $\text{Ga}_2\text{O}_3$  epitaxial films grown by ozone MBE is typically better than those grown by plasma-assisted molecular beam epitaxy (PAMBE). High-density Si and N impurities are unintentionally doped (UID) in  $\text{Ga}_2\text{O}_3$  films grown by PAMBE [49]; on the other hand, densities of both impurities in UID films grown by ozone MBE are below detection limits of secondary ion mass spectrometry. The Si atoms in the PAMBE-grown films are probably supplied from a plasma bulb made by quartz in the plasma cell. The source of N atoms is still unclear; however, it is likely the  $\text{N}_2$  impurity gas incorporated in the high-purity  $\text{O}_2$  source gas. Due to the short lifetime of ozone in vacuum, a nozzle head of the ozone inlet tube has to be set in a very short distance of  $<5$  cm from a substrate. This configuration leads to poor in-plane thickness uniformity of the ozone MBE-grown films. In case of PAMBE, good thickness uniformity can be obtained since enough long distance is kept between a plasma cell and a substrate.

There is a unique technical issue for in situ donor doping during oxide MBE growth. Normally, the donor metal source is installed in a Knudsen cell and thermally evaporated or sublimated to generate the dopant flux. However, under



**Figure 22.2** Schematic of ozone/RF-plasma MBE system illustrating  $\text{Ga}_2\text{O}_3$  thin film growth using ozone as O source.

the typical vacuum pressure of  $10^{-6}$ – $10^{-4}$  Torr in the growth chamber, which is determined primarily by the background O<sub>2</sub> pressure during growth, the surface of the heated dopant metal is readily oxidized, and volatile compounds are formed. As a result, the donor dopant flux is limited by the formation of volatile metal oxides rather than the vapor pressure of the donor metal itself [50]. In consequence, the large increase in the dopant flux supplied to the growth surface makes it very difficult to precisely control the low-level donor doping on the order of  $10^{15}$ – $10^{16}$  cm<sup>-3</sup>. This is a common issue for both ozone MBE and PAMBE.

### 22.4.2 HVPE

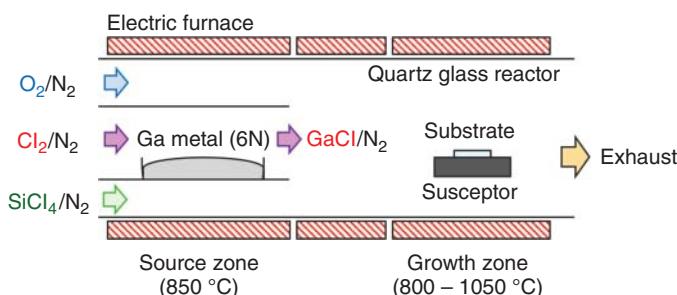
Successful development of Ga<sub>2</sub>O<sub>3</sub> HVPE growth technology in 2014 initiated current worldwide development trend of vertical Ga<sub>2</sub>O<sub>3</sub> transistors and SBDs [51, 52]. An atmospheric-pressure horizontal hot-wall HVPE system for Ga<sub>2</sub>O<sub>3</sub> thin-film growth is schematically illustrated in Figure 22.3. GaCl generated by reaction of high-purity Ga metal with Cl<sub>2</sub> gas is used as a Ga source, and O<sub>2</sub> gas is an O source. SiCl<sub>4</sub> gas is used for donor doping to grow n-Ga<sub>2</sub>O<sub>3</sub> films. The growth rate can be increased to  $\sim$ 20  $\mu\text{m}/\text{h}$  without any degradation of the crystal quality.

UID  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> thin films grown by HVPE on Ga<sub>2</sub>O<sub>3</sub> substrates possess excellent structural and electrical properties, which were confirmed by an extremely low residual *n* of less than  $1 \times 10^{13}$  cm<sup>-3</sup> [52]. The n-type conductivity of Ga<sub>2</sub>O<sub>3</sub> films can be controlled by Si doping in the wide range of  $n = 10^{15}$ – $10^{19}$  cm<sup>-3</sup>. The peak room- and low-temperature electron mobilities of Si-doped n-Ga<sub>2</sub>O<sub>3</sub> films were estimated to be  $\sim$ 150 and  $\sim$ 5000 cm<sup>2</sup>/Vs, respectively [53].

Now, HVPE-grown  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> epitaxial wafers are commercially available, and many universities and research institutes have started developments of vertical Ga<sub>2</sub>O<sub>3</sub> devices by using the commercial HVPE wafers.

### 22.4.3 MOCVD

MOCVD has been an epitaxial growth technique widely used for mass production of optical and electrical compound semiconductor devices. For Ga<sub>2</sub>O<sub>3</sub>, development of MOCVD was a little behind those of MBE and HVPE; however, crystal qualities of MOCVD-grown Ga<sub>2</sub>O<sub>3</sub> films have improved rapidly over the past few years.



**Figure 22.3** Schematic of atmospheric-pressure HVPE system for Ga<sub>2</sub>O<sub>3</sub> growth.

Traditional Ga precursors, such as trimethylgallium and triethylgallium, and O<sub>2</sub> gas are used for Ga<sub>2</sub>O<sub>3</sub> growth [54]. Growth temperatures are typically set at 800–900 °C, which is 100–200 °C lower than that for GaN MOCVD. Si can be doped in an epitaxial film during growth by simultaneously supplying Si-containing precursors such as silane and tetraethyl orthosilicate. The growth rate is typically in the range of 0.1 to a few μm/h.

The residual *n* at a low level of less than  $1 \times 10^{16} \text{ cm}^{-3}$  in MOCVD-grown UID Ga<sub>2</sub>O<sub>3</sub> films has been reported recently [55, 56]. The peak electron mobilities of Si-doped n-Ga<sub>2</sub>O<sub>3</sub> films were ~180 and ~5000 cm<sup>2</sup>/Vs at room temperature and 45 K, respectively [56]. These electrical properties are comparable with those of HVPE-grown films. High-quality (AlGa)<sub>2</sub>O<sub>3</sub> epitaxial films have also been grown by MOCVD [57].

#### 22.4.4 Mist CVD

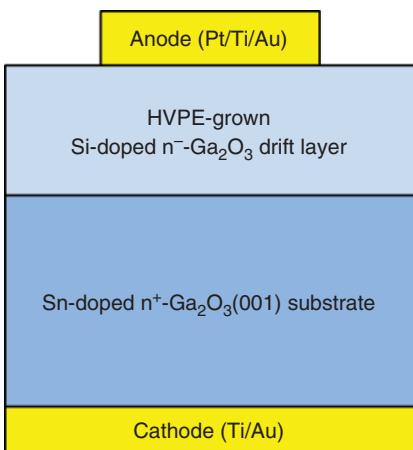
Mist CVD was developed as a technique mainly focusing on oxide semiconductors. Especially, mist CVD has shown its strength on heteroepitaxial growth of metastable Ga<sub>2</sub>O<sub>3</sub> films with α- [10, 58], γ- [59], and ε-phases [60] on foreign substrates. In the mist CVD process, mist atomized from Ga precursors dissolved in water is generated by ultrasonic transducers and then transferred by carrier gas to a growth chamber. Then, epitaxial growth of Ga<sub>2</sub>O<sub>3</sub> films happens on a substrate kept at growth temperature. High-quality Ga<sub>2</sub>O<sub>3</sub> films can be obtained, even though it is a simple technique.

### 22.5 Vertical Diodes

At this time, there have been much more reports on SBDs compared with those on FETs owing to their simple structures and commercially available HVPE-grown epitaxial wafers. Ga<sub>2</sub>O<sub>3</sub> SBDs have already shown their promising performance such as a breakdown voltage ( $V_{br}$ ) of over 2 kV [61, 62], a large forward on-current of over 10 A [63], and high-temperature operation up to 500 °C [64]. In this section, the primitive SBD developments conducted by the author's group are first discussed. Then, state-of-the-art Ga<sub>2</sub>O<sub>3</sub> SBDs and heterojunction p–n diodes using amorphous p-type oxides are described.

#### 22.5.1 SBD with HVPE-Grown Drift Layer

We first fabricated simple SBD structures on 7-μm-thick n-Ga<sub>2</sub>O<sub>3</sub> drift layers with a Si doping concentration on the order of low- $10^{16} \text{ cm}^{-3}$  grown on n<sup>+</sup>-Ga<sub>2</sub>O<sub>3</sub>(001) substrates by HVPE to mainly characterize basic material properties of the drift layers and Schottky contacts [65]. A cross-sectional schematic illustration of the SBD structure is shown in Figure 22.4. The backside ohmic cathode and circular Schottky anode electrodes were fabricated by Ti/Au and Pt/Ti/Au stacks, respectively.



**Figure 22.4** Schematic cross section of vertical Ga<sub>2</sub>O<sub>3</sub> SBD structure.

From linear fits to the forward current density–voltage ( $J$ – $V$ ) curves within the range of  $J = 100\text{--}200 \text{ A/cm}^2$ , the specific on-resistances ( $R_{\text{on}}$ ) were estimated to be  $3.0 \text{ m}\Omega \text{ cm}^2$  for the device with a net donor concentration ( $N_d - N_a$ ) of  $1.4 \times 10^{16} \text{ cm}^{-3}$  in the drift layer and  $2.4 \text{ m}\Omega \text{ cm}^2$  for the one with  $N_d - N_a = 2.0 \times 10^{16} \text{ cm}^{-3}$ . Excellent ideality factors of  $1.02 \pm 0.01$  were also obtained for the SBDs. The reverse  $J$ – $V$  characteristics revealed a  $V_{\text{br}}$  of  $\sim 500 \text{ V}$  for both SBDs.

In an operating temperature range from 21 to  $200^\circ\text{C}$ , the Pt/Ga<sub>2</sub>O<sub>3</sub>(001) Schottky contact exhibited a zero-bias barrier height of  $1.09\text{--}1.15 \text{ eV}$  with a constant near-unity ideality factor. The  $J$ – $V$  characteristics of the SBDs were well fitted by the thermionic emission model in the forward regime and the thermionic field emission model in the reverse regime over the entire temperature range, indicating the high-quality Schottky interface.

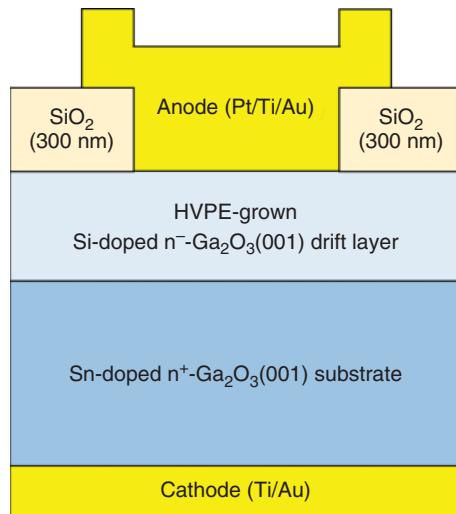
### 22.5.2 Field-Plated SBD

A field plate (FP) is a metal–oxide overlap structure that has mitigating effect of electric field concentration at an anode electrode edge when a SBD is reverse-biased. It is often utilized for the electric field termination to enhance  $V_{\text{br}}$  of SBDs and FETs. Based on the simple SBD structures, Ga<sub>2</sub>O<sub>3</sub> FP-SBDs as shown in Figure 22.5 were fabricated to enhance  $V_{\text{br}}$  [12]. The  $R_{\text{on}}$  of the typical Ga<sub>2</sub>O<sub>3</sub> FP-SBD was estimated to be  $5.1 \text{ m}\Omega \text{ cm}^2$ . Successful FP engineering led to a large enhancement of  $V_{\text{br}}$  from  $\sim 500 \text{ V}$  for the non-FP devices to  $1076 \text{ V}$ . This was the first demonstration of  $V_{\text{br}}$  over  $1 \text{ KV}$  for any Ga<sub>2</sub>O<sub>3</sub> transistors and diodes. At the breakdown condition, the simulated maximum electric field under the anode foot edge reached to  $5.1 \text{ MV/cm}$ , which is much larger than theoretical limits for SiC and GaN.

### 22.5.3 Field-Plated SBD with Guard Ring Formed by Nitrogen-Ion Implantation

To further improve  $V_{\text{br}}$ , Ga<sub>2</sub>O<sub>3</sub> SBDs having a N-ion-implanted guard ring (GR) in a drift layer and a dielectric FP formed on the GR were developed [66]. Note that N is a

**Figure 22.5** Schematic cross section of vertical  $\text{Ga}_2\text{O}_3$  FP-SBD structure.



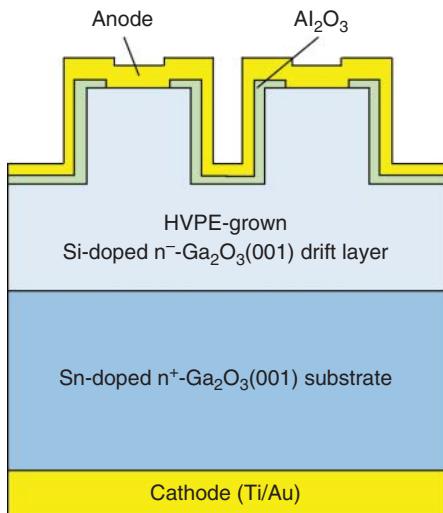
deep acceptor in  $\text{Ga}_2\text{O}_3$  and that N-doped  $\text{Ga}_2\text{O}_3$  acts as a current blocker in n- $\text{Ga}_2\text{O}_3$  by the built-in potential of the p-n junction [67]. N ions were implanted into an HVPE-grown drift layer at multiple energies to form a 0.8- $\mu\text{m}$ -deep box profile with a doping concentration of  $1.0 \times 10^{17} \text{ cm}^{-3}$ , followed by thermal annealing at 1100 °C for recovering implantation damage of the crystal and activating the implanted N atoms. Excellent device characteristics such as an  $R_{\text{on}}$  of 4.7 mΩ cm<sup>2</sup> and a  $V_{\text{br}}$  of 1.43 kV were obtained for the typical SBD due to the effects of the FP and GR.

#### 22.5.4 Trench SBD

Employment of a trench SBD structure is another standard technique for vertical semiconductor devices to enhance  $V_{\text{br}}$ . This structure could be especially useful for  $\text{Ga}_2\text{O}_3$  devices because  $\text{Ga}_2\text{O}_3$  lacks of hole-conductive p-type. Li et al. reported vertical trench  $\text{Ga}_2\text{O}_3$  SBDs with a fin channel width of a few micrometer as shown in Figure 22.6 [62, 68]. The  $V_{\text{br}}$  monotonically increased with decreasing the fin width and reached 2.44 kV. The electric field concentration at the anode edge can be effectively suppressed by depletion regions from the fin sidewalls.

#### 22.5.5 $\alpha\text{-Ga}_2\text{O}_3$ SBD

FLOSFIA Inc., which is a spin-off company from Kyoto University, demonstrated SBDs using  $\alpha\text{-Ga}_2\text{O}_3$  films grown on sapphire substrates by mist CVD [69]. It can be pointed out as a key feature in the device process of the  $\alpha\text{-Ga}_2\text{O}_3$  SBDs that an epitaxial lift-off technology was employed. The free-standing n- $\text{Ga}_2\text{O}_3$  film was peeled from the sapphire wafer, and anode and cathode metal electrodes were directly deposited on the front and back surfaces, respectively. It can be considered that the device structure is effective to improve  $R_{\text{on}}$  and heat dissipation.



**Figure 22.6** Schematic cross section of vertical Ga<sub>2</sub>O<sub>3</sub> fin-channel SBD structure.

### 22.5.6 Heterojunction p-Amorphous Oxide/n-Ga<sub>2</sub>O<sub>3</sub> Diode

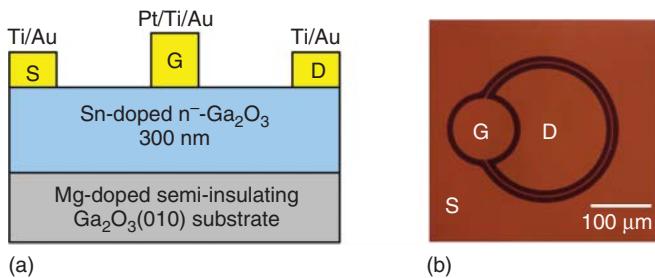
A heterojunction between different oxide materials usually provides relatively good interface properties in contrast to the other compound semiconductors, even though they are not lattice matched. By using the benefit, there have been some reports on heterojunction p-n diodes depositing amorphous p-type oxides on n-Ga<sub>2</sub>O<sub>3</sub>. A p-Cu<sub>2</sub>O/n-Ga<sub>2</sub>O<sub>3</sub> diode demonstrated decent device characteristics such as a forward  $J$  of more than 100 A/cm<sup>2</sup>, an  $R_{on}$  of 8.2 mΩ cm<sup>2</sup>, and a large  $V_{br}$  of 1.49 kV. The  $V_{br}$  was twice larger than that of a normal SBD simultaneously fabricated on the same wafer. [70]

## 22.6 Lateral FETs

In the primitive development stage of Ga<sub>2</sub>O<sub>3</sub> FETs, as other semiconductors, there have been many challenges for developing lateral devices prior to vertical ones because it is typically easier and simpler to fabricate lateral geometry than vertical one. Many fundamental process technologies for Ga<sub>2</sub>O<sub>3</sub> devices have been developed in the efforts.

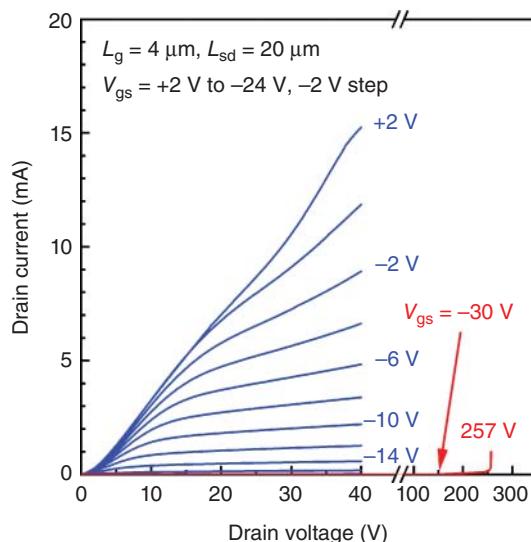
### 22.6.1 MESFET

Transistor action for single-crystal Ga<sub>2</sub>O<sub>3</sub> devices was first demonstrated using simple metal-semiconductor field-effect transistors (MESFETs) fabricated by the author of this chapter and collaborators in 2011 [71]. Figure 22.7a shows a schematic cross section of the MESFET structure. The MESFET having a circular geometry as shown in Figure 22.7b showed decent device characteristics as the first FET, such as effective modulation of drain current ( $I_d$ ) by gate voltage ( $V_g$ ) swing, a three-terminal



**Figure 22.7** (a) Schematic cross section and (b) optical micrograph of  $\text{Ga}_2\text{O}_3$  MESFET structure.

**Figure 22.8** DC output characteristics of  $\text{Ga}_2\text{O}_3$  MESFET.

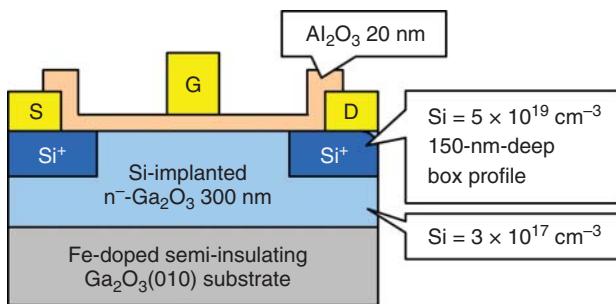


destructive  $V_{br}$  of over 250 V, and an  $I_d$  on/off ratio of 4 orders of magnitude. DC output characteristics of the circular MESFET are shown in Figure 22.8. The non-linear turn-on and poor saturation  $I_d$  characteristics as a function of drain voltage ( $V_d$ ) were caused by poor ohmic characteristics of the source and drain electrodes.

It is worth noting that the community of  $\text{Ga}_2\text{O}_3$  researchers and engineers rapidly grew after the report of the MESFET demonstration. Therefore, this accomplishment has been considered as the most important breakthrough for  $\text{Ga}_2\text{O}_3$  technologies.

### 22.6.2 Depletion-Mode MOSFET

The  $\text{Ga}_2\text{O}_3$  MESFETs exhibited good device characteristics as a first trial. However, the devices also revealed two clear issues of a large ohmic contact resistance of source and drain electrodes and a small current leakage through the  $\text{Ga}_2\text{O}_3$  surface. To overcome the drawback of ohmic contact, Si-ion implantation doping technology was developed [72]. Implanted Si atoms in  $\text{Ga}_2\text{O}_3$  are well activated by thermal annealing at 900–1000 °C. Selective-area high-density Si-ion implantation doping under the

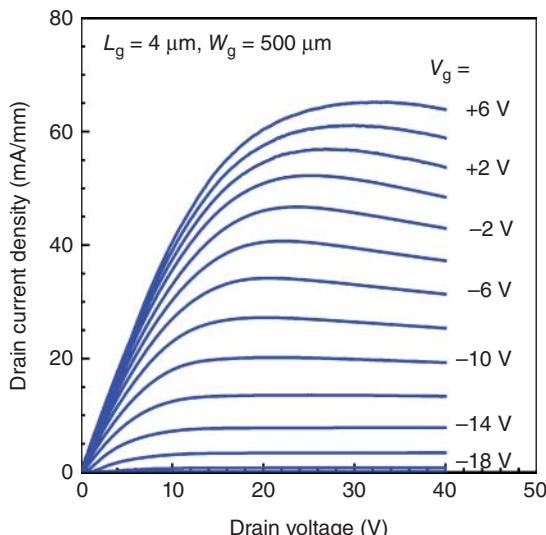


**Figure 22.9** Schematic cross section of D-mode Ga<sub>2</sub>O<sub>3</sub> MOSFET structure fabricated by Si-ion implantation doping.

source and drain electrode areas can provide a specific contact resistance of less than  $1 \times 10^{-5} \Omega \text{cm}^2$ ; this is an enough low value for various Ga<sub>2</sub>O<sub>3</sub> device applications. The other issue of the surface leakage was drastically suppressed by Al<sub>2</sub>O<sub>3</sub> surface passivation.

By employing the new device processes, depletion-mode (D-mode) Ga<sub>2</sub>O<sub>3</sub> metal oxide-semiconductor field-effect transistors (MOSFETs) as schematically depicted in Figure 22.9 were fabricated [73]. A UID Ga<sub>2</sub>O<sub>3</sub> layer was grown on an Fe-doped semi-insulating Ga<sub>2</sub>O<sub>3</sub>(010) substrate by ozone MBE. A channel, and source and drain ohmic regions were fabricated by Si-ion implantations with densities of  $3 \times 10^{17}$  and  $5 \times 10^{19} \text{ cm}^{-3}$ , respectively. The Al<sub>2</sub>O<sub>3</sub> gate dielectric and passivation layer was formed by plasma atomic layer deposition.

Figure 22.10 shows  $I_d - V_d$  output characteristics of the representative D-mode MOSFET. The turn-on linearity and saturation of  $I_d$  were drastically improved from the characteristics of the MESFET. The maximum  $I_d$  was 65 mA/mm at  $V_g = +6 \text{ V}$ , which was more than twice as large as that of the MESFET. The three-terminal



**Figure 22.10** DC output characteristics of D-mode Ga<sub>2</sub>O<sub>3</sub> MOSFET.

off-state  $V_{br}$  was enhanced to 400 V, and the off-state leakage was drastically decreased to less than the lower limit of a measurement instrument. Due to the large decrease in leakage current, the  $I_d$  on/off ratio was increased to over 10 orders of magnitude. High-temperature stable operation up to 300 °C was also demonstrated without permanent degradation in electrical device characteristics.

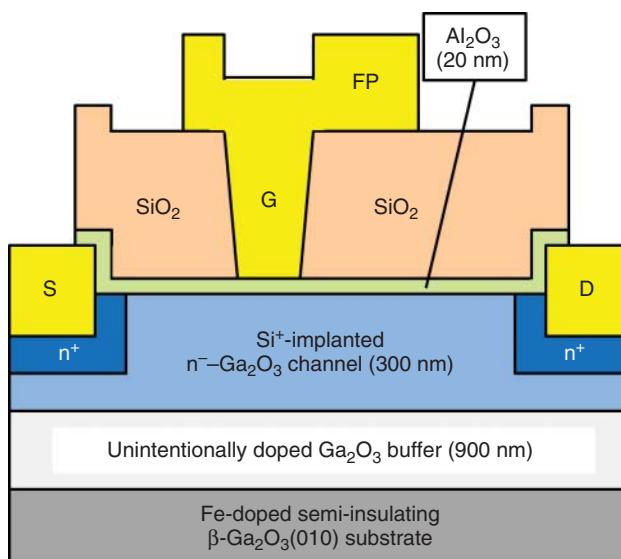
This device has been a base structure for following developments of lateral  $\text{Ga}_2\text{O}_3$  FETs conducted all over the world.

### 22.6.3 Field-Plated MOSFET

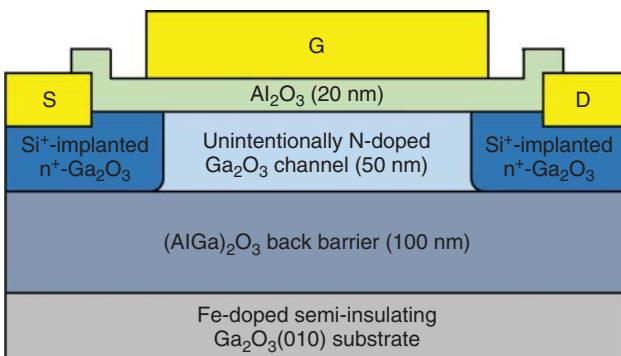
An FP is commonly used as an edge termination structure for lateral FETs to enhance  $V_{br}$  by preventing the electric field concentration at a drain side edge portion of a gate metal. Figure 22.11 shows a cross-sectional schematic of a  $\text{Ga}_2\text{O}_3$  MOSFET structure with a gate-connected FP [74]. The FP contributed to a large enhancement of  $V_{br}$  from ~400 to ~750 V without any degradation of on-state device characteristics from those of the D-mode MOSFET without an FP. The device also exhibited no DC-RF dispersion due to the effect of the thick  $\text{SiO}_2$  passivation. As a result of continuing development, the  $V_{br}$  of lateral  $\text{Ga}_2\text{O}_3$  FP-MOSFETs has been enhanced to over 2 kV [75, 76].

### 22.6.4 Modulation-Doped FET

$(\text{AlGa})_2\text{O}_3/\text{Ga}_2\text{O}_3$  modulation-doped field-effect transistors (MODFETs), which are analogous to AlGaAs/GaAs MODFETs, were developed [77, 78]. Either Si or Ge



**Figure 22.11** Schematic cross section of  $\text{Ga}_2\text{O}_3$  FP-MOSFET structure.



**Figure 22.12** Schematic cross section of  $\text{Ga}_2\text{O}_3$  MOSFET structure with N-doped channel layer.

was doped in the  $(\text{AlGa})_2\text{O}_3$  barrier layer as a donor, and two-dimensional electron gas (2DEG) with a sheet charge density of low  $10^{12} \text{ cm}^{-2}$  was formed at the interface. Zhang et al. succeeded in not only confirming 2DEG formation at the interface but also estimating the electron effective mass of  $0.313 \pm 0.015 m_0$  in  $\text{Ga}_2\text{O}_3$  from Shubnikov-de Haas oscillations of the  $(\text{AlGa})_2\text{O}_3/\text{Ga}_2\text{O}_3$  MODFET [19]. A high  $V_{\text{br}}$  of 1.37 kV and a large average  $E_{\text{br}}$  of 3.9 MV/cm have also been demonstrated [79]. The MODFETs are expected to be useful especially for high-frequency applications.

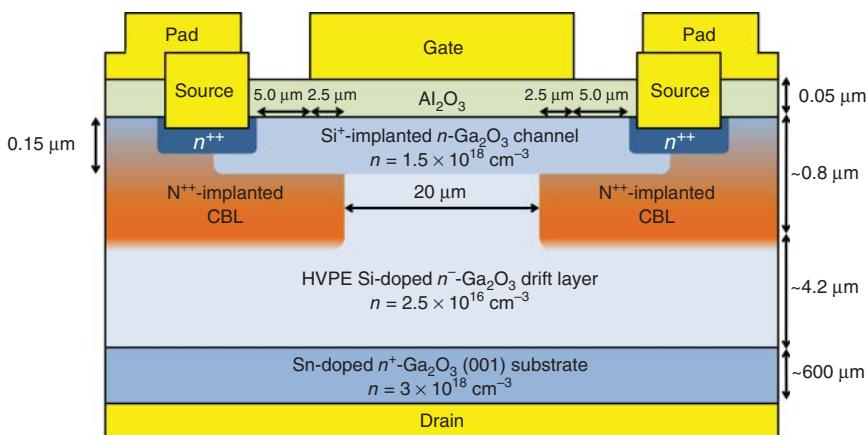
### 22.6.5 Normally Off FET

Planar enhancement-mode (E-mode)  $\text{Ga}_2\text{O}_3$  MOSFETs realizing normally off operation were fabricated by decreasing a thickness and/or a doping concentration of a channel layer to enable full depletion under a gate at  $V_g = 0 \text{ V}$ . Early E-mode operations were demonstrated for wrap-gate FETs [80], nanomembrane FETs [31], MOSFETs with a UID channel layer [81], and MOSFETs with a recessed gate [82].

Recently, the author's group achieved normally off operation for  $\text{Ga}_2\text{O}_3$  MOSFETs with an unintentionally N-doped  $\text{Ga}_2\text{O}_3$  channel layer grown by PAMBE, as illustrated in Figure 22.12 [49]. The channel layer had N and Si concentrations of  $1 \times 10^{18}$  and  $2 \times 10^{17} \text{ cm}^{-3}$ , respectively, indicating that it should be a p-type material with  $N_a > N_d$ , if both N and Si atoms were highly activated. The MOSFETs demonstrated a turn-on threshold  $V_g$  of larger than +8 V, implying formation of an inversion channel at an interface between an  $\text{Al}_2\text{O}_3$  gate dielectric and the N-doped  $\text{Ga}_2\text{O}_3$  layer.

## 22.7 Vertical FETs

As of the time of this writing, to the best of the author's knowledge, there have been a few groups developing vertical  $\text{Ga}_2\text{O}_3$  transistors in the world. The following section will discuss two representative developments of vertical  $\text{Ga}_2\text{O}_3$  FETs.



**Figure 22.13** Schematic cross section of vertical D-mode  $\text{Ga}_2\text{O}_3$  MOSFET structure with current aperture.

### 22.7.1 Current Aperture FET

Vertical FETs with a current aperture were often selected as a first structure in the history of vertical transistor developments due to its simple structure. Figure 22.13 shows a schematic cross section of a vertical D-mode  $\text{Ga}_2\text{O}_3$  MOSFET with a current aperture that was bounded laterally by N-implanted current blocking layers (CBLs) [83]. It should be noted that three ion implantations were performed to form the N-doped p- $\text{Ga}_2\text{O}_3$  CBLs, a Si-doped n- $\text{Ga}_2\text{O}_3$  channel, and heavily Si-doped n<sup>++</sup>- $\text{Ga}_2\text{O}_3$  source ohmic contact regions. Decent device characteristics such as a maximum  $I_d$  of 0.42 kA/cm<sup>2</sup> and a specific  $R_{on}$  of 31.5 m $\Omega$  cm<sup>2</sup> were demonstrated. The  $I_d$  on/off ratio recorded more than 8 orders of magnitude. The three-terminal off-state  $V_{br}$  was limited to <30 V owing to large electric field in the  $\text{Al}_2\text{O}_3$  gate dielectric due to the high Si doping density of the channel.

E-mode operation of vertical  $\text{Ga}_2\text{O}_3$  MOSFETs was also demonstrated [84]. The device fabrication process and structure of the E-mode MOSFETs were almost the same as those of the D-mode devices. There were two modifications from the D-mode structure. One was a decrease in the Si doping density of the channel from  $1.5 \times 10^{18}$  to  $5.0 \times 10^{17} \text{ cm}^{-3}$ . The other was the formation of an n<sup>++</sup>-region-gate overlap to avoid full channel depletion in the gate-source access region at thermal equilibrium. A turn-on threshold  $V_g$  of larger than +3 V and an  $I_d$  on/off ratio of more than 6 orders of magnitude were demonstrated, which are sufficiently large values for practical switching applications. Furthermore, the off-state  $V_{br}$  was largely improved to ~250 V due to the reduction of the Si density in the channel.

### 22.7.2 Fin Channel FET

Trench structures are also effective for vertical transistors on electric field management. The same group of Cornell University that developed the trench SBDs reported vertical  $\text{Ga}_2\text{O}_3$  transistors with a sub-micrometer fin channel [85]. E-mode operation

was achieved for the devices due to full depletion from the sidewalls at  $V_g = 0$  V. The fin FETs revealed excellent device characteristics such as a large  $I_d$  of  $1\text{ kA}/\text{cm}^2$ , a specific  $R_{on}$  of  $10\text{--}20\text{ m}\Omega\text{ cm}^2$ , an  $I_d$  on/off ratio of 8 orders of magnitude, and an off-state  $V_{br}$  of  $\sim 1$  kV.

## 22.8 Summary

This chapter presents an overview of current status of research and development on  $\text{Ga}_2\text{O}_3$  power devices, which covers material properties, melt bulk growth, epitaxial thin-film growth, and device technologies. The extremely large Baliga's FOM and availability of high-quality, large-diameter single-crystal wafers produced from melt-grown bulks are especially appealing to the semiconductor power device community. Over the past 10 years, significant progress in all the aspects of  $\text{Ga}_2\text{O}_3$  material and device technologies has been made and several milestones on the way to industrialization and commercialization of  $\text{Ga}_2\text{O}_3$  power transistors and diodes have already been achieved. However, there is no room for doubt that the current  $\text{Ga}_2\text{O}_3$  power device technologies are still immature and that we still have a long way to start to introduce them to practical markets. Future intense efforts are indispensable to develop advanced device structures to further improve device characteristics. Overcoming the two drawbacks related to fundamental material properties, which are the absence of hole-conductive p- $\text{Ga}_2\text{O}_3$  and the poor thermal conductivity, should be tough challenges. However, the author believes that potential of  $\text{Ga}_2\text{O}_3$  power devices is sufficiently deserved for the efforts.

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