Solid State Electronics 139 (2018) 31–38

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Accurate diode behavioral model with reverse recovery

Stanislav Baná[a,b], Jan Divín[a,b], Josef Dobeš[b], Václav Paňko[a,*]

[a] ON Semiconductor, SCG Czech Design Center, Department of Design System Technology, 1. maje 2594, 756 61 Roznov pod Radhostem, Czech Republic
[b] Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Radioelectronics, Technicka 2, 166 27 Prague 6, Czech Republic

ARTICLE INFO

The review of this paper was arranged by Prof. A. Zaslavsky

Keywords:
Reverse recovery
Behavioral modeling
SPICE model
Characterization
Parameter extraction
High voltage
S-parameters
Transient analysis

ABSTRACT

This paper deals with the comprehensive behavioral model of p-n junction diode containing reverse recovery effect, applicable to all standard SPICE simulators supporting Verilog-A language. The model has been successfully used in several production designs, which require its full complexity, robustness and set of tuning parameters comparable with standard compact SPICE diode model. The model is like standard compact model scalable with area and temperature and can be used as a stand-alone diode or as a part of more complex device macro-model, e.g. LDMOS, JFET, bipolar transistor. The paper briefly presents the state of the art followed by the chapter describing the model development and achieved solutions. During precise model verification some of them were found non-robust or poorly converging and replaced by more robust solutions, demonstrated in the paper. The measurement results of different technologies and different devices compared with a simulation using the new behavioral model are presented as the model validation. The comparison of model validation in time and frequency domains demonstrates that the implemented reverse recovery effect with correctly extracted parameters improves the model simulation results not only in switching from ON to OFF state, which is often published, but also its impedance/admittance frequency dependency in GHz range. Finally the model parameter extraction and the comparison with SPICE compact models containing reverse recovery effect is presented.

1. Introduction

The requirements on the accuracy of SPICE models are being continuously increased due to new branches, e.g. deep sub-micron technologies, high power applications, RF applications, etc. The main effort of model developers is of course focused on the development of MOSFET model. However, most of components including MOSFET contain one or more p-n junctions, which need to be precisely modeled, too. The new technologies and new applications with the accent on the high speed and low power consumption require SPICE device models to be accurate in full operating range, including high speed in combination with high voltage. One of the very important effects is the reverse recovery of p-n junction, where both the reverse current and the reverse voltage can be simultaneously large, which significantly affects the resulting power consumption. Unfortunately, standard compact SPICE models often neglect this effect, which can be crucial for some applications.

Fundamental reverse recovery modeling researches used in this paper have been published in [1–3]. Some of the recently published papers are focused to ultrafast diodes of various types, e.g., Si fast recovery diode, SiC Schottky barrier diode [4], or PIN diodes [5,6]. There also exist several studies focused to measurement methods of the reverse recovery time [7,8]. The reverse recovery is not naturally the domain of diode components only, but it also influences parasitic p-n junctions (parasitic diodes) of other components, where the most important category is the reverse recovery in high frequency power transistors, typically laterally diffused MOSFETs (LDMOS) [8–10]. The DC/DC converter can be considered one of typical applications, where the reverse recovery must be correctly modeled [11,12].

Some of resulting solutions however did not pass the convergence tests, results in some cases were not enough accurate or the solution contains reverse recovery effect only and does not cover other important phenomena, required for p-n junction modeling in production designs.

This paper demonstrates comprehensive behavioral model of p-n junction directly applicable to all common SPICE simulators supporting Verilog-A [13,14]. It deals with the basic equations, used solutions and test methods for the parameter extraction in time and frequency domains.

* Corresponding author.
E-mail addresses: stanislav.banas@onsemi.com (S. Baná), jan.divins@onsemi.com (J. Divín), dobes@feld.cvut.cz (J. Dobeš), vaclav.panko@onsemi.com (V. Paňko).

http://dx.doi.org/10.1016/j.sse.2017.10.034
Received 20 June 2017; Received in revised form 16 September 2017; Accepted 9 October 2017
Available online 13 October 2017
0038-1101/

2. Model development

2.1. Basic equations of compact SPICE diode model

This section deals with the set of well known basic diode equations, used as a ground for the behavioral model development. The goal of this section is not to describe full set of compact diode SPICE model equations and parameters, which can be found in each SPICE manual.

The total diode current in standard SPICE compact diode model is described as [15,16]

$$i = I_{\mathrm{pn}} + \frac{dQ_{\mathrm{inj}}}{dt} + \frac{dQ_{\mathrm{j}}}{dt} \tag{1}$$

where I_{pn} is the large signal current defined for $V > 0\mathrm{V}$ as [15,16]

$$I_{\mathrm{pn}}(V) = I_S\left(\exp\left(\frac{V}{nV_t}\right) - 1\right) \tag{2}$$

and for $V < 0\mathrm{V}$ as [15,16]

$$I_{\mathrm{pn}}(V) = I_S \tag{3}$$

where I_S is saturation current, n is emission coefficient and V_t is thermal voltage. Except the thermal voltage all these parameters are used as tunable compact SPICE model parameters.

Q_{inj} in (1) is charge of injected carriers, dominant mainly with positive voltage applied to p-n junction ($V > 0\mathrm{V}$), defined as [15,16]

$$Q_{\mathrm{inj}}(V) = T_T I_{\mathrm{pn}}(V) \tag{4}$$

where T_T is transit time used as a tunable compact SPICE model parameter. Derivative of this charge with respect to applied voltage is often denoted as the injection capacitance

$$C_{\mathrm{inj}}(V) = \frac{dQ_{\mathrm{inj}}}{dV} \tag{5}$$

Q_{j} in (1) is fixed charge of ionized dopant atoms, dominant mainly with negative voltage applied to p-n junction. This charge is stored in voltage dependent barrier or drift capacitance [15–17]

$$C_{\mathrm{j}}(V) = \frac{dQ_{\mathrm{j}}}{dV} = \frac{\mathrm{C_{J0}}}{\left(1 - \frac{V}{\mathrm{V_J}}\right)^{\mathrm{M_J}}} \tag{6}$$

where $\mathrm{C_{J0}}$ is the zero-bias junction capacitance, $\mathrm{V_J}$ is junction potential and $\mathrm{M_J}$ is a grading coefficient, all used as tunable compact SPICE model parameters.

In fact, (6) is actually not implemented in the SPICE programs. Instead of (6) a charge-controlled formulation of the junction capacitance is implemented, which can be obtained by an integration of $\mathrm{d}Q_{\mathrm{j}} = C_{\mathrm{j}}\mathrm{d}V$:

$$\int_0^{Q_{\mathrm{j}}} \mathrm{d}Q'_{\mathrm{j}} = \int_0^{V} \frac{C_{\mathrm{J0}}}{\left(1 - \frac{V'}{\mathrm{V_J}}\right)^{\mathrm{M_J}}} \mathrm{d}V'. \tag{7}$$

For evaluating this integral equation, let us make a substitution

$$1 - \frac{V'}{V_{\mathrm{J}}} = x \;\Rightarrow\; \mathrm{d}V' = -V_{\mathrm{J}}\mathrm{d}x, \tag{8}$$

which gives the integral

$$Q_{\mathrm{j}} = -V_{\mathrm{J}} \int_1^{1-\frac{V}{V_{\mathrm{J}}}} \frac{C_{\mathrm{J0}}}{x^m} \mathrm{d}x, v \tag{9}$$

to be solved, after that a final formula for the junction charge is obtained:

$$Q_{\mathrm{j}} = \frac{C_{\mathrm{J0}} V_{\mathrm{J}}}{1 - \mathrm{M_J}}\left[1 - \left(1 - \frac{V}{V_{\mathrm{J}}}\right)^{1-\mathrm{M_J}}\right]. \tag{10}$$

The formula (10) is actually implemented, and a current created by the junction capacitance is calculated in the standard way as $\dot{Q}_{\mathrm{j}}$.

Although the full set of diode model parameters contains a parameter called transit time, the T_T in (4) is not a real transit time. The transit time normally means an amount of time needed for carriers to travel at a finite velocity the distance from the middle of the diode to the external terminals. But SPICE model does not include such a concept, as it is clearly seen in (4). The stored injected charge Q_{inj} is an instantaneous function of the applied voltage.

2.2. Principle of reverse recovery behavioral model

Therefore, we were looking for a way to model the reverse recovery correctly. Several published lumped and behavioral models of reverse recovery were tested [1–3,10–12], but the simulation results of many of them were not satisfying. Either convergence or accuracy issues were observed during simulation. Finally the concept published in [1] was chosen.

The total diode current is there defined as

$$i = I_{\mathrm{inj}} + I_{\mathrm{j}} = \frac{dQ_{\mathrm{inj}}}{dt} + \frac{dQ_{\mathrm{j}}}{dt} \tag{11}$$

where I_{inj} is injection current defined as time derivative of the charge of injected carriers Q_{inj} and I_{j} is junction current defined as time derivative of the fixed charge of ionized dopant atoms Q_{j}.

Injection current I_{inj} is then in [1] expressed as

$$I_{\mathrm{inj}} = \frac{Q_{\mathrm{e}} - Q_{\mathrm{m}}}{T_{\mathrm{M}}} \tag{12}$$

where T_{M} is diffusion transit time used as a tunable model parameter, Q_{e} is the charge of carriers injected to the p-n junction and Q_{m} is the charge of carriers injected away from the p-n junction. Charges Q_{e} and Q_{m} are modeled by following equations [1]

$$Q_{\mathrm{e}} = \tau I_S \exp\left(\frac{V}{nV_t} - 1\right) \tag{13}$$

$$Q_{\mathrm{m}} = \tau I_{\mathrm{inj}} - \frac{d(\tau Q_{\mathrm{m}})}{dt} \tag{14}$$

where τ represening minority carrier lifetime is used as a tunable model parameter.

The injection capacitance from Eq. (5) can then be expressed as [1]

$$C_{\mathrm{inj}} = \frac{d(Q_{\mathrm{e}} - Q_{\mathrm{m}})}{dV} \tag{15}$$

The description of fixed charge of ionized dopant atoms Q_{j} as well as the drift capacitance C_{j} provided by (6) remain unchanged in the modified model.

2.3. Realization of model development

The reverse recovery model published in [1] has been developed in language MAST for Saber simulator, not compatible with SPICE simulators used, like ELDO, SPECTRE or HSPICE. So it was necessary to translate the model to more universal HDL language Verilog-A [13,14] applicable to most of standard SPICE simulators. However, the quite complex dependence between (12) and (14) demonstrated in Fig. 1 was found very difficult for the simulation and convergence in Verilog-A.

The first approach of dealing with this challenge was to use current controlled voltage source as a calculator for the charge Q_{m}. The charge Q_{m} from (12) became an auxiliary voltage to enable Verilog-A to

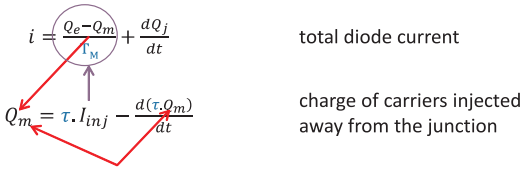

Fig. 1. Interdependencies in diode reverse recovery formulas.

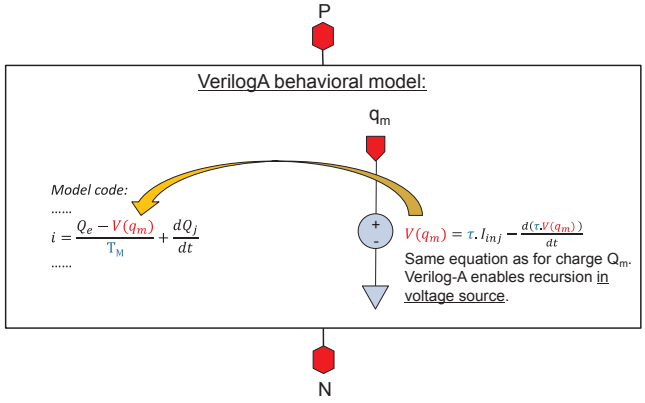

Fig. 2. Solving the recursive calculation of reverse recovery charge.

express result of (14) using arbitrary voltage source and then the result returns back as the charge to (14). The solution is graphically demonstrated in Fig. 2.

However, such solution is not recommended for robust models, as it can cause convergence issues [18]. This happens during model verification using latest versions of ELDO simulator. The convergence issue appeared during transient analysis. So although SPECTRE simulation, HSPICE simulations as well as the simulation with older ELDO versions passed well, we had to look for an alternative solution.

Based on recommendations in [18], the Eq. (11) represented in Verilog-A by the current source was divided into two parallel equations represented in Verilog-A by two parallel current sources flowing through two separate branches as depicted in Fig. 3. The first branch represents the junction current

$$I_j = \frac{dQ_j}{dt} \tag{16}$$

the second branch represents the injection current I_{inj}, specified by (12).

The recursion then appears only in the branch with injection current I_{inj}. Substitution of (14) into (12) gives

$$I_{inj} = \frac{Q_e - \left(\tau I_{inj} - \frac{d(\tau Q_m)}{dt}\right)}{T_M} \tag{17}$$

Minority carrier lifetime τ is a tuning parameter, so it can be as a constant factored out of the time derivative. Eq. (17) can then be expressed as

$$I_{inj} = \frac{Q_e - \tau I_{inj}}{T_M} + \frac{\tau \frac{dQ_m}{dt}}{T_M} \tag{18}$$

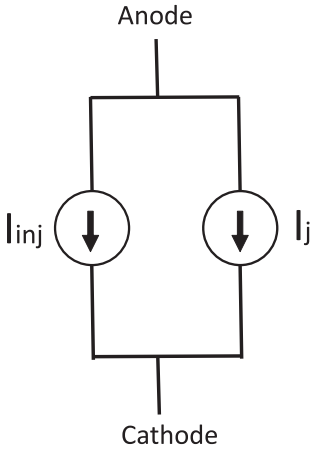

Fig. 3. Example of using two parallel branches for modeling of injection and junction currents independently.

where Q_m is from (12) obtained as

$$Q_m = Q_e - T_M I_{inj} \tag{19}$$

The total diode current in the model is then composed of two parallel currents defined by Eqs. (18) and (16). Eqs. (18) and (19) still contain recursion, but much simpler than in the original approach, so Verilog-A simply solves it. Another advantage of using the (18) form is its clear separation between real and imaginary parts, which helps in AC analysis described later.

The next goal was to add temperature scalability to the model, using the standard temperature dependency equations. The most dominant for the diode is temperature dependency of saturation current, defined by equation [15,16]

$$I_S(T) = I_S(T_{nom})\left(\frac{T}{T_{nom}}\right)^{X_{TI}} \exp\left(\frac{qE_G}{k_b T}\left(\frac{T}{T_{nom}} - 1\right)\right) \tag{20}$$

where T is absolute temperature, T_{nom} is nominal temperature, for which the parameters of the device are defined (typically $T_{nom} = 300$ K), X_{TI} is saturation current temperature exponent used as a SPICE parameter for the tuning of temperature model, q is elementary charge, k_b is Boltzmann constant and E_G is the band-gap energy.

The temperature dependency of silicon band-gap energy is defined as [19]

$$E_G(T) = E_G(0) - \frac{\alpha T^2}{T + \beta} \tag{21}$$

where experimentally obtained constants for silicon are $E_G(0) = 1.16$ eV, $\alpha = 7.02 \times 10^{-4}$ eV/K and $\beta = 1108$ K.

The nominal temperature saturation current $I_S(T_{nom})$ in (20) was extended with the high-injection parameters by adding the factor

$$K_{fwd} = \frac{1}{1 + \sqrt{\frac{I_S(T)\exp\left(\frac{V - R_S I_{pn}}{nV_t} - 1\right)}{I_K}}} \tag{22}$$

where I_K is high-injection knee current and R_S is series resistance. Both parameters are used as model tunable parameters. The final $I_S(T_{nom})$ is then calculated as

$$I_S(T_{nom}) = I_S K_{fwd} \tag{23}$$

The temperature dependency was also added to the series resistance parameter, using following equation [17]

$$R_S(T) = R_S(T_{nom})(1 + T_{RS}(T - T_{nom})) \tag{24}$$

where T_{RS} is temperature coefficient of series resistance used as a tunable model parameter. The impact of series resistance was added also to (13) modified to form

$$Q_e = \tau I_S(T)\exp\left(\frac{V - R_S(T) I_{pn}}{nV_t} - 1\right) \tag{25}$$

where $V - R_S I_{pn}$ represents voltage in p-n junction reduced by voltage drop across series resistance.

The temperature dependency was also added to the calculation of barrier drift capacitance, especially to the parameter V_J, using following equation [15,16]

$$V_J(T) = V_J(T_{nom})\left(\frac{T}{T_{nom}}\right) + 2V_t \ln\left(\frac{n_i(T_{nom})}{n_i(T)}\right) \tag{26}$$

where n_i is intrinsic concentration of used material, in our case silicon, with its own temperature dependency [19]

$$n_i(T) = n_i(T_{nom})\left(\frac{T}{T_{nom}}\right)^{X_{tni}} \exp\left(\frac{q}{2k}\left(\frac{E_G(T_{nom})}{T_{nom}} - \frac{E_G(T)}{T}\right)\right) \tag{27}$$

where X_{tni} is intrinsic concentration temperature exponent, typically set to a value of 1.5.

The scalability of the model with dimension of the p-n junction was created by adding of area factor *area*, which multiplies current parameters I_S or I_K and capacitance parameter C_{J0} and divides series resistance parameter R_S. More sophisticated scaling can be implemented by replacement of these model parameters with customized scaling equations dependent on length, width, perimeter, number of fingers, etc.

The model convergence was assured by adding parallel conductance controlled by the general SPICE parameter GMIN, representing minimal conductance of the model for the case, that the simulated current is too low. SPICE simulators clamp the maximum resistance to 1/GMIN, which defaults to 10^{12} Ω and can be set as an option parameter [16].

The original model prototype contained also avalanche breakdown parameters. But after testing of model convergence using transient simulation, AC and DC simulations or temperature simulations, the avalanche effect was found to cause convergence issues. Therefore it was decided to omit this capability and prioritize the model stability and perfect convergence. Breakdown voltage can be modeled externally using compact diode SPICE model connected in parallel to this behavioral model. Similar practice is commonly used in bipolar transistor model, diffusion/implanted resistor model or some other models containing p-n junction.

Also flicker noise parameters were omitted, however in this case the implementation should not cause any convergence troubles.

3. Model validation

The best validation of the final behavioral model is its application to real device and use for the simulation of real design. In our case the model parameters of two different components were measured and extracted: Zener diode manufactured in integrated 0.25 µm BiCMOS technology and drain-bulk diode of power LDMOS transistor manufactured in fast discrete 0.25 µm technology developed for fast GHz applications.

3.1. Validation in time domain

Time domain measurement was provided using pulse generator Agilent 81104A and oscilloscope Tektronix DPO 7104C with current probe Tektronix CT1. The simulation netlist must reflect the reality including all the parasitic effects. The signal simulated by the ideal SPICE pulse source does not reflect the real signal at the end of cable coming from real pulse source. Therefore it is necessary to add all the parasitic phenomena to the netlist, as it is depicted in Fig. 4. The measurement was provided on wafer to eliminate the impact of the package, which on the other hand made taking the voltage and current probes close to DUT (Device Under Test) very difficult or even impossible. To see the current flowing directly through DUT without impact of parasitic cable between current probe and DUT, it was necessary to add the parasitic RLC circuit to the netlist. The highest impact comes from the parasitic capacitance, which has to be considered in the calculated deembeded measured current used instead of current coming from oscilloscope – see Fig. 4.

The circuit depicted in Fig. 4 is used directly for the simulation and

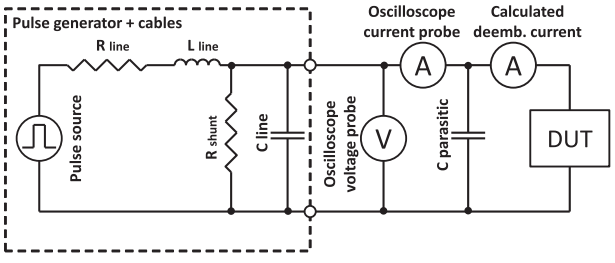

Fig. 4. Setup for pulse measurement of diode reverse recovery.

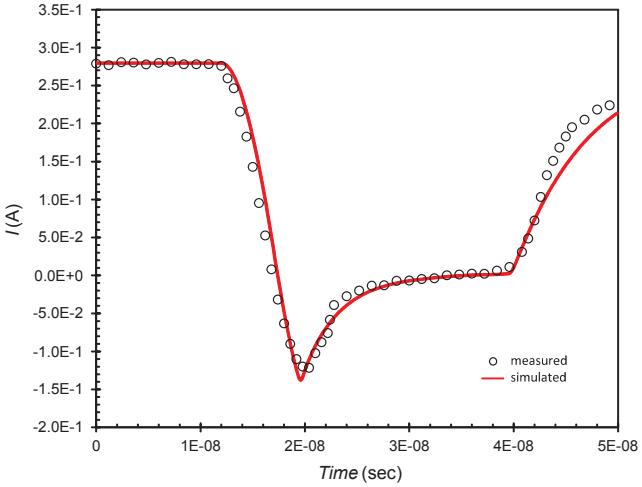

Fig. 5. Current forward-to-reverse transient of Zener diode with area = 0.01 mm^2.

tuning model based on measured data. The first step is to measure the "open" circuit (connected probes, connected cables, needle up) and tuning the netlist RLC parameters to fit the "open" simulation with "open" measured data. The second step is to connect DUT and measure. The final DUT current is then calculated as the current measured in current probe minus simulated current at the capacitor $C_{\text{parasitic}}$.

Measured pulse characteristics compared with simulated results are shown in Figs. 5 and 6. It is apparent, that the parasitic drain-bulk diode of discrete power LDMOS with gate width 2.5 m containing several narrow fingers of p-n junction with relatively large area and perimeter has significantly larger reverse recovery time than the integrated Zener diode. The model is able to cover large portfolio of various device types. The first step prior to the reverse recovery extraction must be of course the accurate DC model and mainly accurate model of reverse bias barrier capacitance. The example of the measured vs. simulated barrier capacitance of power LDMOS drain-bulk diode is in Fig. 7.

The temperature dependency was verified by the comparison with standard SPICE diode model. The I-V and C-V curves scale exactly same as in standard SPICE diode model. Simulated reverse recovery temperature dependency is demonstrated in Fig. 8.

The scalability of the model was verified by the comparison with standard SPICE diode model. The I-V and C-V curves scale exactly same as in standard SPICE diode model. Current response transient characteristics unlike standard SPICE model contain the reverse recovery effect with the scaling correlated to the DC scaling see Fig. 9. Larger device simulates larger current also in reverse recovery. Voltage

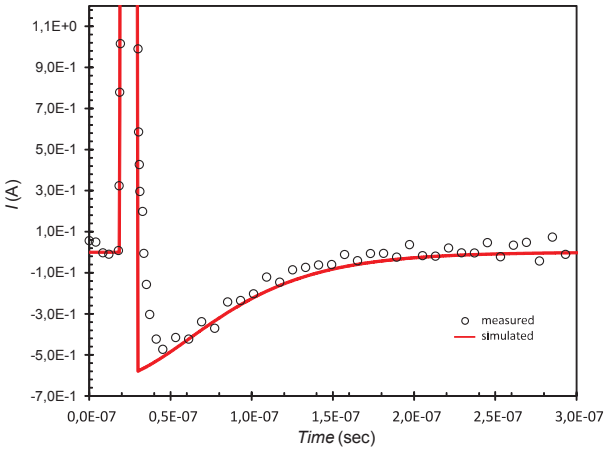

Fig. 6. Current forward-to-reverse transient of discrete power LDMOS parasitic drain-bulk diode. LDMOS gate width is about 2.5 m.

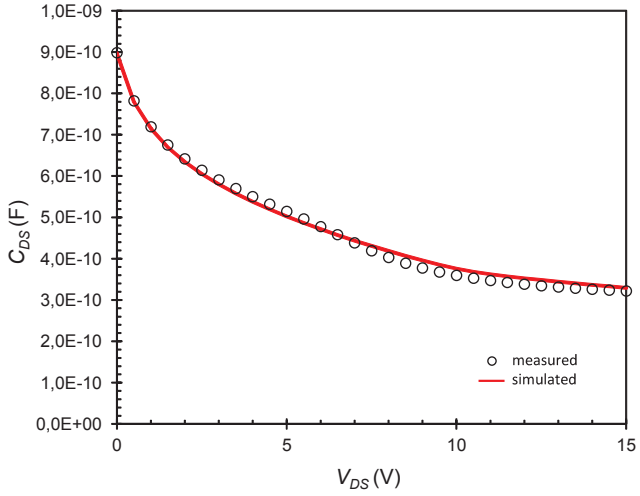

Fig. 7. C-V characteristic of discrete power LDMOS parasitic drain-bulk diode. LDMOS gate width is 2.5 m.

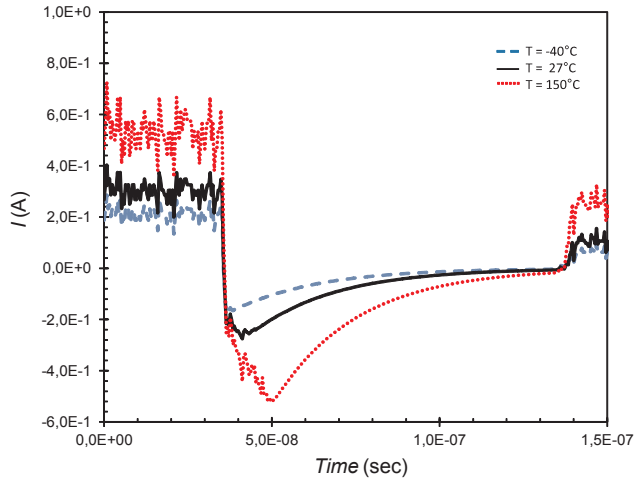

Fig. 8. Verification of the model temperature dependency – simulation of current response forward-to-reverse transient.

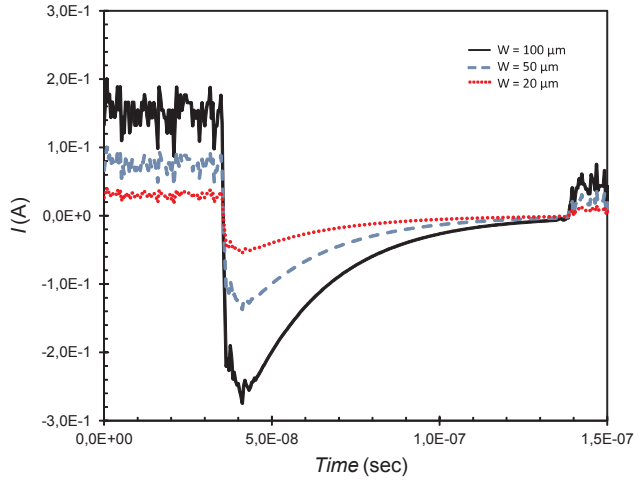

Fig. 9. Verification of the model scalability – simulation of current response forward-to-reverse transient.

response transient characteristics in the other hand follows CV scaling. Larger device with larger capacitance simulates larger delay of dV/dt – see Fig. 10. The smallest device with the negligible simulated reverse

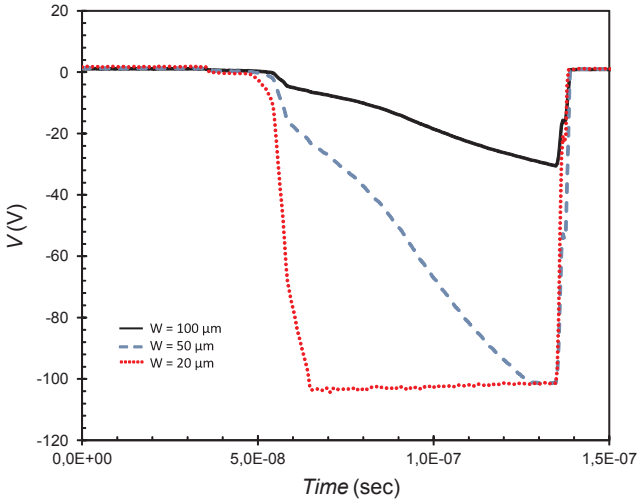

Fig. 10. Verification of the model scalability – simulation of voltage response forward-to-reverse transient.

recovery depicted as dotted line in Fig. 9 has simulated voltage response similar to the simulated standard SPICE diode model without implemented reverse recovery, as it is demonstrated in Fig. 10.

3.2. Validation in frequency domain

As a verification of physical correctness the reverse recovery model, it was decided to measure the admittance of discrete power LDMOS drain-source diode manufactured in fast GHz discrete 0.25 µm technology and compare measured data with simulated results of standard SPICE diode model and simulated results of new Verilog-A diode behavioral model. For the measurement the network analyzer Agilent 8753 and DUT designed as two-gate in ground-signal-ground layout were used. The schematic of test method is presented in Fig. 11.

The applied DC forward voltage at p-n junction was set to range 0.7–0.8 V. For a voltage below 0.7 V the measured current is lower than network analyzer noise floor, for a voltages above 0.8 V the measured data are affected by series resistance. The device was measured at frequencies from 300 kHz to 3 GHz.

Measured scattering S-parameters were converted to admittance Y-parameters using conversion equations [20] implemented in ICCAP model extraction tool and plotted as a real and imaginary parts vs. frequency.

Fig. 12 demonstrates the real part of LDMOS parasitic drain-bulk diode admittance using standard SPICE diode model. Dotted line demonstrates the impact of standard diode parameters. Fig. 13 shows the same measured data compared with simulated results of behavioral diode model containing the reverse recovery effect. It is apparent, that although the model fit is not ideal, the new Verilog-A model has much better trends than the original SPICE model. This improvement is even more visible in imaginary part of admittance, where Fig. 14 shows the measured data vs simulations of standard SPICE diode model, while Fig. 15 demonstrates the same data vs simulation of new Verilog-A model.

As it was already mentioned, the model accuracy in Figs. 13 and 15 is still unsatisfactory especially at high frequencies. But it is still much more accurate than in the case of standard SPICE model demonstrated in Figs. 12 and 14. The main reason of publishing these plots is to demonstrate, that the implementation of reverse recovery naturally improves the model even in the forward area.

In the case of very large fast power devices, or in the cases, where measured p-n junction is part of some more complex device and the quality of p-n junction is controlled by more terminals (e.g. drain-source diode in LDMOS controlled by the gate voltage), it can be very

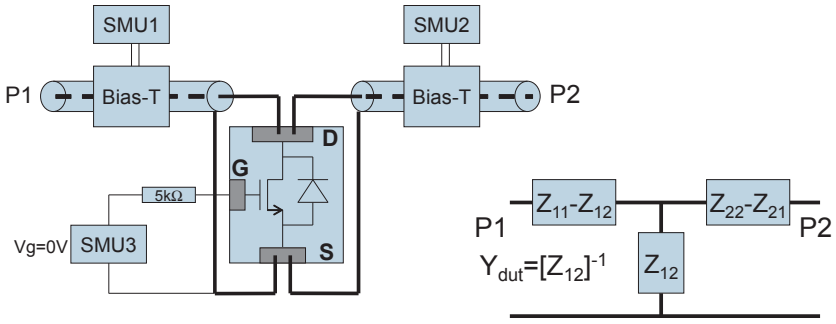

Fig. 11. Setup for MOSFET drain-source diode S-parameter measurement.

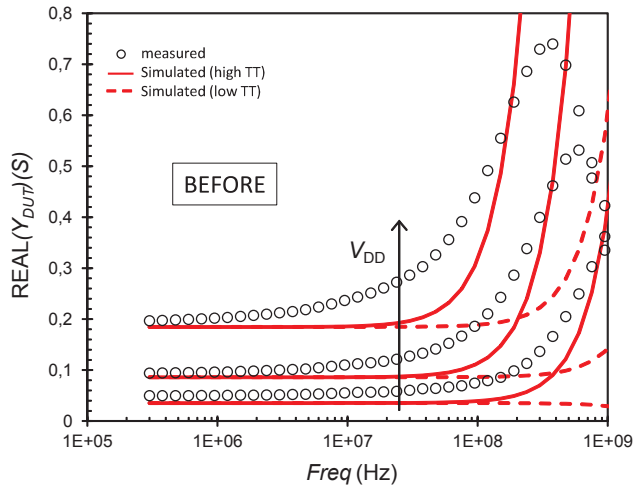

Fig. 12. Measured data vs. simulation BEFORE implementation of new behavioral model: Real part of admittance of discrete power LDMOS parasitic drain-bulk diode. LDMOS gate width is 2.5 m, the applied V_{DD} is 0.7 V, 0.75 V and 0.8 V.

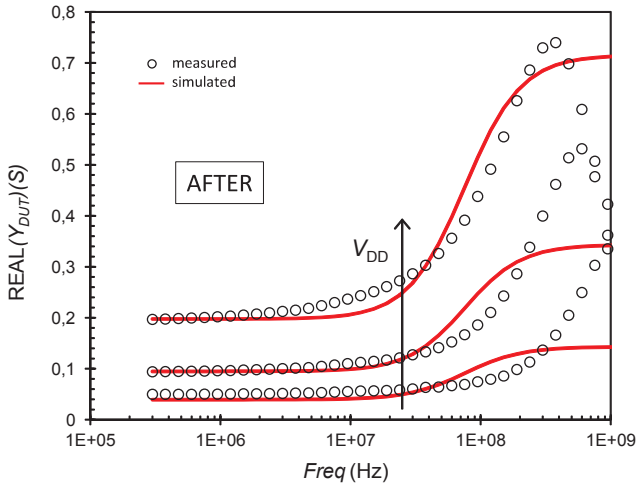

Fig. 13. Measured data vs. simulation AFTER implementation of new behavioral model: Real part of admittance of discrete power LDMOS parasitic drain-bulk diode. LDMOS gate width is 2.5 m, the applied V_{DD} is 0.7 V, 0.75 V and 0.8 V.

difficult to measure transient of diode switching from on to off state. In such a case the measurement of S-parameters of twoport using the network analyzer can be used as an alternative.

The disadvantage of this method is current and voltage limitation of the network analyzer, the need for a of special ground-signal or ground-signal-ground test structures and a more difficult parameter extraction, especially difficult differentiation between parameters τ and T_M. The advantage is less noisy measured data in some cases and an easy separation of measurements in various bias points and their potential

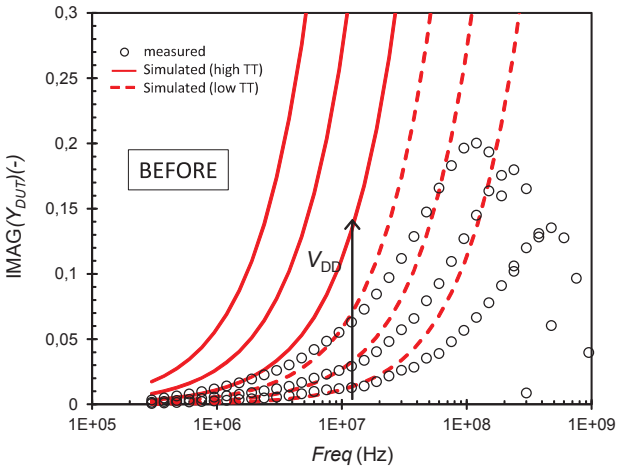

Fig. 14. Measured data vs. simulation BEFORE implementation of new behavioral model: Imaginary part of admittance of discrete power LDMOS parasitic drain-bulk diode. LDMOS gate width is 2.5 m, the applied V_{DD} is 0.7 V, 0.75 V and 0.8 V.

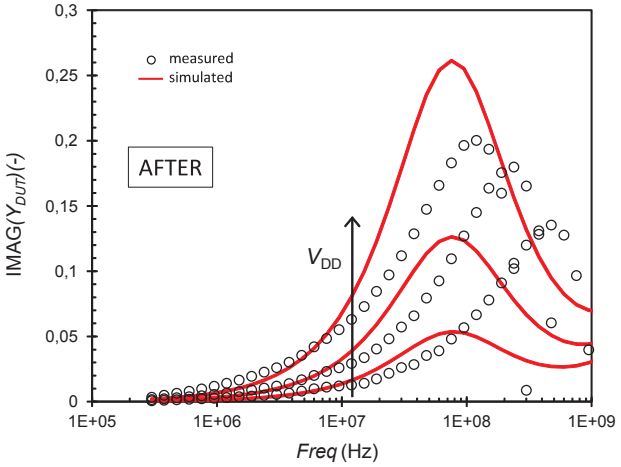

Fig. 15. Measured data vs. simulation AFTER implementation of new behavioral model: Imaginary part of admittance of discrete power LDMOS parasitic drain-bulk diode. LDMOS gate width is 2.5 m, the applied V_{DD} is 0.7 V, 0.75 V and 0.8 V.

customization and parametrization in the model.

4. Model parameter extraction

The final model is compatible with the standard SPICE diode [16] implemented in common SPICE simulator as *level*1. Table 1 demonstrates the key model parameters of published model having the same meaning like in *level*1 model. Therefore also the model parameter extraction is the same.

The main difference of the model parameter set in Table 1

Table 1
Set of basic tunable model parameters.

Parameter	Description	Unit	Default
AREA	Area factor	–	1
I_S	Saturation current	A	10^{-14}
n	Emission coefficient	–	1
C_j	Zero-bias junction capacitance	F	0
M_j	Grading coefficient	–	0.5
V_j	Junction potential	V	1
T_M	Diffusion transit time	sec	10^{-12}
τ	Minority carrier lifetime	sec	10^{-12}
R_S	Series resistance	Ω	0
I_K	High-injection knee current	A	1
T_{nom}	Nominal model temperature	K	300
T	Absolute model temperature	K	300
X_{TI}	Saturation current temperature exponent	–	3
E_G	Band-gap energy	eV	1.11
T_{RS}	Temperature coefficient of series resistance	1/K	0

comparing to model parameter set in [16] is, that the *level*1 SPICE parameter transit time T_T has been replaced by two new parameters diffusion transit time T_M and minority carrier lifetime τ.

The transfer of *level*1 to the published behavioral model containing the reverse recovery effect is therefore very simple. The two new parameters T_M and τ can be simply extracted from the measured transient characteristics containing reverse recovery effect demonstrated in Fig. 5 or Fig. 6.

Due to the simplicity, this publication does not focus to the model details contained in *level*1 as for example area vs perimeter vs length/width scaling or modeling of parasitic metal capacitor. Therefore Table 1 contains only the key model parameters, related to the published reverse recovery effect.

5. Comparison with SPICE compact models containing reverse recovery effect

The main reason of developing our Verilog-A diode model was the lack of diode SPICE compact model containing reverse recovery. The first prototype of the model was developed in cooperation with prof. Lauritzen from the University of Washington [1] and the Verilog-A code was placed in the University of Washington web pages.

However, during the time the new compact diode models containing reverse recovery as for example hisim_diode or diode_cmc appeared in some SPICE simulators. Our concept was to make the diode model compatible with the original SPICE diode model [16] to allow the simple transfer of the standard diode SPICE model to the new model only by adding the reverse recovery effect using two simple model parameters. Diode_cmc has completely different set of model parameters, so our interest for the below described model-to-model comparison was focused to the comparison of our Verilog-A diode model with HiSim diode model, in Spectre simulator called hisim_diode.

Although the Spectre simulator has declared the HiSim reverse recovery model, actual simulations still ignore the parameters for the reverse recovery. So in this case for the model comparison only the simulator Eldo [21] was used.

Both our Verilog-A and compact HiSim model are based on similar source [1], so the same or very similar simulation results were expected. As it is demonstrated in Fig. 16, the simulated current pulses of HiSim model and published Verilog-A model are comparable, while the simulated current pulse of standard compact SPICE model does not contain reverse recovery effect.

However, as it is demonstrated in Fig. 17, in the area of high injection the HiSim diode model differs from next two models due to missing parameter knee current I_K. This area is calculated differently in

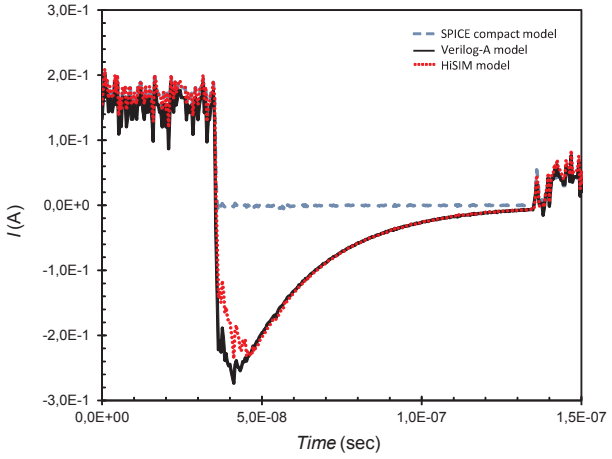

Fig. 16. Comparison with HiSim and standard level1 SPICE model – simulation of current response forward-to-reverse transient.

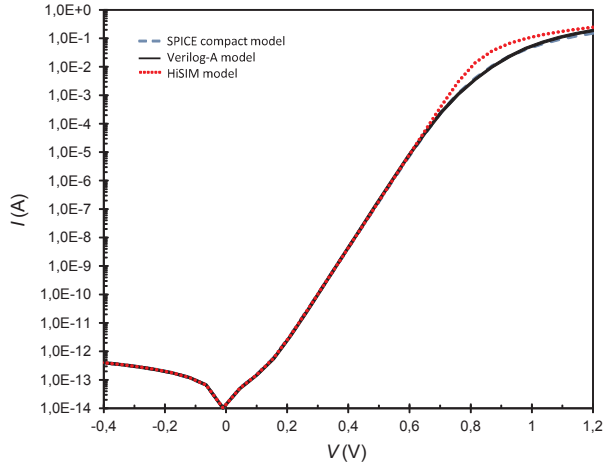

Fig. 17. Comparison with HiSim and standard level1 SPICE model – simulation of DC I-V characteristic.

HiSim model, while the published Verilog-A model uses the same equations like standard SPICE diode model [16] in this area.

So, although published Verilog-A model and HiSim model have comparable simulated results for low current, for high forward current the published Verilog-A model follows the original standard SPICE diode model and can be used for simple adding reverse recovery effect to already existing extracted SPICE model. Moreover, it should be pointed out that only the models based on I_K (as our Verilog-A one) define the diode high-current area correctly (on principle).

6. Conclusion

The complex robust temperature and area scalable Verilog-A model of diode containing reverse recovery effect has been presented.

The model can be used as stand-alone 2-terminal diode or as a parasitic p-n junction of more complex lumped macro-model, e.g. MOSFET, JFET, bipolar transistor or IGBT. Due to the implemented reverse recovery effect the model is useful especially for high-speed or high-voltage power devices. The model is simply applicable in all SPICE simulators supporting Verilog-A and its speed and convergence is comparable with the SPICE compact diode model without reverse recovery effect.

Two methods of model parameter extraction or model validation have been demonstrated – time domain pulse method and frequency domain S-parameter method.

The comparison with HiSim model demonstrated differences in high

injection area, where the published Verilog-A model uses the same concept as the basic diode model [16]. It was also presented, that the Verilog-A model is applicable even in the simulators where the HiSim compact model is not implemented yet.

Acknowledgements

This work was supported by ON Semiconductor company and by the Grant Agency of the Czech Technical University in Prague, Grant No. SGS16/164/OHK3/2T/13 and by the Technology Agency of the Czech Republic under the Grant No. TE01020186.

The authors would like to thank to Jan Míchal for his English proofreading and contribution after careful reading of the manuscript.

References

[1] Lauritzen PO, Ma CL. A simple diode model with reverse recovery. IEEE Trans Power Electron 1991;6(2):188–91.
[2] Ma CL, Lauritzen PO, Sigg J. Modeling of power diodes with the lumped-charge modeling technique. IEEE Trans Power Electron 1997;12(3):398–405.
[3] Ma CL, Lauritzen PO. A simple power diode model with forward and reverse recovery. IEEE Trans Power Electron 1993;8(4):342–6.
[4] Kang I, Kim S, Bahng W, Joo S, Kim N. Accurate extraction method of reverse recovery time and stored charge for ultrafast diodes. IEEE Trans Power Electron 2012;27(2):619–22.
[5] Drozdovski N, Drozdovskaia L, Caverly R, Quinn M. Modeling the zero and forward bias operation of PIN diodes for high-frequency applications. Solid-State Electron 2002;46(11):2001–8.
[6] Cappelluti F, Bonani F, Furno M, Ghione G, Carta R, Bellemo L, et al. Physics-based mixed-mode reverse recovery modeling and optimization of Si PiN and MPS fast recovery diodes. Microelectron J 2006;37(3):190–6.
[7] Sauter M, Simbürger W, Johnsson D, Stecher M. On-wafer measurement of the reverse-recovery time of integrated diodes by transmission-line-pulsing (TLP). Microelectron Reliab 2011;51(8):1309–14.
[8] Rajagopal K, Concannon A, Hower P, Farbiz F, Salman A, Arch J, et al. Investigation of reverse recovery effects on the SOA of integrated high frequency power transistors. In: Reliability physics symposium (IRPS), 2016 IEEE international. IEEE; 2016. p. 6A-3.
[9] Khorasani AE, Griswold M, Alford T. Gate-controlled reverse recovery for characterization of LDMOS body diode. IEEE Electron Device Lett 2014;35(11):1079–81.
[10] Elferich R, Lopez T. Impact of gate voltage bias on reverse recovery losses of power MOSFETs. In: Applied power electronics conference and exposition, 2006. APEC'06. Twenty-first annual IEEE. IEEE; 2006. p. 6.
[11] Reiter T, Polenov D, Probstle H, Herzog H-G. Optimization of PWM dead times in DC/DC-converters considering varying operating conditions and component dependencies. In: Power electronics and applications, 2009. EPE'09. 13th European conference on. IEEE; 2009. p. 1–10.
[12] Polenov D, Reiter T, Baburske R, Probstle H, Lutz J. The influence of turn-off dead time on the reverse-recovery behaviour of synchronous rectifiers in automotive DC/DC-converters. In: Power electronics and applications, 2009. EPE'09. 13th European conference on. IEEE; 2009. p. 1–8.
[13] FitzPatrick D, Miller I. Analog behavioral modeling with the Verilog-A language. Springer Science & Business Media; 2007.
[14] Sagdeo V. The complete Verilog book. Springer Science & Business Media; 2007.
[15] Massobrio G, Antognetti P. Semiconductor device modeling with SPICE. 2nd ed. New York: McGraw-Hill; 1993.
[16] Vladimirescu A. The SPICE book. John Wiley & Sons, Inc.; 1994.
[17] Gildenblat GS. Compact modeling: principles, techniques and applications. Springer Science & Business Media; 2010.
[18] McAndrew CC, Coram GJ, Gullapalli KK, Jones JR, Nagel LW, Roy AS, et al. Best practices for compact modeling in Verilog-A. IEEE J Electron Devices Soc 2015;3(5):383–96.
[19] Nalwa HS. Silicon-based material and devices, two-volume set: materials and processing, properties and devices, vol. nalwa2001silicon. Academic Press; 2001.
[20] Frickey DA. Conversions between S, Z, Y, H, ABCD, and T parameters which are valid for complex source and load impedances. IEEE Trans Microwave Theory Tech 1994;42(2):205–11.
[21] Eldo Device Equations Manual. Release 16.2. Mentor Graphics Corporation; 2016.