ULTRASONIC TREATMENT EFFECTS ON $CuS_{1.8}$ – CdSe STRUCTURES

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Ultrasound (US) is established to affect properties of II-VI semiconductors[1,2]. However to the best of our knowledge, there have not reports on US influence on II-VI–based solar cells, whereas similar effects are detected in other barrier structures[3]. Our work has focused on the modification by US treatment (UST) of electrical properties of $CuS_{1.8}$ – CdSe thin film photodetector. The longitudinal waves (8.4 MHz) were used for UST. The current-voltage (*I-V*) characteristics were measured over a temperature range 290-340 K both before and after UST. The fitting were done by using differential evolution method.

The following expression, which is expected for recombination–tunneling currents in the investigated strusture[4], is used for a forward *I-V* characteristics fitting:

$$I = I_0 \exp[\alpha(V - IR_s)] + (V - IR_s)/R_{sh}, \quad (1)$$

where $I_0 = I_{00}\exp(\beta T)$ is the saturation current, R_s and R_{sh} are the series and shunt resistances, the factor α does not depend on the voltage. The extracted temperature dependences of parameters are shown in Fig. 1. In particular, it was ascertained, that R_s is thermoactivated ($R_s = R_{s0}\exp(-E_R/kT)$) and R_{sh} is described by dislocation–induced impedance theory[5]. It was found out that UST had led to change of α, β, and R_s as well as R_{sh} activation energy. The sample room temperature (RT) storage results in

complete recovery of both α and R_{SH} value, but acoustically induced (Al) residual both series resistance increase and saturation current decrease are observed.

The analysis has shown that reverse branch of *I-V* characteristics is determined by trap-assisted tunneling (TAT) at low bias (V > -0.8 V) and by trap-charge limited current (TCLC), which is induced by energetically exponentially distributed defects, at high bias (V < -2.5 V). The TAT current can be described[6] as

$$I_{TAT} = I_{TAT,0} \frac{(V_d - V)}{E_t} \exp\left(- \frac{8\sqrt{\varepsilon\varepsilon_0 m^*} E_t^{3/2}}{3q\hbar\sqrt{qN_D(V_d - V)}} \right), \quad (2)$$

where $I_{TAT,0}$ is proportional to the trap density, V_d is the built in voltage due to the band bending, E_t is the position of the trap in the band gap, the N_d and ε are the donor density and the dielectric constant of CdSe. The power low

$$I_{TCLC} = I_{TCLC,0} V^m \quad (3)$$

was used to TCLC current fitting. In this case[7], power index m > 3 and $(m - 1) = T_c / T$, where T_c is the characteristic temperature parameter of the trap distribution and $I_{TCLC,0} = C\exp(-E_x / kT)$, where E_x is the activation energy that defines a finite Fermi level with free-charge carriers being emitted from low-lying filled traps.

The results, which are obtained from the reverse *I-V* characteristics, are shown in Fig. 2. As one can recognize, UST affects the energy characteristics of defects, which located both in space charge region (see Fig.2(a,b)) and in diode base (see Fig.2(c,d)). Thus E_x had decreased from 0.48 eV to 0.28 eV after UST immediately and E_t had risen

by 0.1 eV at same conditions. Al defect system disturbance disappears in p-n region practically completely and in the quasi-neutral region partly after RT storage.

On our opinion, the observed effects deal with the Al defect generation.

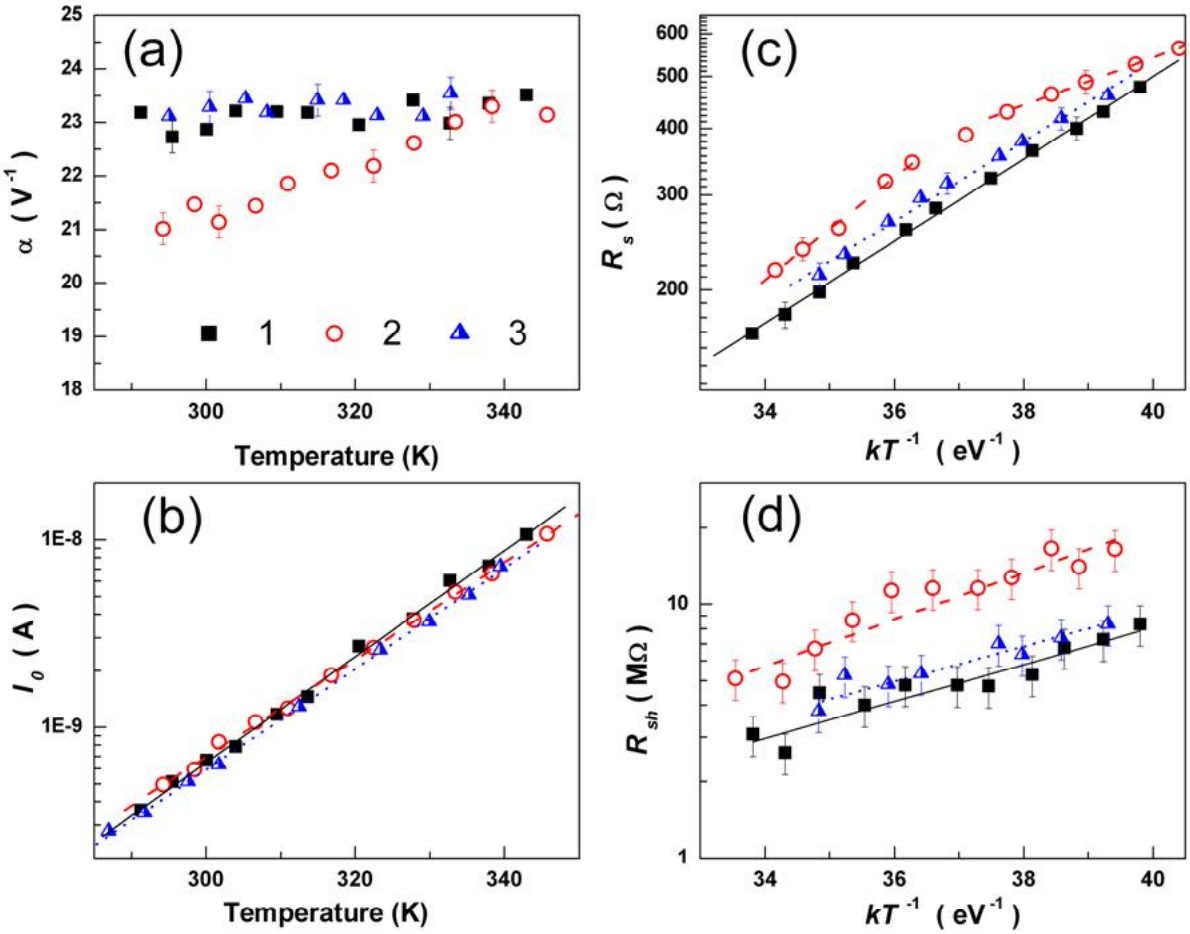

Figure 1. Temperature dependencies of parameters, which were determined from forward *I-V* characteristics. The measurements were taken before UST (curves 1, squares), immediately after UST (curves 2, circles), and after UST and ~75 h RT storage (curves 3, triangles).

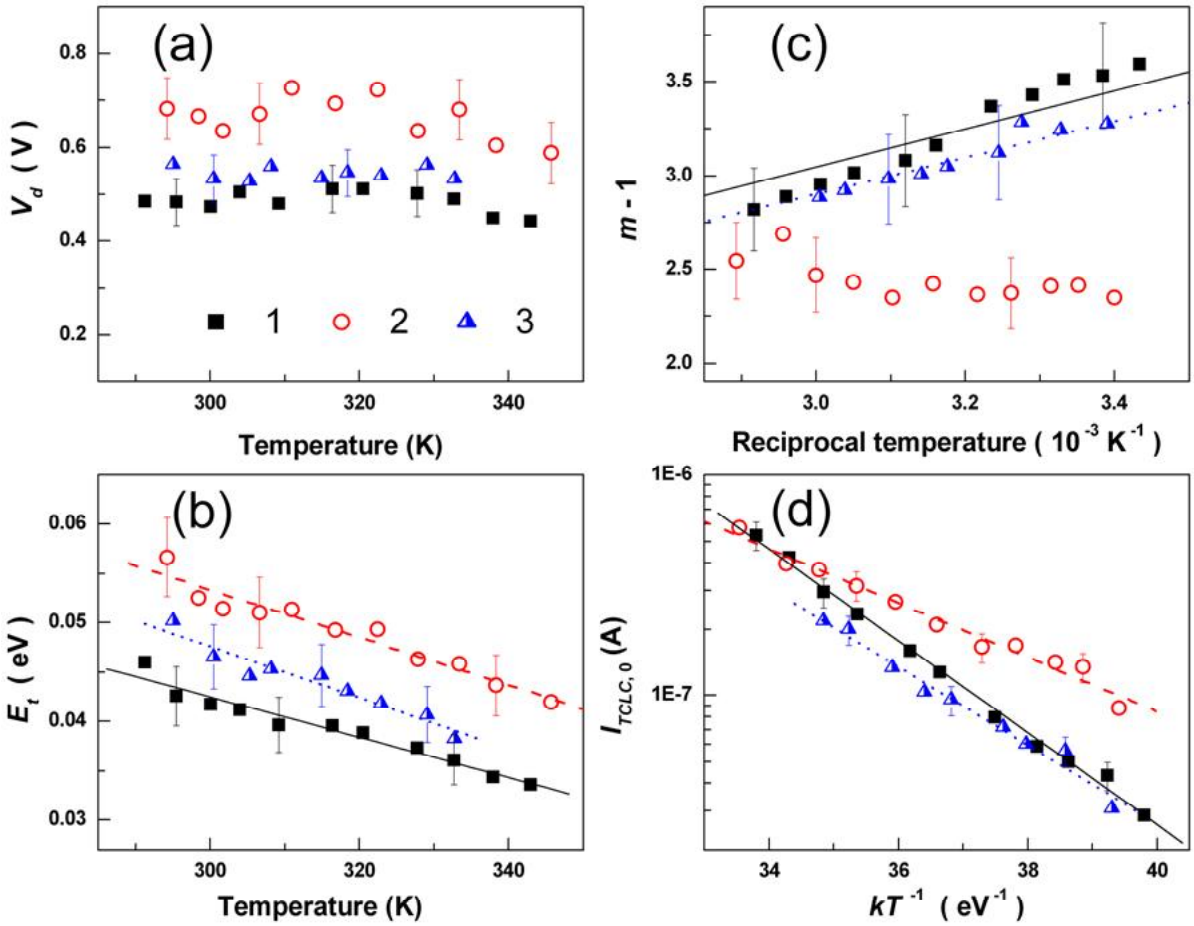

Figure 2. Temperature dependencies of TAT (a, b) and TLCL (c, d) parameters. The measurements were taken before UST (curves 1, squares), immediately after UST (curves 2, circles), and after UST and ~75 h RT storage (curves 3, triangles).

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