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n-Si–Organic Inversion Layer Interfaces: A Low Temperature Deposition Method for Forming a p–n Homojunction in n-Si

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Recent interest in hybrid solar cells has led to reports of above 11% efficiency in n-Si–polyethylene dioxythiophene–poly(styrene)sulfonate (PEDOT:PSS) solar cells.[1] PEDOT:PSS is a transparent, wide-bandgap, organic hole conductor with a relatively high work function, $\phi_m = 5.0$ eV.[2] Silicon-PEDOT:PSS hybrid devices have been described as either Schottky barrier solar cells,[3] where the highly conductive PEDOT:PSS serves as the metallic contact, or as p–n junction type devices, where PEDOT:PSS acts as the "p-type" layer, providing charge separation by its hole-selective nature.[4] Parsing the relative importance of these two device models in these junctions is crucial to narrowing future efforts at device improvement.

In a typical Schottky barrier junction, charge transfer between a high (low) work function metal in contact with an n-(p-)type semiconductor can form, across the barrier, a built-in voltage, $V_{bi} = \phi_m - E_F$, where E_F is the semiconductor Fermi energy. The barrier height, ϕ_b, determined from current–voltage measurements, is related to V_{bi} by $\phi_b = V_{bi} + |E_c - E_F|$, for an n-type semiconductor–metal junction (**Figure 1**a). It follows from analysis of Figure 1 that, if V_{bi} exceeds a critical value, $V_{bi} > |E_F - E_i|$, where E_i is the intrinsic Fermi level, the majority carrier at the surface of the semiconductor is of opposite type to that in the bulk, generating a p–n junction without the need for dopant diffusion. This process is known as inversion and the p-type layer, in our example, as an inversion layer, which is generated by the large work function difference between the metal and semiconductor. Strong inversion occurs when the concentration of carriers in the inversion layer exceeds the dopant concentration in the bulk, at $V_{bi} > 2|E_F - E_i|$ (Figure 1a). The fundamental difference between a standard Schottky-type solar cell with a barrier height resulting in depletion at the surface, and an inversion layer solar cell is the existence of a p–n junction within the semiconductor itself, leading to transport that is dominated by what are the minority carriers in the bulk of the material, regardless of the type of contact. In the strong inversion regime, the low bulk majority carrier density at the semiconductor surface prevents recombination at defects at the interface with the inversion-inducing contact, and the high bulk minority carrier density improves screening of donor ion impurities. While a device operating in strong inversion is less sensitive to interface defects than a Schottky barrier or weak inversion device, a large defect density at the interface can actually prevent inversion from forming, due to Fermi level pinning (Figure 1b).[5]

Silicon–metal junctions do not typically form inversion layers, due to Fermi level pinning, which limits V_{bi} to approximately $E_g/2$ (Figure 1b).[5] Inversion layer solar cells have been demonstrated, instead, in Si-oxide systems,[6] in amorphous Si/crystalline Si HIT devices,[7] and in Si-electrolyte systems,[8] yielding high open-circuit voltage, V_{oc}, values in devices based on these concepts. In the case of HIT cells, V_{oc} reaches 700 mV for a c-Si substrate with doping concentration of 5×10^{15} cm^{-3}.[7] However, a simple, low-cost method for forming an inversion layer in a Si-based solid state device is lacking. Identifying such a method can open doors in Si device processing, with implications beyond photovoltaic devices.

For PEDOT:PSS–n-Si junctions, the low-temperature processing has the potential to prevent formation of the interface defects that plague Si-metal junctions, avoiding Fermi level pinning and allowing large barrier heights. Another advantage of the low temperature processing is the stability of molecular passivation layers, such as methyl termination,[9] to deposition conditions. Additionally, a thin oxide passivation layer has been found to slightly enhance solar cell performance over H-terminated devices,[10] suggesting some improvement in surface passivation is possible for certain device conditions. Indeed, relatively high open-circuit voltages have been reported, reaching 610 mV for substrates with $N_D = 6 \times 10^{15}$ cm^{-3} when the Si surface was passivated with SiO_x.[10] While this is slightly less than the V_{oc} reached in HIT inversion layer devices for similar N_D, it is high enough to suggest that the Si has been pushed to inversion. Additionally, V_{bi} values indicative of inversion have been reported in the past, but they were not identified as such, and the implications were not discussed.[11] In a recent review article[3a] we suggested that these devices operate in inversion, but we did not have experimental evidence of strong inversion.

The key distinction between an inversion layer model and a charge-selective electrode model is the role of the top contact. In an inversion layer device, charge separation has already occurred within the (n-type) semiconductor, because the surface is inverted (p-type). Charge selectivity of the contact is not necessary for device operation, as the p–n junction created in the semiconductor has already done the job. Within this model, a charge-selective electrode can further improve device performance by reducing recombination, as even a device operating in strong inversion can have some carrier density of both types

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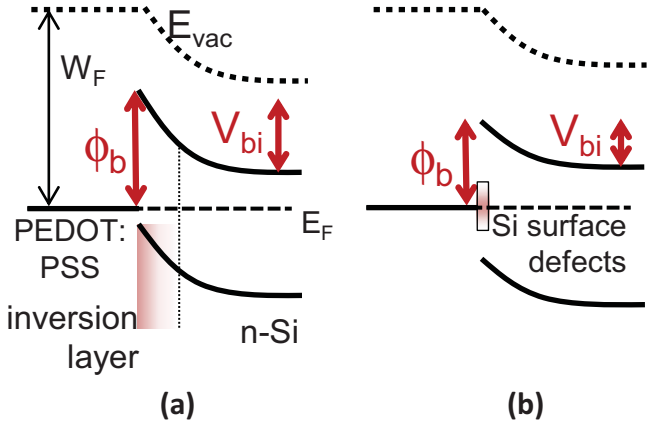

Figure 1. Energy band diagram for a) an inversion layer formed between PEDOT:PSS and n-type Si and b) the energy band alignment that results with a significant number of defects at the Si–contact interface.

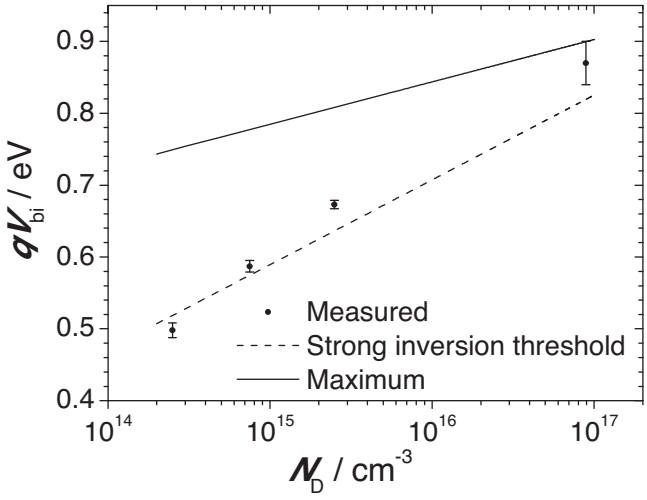

Figure 2. V_{bi} (circles), vs. N_D for the devices shown in figure 1. Both V_{bi} and N_D were calculated from A^2/C^2 vs. V curves. Error bars represent the standard deviation of measurements on three devices each. The threshold value of V_{bi} where strong inversion sets in (dashed line), and the maximum possible V_{bi} (solid line) were calculated as described in the main text.

at the surface. Within an inversion-layer model, further device improvements should focus on increasing the magnitude of V_{bi}, by pushing the semiconductor further into inversion, where charge separation is more efficient and the density at the surface of what are majority carriers in the bulk is smaller, leading to less recombination. This is done by improving interface passivation, or by modifying the work function of either the semiconductor or the inverting contact, rather than by focusing on band alignment at the interface.

Here, we use the PEDOT:PSS–n-Si system, and present results of capacitance–voltage ($C(V)$) measurements to determine V_{bi}, and analyze current–voltage ($J(V)$) curves to extract ϕ_b. Both of these methods demonstrate inversion in n-Si–PEDOT:PSS contacts for all substrate doping concentrations investigated, reaching strong inversion for substrate doping concentrations above 2.5×10^{14} cm^{-3}. We conclude that PEDOT:PSS induces strong inversion in Si, forming a p–n junction using only low temperature solution processing. Finally, we show that we can use this inversion layer to measure effective mobility of p-channel Si FETs, with Al_2O_3 gate dielectric and inversion layer source and drain electrodes created by the PEDOT:PSS contacts using only simple, low-temperature processing methods that can be done in almost any laboratory. This provides evidence of the general utility of this method of forming inversion in Si. Solar cell devices, presented in supporting information, show 10.4% power conversion efficiency, indicating that these junctions are representative of those presented in the literature.[1,4]

The built-in voltage, V_{bi} was determined from $C(V)$ profile measurements on small-area samples. For all devices measured, plots of A^2/C^2 vs. V, where A is the device area, show linear behavior from the lowest voltage measured, –1.5 V, to above 0.25 V, as shown in the supporting information. The silicon substrate donor concentration, N_D, was calculated from the slope of a plot of A^2/C^2 vs. V, according to the equation

$$\frac{1}{N_D(W_D)} = \frac{qK_s\varepsilon_0}{2}\frac{d\left(\frac{A^2}{C^2}\right)}{dV} \quad (1)$$

where W_D is the depletion width, q is the electron charge, $K_s = 11.68$ is the dielectric constant of Si, and ε_0 is the permittivity of free space.[13] V_{bi} was taken as the value where $W_D = K_s\varepsilon_0 A/C = 0$.[13] In all cases, the value of N_D calculated in this way matched the range given by the wafer supplier. The built-in voltage for all samples investigated is shown in **Figure 2**, compared to both the threshold value for strong inversion, V_{bi}(threshold) = $2(E_F - E_i)$, and the maximum theoretical value, V_{bi}(max) = ϕ_m(PEDOT) – E_F(Si), where E_F(Si) is determined by N_D, which is calculated from $C(V)$ data as described above. For all but the lowest N_D measured, V_{bi} exceeds the threshold for strong inversion, and for samples with the highest N_D, it reaches 90% of V_{bi}(max).

The results of $J(V)$ measurements in the dark for the same small area devices investigated in $C(V)$ measurements are shown in **Figure 3**. Excellent rectification is observed for higher doping devices, where strong inversion is expected. However, for the device with $N_D = 2.5 \times 10^{14}$ cm^{-3}, an increased reverse bias current and weaker rectification is found. This is consistent with weaker inversion and lower V_{bi}, as demonstrated in the above $C(V)$ results.

For higher doping substrates, where strong inversion is found, three regimes are apparent in the forward bias region of the log(J) vs. V curves shown in Figure 3. Above 0.6 V, series resistance dominates. In the 0.4–0.6 V region linear behavior is observed, and below 0.4 V, excess recombination current is apparent resulting in an increase in log(J) above the linear extrapolation. In a p–n diode model, this excess dark current at low forward bias can be attributed to recombination in the space-charge region.[12] The barrier height, ϕ_b, was determined from these $J(V)$ plots in the 0.4–0.6 V region, where this excess recombination current is not a factor, according to the relation

$$J = A^* T^2 e^{-q\phi b/nkT}\left(e^{qV/nkT} - 1\right) \quad (2)$$

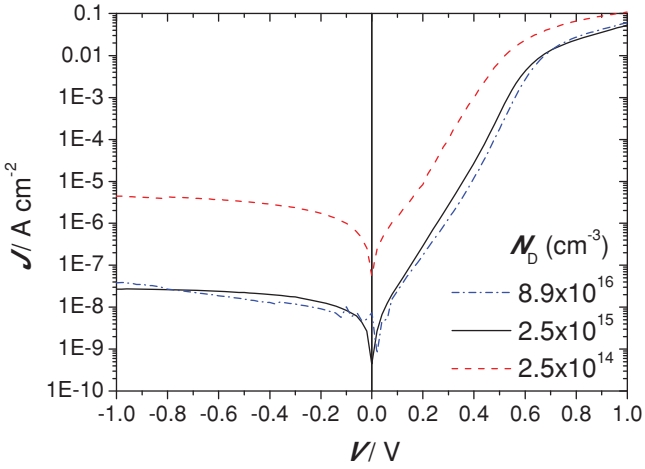

Figure 3. Current–voltage curves in the dark for the same devices as those measured by $C(V)$. Each curve represents an average of two ($N_D = 8.9 \times 10^{16}$ cm^{-3}) or three (all others) devices.

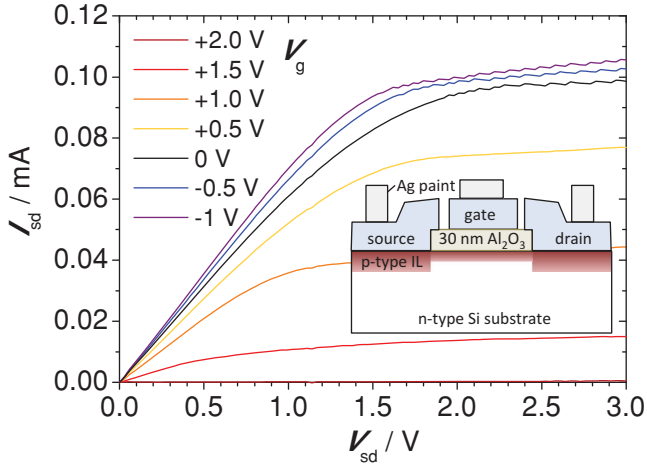

Figure 4. Results of measurements on transistor test devices, used to determine mobility in the channel under the Al_2O_3 gate dielectric. I_{sd} is shown as a function of V_{sd}, for different values of V_g. Leakage current has been subtracted uniformly. The inset shows a schematic of the device, where source, gate, and drain electrodes, shown in blue, are all PEDOT:PSS.

where $A^* = 112$ A m^{-2} K^{-2} is the Richardson's constant for Si, and k is the Boltzmann constant.[12] Fits to the linear region of ln(J) vs V yielded the values for ϕ_b shown in **Table 1**, with the ideality factor, n, ranging from 1.4 to 1.7. These results match well with the relation $\phi_b = V_{bi} + |E_c - E_f|$, with V_{bi} measured by $C(V)$, and $|E_c - E_f|$ calculated from N_D, which was determined from the $C(V)$ profile. This presents a consistent picture of strong inversion for samples with $N_D > 2.5 \times 10^{14}$ cm^{-3}.

As an additional demonstration of the utility of a spin-on, inversion layer-inducing compound, we prepared inversion layer source and drain electrodes for Al_2O_3 gate dielectric p-channel FETs using the n-Si-PEDOT:PSS junction (inset to **Figure 4**). We then used this device to measure the mobility of holes in the channel. Results of measurements of source-drain current, $I_{sd}(V_{sd})$, for increasing values of gate voltage, V_g, are shown in Figure 4. For these devices, a large leakage current was found, which is likely due to poorly optimized device geometry and allowed significant current to flow under the Al_2O_3 gate dielectric, but around the gate contact, even when the channel was nominally closed. This leakage current was subtracted for the data shown in Figure 4. Additionally, a passivating molecular monolayer[6a] was added to the contact, which was found to improve device results.

From these data, effective mobility, μ_{eff}, can be determined for each value of V_g, according to the equation

$$\mu_{eff} = \frac{Lg_d}{WC_{ox}(V_g - V_T)} \quad (3)$$

where L and W are the channel length and width, respectively, g_d is the drain conductance, given by $g_d = \partial I_{sd}/\partial V_{sd}|_{V_g}$, and $C_{ox} = 4.1(3) \times 10^{-7}$ F cm^{-2} is the oxide capacitance, [12] measured for this Al_2O_3 layer by $C(V)$.[5a] Because of high negative interface charge density in the Al_2O_3-Si interface,[13] an inversion layer is already present at $V_g = 0$, and the device operates in depletion mode. It is therefore possible to measure the effective mobility in the channel at $V_g = 0$. Two different substrate donor concentrations were investigated. For $N_D = 5 \times 10^{13}$ cm^{-3}, $\mu_{eff} = 95(3)$ cm^2 V^{-1} s^{-1}, and for $N_D = 6 \times 10^{14}$ cm^{-3}, $\mu_{eff} = 49(4)$ cm^2 V^{-1} s^{-1}, with $V_g = 0$ in both cases. These values are consistent with effective mobilities measured in p-channel Si-based FETs, which are typically less than 150 cm^2 V^{-1} s^{-1}.[11] Additionally, the increase in mobility with lower N_D value is consistent with previous findings of stronger inversion for lower N_D in Al_2O_3–n-Si junctions.[5a] This quick and easy deposition of p-type contacts, using an inversion layer induced by PEDOT:PSS, is thus a useful tool for many laboratory measurements that would otherwise require expensive or time-consuming processing to complete.

We have presented evidence that PEDOT:PSS–n-Si junctions operate in strong inversion over a wide range of Si substrate doping densities. We conclude that the primary driver of charge separation in these devices is the internal electric field in the Si, itself, and that charge-selectivity of the contact is not necessary, as the majority carriers at the Si surface are already holes. These findings should influence the future direction of research into Si hybrid solar cells towards improving interface passivation and work function modification, to increase band bending and improve carrier extraction. Additionally, the PEDOT:PSS–n-Si system provides a simple laboratory tool for making p–n junctions in Si at low temperature, using only spin-coating methods. This is the first demonstration of an

Table 1. Results of fits to Equation (2) in the linear region of ln(J) vs V, yielding ϕ_B, compared to V_{bi} extracted from $C(V)$, and the theoretical relation, $\phi_B = V_{bi} + |E_c - E_F|$. Error values represent the standard deviations of fits to each individual sample.

N_D [cm^{-3}]	ϕ_B [eV]	V_{bi} [eV]	$V_{bi} + \|E_c - E_F\|$ [eV]
8.9×10^{16}	1.0(3)	0.86(3)	1.0(3)
2.5×10^{15}	0.91(2)	0.67(1)	0.91(1)
2.5×10^{14}	0.83(3)	0.50(1)	0.80(1)

inversion layer in Si that is generated by solution deposition at room temperature. The general utility of this was demonstrated by measuring effective mobility in a p-channel FET using an Al_2O_3 gate dielectric, using the PEDOT:PSS–generated inversion layer source and drain electrodes.

Experimental Section

Single-side polished (for resistivity 0.05–0.1 and 1–20 Ω cm) or double-side polished (for resistivity 1–4 and 20–60 Ω cm), 400–500 µm thick, phosphorus-doped, Czochralski-grown, (100)-oriented single crystal silicon wafers were prepared by degreasing with organic solvents, followed by oxidizing in oxygen plasma, etching 1 minute in 2% HF solution, oxidizing in plasma again, and finally etching 1 min in 2% HF to prepare Si-H termination. PEDOT:PSS (Heraeus PH510), diluted with water (25% v/v) and doped with ethylene glycol (7 wt%) and zonyl (0.5 wt%) surfactant, was deposited by spin-coating at 1000 RPM, then annealed 30 min at 150 C in inert environment, to prepare a 70 nm thick film. Indium-gallium eutectic was used as a back contact.

For $C(V)$ and dark $J(V)$ measurements, small area devices (0.04–0.09 cm^2) were scribed mechanically, and contact was made to the PEDOT:PSS using a hanging mercury electrode. Both $C(V)$ and $J(V)$ were measured using a Keithley 4200-SCS. $C(V)$ was measured at 100 kHz applied frequency.[11] A simple parallel capacitor and resistor model was used to interpret the data, after series resistance in the wires was compensated for by the instrument.

Transistors were made using (111)-oriented single-side polished n-type wafers, with 30 nm Al_2O_3, deposited by plasma-ALD, as described previously.[5a] In this case, the use of (111) orientation was chosen for improved Al_2O_3 passivation quality, as was found experimentally. The gate was masked with a narrow piece of Kapton tape, and the device was etched 10 min in 40% NH_4F that had been degassed by bubbling with nitrogen, then oxidized in a plasma asher, and etched in NH_4F again. In this case, a passivating molecular monolayer of ethylene toluene was found to improve performance, possibly due to the low substrate doping used for the transistors, which, as was shown above, reduces the level of inversion. Ethylene toluene was deposited on the exposed electrodes, and PEDOT:PSS was deposited over the entire device by lift-off deposition.[5a] Source, drain, and gate electrodes were scribed from the PEDOT:PSS, and silver paint was used as a contact to each. Devices were measured in four-terminal configuration. Gate leakage current was 20 nA at 1 V, and source-drain leakage current was 1 µA at 1 V, with V_g = 2 V. The gate length was 1.15 mm and the width was 2.3 mm. As mentioned above, the large source-drain leakage is likely due to geometric factors in this unoptimized device structure, specifically conduction through the inversion layer already present under Al_2O_3 when V_g = 0, to the sides of the scribed gate electrode. This could not be avoided without moving to higher-level device processing, which was counter to the point of the exercise of demonstrating a simple tool for measuring μ_{eff}. In any case, this effect does not change with gate voltage, and can easily be subtracted. When the current measured at V_g = +2.5 V, where linear behavior is observed over the entire range of V_{sd}, was subtracted from all of the $I_{SD}(V)$ curves, the "on" state current showed saturation at high V_{sd}, as observed in Figure 4.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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