

Photoinduced Self-Gating of Perovskite Photovoltaic Cells in Ionic Liquid

Grigorii Verkhogliadov,[†] Abolfazl Mahmoodpoor,[†] Pavel Voroshilov, Ross Haroldson, Masoud Alahbakhshi, Albert G. Nasibulin, Sergey V. Makarov, and Anvar A. Zakhidov*



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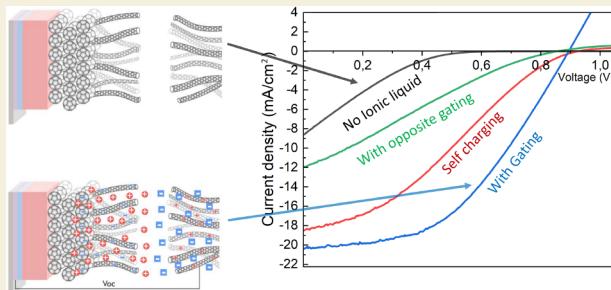
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ABSTRACT: We demonstrate that the power conversion efficiency (PCE), photocurrent, and fill factor (FF) of perovskite solar cells (PSC) can be significantly improved by the photoinduced self-gating in ionic liquids (ILs) via n-doping of the carbon nanotube (CNT) top electrode on the fullerene electron transport layer (ETL). CNTs, graphene, and other carbon electrodes have been proven to be stable electrodes for PSC, but efficiency was not high. We have previously shown that the performance of PSCs with CNT electrodes can be improved by IL gating with gate voltage (V_g) applied from an external power source. Here we demonstrate that effective self-gating in ILs is possible by a photoinduced process, without an external source. The open circuit voltage (V_{oc}) generated by the PSC itself can be applied to the CNT/C₆₀ electrode as V_g leading to photogating. This self-gating with V_{oc} is compared to photocharging of CNTs in ILs without any gating for two types of fullerene ETLs: C₆₀ and C₇₀. Two types of ILs, DEME-TFSI and BMIM-BF₄, are tested for two types of nanotubes electrodes: single wall (SWCNT), and multiwall (MWCNT). The resulting improvements are analyzed using the effective diode-circuit (DC) and the drift-diffusion (DD) models. Self-gating allows the PCE improvement from 3–5% to 10–11% for PSCs with a thick ETL, while for optimal combination of a thin SWCNT/ETL with added layers for improved stability, the PCE reached 13.2% in DEME-TFSI IL.



KEYWORDS: carbon nanotube electrode, work function tuning, ionic liquid gating, ionic liquid, perovskite photovoltaic, solar cell

1. INTRODUCTION

Organic–inorganic halide perovskites are a highly promising material for a variety of optoelectronic applications, including solar cells (SCs), light-emitting diodes (LEDs), and photodetectors (PDs), due to their remarkable properties such as a high absorption coefficient, narrow spectral emission line, and tunable bandgap. In the past decade, the efficiency of perovskite SCs has significantly increased from 3% to over 25%, which is now comparable to that of the best silicon SCs.^{1–4} To further improve the performance of these devices, ongoing research is focused on optimizing the device architecture, transport layers, and electrode selection.⁵

Ionic liquids (ILs) have been identified as a promising additives to enhance device performance.^{6–9} ILs can be used to dope transport layers, improving their conductivity and reducing hysteresis in final SC devices.¹⁰ Alternatively, direct doping of perovskite layers with various ILs has been shown to passivate defects and improve SC performance.^{11–13} In addition, some ILs can increase grain size and quality, which further improves device performance while also protecting perovskites from decomposition in humid environments since they are usually deposited on grain boundaries.^{14–16} Moreover, to passivate the perovskite layer, an IL can be deposited as a separate layer on top of the perovskite, which both passivates

surface defects and improves the energy-level alignment at the interface between the perovskite and the adjacent layer.^{17,18}

Ionic liquid gating (ILG) is a commonly used technique in transistors as it forms a double layer, resulting in a significant increase in capacitance.^{19–22} Similarly, ILG has been applied in organic photovoltaic (OPV) devices with CNTs as an electrode.^{23,24} In this approach, gating voltage is applied from an external source to dope the CNT electrode with ions from the ionic liquid. While CNTs have been used as both anode and cathode in perovskite photovoltaics,^{25–28} they also offer several advantages over traditional metal electrodes, including high transparency, low cost, and hydrophobicity, as well as superior stability.^{29–31} In our previous work, we successfully implemented ILG in perovskite photovoltaic devices using an external gate-source.³²

In this article, we present a novel architecture scheme that utilizes the ionic gating effect in PSC devices without requiring

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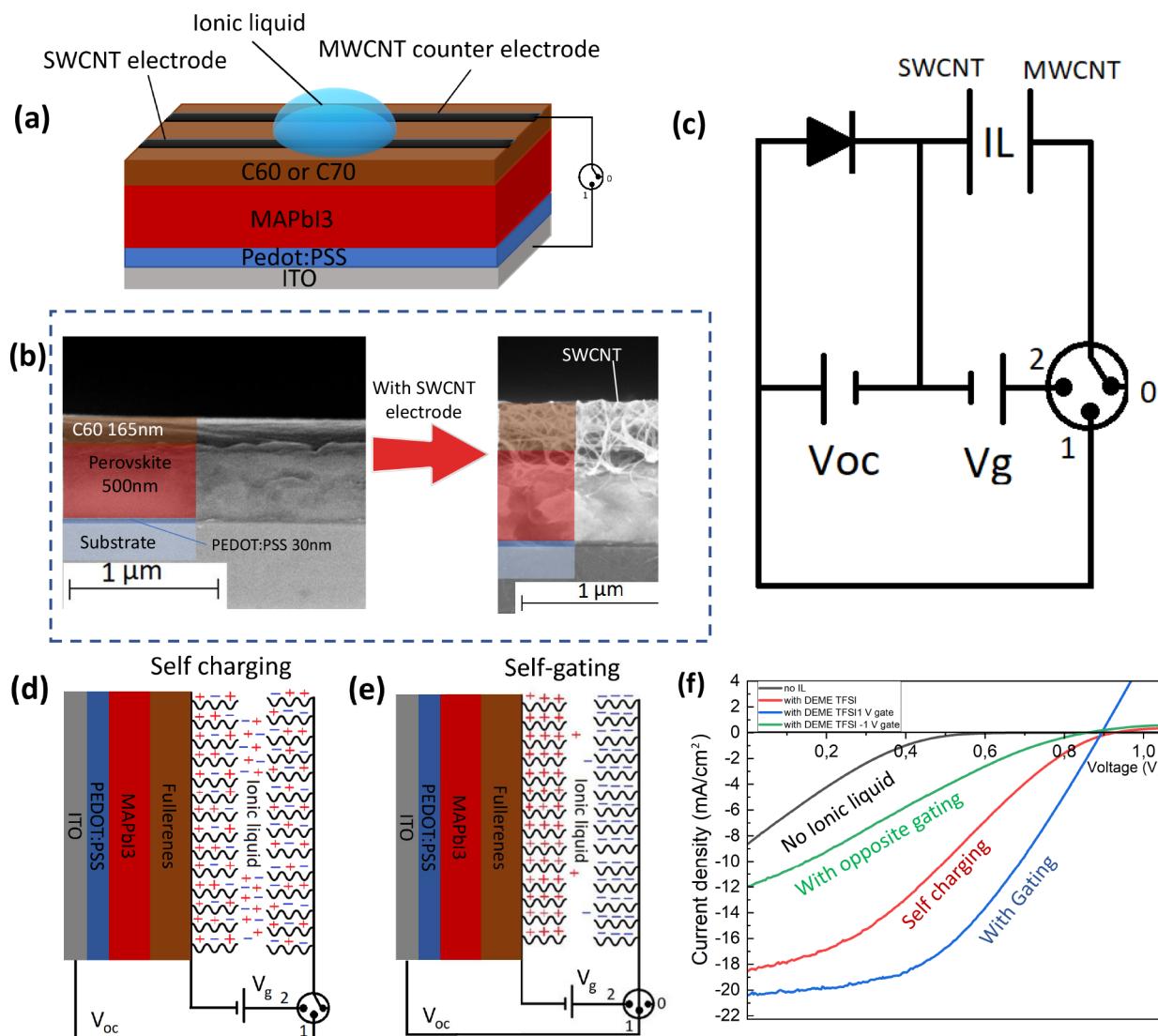


Figure 1. Device architecture with IL self-gating. (a) Schematic device architecture. (b) Cross-sectional SEM images of a device without and with an SWCNT layer on top. Perovskite layer thickness 500 nm; C₆₀ layer thickness about 165 nm. (c) Equivalent circuit of PSC. (d) Schematic operation of perovskite SC in the self-charging regime. (e) Schematic operation of perovskite SC in the self-gating regime. (f) Ionic gating effect on J-V curves of PSC with C₆₀ as ETL and 1 layer of SWCNTs as a top electrode.

a gate voltage from an external source. Specifically, the voltage applied to the gate in our devices is generated by the device itself as V_{oc} and is applied as a self-gating voltage to the CNT gate counter-electrode (CE) upon illumination of the PSC. To achieve this goal, we intentionally create a PSC with a thick ETL of fullerenes C₆₀ and C₇₀ coated with single-walled and multiwalled CNTs (SWCNT and MWCNT, respectively), which together play the role of a tunable electrode interface based on highly porous CNT sheets and robust fullerene ETL. It is well-known that thicker transport layers in organic SCs, if properly doped to achieve higher conductivity, allow for improvements in the stability of the SC. This argument has motivated the development of n- and p-type electronic doping methods, pioneered by Leo and co-workers,^{33–35} in order to decrease the series resistances of the ETL and HTL. From a technological standpoint, it is convenient to have an overall thicker SC to avoid pinholes and defect-related shorts in very thin PSC devices. Moreover, using thicker ETL in PSC also allows for the protection of the photoactive perovskite layers from degradation by the humid atmosphere, by "encapsulating"

the perovskite layer with a thicker n-doped ETL with low series resistance in thick fullerene. We achieve this n-doping via ion penetration into the porous CNT and modifying and improving the CNT/ETL interface (by passivating defects and trap states). They further penetrate into the fullerene layer by self-gating upon photoexcitation, as described in detail below.

In this study, we present an architecture similar to one recently described in our previous work.³² We then fabricate and characterize the internal p-i-n structure within the perovskite photoactive layer and the n-ETL/n-CNT interface controlled by a horizontal CNT ionic gate CE placed next to the PSC pixel. In this device, the high initial series resistance of the undoped thick ETL layer and the series resistance of the CNT electrode/ETL interface are reduced by ion accumulation from an IL upon exposure to sunlight. Our results demonstrate the effectiveness of the ionic self-gating as a low-photovoltage tool that can significantly improve the solar cell output parameters.

We compare the device structures with two types of fullerene ETLs, C₆₀ and C₇₀, in thicknesses ranging from 160

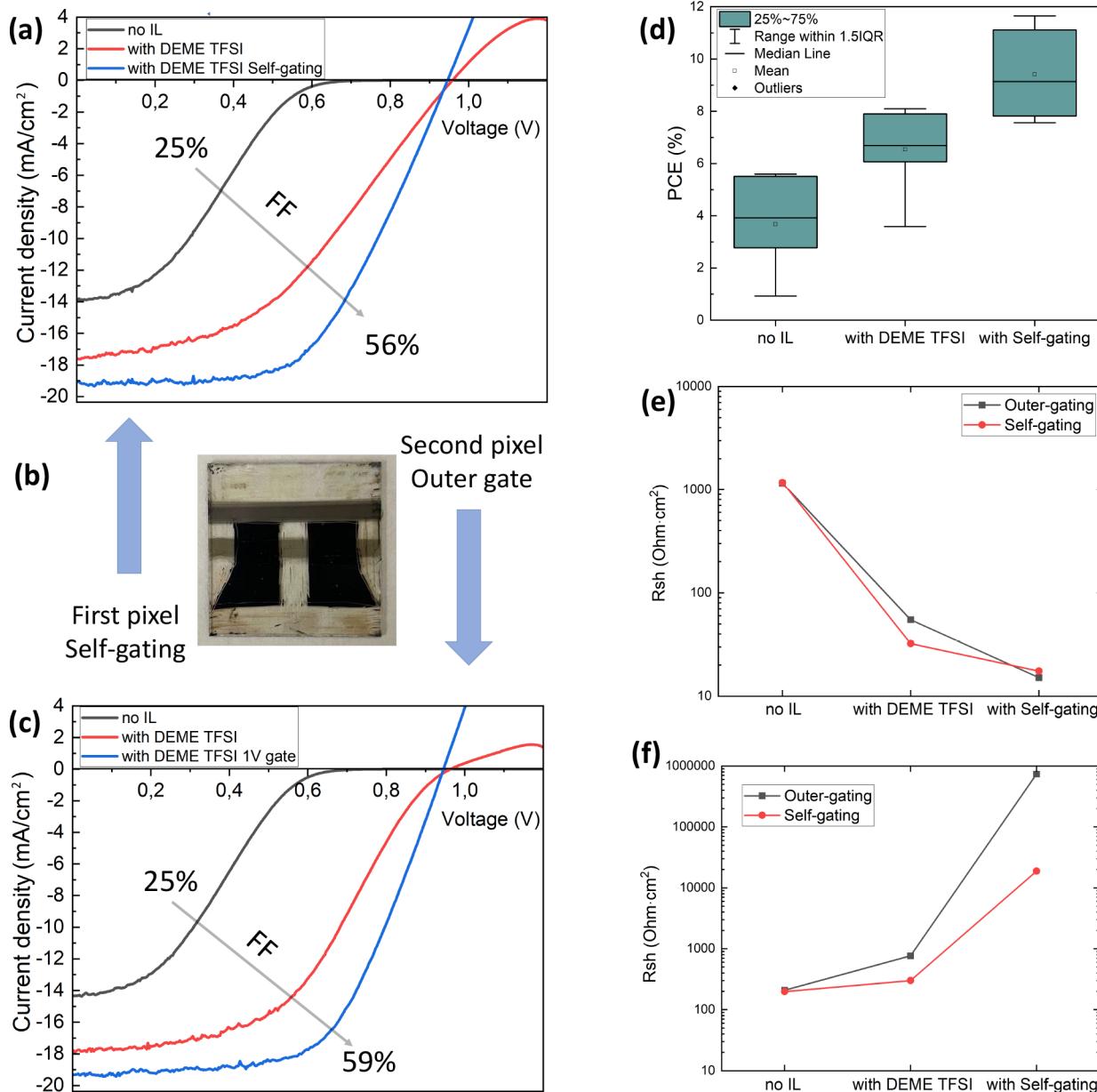


Figure 2. Performance of devices with C₆₀ as ETL with DEME-TFSI as IL, and SWCNT as a top electrode. (a) J–V curves of the first pixel of the device with a self-gating connection. (b) Picture of the device. (c) J–V curves of the second pixel of the device with an outer-gating connection. (d) PCE boxplot for devices with C₆₀ as an ETL. (e) R_s for devices with C₆₀ as ETL. (f) R_{sh} for devices with C₆₀ as ETL.

to 80 nm, where we compare self-gating at photovoltage V_{oc} with external gating at similar low V_g (1 V) as well as the no-gate regime upon photoexcitation in wet conditions by IL (called below as photocharging or self-charging regime). The J–V curves and output parameters of the PSCs are analyzed using two numerical methods: the effective diode-circuit model and the drift-diffusion model. We show how the parameters of the microscopic drift-diffusion model are related to the parameters of the phenomenological diode-circuit model. A detailed comparison of the experimentally observed characteristics of self-gated PSCs with the fitting parameters of both models is provided. We find that self-gating leads to an increase in power conversion efficiency from 2 to 3% for PSCs with dry SWCNT electrodes to 10–11% for self-gated SWCNT electrodes in DEME-TFSI ionic liquid for thick ETLs. Furthermore, we demonstrate that the PCE can be

further increased to 13–14% by using a thinner fullerene layer in combination with other layers.

2. MATERIALS AND METHODS

The perovskite precursor solution was prepared by dissolving 1.5 mmol of MAI in dimethylformamide (DMF)/γ-butyrolactone (GBL) in 1:1 volume ratio, then 1.5 mmol of PbI₂ was added to the MAI solution. Dimethyl sulfoxide (DMSO) was added such that there is a 1:1 molar ratio of DMSO/PbI₂. The solution was heated overnight at 70 °C. Glass substrates with patterned ITO were cleaned in deionized water (2 times), acetone, toluene, and isopropanol in an ultrasonic cleaner for 20 min each. Each substrate was exposed to ultraviolet-ozone treatment for 15 min before spin-coating the first layer in a nitrogen glovebox.

For devices, we have chosen the inverted architecture of ITO/PEDOT:PSS/MAPbI₃/fullerene/CNT. PEDOT:PSS, which is an HTL, was filtered through a PTFE 0.45 syringe filter. PEDOT:PSS was spin-coated onto cleaned and UV-ozone treated substrates with

patterned ITO at 3000 rpm for 60 s and annealed at 150 °C for 10 min after deposition. After annealing, the samples were transferred to a nitrogen-filled glovebox for perovskite deposition. Then 150 μL of MAPbI₃ solution was deposited onto PEDOT:PSS layer in a two-step spin cycle. The first step was at 1000 rpm for 20 s, the second step was at 4000 rpm for 25 s, and 300 μL of antisolvent, which is toluene, was dropped during rotation at the 15th second of the second step. After deposition, samples were preheated at 50 °C for 1 min and annealed at 100 °C for 10 min to form the perovskite film. C₆₀ and C₇₀ fullerenes were deposited by thermal evaporation in a vacuum chamber. The thickness of fullerene was about 160 nm. One layer of SWCNT or five layers of MWCNT stripe were deposited by manual dry lamination on top of the fullerenes as the top electrode. Five layers of MWCNT stripe were placed at a 3 mm distance from the electrode as a CE. CNTs were densified with 3M-Novec-7100 fluid. Five layers of MWCNT were used since MWCNTs have a lower conductivity than SWCNTs do. The conductivity of one layer of SWCNTs is comparable to five layers of MWCNT. Figure 1a shows the architecture of perovskite SC. The scanning electron microscopy (SEM) image in Figure 1b shows a cross section of perovskite SC. We can see the PEDOT:PSS layer thickness is about 30 nm and the perovskite layer is 500 nm with a 165 nm C₆₀ layer; we also see a cross-section with SWCNTs on top, which partially cover the C₆₀ layer.

A 2 μL droplet of IL was placed between the CNT electrode and CE and was squeezed by a cover glass. Self-gating was realized by the direct connection between the ITO and CE. The outer gate was realized by connecting positive voltage to the CE and ground to the SWCNTs from the outer source.

J–V curves were performed with a Newport ABB solar simulator at AM 1.5G calibrated with a silicon certified cell, and a Keithley-2400 source meter unit. SEM images have been obtained on DM07 Zeiss Supra 40 scanning electron microscope. External quantum efficiency (EQE) measurements were obtained on a QEX10 Solar cell spectral response measurement system (PV MEASUREMENTS) calibrated with a KG-9 silicon reference cell.

3. RESULTS AND DISCUSSION

Here we experimentally study physical processes in the SC device with porous CNT electrodes on top of ETL immersed with IL taking place upon photoexcitation: photo charging and various types of gating (self-gating V_{oc} vs outer source gating V_g) can be explained and understood at a qualitative level from the schematic diagrams of Figure 1d and e. Figure 1d shows the structure with IL immersed, but without gate potential applied to the CE. This is a regime of self-charging when IL ions of both signs can penetrate into both porous CNT sheets. Figure 1e is the most desired regime of photoinduced self-gating when the photogenerated V_{oc} is applied to gate CNT-CE. In this case, the CNT electrode is filled by positive ions of IL, i.e., DEME⁺, while the CE is filled by negative ions of IL, i.e., TFSI⁻, because the V_{oc} is applied as a positive potential from the ITO electrode of the device. Corresponding electrical switch positions are sketched in Figure 1c, indicating that for this experiment we have used a three position switch, that allows connecting CE to the external power source when the switch is turned to position 2 and comparing this connection for photoinduced self-gating when the switch is in position 1. Obviously, position 0 corresponds to no voltage applied to CNT-CE.

3.1. J–V Curve Analysis

Figure 1f presents the J–V curves of a PSC device in different regimes. The black curve demonstrates the J–V curve for the no IL case, the red curve corresponds to self-charging, and the blue curve shows device with applied positive gate voltage to CE and negative voltage to the SWCNT electrode. In order to

demonstrate that the enhancement of solar cell parameters is due to the accumulation of positively charged ions of the IL on the CNT electrode and the elimination of the potential barrier between the CNTs and ETL, an opposite gate voltage was applied. Specifically, by applying a positive voltage to the SWCNT electrode and a negative voltage to the CE, it was expected that the potential barrier would increase. This is expressed in the deterioration of the parameters on the green J–V curve in Figure 1f. Notably, all parameters were observed to increase after the introduction of the IL into the device, and application of a positive gate voltage resulted in a further increase. However, upon application of the opposite gate voltage, all parameters (e.g., J_{sc} , V_{oc} , and FF) exhibited a marked reduction and approached the initial curve without any IL.

Results of the light-induced effect of self-gating are presented in a series of figures below, in which we compare three different cases to each other. First, we use two types of ETL with a thickness of about 160 nm of C₇₀ fullerene and C₆₀. Second, we used two types of ILs, DEME-TFSI and BMIM-BF₄⁻ in a small amount, around 2 μL , touched on the top of the CNTs. Two types of CNTs have been used: Multiwall transparent sheets which have been placed dry of a vertically aligned MWCNT forest following the procedures well-described in our previous paper.²³ MWCNTs were compared to SWCNTs obtained by aerosol synthesis and collected on the membranes. As depicted in Figure 2a and c, the J–V curves for a device with SWCNTs as the top electrode and C₆₀ as the ETL demonstrate quite poor parameters in dry conditions (i.e., without any IL). Specifically, the short-circuit current density (J_{sc}) is approximately 14 mA/cm², and the open-circuit voltage V_{oc} approaches a strong s-shape curve to the values of 0.7–0.8 V. The poor charge collection at the SWCNT electrode may be attributed to the space charge accumulation at the interface either between the ETL and CNT or between the perovskite and ETL. J_{sc} is smaller because charge collection is inhibited by traps at the interface. The improvement of the J–V curve was observed when CNTs were immersed with a small amount of IL, namely, DEME-TFSI (about 2 μL). Positive ions of IL under light illumination accumulate at the CNT electrode in the self-charging regime. It is noteworthy that, within the self-charging mechanism, the primary structure of the porous CNT is filled by both negative and positive ions of IL since there is no electric potential to separate cations from anions. As a consequence, all ions diffuse into the CNT structure. The experimental results depicted in Figure 2, illustrate an enhancement in J_{sc} and a transition toward a more diode-like shape with increased FF. Nevertheless, the FF remains relatively low, approximately 35–40% or lower. Performance can be improved further when the generated V_{oc} is applied to the CE. Figure 1e demonstrates the connection between ITO and MWCNTs which allows the photogenerated V_{oc} of the device to serve as the gating voltage for the MWCNT CE. The application of V_{oc} as the gate bias results in the accumulation of TFSI anions at the MWCNT CE and DEME cations at the SWCNT electrode interface. Additionally, this promotes penetration of IL into the fullerene layer and consequently improves ETL conductivity. Figure 2a and c shows two different pixels of one device with C₆₀ as the ETL. Black curves on both of them demonstrate pixel performance in dry conditions, without any IL; red curves in both Figure 2a and c show pixel performance right after adding the IL but without any gating bias. The blue curve in Figure 2a shows the J–V

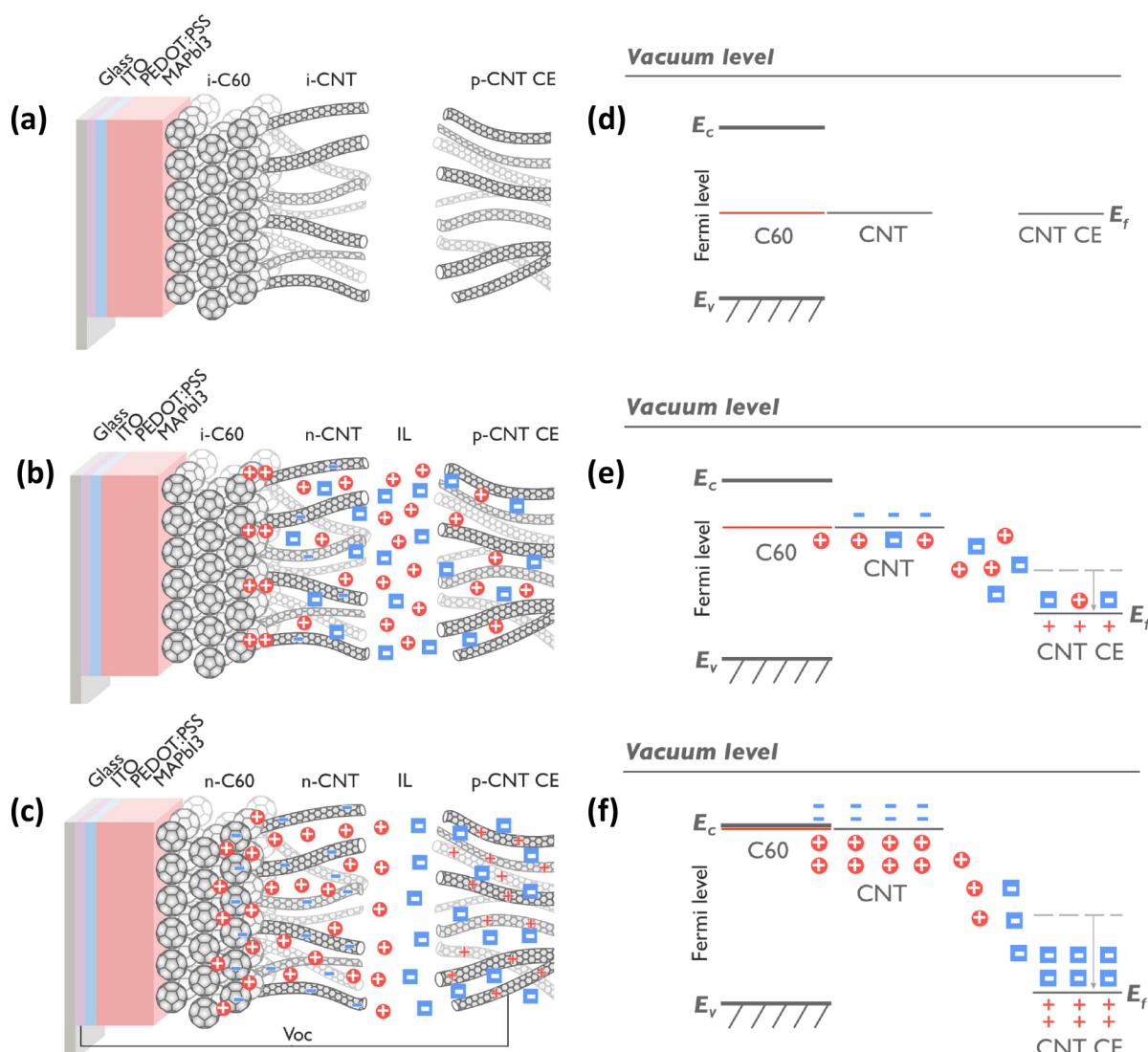


Figure 3. Ionic liquid gating effect on CNT work function. (a) Dry state with no IL, (b) wet CNT/C₆₀ interface, no V at CE: both + and - ions diffused to the porosity of both CNT and CE. Only the CNT/C₆₀ interface has positive ions of IL, attracted by photoexcited electrons in C₆₀; the interface has CNTs n-doped, and some + ions penetrate in a thin layer of C₆₀. CE is initially p-doped and a small amount of -ions of IL create the EDL on p-doped CNT. The improved I_{sc} and better J-V curve in this wet state are due to photo changing (called self-charging) of the CNT/C₆₀ interface. (c) Self-gating with plus potential from PV ITO electrode applied to CE: initially, low V_{oc} is increased due to n-doping of CNT and C₆₀. (d) Energy diagram of dry state: Fermi levels of CNT and CE are not shifted. The trap state at interface and barrier result in high R_{ct} . (e) Wet state: IL in SWCNTs eliminates barrier also neutralizing trap states and “polarization” n-doping of C₆₀ surface layer by DEME + ions. V_{oc} is increased due to partial pinning of E_f . (f) energies in self-gated case: + V_{oc} applied to CE creates potential between SWCNT and CE, EDL charging and n-doping of SWCNTs, enhancing FF and lowering R_s .

curve with a self-gating connection, and the blue curve in Figure 2c shows pixel performance with a 1 V outer gate instead of self-gating.

Figure 2d shows a box-plot of PCE values without IL, with IL and no bias, and with IL and self-gated bias for a C₆₀ based device. Statistically, the efficiency of PSC with C₆₀ tends to increase after adding IL, and then the self-gating connection leads to a further increase. The series resistance (R_s) for devices with SWCNTs as a top electrode and C₆₀ as the ETL with DEME-TFSI IL is shown in Figure 2e to be decreasing which corresponds to decreasing contact resistance between the SWCNT electrode and C₆₀ layer and the increasing conductivity of the SWCNT electrode from doping. The shunt resistance R_{sh} shown in Figure 2e increases due to the lower

leakage current from the better-aligned work functions and energy levels of the doped SWCNTs and C₆₀ ETL with IL.

3.2. Mechanism of Work Function Tuning

Let us discuss the mechanism of device improvements with doped CNTs by IL in our devices. Upon application of a positive potential of 0.9 or 1 V to MWCNT CE in reference to the SWCNT electrode, the TFSI anions migrate toward the MWCNT CE while the DEME cations drift to the surface of the SWCNT. Because of the massive surface area of CNTs, they create an electronic double layer (EDL) at its interface and neutralize the electrons injected there by the gate bias. It understandably corresponds to the n-doping of CNTs, the Fermi level is raised up approaching the conduction band of C₆₀. The effect of the raise of Fermi level in MWCNTs and SWCNTs upon n-doping was observed and described in

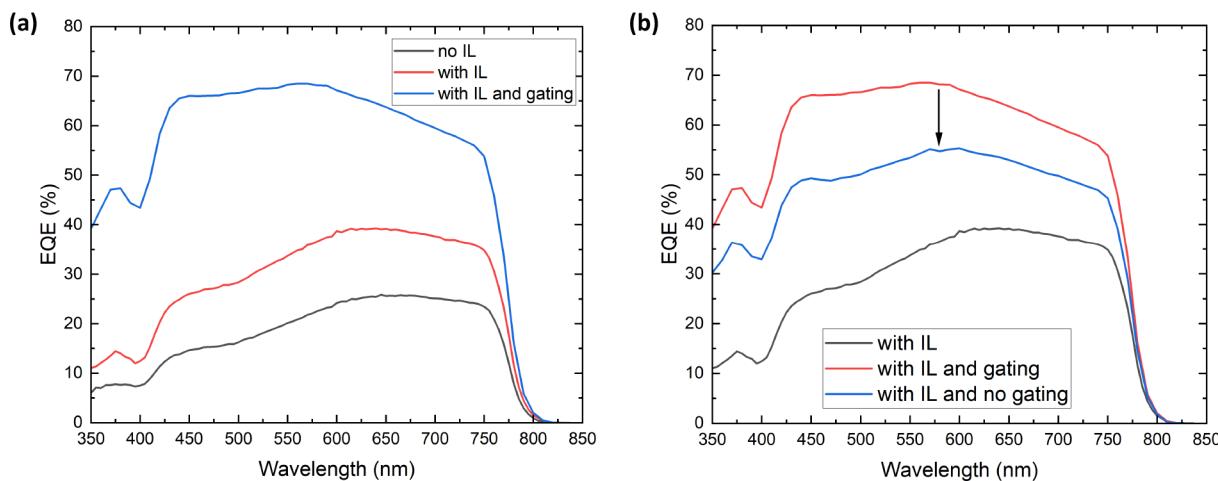


Figure 4. External quantum efficiency (EQE). (a) EQE for devices with C_{60} as ETL, DEME-TFSI as IL, and SWCNT as an electrode. (b) EQE changing with gating and after disconnecting of gating.

previous works.^{36,37} This mechanism is illustrated in Figure 3 as energy diagrams. That process allows the elimination of the interfacial Schottky barrier between SWCNT and ETL. As a result, the internal series resistance decrease while shunt resistance increases as we see in Figure 2e and f.

For self-charging case, when the electrons and holes are generated in perovskite and collected at C_{60} , some of them are still transferred to the CNT because a device is in open circuit condition. Although there is no applied bias between the CE and SWCNT electrode, some DEME⁺ ions still drift into the C_{60} and neutralize the higher energy photoexcited electrons in C_{60} driven by the higher potential they have in reference to the work function of the SWCNTs as illustrated in Figure 3e. So while there is no gating bias and the MWCNT CE is floating, we still have partial n-doping of C_{60} at the interface due to the addition of IL alone.

Figure 3a and d shows the device in the dry state of SWCNT/fullerene. The interface does not provide favorable conditions for electron transfer from C_{60} to the SWCNT, and the collection of photogenerated charges from ETL to SWCNT is weak, due to poor overlap of orbitals and high trap states at the interface, which create space charge of e-negative localized on those traps. Also, pristine SWCNTs are not highly conductive and their Fermi level (E_F) is below the LUMO of C_{60} . The interface of fullerene and SWCNT has defects that act as trap states for photogenerated electrons and with the Schottky junction due to the large difference in Fermi level, it creates a potential barrier interface. The charge transfer between the ETL and CNT is suppressed due to the space charge of filled traps. This phenomenon results in high charge transfer resistance (R_{ct}) and the loss of carriers when biased close to the V_{oc} , leading to the s-shape of the observed $J-V$ curve. J_{sc} is also low, since not all photogenerated carriers are transferred to the electrode (low electron extraction coefficient in the DD model), and recombination is high. The Fermi level of the CNTs is not pinned at the LUMO of the ETL and leads to a lower initial V_{oc} . That phenomenon changes significantly in wet conditions, as shown in Figure 3b and e. The diffusion of IL ions results in their penetration into the porosity space of the SWCNTs and their eventual arrival at the SWCNT/fullerene interface. Ions of both signs fill the pores in SWCNTs, although there is no potential applied between the SWCNT electrode and MWCNT CE. However, due to

some initial p-doped character of MWCNTs and the small ~ 0.3 V shift of potential of zero charge, the CE has some excessive negative ions of TFSI and thus some unbalanced excess of DEME ions at interface with C_{60} . Those ions penetrate into the surface layer of C_{60} and cause n-doping by a polarization mechanism. The filled traps are neutralized by the positive charge of DEME⁺ ions and the partial pinning of the Fermi level of SWCNTs to the LUMO of n-doped C_{60} increases V_{oc} and as a result J_{sc} is raised by elimination of interface barrier.

This is clearly observed in the $J-V$ curves of Figure 3a: the red curve (self-charged wet CNT/ C_{60}) is significantly improved as compared to the black curve of the dry interface. The improvement of FF is due to overall decreased series resistance (R_s) and increased shunt resistance (R_{sh}) which is shown in Figure 2e and f. Operating with gate regime, which is shown in Figure 3c and f, leads to further improvement of parameters.

3.3. Spectral Sensitivity Analysis

In order to demonstrate the self-gating phenomenon, measurements were taken of the EQE of PSC for dry, wet with IL, and wet with applied gate voltage. The resulting EQE values are depicted in Figure 4a. Clearly, applying a voltage to the gate leads to an improvement of J_{sc} and an increase of EQE, especially in the blue-UV spectral region of 420 to 600 nm. It proves that C_{60} is n-doped, leading to enhanced light absorption in C_{60} , since the forbidden electronic transition from t1u, and t1g levels becomes allowed, as in the case of chemical n-doping by alkali metals.³⁸ On the other hand, Figure 4b shows that after disconnecting the gating connection, where the black curve corresponds to no gating case, the red curve is with IL and applied to the gate, and the blue curve is the case with IL and disconnected gating. CNT is dedoped by back diffusion of IL ions causing a decrease of EQE by 10–15% but did not reach the initial EQE of no gating case and the shape of EQE at the spectral band at 450–600 nm remains almost the same, due to dedoping of C_{60} takes much more time compared to dedoping of CNT. which means that the blue curve corresponds to doped C_{60} but discharged CNT.

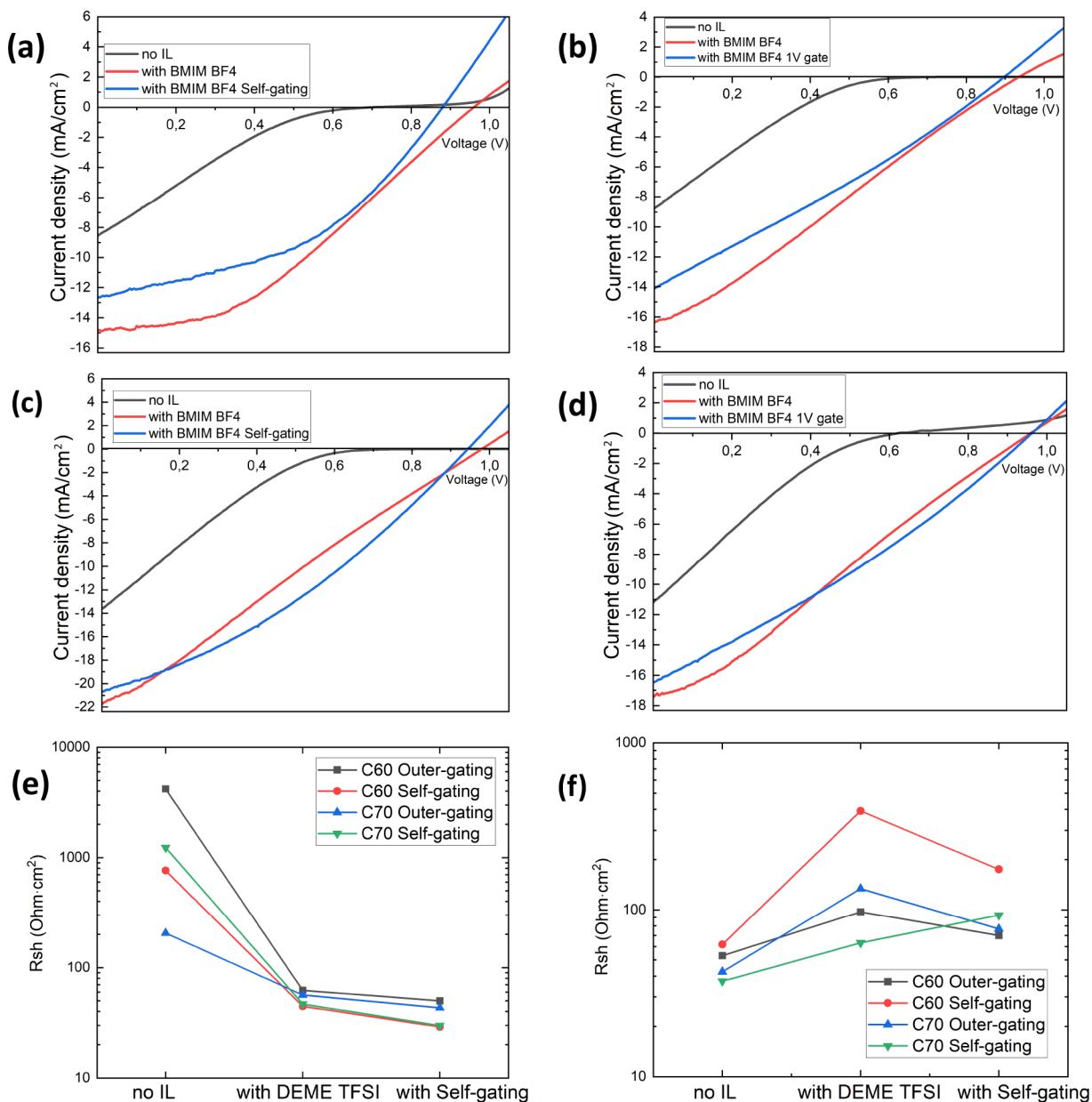


Figure 5. Performance of devices with C_{60} and C_{70} as ETL with BMIM-BF₄ as IL. (a) $J-V$ curves of devices with one layer of SWCNTs as a top electrode and C_{60} as ETL in a self-gating connection. (b) $J-V$ curves of devices with one layer of SWCNTs as a top electrode and C_{60} as ETL in outer-gating connection. (c) R_s for devices with BMIM-BF₄ as IL. (d) $J-V$ curves of devices with one layer of SWCNTs as a top electrode and C_{70} as ETL in self-gating connection. (e) $J-V$ curves of devices with one layer of SWCNTs as a top electrode and C_{70} as ETL in outer-gating connection. (f) R_{sh} for devices with BMIM-BF₄ as IL.

3.4. Alternative Ionic Liquid and Device Architecture Study

To understand the impact of the IL itself, BMIM-BF₄ was used as another type of IL in the same architecture of the device with C_{60} and C_{70} as the ETL and SWCNT as the top electrode. The ion diameter of BMIM⁺ is smaller than that of DEME⁺, 5.7 vs 7.54 Å.^{39,40} Since the ion has a smaller size, lower voltage is needed to stimulate ions to move through the ETL and reach the perovskite layer, which leads to the degradation of the device and its parameters decreasing. Figure 5a and b illustrates the behavior of the device with C_{70} as an ETL, and Figure 5c and d shows the behavior of the device with C_{60} as an ETL. In both cases, an increase of all parameters takes place when the CNT is immersed with IL. However, applying a 1 V

gate voltage or self-gating connection did not stimulate a further significant increase in parameters. J_{sc} , V_{oc} , and FF slightly decrease which indicates that 1 V gate voltage initiates the degradation of device with BMIM-BF₄ as IL. It was also demonstrated that the values of R_s and R_{sh} were altered, as evidence of degradation. R_s and R_{sh} are presented in Figure 5e and f. R_s shows the same trend as for the DEME-TFSI case since the same electrodes (ITO and SWCNT) are used. However, R_{sh} for devices with BMIM-BF₄ shows a decrease after applying any type of gating. The decrease of R_{sh} usually happens due to current leakage through an alternate current path or inefficient hole blocking in the ETL. That path may be caused by excess BMIM⁺ ions, which reach the perovskite layer.

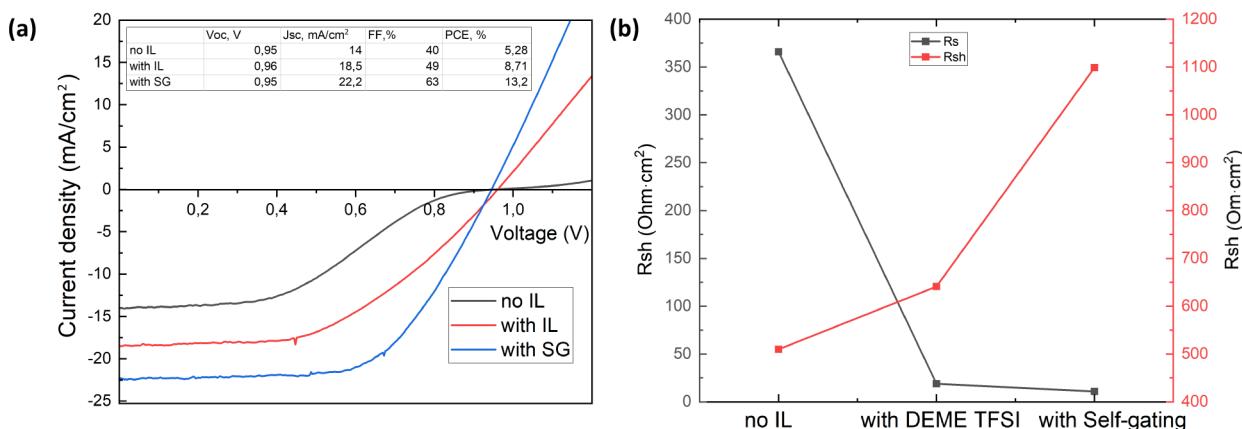


Figure 6. Champion device characteristics. (a) J – V curve of the device with the highest efficiency 13.2%. That device has a thinner C_{60} layer, about 80 nm, along with a layer of BCP on top of C_{60} and a thin layer of LiF between the perovskite and C_{60} for additional protection from the IL. (b) R_s and R_{sh} of the champion device.

In order to demonstrate that IL gating can enhance the performance of the device to a level comparable with that reported in the literature,^{41–44} a modified device architecture was used. The thickness of the C_{60} layer was decreased 2 times and two other layers were added. As a result, an efficiency of 13.2% was achieved, which is comparable to the reported performance of PSCs with a CNT top electrode in p–i–n structures in the literature. Furthermore, our efficiency overcomes the PCE of the device with similar layer choice with optimized layer thicknesses but without IL.⁴⁵ The J – V curves of this device, as well as its series and shunt resistance, are presented in Figure 6.

4. SIMULATION

In the experimental section, we observed that introducing the IL from the side of the SWCNT electrode can significantly improve the performance of solar cells. The porous structure of SWCNTs allows ions to penetrate when the IL droplet is added to the top of the solar cell. In order to obtain a general intuitive understanding of the effect of the ionic liquid on solar cell performance, we employed a diode circuit (DC) model and compared it with the drift-diffusion (DD) model by analyzing the evolution of fitting parameters derived from each model.

4.1. Drift-Diffusion Modeling

The DD model is described in detail in section S2 of the Supporting Information. We used the drift-diffusion equations and energy level information for each layer, as shown in Figure 7b, and implemented the simulation in one dimension, schematically illustrated in Figure S9. The resulting simulations are presented in Figures S10–S12.

By simulating an ionically gated perovskite solar cell using the DD model in our previous work,³² we demonstrated that penetrated ions inside CNTs can raise the electrode Fermi level and convert a Schottky contact into an ohmic one through the reduction of the potential barrier at the ETL/CNT interface. Additionally, at higher gate voltages, positive ions can drift in high concentrations inside the ETL, thereby doping it. In this paper, we investigate the impact of using C_{60} versus C_{70} fullerenes as the ETL, and how the IL affects the solar cell performance. We observed that the C_{60} fullerene provides a higher fill factor (FF) compared to the C_{70} fullerene, and this increase is sustained when applying the DEME-TFSI

IL and connecting the SWCNT to the MWCNT gating electrode using both self-gating (SG) and outer-gating (OG) methods. Applying the IL also increases the short-circuit current for both C_{70} and C_{60} ETLs. However, it is noteworthy that the short-circuit current of C_{70} does not improve any further by connecting the CNT to the gate voltage, while there is a further increase in the J_{sc} for the C_{60} case.

4.2. Diode Circuit Modeling

The equivalent diode circuit model that we used in the modeling is illustrated in Figure 7a. This circuit, indeed, is the well-known equivalent diode circuit model that is used for the simulation of solar cells in addition to three extra elements. A pair of diode and resistance that are in series to the main diode, and a current sink that is in parallel to the photogenerated current. In this circuit, pair of inverse diode and resistance are encircled with a red dashed box to mimic the role of Schottky contact and the other encircled part mimics the recombined current at the perovskite/charge transport layers (CTLs) interface. We calculated the J – V characteristic of this circuit and fitted them to the experimental J – V curves. The current density–voltage characteristics of the circuit can be derived from the following equation⁴⁶

$$(R_{sh} + R_l)J = V_a - RJ + R_{sh}(J_d - J_{ph} + J_{rec}) - R_{d1}J_{d1} \quad (1)$$

where R_{sh} is the area normalized shunt resistance with the dimensionality of $\Omega \times \text{cm}^2$, R_s is the area normalized series resistance, R_l is an area normalized resistance in parallel to the reverse diode that is marked by D_1 in the circuit, J_{ph} is the photogenerated current density, J_{rec} is the current density sink, J_{d1} is the current density that is flowed from the reverse diode, and J_d is the current density that is flowed from the main diode (D) that can be described by

$$J_d = J_{d1} \left(\exp \left[\frac{q}{nkT} (V_a - (R_s + R_l)J - R_{d1}J_{d1}) \right] - 1 \right) \quad (2)$$

and

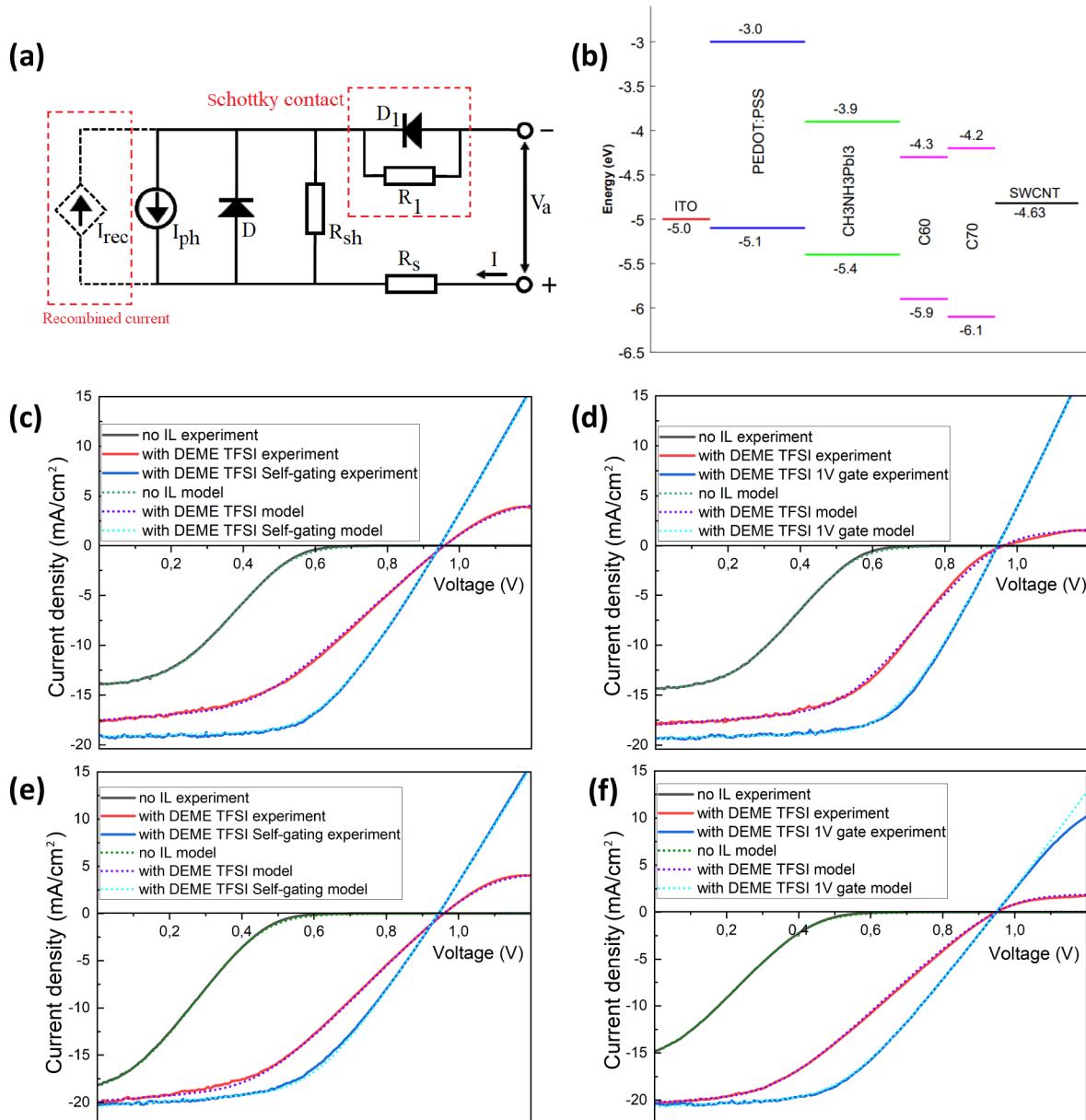


Figure 7. Performance of DC model for SCs when IL is BMIM-BF₄. (a) Diode circuit model for simulation of the ionically gated perovskite solar cell. (b) Simulated J - V curves using the DC model (circle markers) in addition to the experimental results (solid lines) when the ETL is C₆₀ and the self-gating method is used. (c) Simulated J - V curves of the solar cells using the DC model (circle markers) in addition to the experimental results (solid lines) when the ETL is C₆₀ case and the outer-gating method is used. (d) Energy diagram of solar cell layers. (ITO from ref 47, PEDOT:PSS from ref 48 and fitting, perovskite from refs 48, 49, C₆₀ from ref 50 and fitting, C₇₀ from ref 51, and SWCNT from ref 52). (e) Simulated J - V curves of the solar cells using the DC model (circle markers) in addition to the experimental results (solid lines) when the ETL is C₇₀ and the self-gating method is used. (f) Simulated J - V curves of the solar cells using the DC model (circle markers) in addition to the experimental results (solid lines) when the ETL is C₇₀ and the outer-gating method is used.

$$J_{\text{d}1} = J_{\text{s}d1} \left(\exp \left[-\frac{q}{n_1 k T} (V_a - (R_s + R_{\text{sh}}) J \right. \right. \\ \left. \left. + R_{\text{sh}} (J_{\text{d}} - J_{\text{ph}} + J_{\text{rec}}) \right] - 1 \right) \quad (3)$$

In these equations, $J_{\text{s}d}$ and $J_{\text{s}d1}$ are the saturation current density of the main and the reverse diode, respectively. n is the ideality factor of the main diode, n_1 is ideality factor of the reverse diode, k is the Boltzmann constant, and q is the elementary charge and T is the temperature.

We used the simulation parameters of Table S3 and solved eqs 1–3 to fit the J - V curves of the circuit to the experimental J - V curves. Derived J - V curves of the circuit in addition to the experimental J - V curves are illustrated in Figure 7c–f. There is a good agreement between the experiment and the circuit's J - V curves.

For fitting the J - V curves using the DC model, we reduced the R_1 resistance and increased the saturation current of the reverse diode. Indeed, by reduction of R_1 resistance, the reversed diode becomes a short circuit, and J - V curves change from an s-shape to an arc-shape that is observable in Figure 7. The obtained value for this resistance is illustrated in Figure 8a

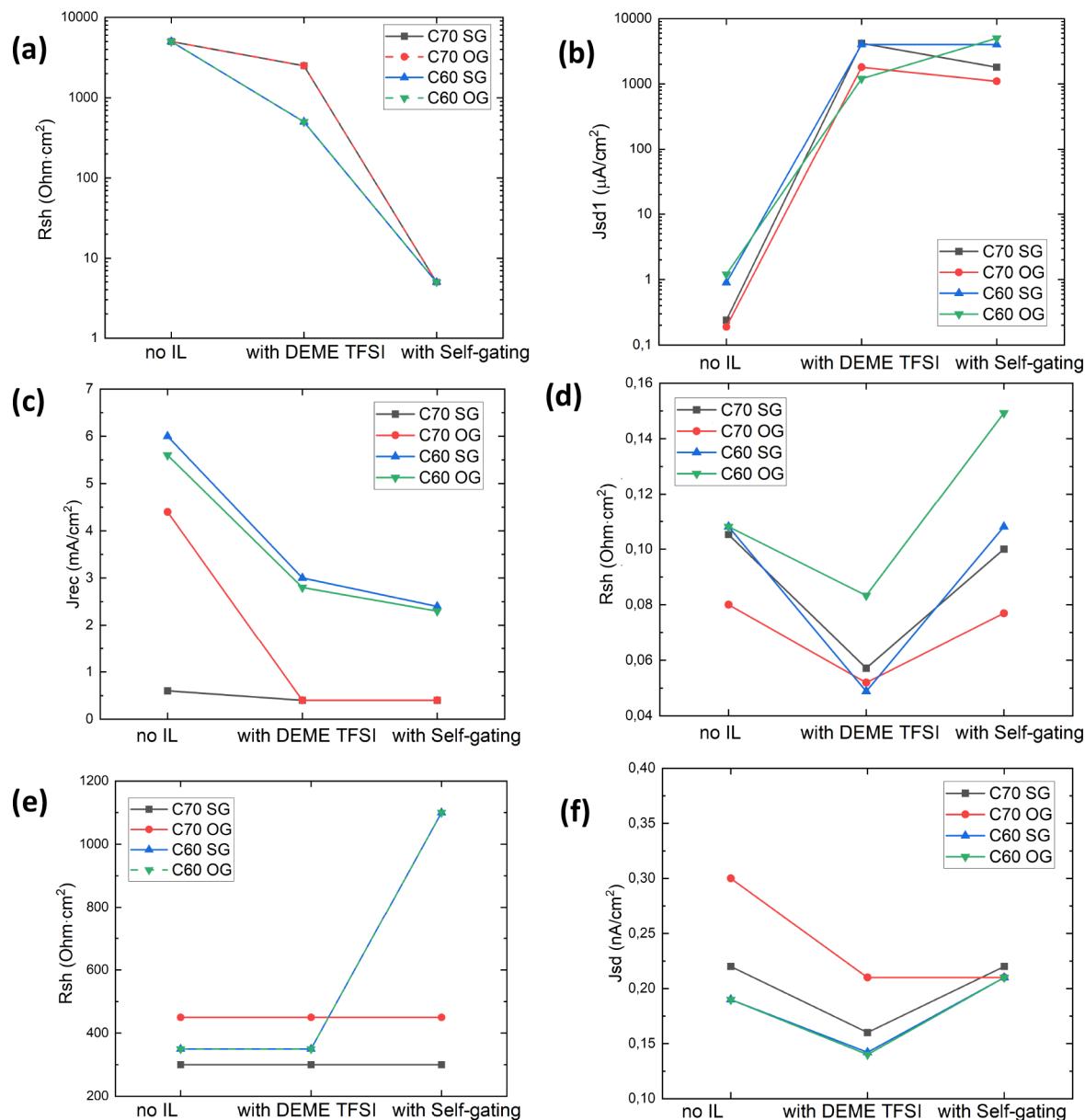


Figure 8. Derived value for the fitting parameters in the DC model. (a) Evolution of the R_1 resistance, (b) saturation current of the reverse diode, (c) recombination current, (d) inverse of the series resistance, (e) shunt resistance, and (f) saturation current of the main diode by applying the IL and gating of the SWCNT electrode for both the self-gating and outer-gating methods.

and derived values for the saturation current of the reverse diode are presented in Figure 8b. Comparing these figures with Figure S11a and b shows very similar behavior between barrier and R_1 resistance, and between the electron extraction coefficient (EEC) at the CNT surface and saturation current of the reverse diode, respectively. Hence, simulation results using the DD model indicate changing of the SWCNT Fermi level and enhancement of the EEC at its surface; it corresponds to the elimination of the reverse diode and increasing of its saturation current at the DC model. In other words, when the saturation current of a diode increases, it means that it is a bad diode and cannot prevent the flowing of the current in the reverse direction. Hence, applying an IL not only eliminates this reverse diode but also converts it to a nonideal diode, and this means nothing but eliminating a Schottky contact and converting it to an ohmic contact.

In addition to the aforementioned parameters, we also have changed the series and the shunt resistances of the circuit. In order to compare these results with DD model results, we have plotted reverse of the series resistance and value of the shunt resistances in Figure 8d and e, respectively. In all cases, upon applying the IL, there is a reduction in the reverse of the series resistance, and by gating of the CNT electrode, it increases. These are similar to the electron mobility change at the ETL that is presented in Figure S11c. It is known that series resistance decreases either by reduction of the material thickness or by doping of the semiconductor. Therefore, since there is a reduction in the electron mobility at the ETL upon applying the gate voltage, we can observe a reduction in the reverse of the series resistance. Then similar to the mobility behavior by gating of the CNT electrode, the reverse of series resistance increases. One may notice that the highest increase in the reverse of the series resistance is related to the C₆₀ outer-

gating case, such that it is even higher than the case without the IL, while the mobility of electrons at C_{60} and the outer-gating case is less than that without IL. The reason for such an increase in the reverse of series resistance is the doping of the ETL upon gating of the CNT that is illustrated by the ETL equilibrium Fermi level in Figure S11d. While one can observe changes in the C_{60} Fermi level by gating of the cathode, there is no change in the C_{70} Fermi level. It means that IL can dope C_{60} easily while it has no effect on the doping level of C_{70} .

Shunt resistance results derived from the DC model are illustrated in Figure 8e for both C_{70} and C_{60} . It is clear that shunt resistance does not change by applying the IL and gating of the CNT electrode for C_{70} fullerene, but the value of shunt resistance is different for the self-gating and outer-gating cases. This is due to the difference in the thickness of the ETL for the case of the outer-gating and self-gating methods. It is found that the ETL thickness at the case of C_{70} fullerene and self-gating is 155 nm while for the rest of the cases it is about 165 nm. Moreover, that is why there is a different series resistance in Figure 8d when there is no IL for self-gating and outer-gating methods. On the other side, one can see a constant shunt resistance for the C_{60} fullerene by applying the IL, and it increases upon gating of the electrode. This increment is related to the doping of C_{60} fullerene that can be realized at a lower gate voltage in comparison to the C_{70} fullerene. At a lower gate voltage, there is no doping of the C_{70} fullerene.

The values that we have derived for the introduced current sink at the circuit in addition to the saturation current of the main diode are presented in Figure 8c and f, respectively. In Figure 8c for the C_{70} case in the self-gating regime, it is observed that the recombination current is low in comparison to the other cases when there is no IL, then by applying the IL it decreases, and by gating the CNT electrode it is constant. Because the recombination current is low in this sample, we can see a higher J_{sc} . Although recombination current is higher for the case of C_{70} and outer-gating method in Figure 8c but similar to the self-gating method, it decreases then again is constant by applying the IL and gating of the CNT electrode. On the other hand, the recombination current for a solar cell with C_{60} fullerene constantly decreases by ionic gating of the CNT electrode for both self-gating and outer-gating methods, as depicted in the graph of Figure 8c. This behavior in the recombination current that we derived in the DC model is similar to the inverse of the carrier lifetime at the right superficial trap states that are illustrated in Figure S12. Then it is easy to conclude that the current sink in the circuit, indeed, mimics the trap states density at the perovskite surfaces. Higher trap states at perovskite surfaces can decrease J_{sc} considerably, suppression of these trap states leads to an increase in the short circuit current, and it can be realized by using of the IL and proper gating voltage.

In the DC model, in order to have the best fitting between simulation and experiment, we also have changed the saturation current of the main diode. As mentioned, these results are presented in Figure 8f. Noticing this saturation current evolution, one may understand that this parameter imitates the role of trap density at the perovskite/CTL interface. Comparing this graph with the orange line in Figure S12 reveals an undeniable similarity between the saturation current of the main diode and the reverse of carriers' lifetime at the right interface trap states. Therefore, the DC model confirms that, by applying the IL, the trap state density at the perovskite/ETL interface decreases and this reduction is due

to the suppression of trap state density by the ions that reach this interface. Maybe a question arises: why there is an increase in the trap state density at the perovskite/ETL interface by gating of the CNT electrode? In order to answer this question, it is noticeable that in the experimental $J-V$ curves that are illustrated in Figures 2 and S8, V_{oc} for all solar cells in the wet condition is greater than that for the gated condition, except in Figure S8c that represents the solar cell with C_{70} fullerene as the ETL and outer-gating method. In this case, V_{oc} is the same for the wet and gated CNT. That is why the inverse of the carriers' lifetime in Figure S12b and saturation current of the main diode for the C_{70} OG case in Figure 8f does not change by gating of the CNT electrode. For all other cases, these parameters slightly increase and lead to a reduction in the V_{oc} . We believe that this small reduction in the V_{oc} is related to the degrading of the perovskite layer that can happen in higher concentrations of the IL at its surface. In fact, by applying the IL, some ions diffuse to the perovskite/ETL interface and suppress the trap states at this interface, but the ion concentration is not so high that it can degrade the perovskite. Once the gating is done, more ions reach this interface and perovskite degradation begins. Therefore, it is important that ionic gating needs to work within an optimum condition. Optimum condition means the IL should suppress the trap states both at the perovskite surface and at the perovskite/ETL interface without damaging it. This is possible by controlling the ion concentration that reaches the perovskite layer, and ion concentration control is achievable by controlling the gating voltage, ETL thickness and, obviously, by ETL uniformity.

The corresponding parameters with similar effects on the solar cell $J-V$ curve for both DC and DD models are summarized in Table 1. Indeed, the left column of this table

Table 1. Corresponding Parameters of DC and DD Models

diode circuit model	drift-diffusion model	
in parallel resistance with the reverse diode	$R_1 \equiv B$	potential barrier at the ETL/CNT interface
saturation current density of the reverse diode	$J_{sd} \equiv EEC$	electron extraction coefficient at the CNT surface
current density sink	$J_{rec} \equiv 1/\tau_{n,p}^{sup}$	inverse of carriers lifetime at the perovskite's surface
saturation current density of the main diode	$J_{sd} \equiv 1/\tau_{n,p}^{int}$	inverse of carriers lifetime at perovskite/ETL interface

shows the DC model inputs that have a corresponding physical meaning in the DD model, which are represented in the right column of the table. Such an established analogy between the DC model and the DD model helps in using and understanding the physical meaning of each parameter in the DC model with less complexity and high accuracy and faster simulation time in comparison to the DD model.

Moreover, Table 2 allows comparing of experimentally observed parameters with the fitting parameters of the phenomenological DC model. The microscopic DD model allows accounting for the poor charge collection by two parameters: EEC and barrier height at the ETL/CNT interface, which both describe the origin of the poor s-shape $J-V$ curve and effectively describe the experimentally observed decrease of R_s and increase of R_{sh} by addition of IL. This table also allows an understanding of the correspondence between Experiment and DC, and Experiment and DD models. One may notice that the observed total series resistance in the dry conditions is very large (>1000 ohm) in the experiment. This

Table 2. Comparison of Experimentally Derived Parameters with Fitting Parameters of the Modeling for the Self-Gating Cells and DEME-TFSI IL^a

DEME-TFSI	experiment		diode circuit model					drift-diffusion model				comments	
	R_s	R_{sh}	R_s	R_{sh}	R_l	J_{sd}	J_{sd1}	I_{rec}	barrier	EEC	$\tau_{n,p}^{sup}$	$\tau_{n,p}^{int}$	
self-gating cells													
dry C ₆₀ (no IL)	1175	198	9.25	350	5000	0.19	0.9	6	0.33	4×10^{-4}	2.5×10^{-12}	1×10^{-11}	b
wet C ₆₀ (self-charging)	32.3	300	20.5	350	500	0.142	4000	3	0.07	4×10^{-2}	4.5×10^{-13}	4.5×10^{-10}	c
wet C ₆₀ (self-gating)	17.5	18761	9.25	1100	5	0.21	4000	2.4	0.03	4×10^{-2}	7.3×10^{-13}	2.8×10^{-11}	d
dry C ₇₀ (no IL)	980	56	9.5	300	5000	0.22	0.24	0.6	0.43	4×10^{-4}	2.5×10^{-12}	1×10^{-11}	e
wet C ₇₀ (self-charging)	29.3	245	17.5	300	2500	0.16	4200	0.4	0.07	4×10^{-2}	2.8×10^{-12}	2×10^{-11}	f
wet C ₇₀ (self-gating)	18.1	1078	10	300	5	0.22	1800	0.4	0.01	3×10^{-2}	2.8×10^{-12}	1×10^{-11}	g

^aThe parameters unit are same as those in Tables S2 and S3. ^bHigh experimental R_s of $1175 \Omega \times \text{cm}^2$ correlates with $R_s + R_l$, reflecting big R_{ct} at interface and increase of small R_{sh} to wet correlates with increased J_{sd1} leakage in the wet case. ^cExperimental R_s (wet) correlates now with better fitting R_s (wet) of DC-model and R_l drops. ^dExperimental R_s (SG) further drops due to doping of CNT caused drop of R_s (CNT), which correlates with drop of R_l by 2 orders. ^eChange of R_l from dry to wet correlates with decrease of interface barrier (0.33 eV drop to 0.07 eV). ^fEEC of DD model improves upon wet self-charge by 2 orders, correlating also with barrier disappearance. ^gBarrier of DD model drops further (0.07 to 0.01 eV) upon self-gating, in correspondence with R_s (SG) drop in DC model.

total series resistance can be viewed as a sum of the series resistance of each layer of PSC and charge transfer resistance (R_{ct}) at the interface:

$$R_{\text{ser}} = R_{\text{ser}}(\text{perovskite}) + R_{\text{ser}}(C_{60}) + R_{\text{ser}}(\text{CNT}) + R_{\text{ct}} \quad (4)$$

One should keep in mind that, in the simple DC model for SC, the additional R_l is not accounted for. Therefore, when the DC model fits the experiment with a combination of R_s , R_l , and other parameters, one should compare experimental R_s with $R_s(\text{DC-model}) + R_l(\text{DC-model})$ in addition to taking into account J_{sd} and J_{sd1} for each case. Indeed, from Table 2, the observed experimental R_s in the dry cases correlates well with large R_l , while $R_s(\text{DC-model})$ is 3 orders lower than the experimental value, and in wet cases, R_l drops an order of magnitude from 5000 to 500 (same as in experimental R_s), reflecting the decrease of R_{ct} and $R(C_{60})$. Upon self-gating, R_l further drops from 500 to 5 for a best fit with the experimental $J-V$ curve. We can now find the correlation of DC model parameters with the DD model microscopic EEC: electron extraction coefficient. Those correlations are partially shown in brief in the table notes of Table 2.

5. CONCLUSION

In this work, we have demonstrated that effective self-gating in the IL is possible by a photoinduced process, without an external source. We have used two types of CNTs as the top electrode of a perovskite solar cell, SWCNTs and MWCNTs, where energy offset at the ETL/CNT and low capability of charge extraction due to the high work function of CNTs and poor stickiness of CNTs to the ETL are not favorable for achieving high-performance solar cells in dry conditions, i.e., without an IL. On the other hand, using CNT provides some undeniable advantages like ease of deposition, semitransparent electrode, and stable contact for perovskite-based solar cells. Experimentally, we have shown that the immersion of CNT within a proper ionic liquid enhances the solar cell performance considerably and we numerically proved that this enhancement is related to the energy offset correction at the ETL/CNT interface and a huge enhancement in the electron extraction coefficient at the CNT surface. Moreover, we have

shown that using fullerenes as the electron transport layers under the CNT enables external doping of the ETL and provides further enhancement. We showed that doping of the ETL is achievable by an external electric field that makes ions penetration inside the fullerene layer possible by drifting. This external electric field is achievable by sandwiching the IL between the CNT electrode and a third counter electrode. The electric potential V_g required for establishing an external electric field can be obtained by connecting the CE to the ITO electrode of the solar cell, and we call it a self-gating method since V_{oc} plays the role of V_g . Self-gating in comparison to the outer-gating of $V_g = 1 \text{ V}$ (close to V_{oc}) provides a similar performance in a solar cell, but it eliminates the requirement for external power supply for the gating process. Analyzing $J-V$ curves using the numerical method, we showed that an optimum condition is required for cell performance enhancement and this optimal condition enables the use of the self-gating method. Moreover, we have established an in-detail analogy between the drift-diffusion model and the diode circuit model to provide simple tools for analyzing the ionically gated perovskite solar cells using the diode circuit model.

■ ASSOCIATED CONTENT

SI Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsmaterialsau.3c00006>.

$J-V$ curves of solar cell using MWCNT as the top electrode instead of the SWCNT and C₇₀ as a electron transport layer; experimental measuring of FF, J_{sc} , and V_{oc} as provided by box-plots and an in detail explanation about simulation using the drift-diffusion model in addition to the all simulation parameters (PDF)

■ AUTHOR INFORMATION

Corresponding Author

Anvar A. Zakhidov – School of Physics and Engineering, ITMO University, 197101 St. Petersburg, Russia; Physics Department and The NanoTech Institute, The University of Texas at Dallas, Richardson, Texas 75080, United States;

 orcid.org/0000-0003-3983-2229; Email: zakhidov@utdallas.edu

Authors

- Grigorii Verkhogliadov** — Physics Department and The NanoTech Institute, The University of Texas at Dallas, Richardson, Texas 75080, United States; School of Physics and Engineering, ITMO University, 197101 St. Petersburg, Russia
- Abolfazl Mahmoodpoor** — School of Physics and Engineering, ITMO University, 197101 St. Petersburg, Russia
- Pavel Voroshilov** — School of Physics and Engineering, ITMO University, 197101 St. Petersburg, Russia;  orcid.org/0000-0002-4039-4513
- Ross Haroldson** — Physics Department and The NanoTech Institute, The University of Texas at Dallas, Richardson, Texas 75080, United States
- Masoud Alahbakhshi** — Department of Electrical and Computer Engineering, The University of Texas at Dallas, Richardson, Texas 75080, United States
- Albert G. Nasibulin** — Center for Photonics and Quantum Materials, Skolkovo University of Science and Technology, Moscow 143026, Russia
- Sergey V. Makarov** — School of Physics and Engineering, ITMO University, 197101 St. Petersburg, Russia; Qingdao Innovation and Development Center, Harbin Engineering University, Qingdao 266000 Shandong, China;  orcid.org/0000-0002-9257-6183

Complete contact information is available at:
<https://pubs.acs.org/10.1021/acsmaterialsau.3c00006>

Author Contributions

[†]G.V. and A.M. contributed equally to this work. CRediT: **Grigorii Verkhogliadov** formal analysis (equal), investigation (lead), writing-original draft (equal); **Abolfazl Mahmoodpoor** investigation (equal), writing-original draft (equal); **Pavel Voroshilov** validation (equal), writing-original draft (supporting); **Ross Haroldson** investigation (supporting), methodology (equal), software (equal), validation (equal), writing-review & editing (equal); **Masoud Alahbakhshi** investigation (equal), methodology (equal); **Albert G Nasibulin** conceptualization (equal), resources (equal), supervision (equal), validation (equal); **Sergey V. Makarov** supervision (equal), writing-review & editing (equal); **Anvar A. Zakhidov** conceptualization (lead), resources (equal), supervision (lead), writing-review & editing (lead).

Notes

The authors declare no competing financial interest.

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