Investigation of interface states distribution in metal-oxide-semiconductor structures with very thin oxides by acoustic spectroscopy

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New technique of acoustic spectroscopy to study interface states in metal-oxide-semiconductor (MOS) structures with a very thin oxide layer based on the acoustoelectric effect resulting from the interaction between the longitudinal acoustic wave and semiconductor-insulator interface is presented. The essential principles and theoretical background of this acoustic spectroscopy technique that can determine the interface states distribution from the measured acoustoelectric response signal as a function of gate voltage (U_{ac}-U_g characteristics) are described. The results obtained on the representative set of MOS structures prepared on both n- and p-type Si substrates by nitric acid oxidation of Si technology and undergone also some thermal treatment demonstrate that the introduced technique of acoustic spectroscopy can be a very useful tool for the interface states characterization. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4897454]

I. INTRODUCTION

Interface states at semiconductor-insulator heterojunction in MOS (metal-oxide-semiconductor) structures play an important role in determining their electrical characteristics that are important for practical use in semiconductor devices. A silicon-silicon dioxide (Si/SiO_2) structure mostly prepared by thermal oxidation at above 800 °C in oxidizing atmospheres is widely used for MOS devices.[1] Because the high temperature oxidation results in high interfacial stress producing the interface defect states,[2] the low temperature direct oxidation methods such as plasma oxidation, metal-promoted oxidation, or method of nitric acid oxidation of Si (NAOS) were developed.[3–6] Producing a very thin oxide layer, metal oxides with high dielectric permittivity (high κ dielectrics) can find a successful application as a replacement for SiO_2 gate insulator to break through its physical limit.[7,8] Although due to the many improvements in preparation technology, the density of interface states, especially at SiO_2/Si interfaces is usually very low, still it can seriously affect electrical properties of MOS devices and the interface states need to be well characterized.

Several methods for the interface states determination were developed. The simplest and very often used technique utilizes C-V measurements at very low frequencies.[2] However, a high leakage current in the case of a very thin oxide layer disturbs C-V measurements. Later, computational methods to fit high frequency C-V characteristics especially for MOS capacitors with high-κ dielectrics have been presented.[9,10] To find the distribution of interface states, the deep-level transient spectroscopy (DLTS) can be also used.[11] Recently, the X-ray photoelectron spectroscopy (XPS) under bias was used to obtain the energy distribution of interface states at very thin oxide/Si interfaces determination.[12] Some attempts to determine the interface states density using the acoustoelectric effect (AE) resulting from the interaction of surface acoustic wave (SAW) with interfaces were also performed.[13,14]

When the AE in semiconductor structures has been shown to be an effective tool for the characterization of electrical properties and experimental study of semiconductors, the AE interactions were utilized to carrier transport properties characterization including the conductivity and carrier mobility measurement and later to the interface state determination.[15–17] Consequently, two basic modifications of acoustoelectric (acoustic) deep-level transient spectroscopy (A-DLTS) were introduced. The former SAW technique uses a nonlinear AE interaction between the SAW electric field and free carriers in an interface region, which generates a transverse acoustoelectric signal (TAS) across the structure. Both the dc part of the TAS, called transversal acoustoelectric voltage and hf parts of the TAS have been used to study interface traps.[17–19] The latter longitudinal acoustic wave (LAW) technique uses an acoustoelectric response signal (ARS) observed at the interface of the semiconductor structure when a longitudinal acoustic wave propagates through the structure.[20,21]

The LAW, following the pressure modulation of the charge at the semiconductor structure interface, evokes the change of the potential difference that manifests as an ARS. The ARS produced by the interface of MOS structure is then very sensitive to any changes in the space charge distribution in the interface region and its dependence on the bias voltage (U_{ac}-U_g curve) in the case of very thin oxides can be used to study the distribution of interface states.

In the present contribution, the main principles of the acoustic spectroscopy of interface states in MOS structures with a very thin oxide layer are presented. The results obtained on the set of MOS structures prepared by NAOS technology to verify the method are presented, compared, and discussed.

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II. THEORETICAL PRINCIPLES

The interface states at MOS interfaces change their charge state depending on whether they are filled or empty and can be of two categories, donor type (neutral when filled and positive when empty) and acceptor type (negative when filled and neutral when empty). However, the state occupancy varies with gate voltage U_g that changes the band bending ($q\Phi_s$). The gate voltage U_g relates to surface potential φ_s following the equation[11]

$$U_g = \phi_s - \frac{Q_s(\phi_s)}{C_{ox}} - \frac{Q_{it}(\phi_s)}{C_{ox}} + \phi_{ms} - \frac{Q_{ox}}{C_{ox}}, \quad (1)$$

where Q_s is the semiconductor charge, Φ_{ms} is work function difference between gate and semiconductor, Q_{it} is trapped charge at the interface state, Q_{ox} is oxide charge, and C_{ox} is oxide capacitance. The last two terms in Eq. (1) represent the flat band voltage U_{fb}. The charge trapped into interface states changes with any change in the band bending.

The basic principle of an acoustoelectric response signal creation can be explained using the idea of an acoustic wave passing through the MOS structure characterized by the particular space charge region at the interface. Schematic illustration of such MOS structure and its equivalent circuit with interface states is shown in Fig. 1. Here, the buffer rod is used to separate out the acoustoelectric signal produced by MOS structure from the input acoustic pulse and the capacitor C_v protects the receiver input against the dc voltage. The ac voltage U_a represents the acoustoelectric signal creation by the MOS interface due to the interaction with an acoustic wave.

The acoustic wave characterized by acoustic pressure $p = p_0 \cos(\omega t - kx)$, following the pressure modulation of charge density at the MOS interface region evokes the potential difference that manifests as an ARS signal. The ARS produced by the MOS structure propagating by longitudinal acoustic wave can be then expressed using the similarity with the case of electromechanical capacitance transducer of thin planar structure ($d \ll \lambda$) for which the ARS, $U_{ac} \sim U(\delta C/C)$, coincidently provides the relative capacity change relation[22,23]

$$\frac{\delta C}{C} = \frac{\delta x}{x} = \frac{\delta \sigma}{K} = \frac{p}{K}, \quad (2)$$

where $\delta x/x$ is the relative deformation of the capacitor in the x-axis direction, p_0 is the acoustic pressure amplitude, σ is the mechanical stress produced by the acoustic wave, and K is the elastic modulus.

Using Eqs. (1) and (2) and considering the equivalent circuit, the ARS produced by the MOS structure can be expressed by the relation

$$U_{ac} = \phi_s \frac{p}{K_s} - \frac{Q_s(\phi_s)}{C_{ox}} \frac{p}{K_i} - \frac{Q_{it}(\phi_s)}{C_{ox}} \frac{p}{K_i}, \quad (3)$$

and its amplitude

$$U^o_{ac} = \left| \phi_s \frac{p_0}{K_s} - \frac{1}{C_{ox}} \frac{p_0}{K_i} [Q_s(\phi_s) + Q_{it}(\phi_s)] \right|, \quad (4)$$

where K_s and K_i are the elastic moduli of the semiconductor and insulator, respectively, and the physical meaning of the absolute value is that the ARS cannot differ the polarity of total charge or potential. For the oxide charges, we can suppose their influence only in rare cases and in the following considerations, they are neglected. If the situation in the structure without any interface states ($Q_{it} = 0$) is indexed as "ideal" and then, using Eq. (1), the last relation can be expressed in the form

$$U^0_{ac}(ideal) = \left| \frac{p_0}{K_s} |(U_g - U_{fb})| + \frac{Q_s}{C_{ox}} \frac{K_i - K_s}{K_s K_i} p_0 \right|. \quad (5)$$

As it can be seen from Eq. (5), the ARS of ideal MOS structure is the superposition of a linear term with zero at flatband voltage and a term representing the contribution from the semiconductor charge Q_s. To determine the energy distribution of interface states, it is necessary to know the dependence of the semiconductor charge on the surface potential for an ideal MOS structure. This dependence can be obtained using the Terman's model.[2]

The quantity Q_{it} depends on the interface charge state and its occupation by carriers and can be generally expressed as[10]

$$Q_{it} = q \int_{E_v}^{E_i} D_{it}(E_t)[1 - f(E_t)]dE_t - q \int_{E_i}^{E_c} D_{it}(E_t) f(E_t) dE_t, \quad (6)$$

where q is the elementary charge, D_{it} is the density of the interface states, E_v and E_c are the energies of the valence and conduction band edges, E_i is the intrinsic Fermi level, and $f(E_t)$ is the occupation probability of the energy level E_t.

The interface trapped charge can be expressed through the deviation of the ARSs of real and ideal structures, comparing Eqs. (4) and (5), as

$$Q_{it} = S(U^0_{ac} - U^0_{ac}(ideal)), \quad (7)$$

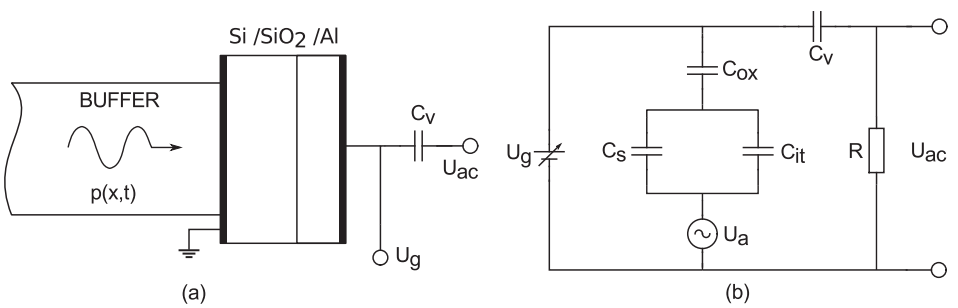

FIG. 1. Schematic illustration of MOS structure passing by a longitudinal acoustic wave (a) and its equivalent circuit including the gate voltage source (b).

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where $S = C_{ox}K_s/p_o$. The interface state density D_{it} can be then expressed, describing the ARS-voltage curves for ideal and real MOS structures, by the relation

$$D_{it}(E_t) = \frac{1}{q}\left|\frac{dQ_{it}}{d\phi_s}\right| = \frac{1}{q}\left|S\frac{d\left(U_{ac}^0 - U_{ac}^0(ideal)\right)}{d\phi_s}\right|. \quad (8)$$

Equation (8) allows then to determine the distribution of interface states from the measured ARS.

The energy level E_t in the band gap of the semiconductor, corresponding to interface traps density $D_{it}(E_t)$, can be calculated then from the equation[11]

$$E_t = E_v + \frac{E_g}{2} + q\phi_s \pm k_B T \ln\left(\frac{N_{D,A}}{n_i}\right), \quad (9)$$

where E_g is the semiconductor band gap energy, $N_{D,A}$ is the concentration of the donors or acceptors, k_B is the Boltzmann's constant, and T is the thermodynamic temperature. The plus sign in Eq. (9) corresponds to the n-MOS and the minus sign corresponds to the p-MOS structure.

In the case of real MOS structure with the interface states, the $U_{ac}^0 - U_g$ characteristics contain the information about the charge at the interface states and because the ARS reflects directly changes in the space charge distribution at the interface region, the interface state density can be extracted comparing the real (measured) and ideal (calculated) $U_{ac}^0 - U_g$ curves (Eq. (8)). As the interface state occupancy varies with the gate bias, the corresponding changes manifest as hops on the real $U_{ac}^0 - U_g$ curve comparing with the ideal one (Fig. 2). To understand the origination of these hops, the ideal and simulated real $U_{ac}^0 - U_g$ characteristics of n-type MOS capacitor (Fig. 2) are compared with the changes in the bands bending of such structure containing assumed two kinds of donor type interface states (Fig. 3).

At zero bias (Fig. 3(a)), interface states present above silicon Fermi level E_{fs} are empty, while those below E_{fs} are occupied by electrons. The surface potential φ_s causes the weak accumulation when electrons are attracted to the semiconductor surface and the semiconductor bands bend as shown in Fig. 3(a). As gate bias is less negative, the surface

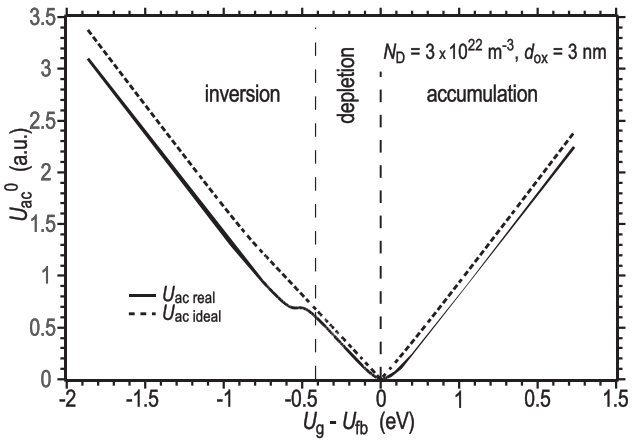

FIG. 2. Theoretical $U_{ac}^0 - U_g$ characteristic of "ideal" n-MOS structure without any interface states (dotted line) compared with simulated "real" $U_{ac}^0 - U_g$ curve corresponding to two kinds of interface states (solid line).

electron density decreases to zero until the flatband (Fig. 3(b)). By the application of a positive bias U_g (continuously accumulated), the electrons are attracted to the silicon surface and zero voltage bands bending increases and at very large positive bias, electron density at the semiconductor surface exceeds electron density in the bulk. So that starting from the flatband to a positive gate bias, the accumulation region on $U_{ac}^0 - U_g$ curve occurs.

In the case of interface states present close to the conduction band, the change in band bending at positive bias, starting from the flatband, leads to the filling of interface states initially present above Fermi level (Fig. 3(c)). That causes a decrease of electron density at the semiconductor surface as well as interface state charge Q_{it} that results in the decrease of the ARS as far as all states are filled (Fig. 3(b)). The next increase of positive gate voltage results in the increase of accumulation charge and consequently the increase of the ARS.

Starting from the flatband to a negative bias, electrons are repelled from the semiconductor surface resulting in the formation of a depletion region. As negative gate bias is increased, the depletion region widens following the formation of inversion layer where the surface hole density increases. Simultaneously, the interface states present initially below Fermi level become unoccupied (Fig. 3(d)), which results in the decrease of Q_{it} and consequently the measured ARS. The presence of another interface states causes another drop of the ARS. Calculating the difference between the ideal and simulated real $U_{ac}^0 - U_g$ curves and using relation (8), the simulated interface states distribution was determined as shown in Fig. 4.

However, the leakage current represented by tunneling transport in the case of a very thin oxide layer (<10 nm) causes a significant problem. The tunneling current for the very thin oxide layer influences the division of the applied voltage U_g between the semiconductor and insulator layer and for the oxide layer thickness <2 nm, the whole applied voltage practically spreads across the semiconductor, especially in the range of inversion.[24] Concerning the tunneling process, the transport of free charge carriers through the thin oxide layer caused by applied electric field has to be taken into account in cases where the tunneling current following with the Fowler-Nordheim mechanism[25] induces additional change of the ARS

$$\Delta U_{ac} = A\left(U_g^2 + B\right)e^{-\frac{C}{U_g}}, \quad (10)$$

where A, B, and C are constants. The tunneling current is supposed to be dependent only on the applied voltage. The simulation of the "ideal" ARS inclusive the calculation of tunnel current contribution gives a new ideal ARS, U_{ac}^0 *(tunnel)*. The interface charge can be then expressed using the new ideal and real ARS-voltage curves for MOS structure by the relation

$$Q_{it} = S|(U_{ac}^0 - U_{ac}^0(tunel))|. \quad (11)$$

The calculation of ideal $U_{ac}^0 - U_g$ curves including the tunneling process of the free charge carriers through the thin

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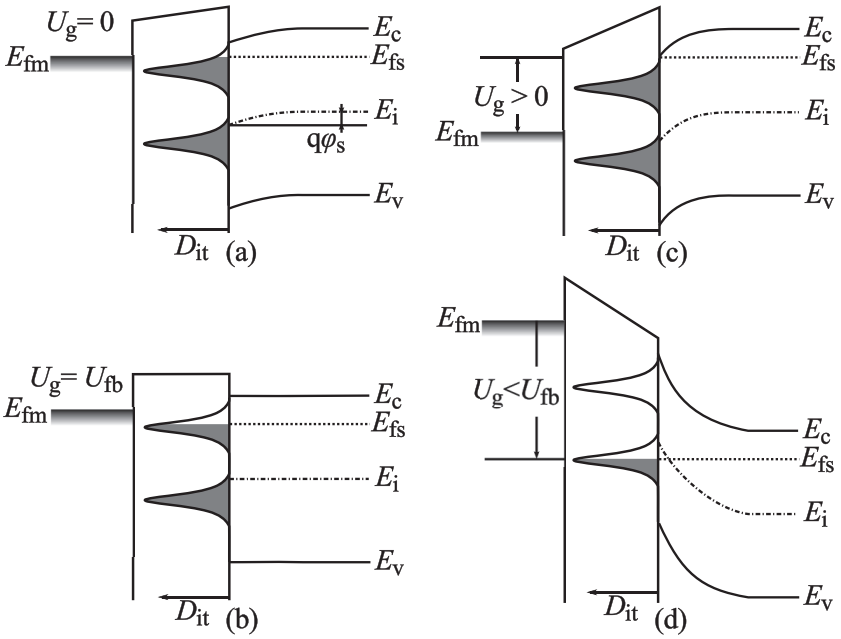

FIG. 3. Energy band diagrams of n-type Si based MOS structure with no bias (a) and as a function of bias at flat-bands (b) at accumulation (c), and at inversion (d) representing the interface states emptying and/or occupying processes of two kinds of interface states. Energy values E_{fs} and E_{fm} are the Fermi levels in the silicon and in the metal, respectively.

oxide layer changes the original "ideal" ARS, $U^0_{ac}(ideal)$ and gives a new ideal ARS, U^0_{ac} (*tunnel*). Fig. 5 illustrates the comparison of $U^0_{ac}(ideal)-U_g$ and $U^0_{ac}(tunnel)-U_g$ curves calculated for 3 nm thick oxide.

Except the leakage current, the Schottky contact on the metal-semiconductor interface can be the reason for some deviation in the measured $U^0_{ac} - U_g$ dependence, especially near the flatband. To eliminate this influence, the added capacitance of Schottky contact[26]

$$C_{sch} = \sqrt{\frac{\varepsilon_{Si}\varepsilon_0 qN}{2(U_c - U_{sch})}} \tag{12}$$

was included in the calculation procedure. Here, U_c is the contact potential, $U_{sch}=f(U_g)$ is the voltage across the metal-semiconductor interface, and $\varepsilon=\varepsilon_o\varepsilon_r$ is the permittivity of semiconductor.

The sensitivity of presented method depends on the accuracy of the acoustoelectric response signal U^0_{ac} measurement, the acoustic signal stability, and the ability to distinguish the changes ΔU_{ac} between the real and "ideal" $U^0_{ac} - U_g$ characteristics.

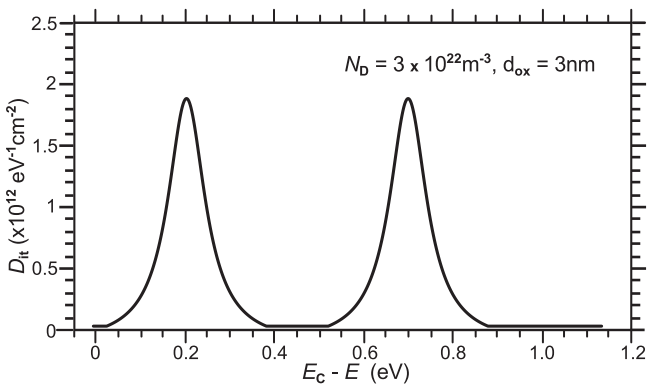

FIG. 4. Simulated distribution of interface states calculated using the ideal and simulated real $U^0_{ac} - U_g$ curves (Fig. 2) for oxide thickness $d_{ox}=3$ nm.

It should be noted that another acoustic technique using a nonlinear acoustoelectric interaction between SAW electric field and free carriers at MOS interfaces could be also used to study interface states by the same way. The SAW technique is based on the fact that the interaction produces TAS across the structure whose hf part can be used to study interface states.[20,27] However, the geometric arrangement of such investigation requires samples with larger surfaces.

III. EXPERIMENTAL

The acoustoelectric investigation of interface states to verify the theoretical principles was applied to the Si MOS structures with very thin oxides prepared on both n- and p-type Si substrates growing by nitric acid (HNO_3) oxidation method of Si (NAOS), which can be performed at relatively low temperatures (~120 °C)[5,6] as well as with high-κ (HfO_2) dielectric layer.

N-Si MOS structures were fabricated from phosphorus-doped Si (100) wafers with ~10 Ω cm resistivity. After

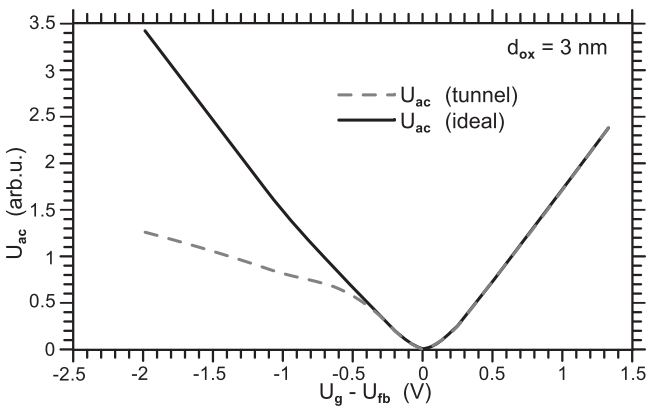

FIG. 5. Theoretical $U^0_{ac} - U_g$ characteristic of "ideal" n-MOS structure without any interface states (dotted line) compared with simulated "ideal" $U^0_{ac} - U_g$ curve for the same structure comprehensive of tunneling process (solid line).

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TABLE I. Summary of investigated Si MOS structures and their characteristics.

Sample	Oxide thickness (nm)	Si type	Treatment
2P0A	3.2	n	POA at 250 °C in N_2 for 1 h
3POA	9.2	n	POA at 250 °C in N_2 for 1 h
5POA	3.8	n	POA at 250 °C in N_2 for 1 h
NAOS	10.7	p	No treatment
POA7	10.7	p	POA at 700 °C in N_2 for 20 min
2A	0.6 (SiO_2) + 5.0 (HfO_2)	n	No treatment

cleaning the wafers using RCA method and etching with dilute hydrofluoric acid, they were immersed in HNO_3 aqueous solutions of various concentrations (58%–68%) at temperature ~110–120 °C for different reaction times to prepare different oxide thickness.[28] P-Si MOS structures were fabricated on boron-doped p-type Si(100) wafers with 10–15 Ω cm resistivity. After RCA cleaning of the Si wafers and the removal of a native oxide layer, a thin oxide layer was formed by immersing the Si wafers in 70% HNO_3 aqueous solutions at 120 °C.[29]

After rinsing with ultrapure water, the wafers were divided to several parts and some parts were treated by post-oxidation annealing (POA) in nitrogen performed for 1 h at 250 °C (n MOS) or 700 °C for 20 min (p MOS). Then, aluminum (Al) dots of 0.15 and 0.30 mm diameter were formed on all parts of prepared wafers, resulting in ⟨Al/SiO_2/Si⟩ MOS diodes. The thickness of the SiO_2 layer was estimated from XPS and/or ellipsometry measurements.

The MOS structure with NAOS-SiO_2/HfO_2 gate dielectric layer was prepared on n-type Si substrate where 5 nm HfO_2 oxide was deposited by atomic layer deposition on 0.6 nm NAOS-SiO_2 oxide film prepared in ~100% HNO_3 vapor.[30] It is well known that when HfO_2, as most of the high-k materials, is deposited in direct contact with Si, an interfacial oxide layer of few nanometers thick is formed.[31] One of the possible procedures to avoid reaction on Si surface is about to grow a controlled free-defect SiO_2 barrier layer between substrate and high-κ dielectric.

The representative set of investigated Si MOS structures including the type of Si, the oxide thickness, and some other parameters is summarized in Table I. The presented choice of MOS structures was made to represent the results obtained on various types of structures including n- and p-type Si substrates, various oxide thickness as well as various kinds of oxide layers.

The experimental arrangement of the present measurement technique is shown in block diagram in Fig. 6. The computer system was used to trigger the apparatus—Pulse Modulator and Receiver—MATEC 7700, to drive bias voltage as well as to record and evaluate the ARS as a function of applied bias voltage. A longitudinal acoustic wave of frequency 13.2 MHz was generated using $LiNbO_3$ transducer in the arrangement illustrated in the A-detail. The ARS produced by the MOS structure was then detected by Receiver, selected using the SRS Gated Integrator and Box-car Averager, recorded and stored by a computer. The $U_{ac}^0 - U_g$ curves were measured using the programmable voltage source, type HAMEG-HM8131-2, providing both the linear increase (decrease) of the gate bias and the variation of increasing (decreasing) rate.

As it was already mentioned, the sensitivity of the used acoustic spectrometer to determine the density of interface states depends on several parameters given by both experimental arrangement and following calculation procedure. The calculated sensitivity limit for our experimental arrangement is $5.0 \times 10^{10}\,eV^{-1}cm^{-2}$. However, in the case of measured MOS structures, especially those with thinner oxide layers, the stability of the measured acoustoelectric signal allowed to determine the density of interface states only with the sensitivity better than $1.0 \times 10^{11}\,eV^{-1}cm^{-2}$.

To know the electrical characteristics, the current–voltage (*I-V*) and capacitance–voltage (*C-V*) characteristics were recorded with HP 4192A impedance analyzer and/or FLUKE PM 6306 programmable automatic RLC meter. The $U_{ac}^0 - U_g$ characteristics were measured at room temperatures (~300 K) and determined interface states distributions were also compared with Acoustic-DLTS results.

IV. RESULTS AND DISCUSSION

The presented distribution of interface states of representative set of Si MOS structures was obtained from the

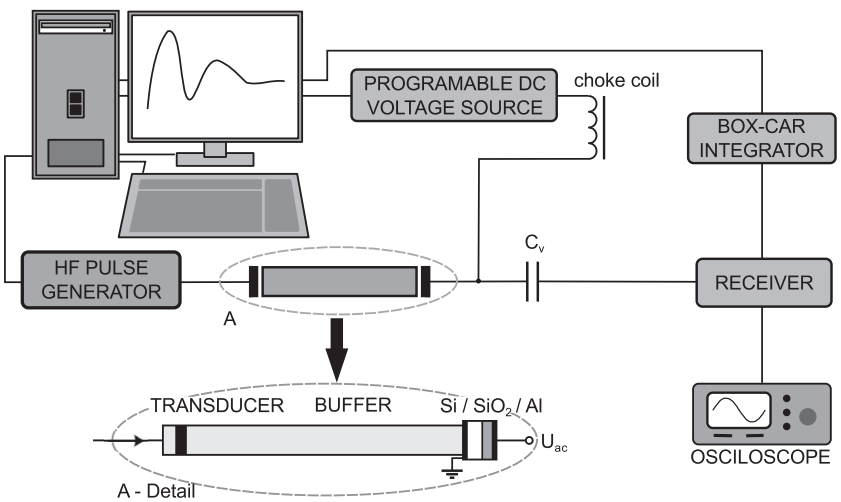

FIG. 6. Block diagram of the experimental setup with the detailed sample configurations.

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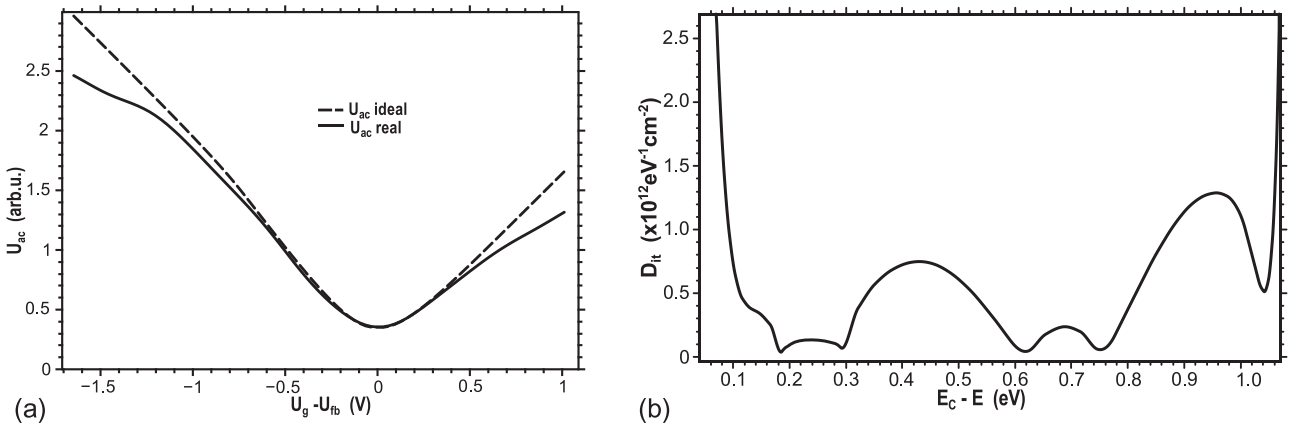

FIG. 7. Measured and ideal $U_{ac}^0 - U_g$ curves (a) and calculated distributions of interface state density (b) for 5POA structure ($d = 3.8$ nm).

measured $U_{ac}^0 - U_g$ characteristics and theoretical principles described before. Fig. 7(a) shows both measured and fitted (ideal) $U_{ac}^0 - U_g$ characteristics for n-type Si MOS structure with 3.8 nm thick oxide (5POA). For simplification and better possibility to compare individual results, there is on x-axis indicated the difference $U_g - U_{fb}$, so that zero voltage corresponds to the flatband where the ARS reaches its minimum. The measured flatband was −0.83 V. Comparing the real and ideal characteristics, several detected humps at both sides of measured characteristic corresponding to accumulated and inversion states imply the presence of high density of interface states. Fitted characteristic was calculated using the proposal model and following measured parameters related to the investigated structure, $N_D = 3.7 \times 10^{21}\,\mathrm{m}^{-3}$; $C_{ox} = 8.65 \times 10^{-3}$ F/m^2 and parameter extracted through the fitting process $p_0 = 1.1 \times 10^{11}$ Pa. Elastic moduli $K_s = 5.36 \times 10^{10}$ Pa and $K_i = 7.3 \times 10^{10}$ Pa for Si and SiO_2, respectively, were used for all investigated structures. The distribution of interface states with respect to the energy levels across the bandgap of silicon, shown in Fig. 7(b), was then calculated by using measured and fitted (ideal) $U_{ac}^0 - U_g$ characteristics (Fig. 7(a)). The determined distribution of interface states indicates its higher density at about 0.35–0.55 eV below the conduction band and also close to the valence band.

The $U_{ac}^0 - U_g$ characteristics of another two MOS structures prepared on n-type Si with oxide thicknesses 0.32 nm (2POA) and 9.2 nm (3POA) are shown in Fig. 8. Fitted characteristic was calculated using the following measured parameters related to the investigated structures, $C_{ox} = 1.28 \times 10^{-2}$ F/m^2; $U_{fb} = 0.68$ V for 2POA and $C_{ox} = 3.84 \times 10^{-3}$ F/m^2; $U_{fb} = -1.45$ V for 3POA and parameters extracted through the fitting process $p_0 = 7.28 \times 10^{10}$ Pa for 2POA and $p_0 = 1.95 \times 10^{11}$ Pa; $U_c = 0.2$ V for 3POA. The donor concentrations in all n-type Si wafers were the same. We can see, in both real characteristics, similar process but with different region (beginning) of tunneling process which, in the case of thicker oxide layer, begins at higher reverse voltage that coincides with our assumption. Corresponding determined distributions of interfaced states are illustrated in Fig. 9. Calculated distribution suggests higher density of interface states in both structures at about 0.55–0.70 eV for sample 2POA and at 0.45–0.70 eV for sample 3POA. It should be noted that obtained results coincide very well with previous results obtained from the Acoustic-DLTS spectra,[28] which indicated interface states about 0.42 eV (5POA), 0.66 eV (2POA), and 0.64 eV (3POA) below the conduction band. Both kinds of interface states, with the energy near the midgap, were observed for SiO_2/Si interfaces with ultrathin oxide by means of XPS under bias. They are attributed to isolated Si dangling bonds, with which no atoms in the oxide layer interact, or were attributed to Si dangling bonds interacting weakly with an oxygen or Si atom in the oxide layer.[4]

Fig. 10(a) shows the measured and ideal curves of the ARS dependence on the gate voltage (U_{ac}^0–U_g curves) for the NAOS samples that were used for the determination of

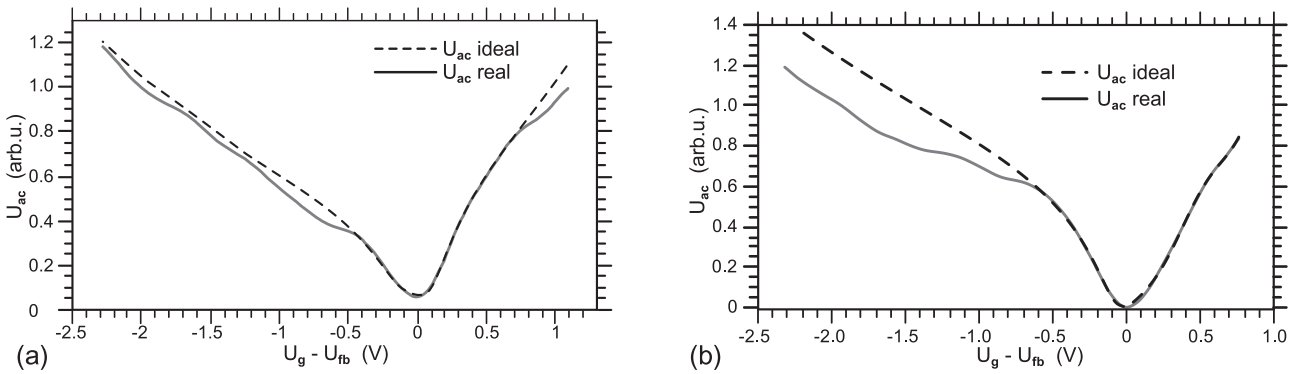

FIG. 8. Measured and calculated $U_{ac}^0 - U_g$ characteristics of samples 2POA ($d = 3.2$ nm) (a) and sample 3POA ($d = 9.2$ nm) (b).

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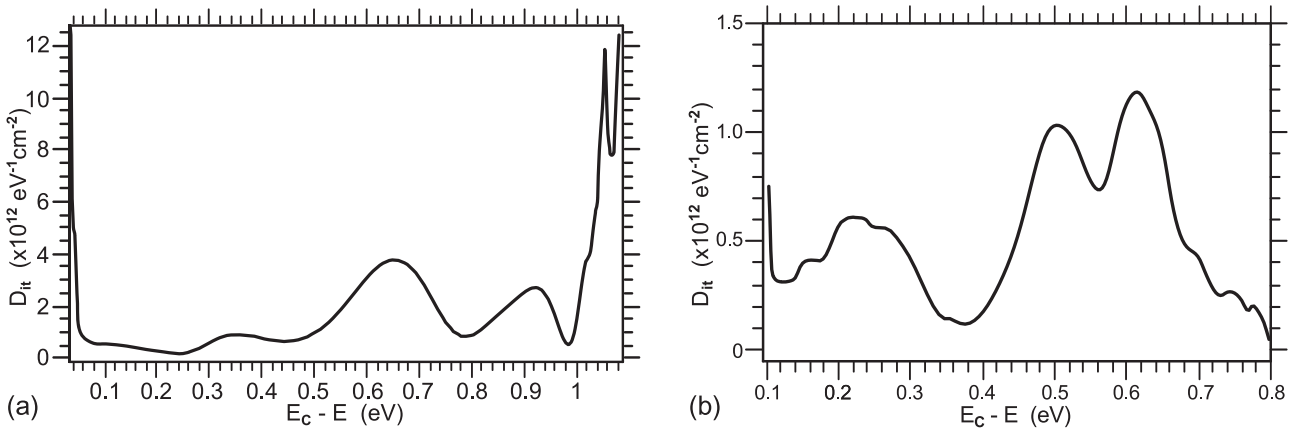

FIG. 9. Distribution of interface state density of samples 2POA (a) and 3POA (b) calculated using measured and ideal $U_{ac}^0 - U_g$ curves (Fig. 8).

interface states distribution illustrated in Fig. 10(b). Fitted characteristic was calculated using following measured parameters related to the investigated structure, $N_A = 4.0 \times 10^{22}\,\mathrm{m}^{-3}$; $C_{ox} = 3.45 \times 10^{-3}$ F/m^2, $U_{fb} = -0.95$ V and parameter extracted through the fitting process $p_0 = 4.3 \times 10^{10}$ Pa; $U_c = 0.2$ V. This figure presents also the comparison of interface state distribution for another NAOS sample with thermal treatment, POA7. It is evident that the density of the interface states is lower after the POA treatment, indicating the elimination of interface states by the annealing processes.

It should be noted that A-DLTS spectra of investigated samples correspond to the interface states with the activation energies 0.21 and 0.24 eV above the valence band edge, respectively,[29] and the observed individual A-DLTS spectra coincide with the density of interface state distribution determined from U_{ac}–U_g measurements. The interface states with an activation energy ≈0.2 eV should correspond to Si dangling bonds interacting weakly with oxygen or Si atoms having unpaired electron.[4,10] The decrease of the density of interface state distribution after the thermal treatment can be attributed to the fact that the POA treatment eliminates some suboxide species, which is a reason also for the decrease of the leakage current density.[4,10]

Fig. 11(a) shows the expanded part of complete measured ARS dependence on gate voltage, U_{ac}-U_g curve for the Si/SiO$_2$/HfO$_2$/Al MOS structure A2 (inside) corresponding to the Si/SiO$_2$ interface including its theoretical U_{ac}-U_g characteristics. The difference from previous structures is evident and unlike U_{ac}-U_g characteristics of Si/SiO$_2$ interface containing one minimum corresponding to flatband, the U_{ac}-U_g curve of Si/SiO$_2$/HfO$_2$, besides minimum corresponding to flatband on Si/SiO$_2$ interface at −0.58 V, contains another minimum at +1.5 V corresponding to the SiO$_2$/HfO$_2$ interface. The reason that the flatband corresponding to this Si/SiO$_2$ interface is at quite large ARS compared with the ARS of SiO$_2$/HfO$_2$ interfaces is probably due to the large fixed charge density that is then compensated (decreasing part of U_{ac}-U_g characteristics). Using these real and theoretical characteristics, the density of interface states could be determined (Fig. 11(b)). Fitted characteristic was calculated using the following measured parameters related to the investigated structure, $N_D = 4.7 \times 10^{21}\,\mathrm{m}^{-3}$; $C_{ox} = 1.95 \times 10^{-2}$ F/m^2 and parameter extracted through the fitting process $p_0 = 2.8 \times 10^{10}$ Pa; $U_c = 0.22$ V. We can see in the first place that our theoretical calculation of ideal U_{ac}-U_g curve very well coincides with real one and second that the density of interface states course corresponds to the presence of interface states with energies around ∼0.2–0.3 eV obtained

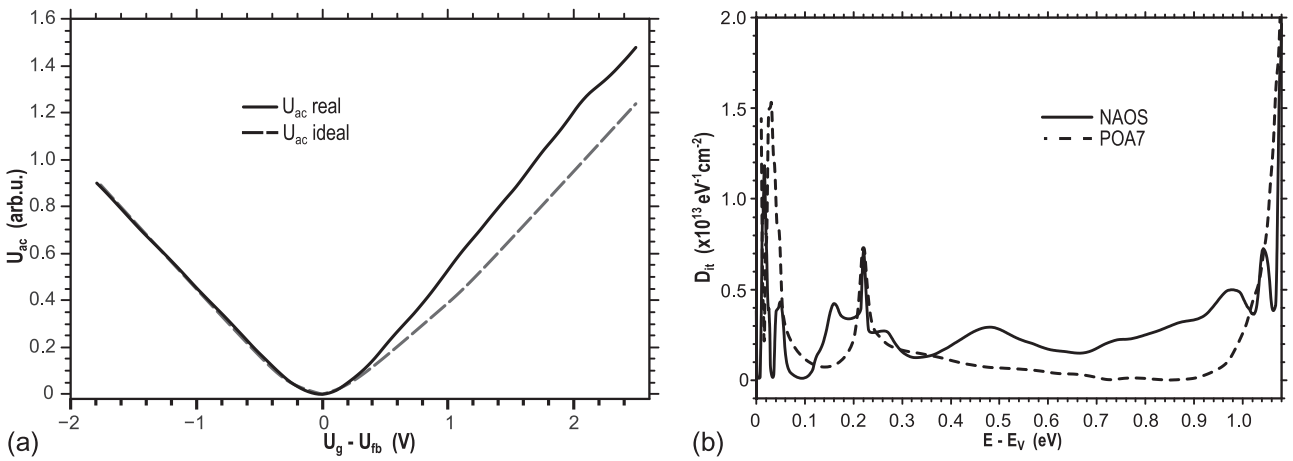

FIG. 10. Measured and ideal $U_{ac}^0 - U_g$ curves for NAOS structures (a) and calculated distributions of interface state density for structures NAOS and POA7 ($d = 10.7$ nm) (b).

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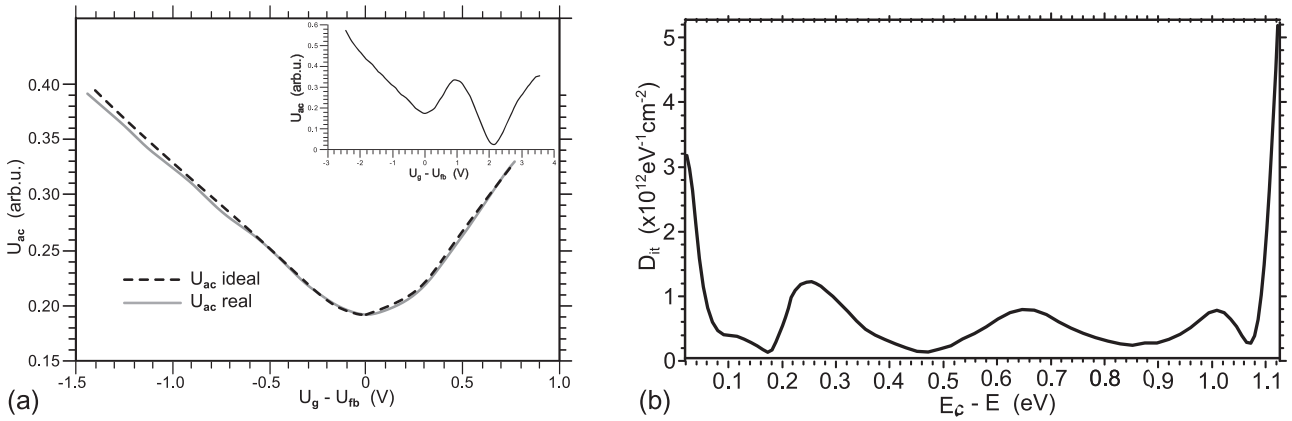

FIG. 11. Theoretical U_{ac}-U_g characteristics of "ideal" $Si/SiO_2/HfO_2$ structure (dashed line) and compared with real $U^0_{ac} - U_g$ curve (thick line) for original structure (A2) (a) and distribution of interface states calculated from $U^0_{ac} - U_g$ characteristics (b).

in previous results using A-DLTS[30,31] and can be attributed to the Si/SiO_2 interface. However, the calculation for the SiO_2/HfO_2 interface[32] allowed us to include also the defects at the interfacial layer that were detected by A-DLTS.

V. CONCLUSION

The investigation of MOS structures with very thin oxides by the new acoustic technique utilizing the acousto-electric response signal produced by MOS interfaces as a function of gate voltage (U_{ac}-U_g characteristics) is presented as an effective tool for the determination of interface states distribution. Comparison of the measured and fitting (ideal) U_{ac}-U_g characteristics allow to determine the interface states distribution and together with A-DLTS, it provides complete acoustic investigation of MOS structures and also provides information comparable with C-U_g and G-U_g measurements. The presented technique used for interface states investigation induced also some advantages compared with other techniques: the ARS is produced directly by the interface containing the space charge so that any changes in its distribution are immediately reflected by the ARS; the strong acousto-lattice interaction allows to discover some new interface states; the quality of the ohmic contacts should not play so important role as in electrical techniques.

The investigation of several kinds of MOS structures formed by NAOS method verified the presented method. The interface state distributions were determined for MOS structures with very thin oxides prepared on both n- and p-type silicon wafers as well as in combination with high-κ dielectrics. The position of determined interface states coincides with both results obtained by A-DLTS and results obtained by different techniques.

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