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Materials Science and Engineering B 124–125 (2005) 327–330

MATERIALS SCIENCE & ENGINEERING B

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Characteristics of silicon p–n junction formed by ion implantation with in situ ultrasound treatment

V.P. Melnik, Y.M. Olikh, V.G. Popov, B.M. Romanyuk, Y.V. Goltvyanskii, A.A. Evtukh *

Institute of Semiconductor Physics, National Academy of Science of Ukraine, 41 Prospect Nauki, 03028 Kiev, Ukraine

Abstract

The forming peculiarities of electrically active impurities (B, As, Sb) in silicon with in situ ultrasound (US) excitation have been investigated. The US excitation influences significantly on the redistribution of defects generated by ion implantation. It is shown that there is the possibility of controlling the p–n junction parameters by varying the frequency and intensity of US excitation. The changing of p–n junction parameters is caused by the influence of the US treatment due to interaction of Si structural defects with implanted impurity. The changing of both the quantity of defects and impurities redistribution are realized with the activation annealing that follows implantation. The influence of US treatment on Si shallow p–n junction parameters has been studied in detail. It is shown that the use of US defect engineering is perspective at forming high-quality Si p–n junctions.

Keywords: Si p–n junctions; Electrically active impurities; Implantation; Ultrasound treatment

1. Introduction

Ion implantation is widely used in technology of ICs due to it main advantages: (i) possibility of precise control of the quantity of introduced impurity atoms and (ii) the easy control of the distribution profile of implanted atoms in the substrate [1]. The further development of CMOS and BiCMOS technologies requires the reduction of the p–n junction depth below 30 nm. There are some phenomena which can cause the redistribution of doping atoms during p–n junction fabrication, such as: (i) ion channeling during implantation, (ii) transient enhanced diffusion (TED) [2], (iii) doping dose loss at the SiO_2–Si interfaces, and (iv) formation of clusters [3].

The ion implantation of As gives the possibility to create shallow n^+ layers due to it low projection length (R_p) (≈30 nm at $E = 30$ keV). Introduction of heavy ions creates an amorphous layer and can reduce the channeling effect. For formation of ultra-shallow p^+ layers, as a rule, BF_2 ions are used.

The use of ultrasound treatment (UST) allows improvement of the shallow p–n junction parameters. It has been suggested that ultrasound waves propagating through the semiconductor can affect the generation of point defects [4,5]. In our previous works [6–8], the influence of in situ ultrasound treatments during ion implantation on amorphization and peculiarities of p–n junction formation in silicon have been studied. In addition, the suppression of boron TED in silicon due to influence of UST have been revealed.

In this work, we study the influence of in situ UST with ion implantation on electrical parameters of ultra-shallow p–n junctions. The possibility to improve p–n junction parameters by the in situ UST is demonstrated.

2. Experiment

The phosphorus-doped ($\rho = 12\ \Omega$ cm) and boron-doped ($\rho = 10\ \Omega$ cm) (1 0 0)-CZ-Si wafers were used for p^+ and n^+ shallow doped layer formation, respectively. The samples were mounted inside the implanter chamber on a piezoelectric transducer with an acoustics binder. Low-amplitude ultrasound vibrations were generated in the wafer by operating the transducer in a resonance vibration mode. The basic resonance frequency was varied from 6 to 14 MHz. The amplitude of the generated deformation did not exceed 1×10^{-5} of the lattice constant corresponding to an acoustic power of 0.2–0.5 W cm^{-2}. For implantation, we used B^+ and As^+ ions with energies $E = 33$ and 50 keV, respectively, at a dose of 5×10^{14} cm^{-2}, with implan-

* Corresponding author. Tel.: +380 44 525 3852; fax: +380 44 525 8342.
E-mail address: evtukh@rambler.ru (A.A. Evtukh).

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doi:10.1016/j.mseb.2005.08.039

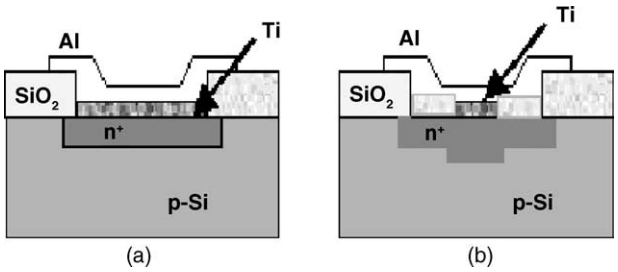

Fig. 1. Different types of contacts to shallow p–n junction without (a) and with (b) deep diffusion region.

tation through a silicon dioxide layer of 125 nm thickness with BF_2 and 30 nm thick for As. The impurity activation was performed by rapid thermal annealing (RTA) in the temperature range of 850–1000 °C.

For measurement of p–n junction parameters, specially designed test structures have been developed. They include capacitors with various areas, perimeters and area to perimeter ratios. The areas of the p–n junction were in the range of 2.25×10^2 to 7.85×10^5 μm^2. Two different configurations of metal electrode to p–n junction are shown in Fig. 1. The two-layer metallization (Ti–Al) with the next sintering at 450 °C during 15 min in N_2 was used for the contact formation to shallow p–n junctions. The technological processes used in formation of investigated structures are compatible with CMOS technology of IC.

3. Results

3.1. Ion implantation with boron

Experimental results on the influence of technological processes on parameters of shallow p^+–n junction show that activation annealing both at $T = 850$ °C, and at $T = 1000$ °C results in high breakdown voltages of p^+–n junction. But in the case of annealing at $T = 1000$ °C, the contact resistance is sometimes lower in comparison with $T = 850$ °C (0.3 and 1.5 Ω, respectively) as was revealed by the measurements of metal–semiconductor contact resistance. With boron implantation, the essential difference between parameters of p^+–n junction formed without and with in situ UST was observed. The current–voltage (I–V) characteristics of diodes with a circled p–n junction of 9.8×10^3 μm^2 area are shown in Fig. 2. The current in the forward direction (1, 2) and in the reverse directions (1a, 2a), in such structures is practically independent of the existence of a guard ring by the p^+–n junction perimeter. The ideality factor of diode structures formed without and with UST was $n = 1.099$ and $n = 1.089$, respectively. As can be seen from Fig. 2, the forward current at the saturation and leakage current at reverse bias are lower in case of in situ UST.

Comparison of the barrier capacity of p^+–n junctions measured at reverse bias shows a reduction at ion implantation with UST (Fig. 3a). Barrier capacity of p^+–n junction can be used for quantitative estimation of free carrier concentration in the semiconductor (in the n region of p^+–n junction). For this, the barrier capacity of p^+–n junction is represented as $1/C_b^2$–U coordinates

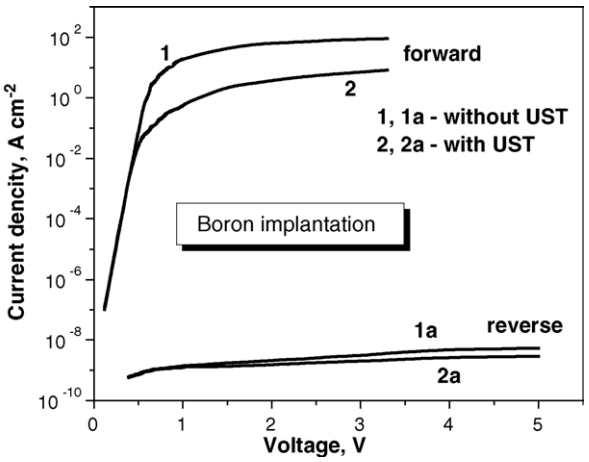

Fig. 2. Current–voltage characteristics of diodes with shallow p^+–n junctions (1, 1a) without and (2, 2a) with UST; (1, 2) forward bias, (1a, 2a) reverse bias.

as in Fig. 3a. The dependencies allow calculating the free carrier concentration using the surface differential method [9]. The results of the calculations are shown in Fig. 3b. As can be seen, the surface concentration of free carriers is noticeably higher by

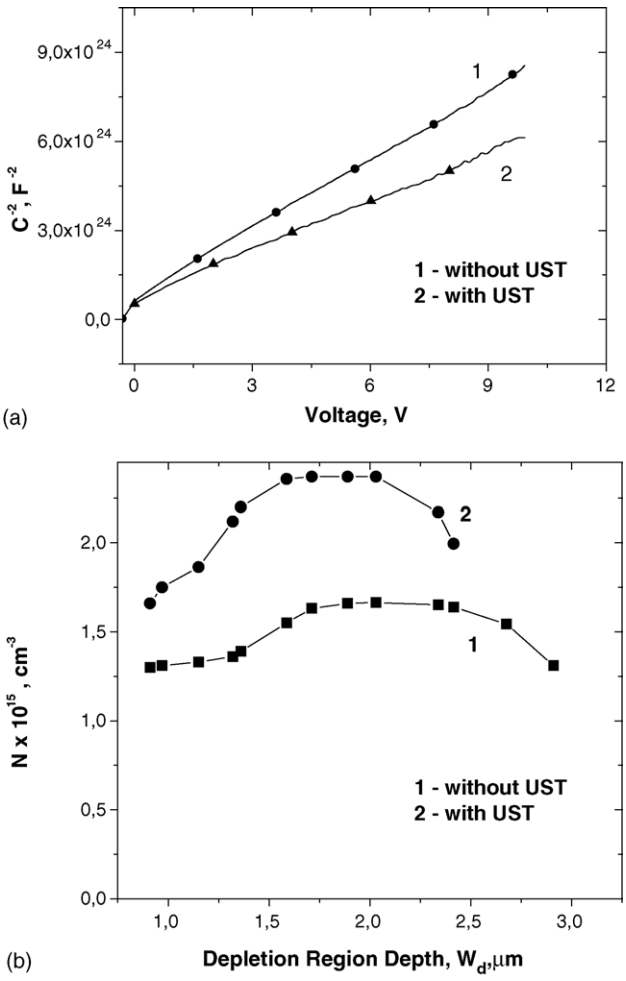

Fig. 3. Capacity–voltage characteristics of reverse biased p^+–n junction in the C^{-2}–U co-ordinates (a) and calculated dependence of free carrier concentration in silicon on width of depletion layer (b): (1) without UST; (2) with UST.

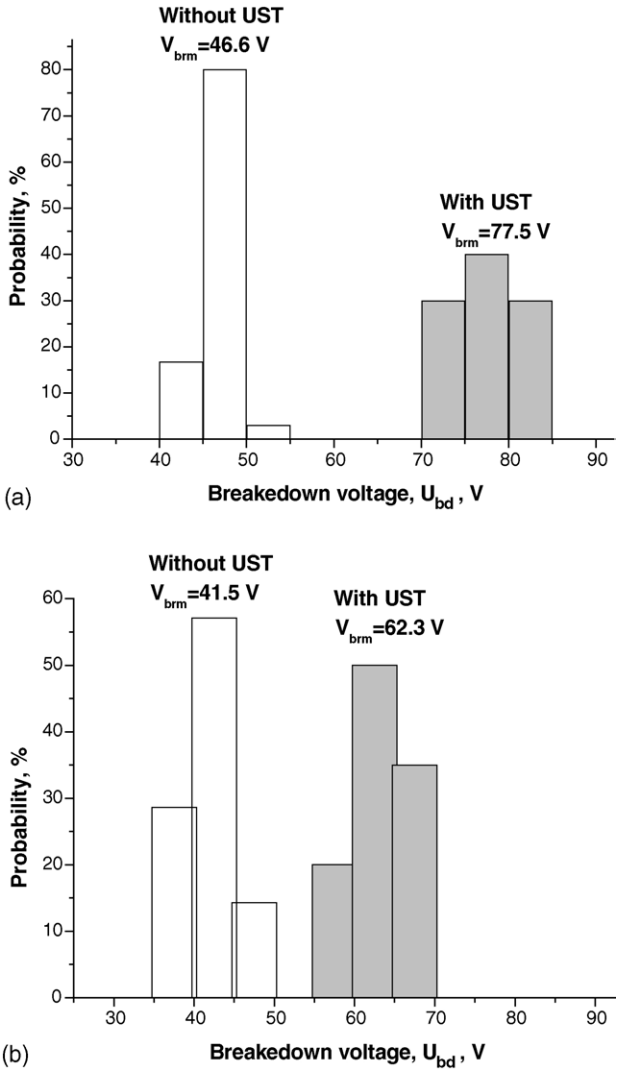

Fig. 4. Distributions of breakdown voltages of reverse biased B-doped p^+–n junction without and with UST: (a) p^+–n junction with guard ring by perimeter and (b) p^+–n junction without guard ring.

nearly a factor of 2 for the case of ion implantation with UST. These results correlate with measurements of surface resistivity by the Van der Pau method on the special square test element with a size of $100 \times 100\ \mu m^2$. The surface resistivity was 246 and 264 Ω/sq for cases with and without UST, respectively.

The investigation of breakdown voltages of p^+–n junctions with reverse bias show the increase of U_{bd} by ∼1.5 times with UST as shown in Fig. 4. This effect takes place for p^+–n junctions with and without guard rings.

3.2. Ion implantation with As

The n^+–p junctions formed by ion implantation of As with $E = 50$ keV were ∼10 nm deep. After sintering of the contacts the breakdown voltages were ∼1 V for all the structures. This was possibly caused by metal diffusion through the n^+–p junction during sintering. Then, we have compared the n^+–p junction parameters without and with UST for ion implantation on structures with deep diffusion region in the center contact as seen in Fig. 1. The n^+–p junction formed by As ion implantation with in situ UST has a sharp breakdown at U_{bd} = 10–11 V, while the n^+–p junctions created without UST has gradual breakdown beginning even at 6 V as shown in Fig. 5.

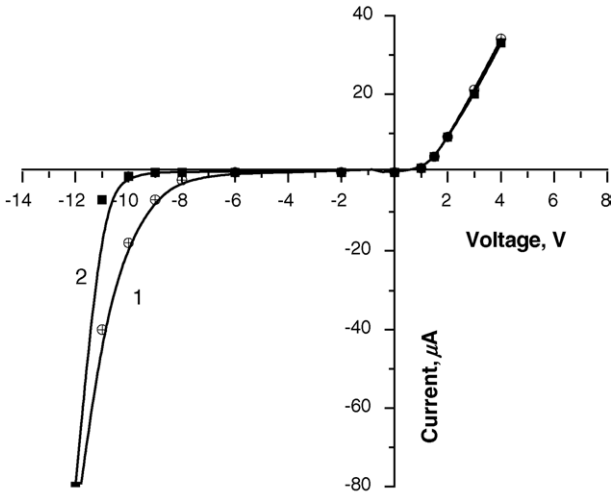

Fig. 5. Current–voltage characteristics of As-doped diodes with shallow n^+–p junctions: (1) without and (2) with UST.

4. Discussion

For explanation of obtained experimental results, we use the model based on the ultrasound wave influence on point defect redistribution, proposed in our previous papers [6–8].

The schematic images of the processes, which take place at ion implantation without and with UST are shown in Fig. 6. TED of implanted B ions is suppressed due to the presence of UST during implantation. This effect is related to UST stimulated diffusion of Si interstitials from the implanted depth region towards the bulk of wafer (Fig. 6b) [6]. Therefore, the formation of the mobile boron interstitials arising due to the interaction of Si_i and substitutional boron B_s (Fig. 6a) is also suppressed. This causes the shift of the boron profile towards the surface in samples implanted with UST.

In the case of As ion implantation, the main processes in general are similar (Fig. 6). The UST promotes the Si interstitial diffusion from implanted region into the bulk and as such suppress the TED. The impurity atoms occupy the vacancies and remain in the electrically active state in the implanted subsurface region. Processes of the vacancy complex creation can be realized, which can have influence on the As clusterization (Fig. 6a).

At ion implantation with in situ UST the depth of p^+–n and n^+–p junctions is smaller and impurity distribution is sharper as it follows from the model proposed and was confirmed by SIMS profile measurements. Such peculiarities of UST influence on the mechanisms of point defect and impurity distribution determine the main electrical parameters of shallow p–n junctions.

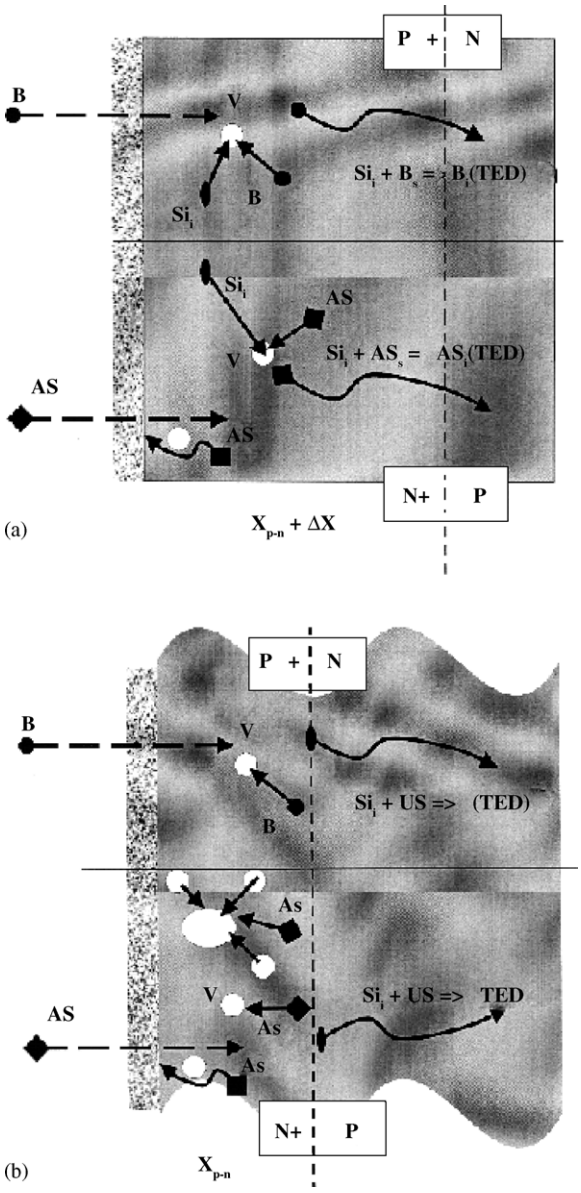

Fig. 6. Schematic images of the processes in silicon at ion implantation of B and As: (a) without UST and (b) with in situ UST.

5. Conclusions

The influence of in situ UST at ion implantation on the basic parameters of shallow p–n junction has been investigated. The increase of breakdown voltages and decrease of the leakage currents of p^+–n and n^+–p junctions were revealed by ion implantation with in situ UST. This points out the utilization of such processes can be beneficial for fabrication of high-performance semiconductor devices and ICs. A model of using the in situ UST and its influence on the impurity redistribution for ion implantation and subsequent RTA has been developed to explain the experimental results. The principal benefits in using the in situ UST for device fabrication are, in our opinion, the possibility of additional monitoring of the impurity profiles in silicon layered structures, and correspondingly, shallow p–n junction basic parameters. The UST can decrease the interstitial defect concentration in the space charge (depletion) region, and as a result, improve the device parameters.

Acknowledgement

The research described in this publication was partially supported by the STCU (Project # 2367).

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