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Fabrication and characterization of GaAs/AlGaAs lateral quantum dot developed by ultrasonic agitation

Q-Z Yang[1,2], G A C Jones[1], M J Kelly[1,2], H Beere[1] and I Farrer[1]

[1] Semiconductor Physics Group, Cavendish Laboratory, University of Cambridge, Cambridge CB3 0HE, UK
[2] Department of Engineering, University of Cambridge, 9 J J Thomson Avenue, Cambridge CB3 0FA, UK

E-mail: qzy20@cam.ac.uk

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Abstract
The multi-surface gate architecture was applied to a small lateral single quantum dot (QD). By employing ultrasonic agitation development, we tried to work out a reliable fabrication scheme for closely-spaced quantum dots, and then tested yield by measuring Coulomb blockade of QD at 300 mK. The yield results (less than 50%) show such a fabrication scheme needs to be refined further.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

A single lateral quantum dot (QD) is a small (∼100 nm diameter) metallic island connected to the source and drain electrodes through tunnel barriers [1, 2]. The electron states in the QD can be modelled by 'a particle in a box', and the energy spacings (ΔE) depend on the size of the box. For a QD with nano-scale dimensions, quantum size effects become important and energy levels in the QD are well resolved at low temperatures. Another important feature is that the energy scale for charging a single electron (e^2/C_Σ, where C_Σ is a self-capacitance of the dot) can be measured at liquid helium temperatures because of the extremely small C_Σ, which results in single electron transport (Coulomb blockade).

A common method to create quantum confinement in the two-dimensional-electron-gas (2DEG) of GaAs/AlGaAs heterostructures is the patterning of surface gates on the top of high-electron-mobility transistors (HEMTs). Application of a voltage to the gate electrodes confines the 2DEG at the heterointerface. Because of its unique features, this QD structure has been discussed as the basic building block of more complex structures for various new applications, such as current standard devices, quantum computing devices, qubits, etc. Here, the reliability of fabrication techniques and the reproducibility and stability of Coulomb oscillations are tested and investigated.

Advanced nano-fabrication techniques based on E-beam lithography have made it possible to fabricate quantum dots with dimensions much less than 1 μm. However, E-beam lithography suffers from several difficulties: (i) the proximity effect, where electrons are scattered by the substrate and return to the surface to expose nearby regions of the resist, generally limiting the uniformity of patterns and the resolution; and (ii) the concern of substrate damage caused by the high energy of the electron beam. Thus, it is necessary to evaluate the technology for a minimum feature size of 45 nm closely spaced patterns, and its required overlay accuracy has to be verified.

2. Fabrication

2.1. Design of gate-confined QD in the few-electron regime

A scanning electronic microscope (SEM) image of a single QD and its equivalent circuit is shown in figure 1. The Schottky gates are placed along side to define a quantum dot in 2DEG. The gate structure consists of four electrodes that can be independently biased, and the top centre gate electrode acts as a 'plunger' gate. When applying negative voltages to the side gates, the underlying '2DEG' is depleted and the dot area is defined in the centre. By varying the plunger gate voltage, the energy levels inside the quantum dot can be moved into and

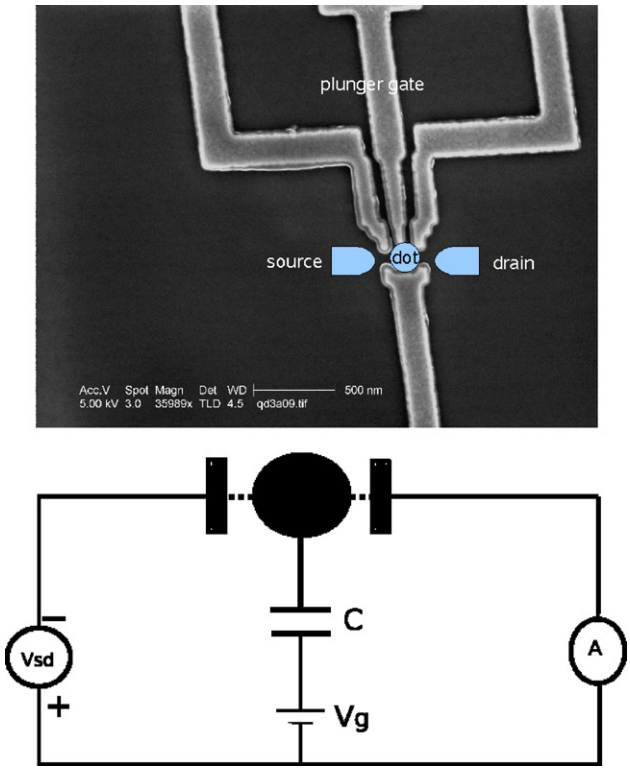

Figure 1. Top: a SEM image of the gate pattern of a QD in the experiment. The Ti/Au metal pattern is formed on the GaAs/AlGaAs surface using E-beam lithography and lift-off. Two-point contacts are adjusted to form the tunnel barriers. Bottom: circuit model of a single QD. The dot is connected to the source and drain electrodes through small tunnel barriers.

out of resonance with the Fermi level in the source and drain contacts. The conductance will increase whenever energies are aligned and decrease in between, forming so-called Coulomb oscillations. Also, by measuring with a difference between source and drain voltage, the Coulomb blockade with excited energy states of the quantum dot can be probed.

The operation of such devices is primarily based on controlling the electron density by varying the confining potential. The key implementation challenge is to gain sufficient gate control in order to define quantum dots in the few-electron regime. One of the solutions is to place these gates sufficiently close to each other to make better gate–dot coupling, allowing efficient electrostatic control. The main technical difficulty is that the surface Schottky gates cannot be reliably made on the 2DEG in GaAs. Besides, if the dot area is too small, all electrons may be depleted from the dot before the two potential barriers form, thus preventing stable operation.

Another concern is the effect of the fringing fields of the gate on each other. The surface gate is used to define depletion patterns in 2DEG, but the pattern does not exactly match the gate geometry. The densely spaced multi-gate designs such as QDs mean that gaps between adjacent gates are very close. The potential profiles defined by individual gates can overlap with each other in the 2DEG, when negative bias is applied to all the gates at the same time. Therefore local spatial potential

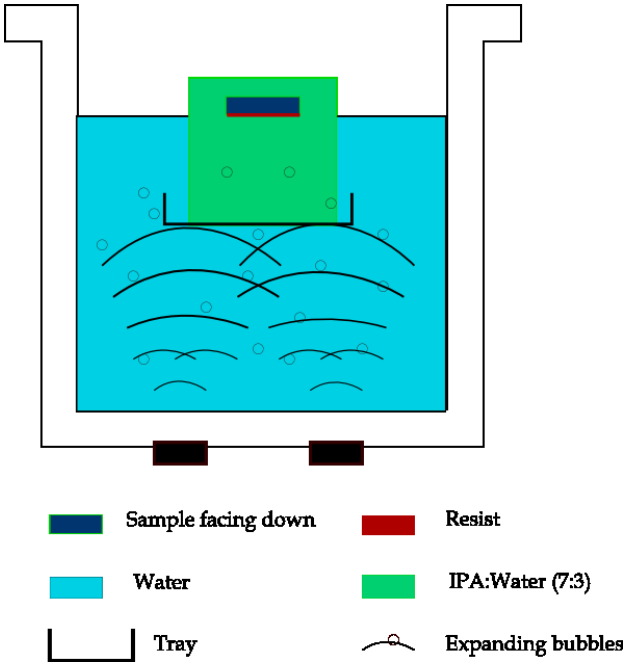

Figure 2. Schematic for the setup of the ultrasonic agitation.

fluctuations occur, which would affect the symmetry of the dot.

2.2. *Sample preparation*

A high mobility modulation-doped GaAs/AlGaAs heterostructure wafer V81 was grown in a Varian Gen II molecular-beam-epitaxy (MBE) machine. The 2DEG in the samples was situated 90 nm below the surface. The electrical properties of the 2DEG were determined by quantum Hall effect and SdH measurements. Typical carrier density of wafer V81 is $\sim 1 \times 10^{11}$ cm^{-2} with mobility $\sim 1 \times 10^{6}$ cm^{2} V^{-1} s^{-1}.

Two samples were picked from wafer V81. Hall bars ($6 \times 2 = 12$) were first patterned by optical lithography, and then the mesa was wet chemically etched. Ohmic contacts to the 2DEG were made by depositing Ni/Ge/Au and annealing at 450 °C. The dot is defined by Ti/Au gates on top of the Hall bar mesa with two QD structures being made on each of them. The fine features of surface gates were written by E-beam lithography and developed by ultrasonic agitation described as follows. The lithographically defined dimension of the dot island is 180 nm $\times$120 nm, and the size of the surface gates is ~40–45 nm. Based on our mesa structure, two single dots have been made on each of the Hall bars, and therefore 24 QD devices ($12 \times 2 = 24$) have been fabricated.

2.3. *Fabrication: lithography and development*

For over 20 years, polymethyl methacrylate (PMMA) has served as the standard positive resist for high resolution E-beam lithography. Yet, there are many questions remain related to its resolution, e.g. problems related to the scattering of electrons (the proximity effect) [3], the swelling of

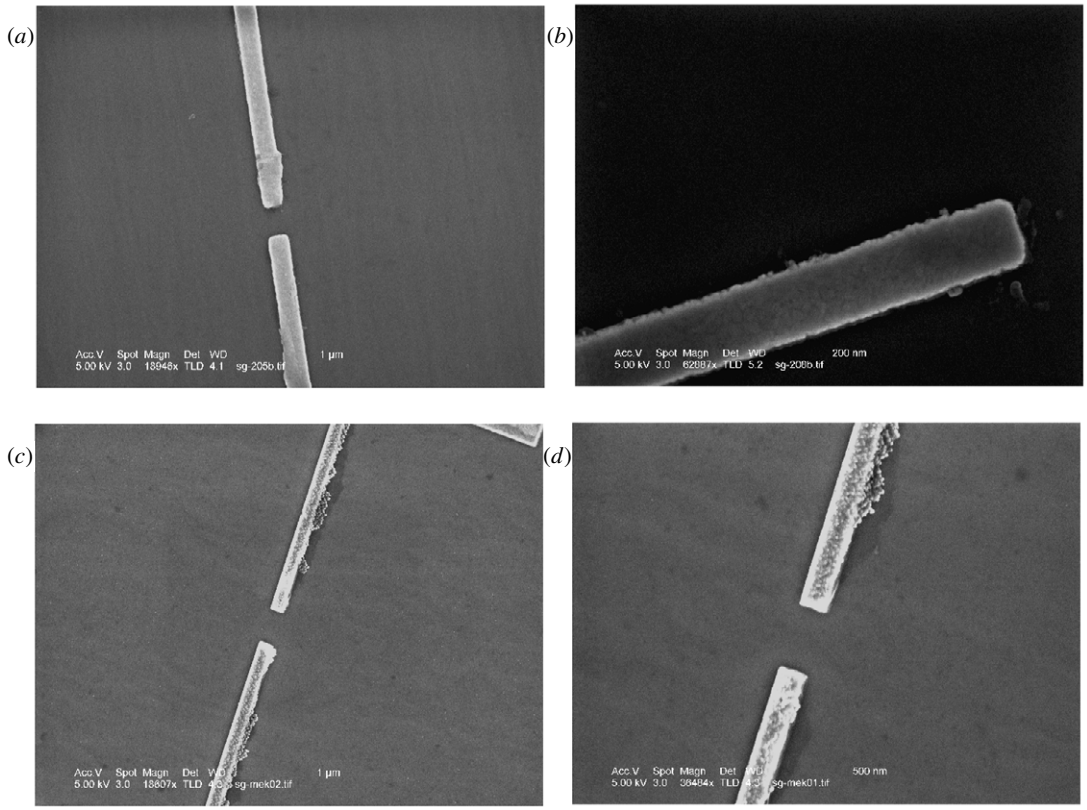

Figure 3. Comparison of dip and ultrasonically assisted resist development of fine isolated nanostructure with linewidth ≅ 200 nm. Top: SEM images of a split gate in different magnifications (*a*), (*b*), using altrasonically assisted development for 5 s in IPA:water (7:3). Bottom: images in different magnifications (*c*), (*d*) of conventional dip development in MIBK:MEK:IPA for 10 s.

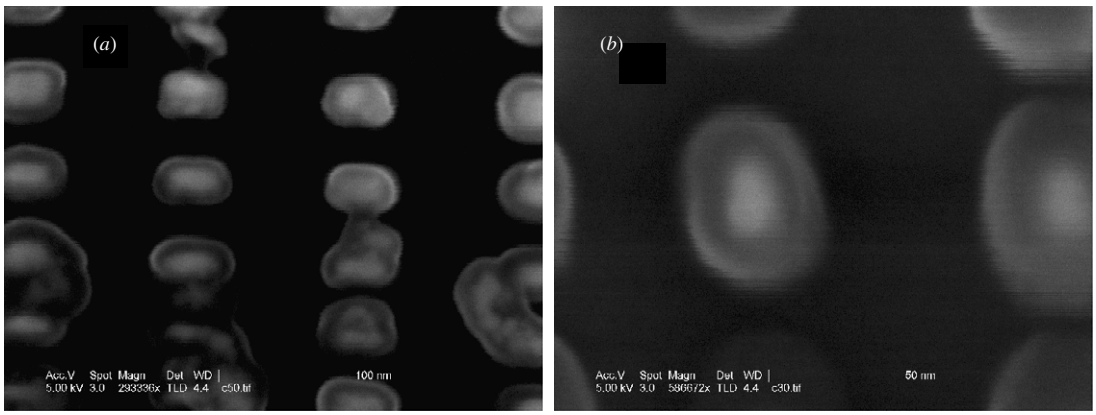

Figure 4. SEM images of (*a*) a dense array of dots (25 nm radius/spaces) with conventional dip development; and (*b*) an array of dots (15 nm radius/spaces) developed by ultrasonic agitation.

unexposed resist, and line edge and surface roughness, have limited its resolution. Using conventional dip development, feature sizes down to 30–45 nm for dense-spaced patterns can be fabricated, but with very low reliability. Therefore, the fabrication reliability of sub-50 nm QD is a challenging problem. A high-yield fabrication scheme for such small QD was explored here, which involves the use of weak developer solution of isopropyl alcohol (IPA):water assisted with ultrasonic agitation to process the exposed resist, instead of MIBK:MEK:IPA (methyl isobutyl ketone:methyl ethyl ketone:isopropyl alcohol) in conventional development. The process would help to (i) minimize the intermolecular forces between exposed and unexposed resist, limit the swelling of the resist features remaining after development, decrease viscosity of polymer–solvent mixtures, and therefore give better line-edge quality [4]; (ii) make exposed resist debris more easily removed from the surface of the resist and substrate [5] during the development time; and (iii) leave the rest of the film with

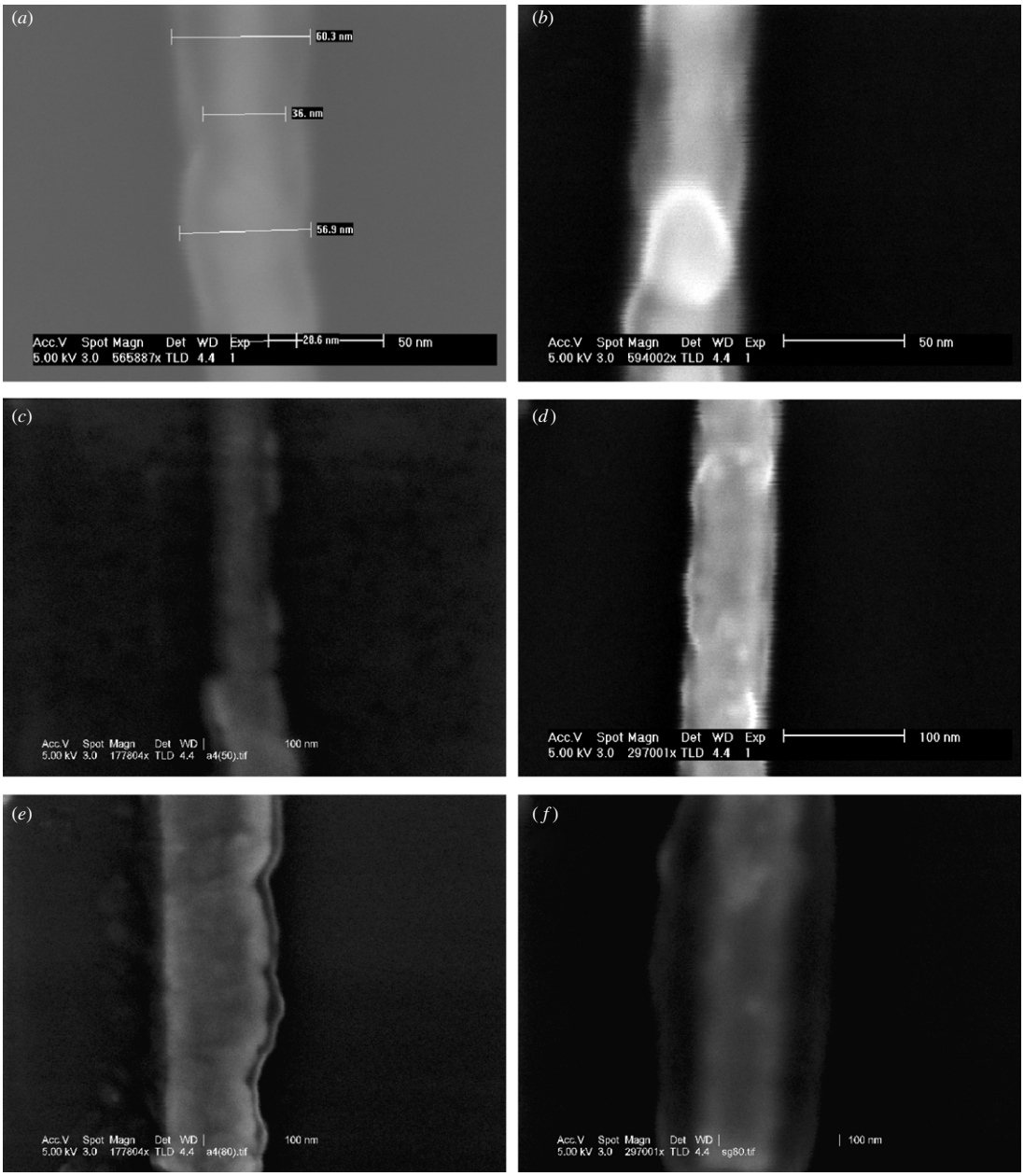

Figure 5. Comparison of resist development with dip (right) and ultrasonic (left) agitation for a dense array of gratings. Top: 30 nm wide line, (*a*) clearly shows that its linewidth swells to 60 nm; middle: 50 nm wide line; bottom: 80 nm wide line.

little or no swelling/distortion. Such improvement is thought to be due to the effect of the extra ultrasonic energy available on the dissolution of the exposed resist into the developer.

A ∼150 nm thick film of PMMA solution in chlorobenzene was spin-coated on the wafers. They were baked at 150 °C in an oven for at least 10 h prior exposure. The wafers were exposed in a LEICA VB6UHR E-beam writer operating at 75 kV with a beam diameter of 3 nm (minimum). Following exposure, ultrasonic assisted development was carried out in a glass beaker suspended in a water bath operated at 50 kHz (a schematic of setup is shown in figure 2). Samples were immersed in the developer (7:3 of IPA:water solution) with the resist-coated surface perpendicular to the propagation of the ultrasonic waves in order to keep the developed resist patterns from being affected by the pressure waves [6]. After cleaning in IPA, fully developed samples were transferred inside a metal evaporator where 12 nm of Ti layer was deposited followed by 30 nm of Au on top.

Patterns developed by ultrasonic agitation are compared with those of conventional dip development. SEM images of the edge profile of surface-gate patterns were taken. A clear improvement in the line quality (edge roughness) is seen using ultrasonically assisted development compared to the use of conventional dip development. Figure 3 compares isolated lines developed with ultrasonic agitation (top) and

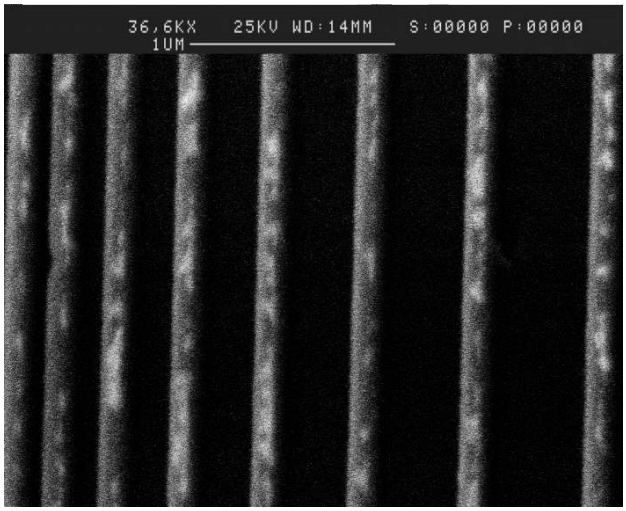

Figure 6. SEM image of gratings from left to right of 20, 30, 50, 80, 100, 200, 300, 400 nm made using water/IPA developer with ultrasonic assistance.

conventional dip (bottom). This improvement is attributed to (i) the improved processing conditions for metallization, e.g. the wafer surface after development had less exposure tail outside the nominally exposed line, and (ii) the development times that may be substantially reduced through the use of ultrasonic assistance compared to the conventional dip development. Swelling of the unexposed resist during development not only limits the resolution but also causes image distortion. In particular, narrow-spaced patterns may swell to such an extent during development that adjacent features may join together. In figure 4(*a*), a dense array of dots (25 nm radius/spaces) using dip development overlap. However, swelling is difficult to avoid, since the polymer absorbs a significant volume of the solvent and increases its dimensions during the development process. The volume of the solvent absorbed (hence the swelling) is proportional to the development time. The shorter development times result in less swelling. Figure 4(*b*) shows that the quality of an array of dots (15 nm radius/spaces) after agitation development for 5 s is improved. Figure 5 shows a grating pattern consisting of single lines of 30 nm (top), 50 nm (middle), 80 nm (bottom) using dip development (left: a, c, e), and using agitation (right: b, d, f). An interesting observation is that there is high degree of linewidth fluctuations in the case of conventional dip development (the left-hand side); on the other hand, resist development was much more uniform with ultrasonic agitation (the right-hand side). Figure 6 shows line/space gratings from left to right of 20, 30, 50, 80, 100, 200, 300, 400 nm linewidth/space using 3:7 water/IPA developer with ultrasonic assisted development.

The average molecular weight of PMMA systematically affects resist performance. This is particularly critical in dense nano-lithographic patterns. Generally, a high molecular weight material is chosen for the highest contrast and resolution performance [3]. But, the higher molecular weight resist PMMA 950 K will also bring more developer-induced swelling than the lower weight resist [7]. Overall, with the interplay between contrast and resist swelling, a lower weight PMMA 495 K resist assisted by agitation was explored here as an optimal approach. In order to ensure high reliability and reproducibility, an experiment was carried out to select the best combination of PMMA and development time scale. Samples were also made using different typical resist development times with 3 s (figure 7(*a*)), and 8 s (figure 7(*b*)), and results were examined in the SEM again. It is found that the use of long development time 8 s resulted in the collapse of the small resist feature, and no collapse of fine resist structure at 3 s development time.

3. Experiments

3.1. Measurements

Electrical measurements were carried out in a Heliox fridge with temperature down to ∼300 mK. By measuring the conductance versus the plunger gate voltage $V_{p\text{-}g}$ while keeping side gates voltages at constant values, Coulomb oscillations in the conductance of a QD are observed. Some of the characteristic features of the fabricated QD device are shown in figure 8. In the figure, sharp resonance peaks are

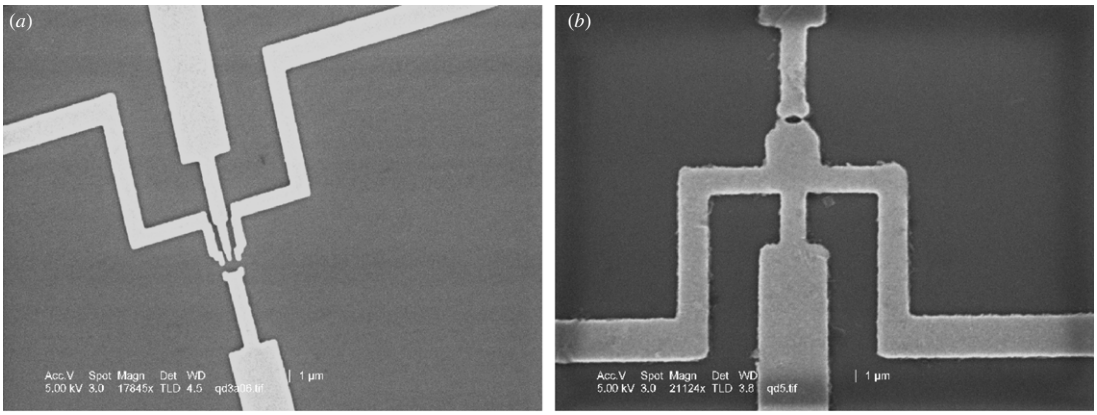

Figure 7. SEM images of resist development time: (*a*) 3 s and (*b*) 8 s using ultrasonic agitation for a small QD with linewidth ≅ 45 nm.

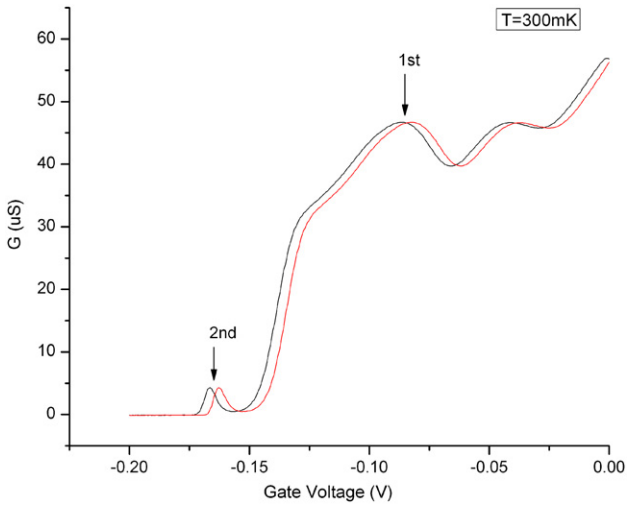

Figure 8. Coulomb blockade oscillations of a single quantum dot. It is measured at 300 mK as a function of the plunger gate voltage (V) versus conductance (G). The data were plotted as the black curve when the plunger gate was swept down, while plotted as the red curve when the plunger gate was swept up. (Colour online: the red curve is displaced to the right of the black curve.)

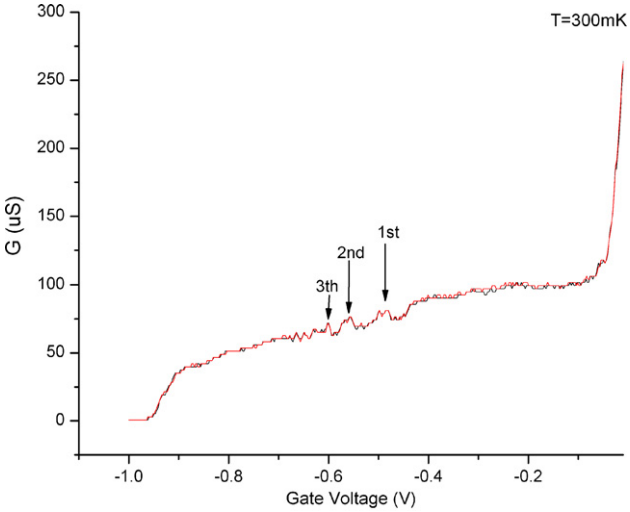

Figure 9. Reproducible conductance fluctuations of another quantum dot as a function of gate voltage (V) versus conductance (G) at 300 mK. The data were plotted as the black curve when the plunger gate was swept down, while plotted as the red curve when the plunger gate was swept up. (Colour online.)

observed, which correspond to the electrostatic de-/population of the dot by a single electron. During the measurement, the QD is defined by means of electrostatic depletion of the 2DEG using three electrodes, and two adjustable tunnel barriers are formed by three surface gates. A counteracting change of the voltage on the two outer gates allows one to stabilize the tunnelling barriers and therefore increase the range of occupation numbers accessible by measurement. The plunger gate voltage controls the number of electrons within the dot, which in turn influences the number of measurable Coulomb oscillations. All surface gates were closed as much as possible to isolate the dot from the source–drain reservoirs, but not pinched off completely. The conductance through the QD is measured using a standard lock-in technique with an ac voltage of only a few hundred microvolts between the source and drain to avoid self-heating of the QD.

3.2. Data analysis

In figure 8 we show experimental results of the Coulomb blockade oscillations as a function of the voltage applied to the plunger gate, during which the point contacts were adjusted to the tunnelling regime, e.g. conductance $G \leqslant e^2/h$. Here, only two Coulomb oscillation peaks appeared in the I–V characteristics of QD devices, while the background conductance remains below e^2/h in the entire trace. By repeatedly sweeping the plunger gate over many cycles, the test data show similar patterns of I–V characteristics, which suggests that the oscillation peak is indeed Coulomb oscillations and not conductance fluctuations. Each of these conductance peaks corresponds to the electrostatic depopulation of the dot by a single electron. The second peak has relatively lower amplitude but it is much better defined. By changing the plunger gate voltage the tunnel barriers are also influenced, which limits the number of measurable Coulomb oscillations, and reduces the peak height at more negative gate voltages.

Instead of sharp resonance Coulomb peaks, we have observed conductance fluctuations superimposed upon the usual Coulomb oscillation in several samples (see figure 9), which at a first glance looks like random noise. However, it is indeed a reproducible fluctuation and was preserved over several sweeps in both directions.

3.2.1. Yields. Twenty-four QD devices in total have been fabricated ($2 \times 6 \times 2 = 24$) and tested. Here, the criteria of device yield for QD should include (i) the device could be pinched off at temperature as low as 300 mK; (ii) the observation of well-defined Coulomb blockade oscillations at 300 mK is considered as a proof of the functionality of these QD devices. The device yield is ∼46% at dark. Among the failures, 5 out of 24 (21%) failed due to the quantum point contacts not working. Fabrication errors realised as broken Schottky gates or the features of gate electrode joined together resulted in 8 devices failing (33%). In a parallel study [8] of over 400 split-gate transistors, the overall functional yield was ∼60%. Our yield here of 46% is higher than we might expect given the extra complexity of the gate structure, and we attribute this in part to the ultrasonic fabrication process.

3.2.2. Reproducibility. In our experiments, the position of the Coulomb peak at the plunger gate voltage $V_{p\text{-}g}$ varied widely from one device to another. The electron tunnelling (Coulomb peak) occurs when the Fermi energy in the source–drain contacts matches an individual discrete energy level of the dot. Therefore, the gate voltage at which a peak occurs is partly determined by the discrete state levels of the dot structure. In general, however, the dot state spectrum is more

complicated because the geometry of the isolated dot is not highly symmetric, and this asymmetry varies from dot to dot. The electrical field generated at the gates induces an electrostatically defined dot in the 2DEG, for which the exact potential profile seen by the 2DEG well away from the gates is complex to calculate. It is significantly perturbed under the gates by metal/semiconductors interface and intermediate layers of the material. Based on these reasons, we assume that such nano-scale imperfections may be contributing to the fabrication errors or the gate fringe field as mentioned above, each of which leads to the individual device having its own random distribution of defects and charges.

It is not uncommon for two devices fabricated in an identical way to have different amplitudes of conductance peaks. At low temperature the conductance of a specific peak depends on the tunnelling matrix element for one particular energy level of the small QD structure. Because this matrix element depends exponentially on the decay length of the wavefunction between the barriers, which is easily influenced by impurities and structural imperfections, the amplitudes fluctuate randomly and vary from one device to another while generally increasing with gate voltage on most devices. Although this can be tolerated for low-temperature investigation of individual devices, it remains a significant setback for circuit construction where identical devices are required.

In addition, even for the same device, the peak-to-valley amplitude is affected by the side-gate voltages on the tunnel barriers, e.g. at more negative gate voltages the higher tunnel barriers in the two-point contacts reduce the peak height. At smaller negative gate voltages, the lower tunnel barriers result in an increase of quantum fluctuations of the charge in the QD. This leads to an increased background and peak conductance.

There are two conductance peaks occurring in most of our samples, within a limited range of voltage. As the gate voltages are increased further, the potential barrier drops rapidly, and the confinement of the dot is lost. Due to the dot being relatively small, further decreasing the gate voltage will effectively 'kill' the dot.

4. Summary

The feasibility of realizing gate-controlled QD in the few-electron regime is based on the ability to utilize the gate bias and the gate size to modulate the physical size of the QD and then the number of confined electrons. It is assumed that the number of electrons in each dot is obtained by integrating the electron density over the dot region. As expected, the dot size decreases with increasing negative gate bias; correspondingly the electron number shrinks as well. It is important to note that the QD confining potential in the 2DEG plane is generated from the electric field generated by the top gate. The features of the dot are a factor of 2–3 smaller than the features of the surface gate geometry [9], of which the scale factor is a function of the depth of the 2DEG. For our gate structure as 180 nm × 120 nm, the area in the 2DEG plane is around 60 nm × 40 nm. For such a small device, the few-electron regime may be realized at reasonable values of gate dimensions and bias voltages, but the gate bias is restricted to a very narrow operating range. This narrow operating range may be the possible explanation why there are only two Coulomb oscillations in our case. Another concern is that the small physical size of surface gate (∼40–45 nm) may not provide sufficient gate control to define the QD. To define the QD, the electric field has to penetrate the intermediate material. Hence, it needs larger biases to establish electron depletion, which is particularly true for a deep 2DEG. This causes the dilemma that there are limited options available, considering the narrow operation range as mentioned above. To achieve much better control over the confining potential, one has to bring the electrons as close as possible to the top surface—the design strategy of 'trading mobility versus gate control' has to be applied [10, 11]. In other words, for such small QDs, if we allow for a reasonable aspect ratio (gate size to layer thickness) of one, then the distance of the 2DEG from the top should be less than 45 nm, instead of 90 nm in our case.

One of the prospects for the surface-gate technique is the ability of controllably loading these dots through capacitive charging. Such structures inevitably suffer from parasitic capacitive coupling to the environment.

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