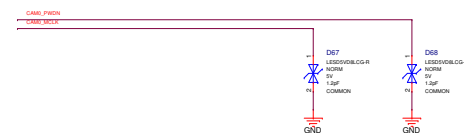
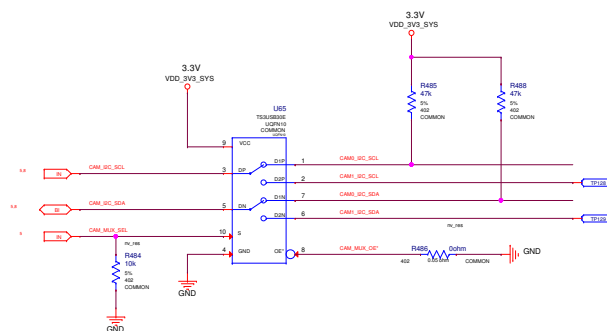


The schematic shows the I/O interface for the AD9670 ADC. It features six level shifters (D49-D55) configured as follows:

- D49:** L6E50B0LGG-R, NORM, 5V, 1.5pf COMMON
- D51:** L6E50B0LGG-R, NORM, 5V, 1.5pf COMMON
- D53:** L6E50B0LGG-R, NORM, 5V, 1.5pf COMMON
- D55:** L6E50B0LGG-R, NORM, 5V, 1.5pf COMMON
- D57:** L6E50B0LGG-R, NORM, 5V, 1.5pf COMMON
- D59:** L6E50B0LGG-R, NORM, 5V, 1.5pf COMMON

The ADC pins are connected to the level shifters as follows:

- DQ[0:5]:** Connected to the outputs of the level shifters.
- CS:** Connected to the common ground of the level shifters.
- VDD_3V3_SYS:** Connected to the 3.3V supply.
- C892:** 0.1µF capacitor connected between VDD_3V3_SYS and GND.



ASSEMBLY	Jetson Nano Carrier Board
PAGE DETAIL	CAM Connector

2701 SAN TOMAS
EXPRESSWAY
SANTA CLARA, CA 95050, USA



NV_PN			
PCB REV		PAGE	18 OF
RCM REV	A	DATE	08-MAY-2019

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED AS IS. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY