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PCD Toolkit Hardware Reference Platform Description V1.0

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1 Introduction

The Power Chain Device (PCD) Toolkit Hardware Reference Platform, referred to as the "reference platform", offers a low cost, scalable hardware system that can be utilized for the rapid development, validation and/or deployment of a variety of Power Chain Management (PCM) Software Toolkit initiatives.

The reference platform consists of two Printed Circuit Board (PCB) assemblies. The first PCB assembly, referred to here as the "Toolkit module" (see Figure 1), is mechanically compliant with the JEDEC MO-190 standard. The Toolkit Module consists of a 1.650" by 2.662" PCB that is used to support the main system hardware including an ARM920T based 32-bit microprocessor, SDRAM, parallel flash memory, and Ethernet PHY controller. All I/O signaling is routed from the processor to the edge card interface, which is designed to mate with a commercially available, industry-standard 144 pin Small Outline DIMM (SO DIMM) connector.

Since most of the system hardware components are located on the Toolkit Module, this strategy allows for the design of a relatively simple second PCB assembly, which will be referred to as the "base platform". The base platform supports a SO DIMM connector, which serves as a means to bridge all 144 I/O signals from the Toolkit Module to the base platform. The base platform then accesses and routes the appropriate Toolkit Module signals to support system user interface connectors (e.g. Ethernet, Serial, USB). Refer to Appendix A for a complete list and description of all the Toolkit Module I/O signaling. If an RS-232 terminal application program (e.g. HyperTerminal) is used to configure the system, an RS-232 transceiver is also required on the base PCB to manage the RS-232-to-TTL signal levels. Refer to the Translator Interface schematic illustrated in Appendix E.

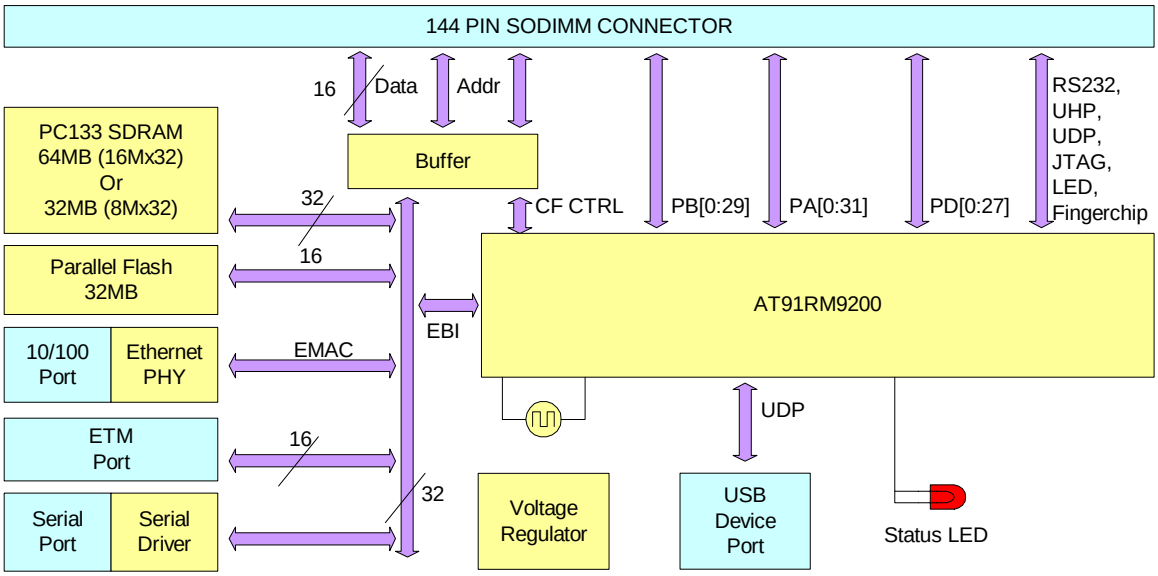
Although the reference platform is preloaded with PCD Toolkit components specific to its use in a UPS environment, the user may use the platform for their own experimentation by selecting their own PCM Toolkit components and building them along with the Linux environment. The reference platform then becomes the playground for experimentation and validation of individual Toolkit resources. The user's Toolkit build may then be loaded as a binary image into the parallel flash provided on the reference platform's Toolkit module.

The hardware reference platform comes pre-loaded with a Linux kernel (currently 2.6.16), system libraries, etc. References to Schematics and Bills of Materials (BOM) of the Toolkit Module and base PCB assembly, along with Eaton part numbers, are also provided in Appendix F in this document.

Figure 1. Toolkit Module

2 Toolkit Module Overview

The Toolkit module consists of an Atmel ARM920T based Atmel AT91RM9200 Processor, SDRAM, Parallel flash memory and Ethernet MAC / PHY controller as illustrated below.



2.1 Atmel AT91RM9200 Microprocessor

The Atmel AT91RM9200 is based on an ARM920T core. The processor is a Harvard architecture device implemented using a five-stage pipeline consisting of Fetch, Decode, Execute, Memory and Write stages. It supports both the 32-bit ARM and 16-bit Thumb instruction sets, allowing the choice of high performance versus code density.

The AT91RM9200 cache architecture supports multi-programmer applications that require full memory management, high performance and low power. The separate instruction and data caches in this design are each 16K bytes with an 8-word line length. The AT91RM9200 includes two enhanced Memory Management Units (MMU) to provide translation and access permission checks for instruction and data addresses.

Detailed ARM9TDMI information is available in the *ARM9TDMI Technical Reference Manual* from Atmel.

2.2 Internal Memory

The AT91RM9200 contains on-chip cache memory configured as 12kB of on-chip, high-speed static RAM. An on-chip cache controller determines cache accesses.

2.3 External Memory

The module contains two JEDEC standard PC133 SDRAM's in TSOP packages and connects to the processor via a 32-bit data bus. The SDRAM capacity is configured as 8M x 32 bits (32MB). An on-chip SDRAM controller arbitrates all SDRAM accesses as well as "housekeeping" functions, and provides a "glueless" interface to the SDRAMs.

2.4 Parallel Flash Memory

32MB of parallel flash memory, located at 0x10000000, is managed by chip select “ncs0”. Common Flash Interface (CFI) is fully utilized by the Linux operating system to determine flash type, size, etc. Once the Linux binary images are loaded into parallel flash, the system is re-configured to bypass the normal masked ROM boot process (as advertised in the Atmel technical reference documentation). Refer to section 2.8 for configuration details.

2.5 Address and Data Buss

The 16-bit address and data busses, conditioned by two on board buffers, are provided at the edge card interface used to drive off-board devices. The address bus is always driven, even if addressing is to on-board resources. To conserve space, the higher-order address bits are omitted. Several of the MSB addresses are available for device selection. Address Bus drive is +/-24mA and is always driven. A 16-bit data bus is available at the edge connector. Data output is driven to ± 24mA, and can also be high impedance during parts of the external bus cycle. All inputs and outputs are 3.3V logic levels. In the data input mode, the buffers have a “bus hold” function. The data bus will retain the last state even if the bus is not driven or pulled up by the host system. This eases the requirements for host timing, prevents possible latch-up to the input buffers, and reduces power consumption and EMI.

2.6 Communication Interfaces

2.6.1 10/100 Ethernet (Port 0)

The Toolkit Module provides a dedicated 10/100Mbit Ethernet communications channel. The media access control (MAC) *address* is factory programmed by Eaton’s supplier and is stored within a small portion of U-boot code located within the first 128k sector of parallel flash.

The Davicom PHY interface device provides layer 1 and translation between the controller and the edge connector. Transmit and receive data signals are provided on pins 1-4 of the 144-pin edge card interface. Ethernet requires filtered power and ground derived by conditioning the main power and ground. The filtered power and ground are made available at the edge interface for use by external Ethernet transformer and/or transformer connector combinations.

Three PHY outputs, provided on pins of the edge card interface, provide Ethernet port 0 speed and activity status. These open collector signals can sink adequate current to drive standard LED’s with a 240 ohm current limit resistor.

2.6.2 High Speed Serial Ports

The Toolkit Module includes 4 high-speed TTL (up to 115.2K baud) ports, all of which are made available at the edge card interface. The signal levels are provided at 3.3V TTL logic levels, and must be translated to the required physical medium (e.g. RS-232, 5 volt TTL) by the base platform. One of the four serial channels support a debug port that provides receive and transmit only. The debug port is used during the manufacturing process to program the Linux file images into the parallel flash device.

2.6.2.1 Serial Port 0

Port 0 supports TxD, RxD RTS and CTS. This port is used by the reference design base platform X-Slot card to communicate with a Powerware UPS. Refer to the base platform schematic for details.

2.6.2.2 Configuration/EMP Serial Port 1

In the reference design, Port 1 serves as the card configuration port. Port 1 is equipped with a full set of modem handshake signaling including TxD1, RxD1, RTS1, CTS, DSR1, DTR1 and

CD1. This port defaults to configuration mode, which is normally used to support local configuration of the system by a user. However, this port can also be configured to communicate with a stand-alone temperature / humidity monitoring device called the Environmental Monitoring Probe (EMP).

2.6.2.3 Port 2

Port 2 supports TxD2, RxD2, RTS2 and CTS2. RTS2 is multiplexed with debug channel DTxD while CTS2 is multiplexed with DRxD. This port is used during manufacturing to program the Linux binary images into the parallel flash device.

2.6.2.4 Port 3

Port 3 supports TxD3, RxD3 CTS3 and RTS3. TxD3 is multiplexed with SPI NPCS2 while CTS3 is multiplexed with SPI NPCS3.

2.6.3 USB

The Toolkit module provides three USB ports that are electrically compliant with the USB 2.0 specification; two “Type A” (host) ports and one “Type B” (device) port. An on-chip AT91RM9200 USB controller handles all USB functions. The signals to/from both ports are routed to the Toolkit Module edge card interface where the base platform accesses and routes the signaling to the appropriate USB connector. The base platform must route 5V to the “Type B” (device) port to allow the module to detect a USB physical connection. The Toolkit module does not provide a powered USB port.

2.7 Power On Reset Initialization

The processor starts an initialization process on power up, or when the #MR input signal is pulled low. #MR is available at the edge card interface, and is pulled up through 65k ohms. An onboard reset controller applies system reset (#NRST) to the system and edge connector as a result of power up, external #MR reset, or under voltage conditions to ensure correct system operation. The processor executes code from address 0 of internal ROM that initializes all peripheral devices to their default states. Internal ARM9 registers (except for the program counter and current program status register) are in a random state during and after reset. Internal clocks are disabled to conserve power. Other system functions are connected to #NRST.

#NRST is an open-collector signal that is available on the edge card interface. External hardware can be reset and synchronized by utilizing #NRST as an output from the module. Although the AT91RM9200 could be reset by driving #NRST, this should be done using the #MR input due to possible reset duration and slew rate violations if #NRST is driven by an external source.

During a reset cycle, all general-purpose I/O lines are pulled up via internal 100k resistors to ensure no inputs are allowed to “float”. Inputs (other than #NRST) are ignored while reset is active. When reset is complete (#NRST high), all general-purpose I/O lines are enabled except for PC7-PC13. The External Bus Interface must drive these memory control lines. The remaining I/O lines can have their pull-up resistors disabled by programming either the PIO controller or the external bus interface.

2.8 Boot Process

The Toolkit Module is designed to boot from the Atmel masked ROM boot loader or directly from the parallel flash. The internal masked ROM boot loader is enabled by removing the zero ohm resistor at reference designator R57 (a factory process). When the reset line (#NRST) is de-asserted and the initialization process is complete, the low-level boot loader code tests the logic state of the Boot Mode Select (BMS) signal PA31. If logic 1 is detected, then the system begins transmitting repeating “C’s” (115.2 k Baud) out the serial debug port 2 that is used to inform the user that the system is ready to accept a file transfer (via a terminal application program).

Otherwise, if the 47k resistor is populated at reference designator R57, this causes the ROM boot loader to detect logic 0 on PA31 during the boot process. This forces the internal masked ROM boot code to automatically execute U-boot and Linux kernel images from parallel flash.

2.8.1 Using Atmel's Loader.bin (Manufacturing)

Loader.bin is used as a bootstrap during the manufacturing process to load the U-boot and Linux images into parallel flash memory. Upon power up, if logic 1 is detected on PA31, repeating "C's" are transmitted out the debug port, which informs the user that the platform is ready to receive Loader.bin. Loader.bin is loaded directly into SRAM via the X-Modem file transfer protocol using a terminal program (e.g. HyperTerminal). When the transfer is complete, a second set of repeating "C's" are transmitted out the debug port, informing the user that the system is ready to accept the U-Boot.bin transfer via the X-Modem protocol. Loader.bin does not reside within parallel flash, it is only used as a means to load U-boot binary into parallel flash.

2.8.2 GNU U-boot.bin (Manufacturing)

Once U-boot is loaded into flash, a jump instruction is performed to begin executing U-boot code from flash where the system hardware parameters (i.e. system clock, static memory controller settings, MAC address assignment, IP address and gateway settings) are initialized.

The U-boot version and command prompt are then displayed by the terminal program, which is used to accept user commands such as memory test, memory read/write, and memory transfer, etc. The main command, "loadb" is used to transfer the Linux images from a local machine to SDRAM located on the Toolkit Module, via Kermit protocol. The copy command "cp.b" is then used to copy the Linux binary images from SDRAM to parallel flash at user specified address locations.

Once the Linux images are loaded into parallel flash memory during manufacturing, a 47k ohm resistor is installed at reference designator R57. Upon power up, PA31 is forced to a logic low, which instructs the internal masked boot loader to begin executing U-boot directly from parallel flash. The Linux kernel image is then decompressed and copied from parallel flash to SDRAM where the kernel is actually executed.

2.9 Clocks

The Toolkit Module contains three clock oscillators. The 32.768kHz clock drives the System Timer, Real Time Clock, and Power Management Controller.

The 4.0 MHz clock is used for a programmable frequency Processor Clock that has a range of 512Hz to 180MHz. The Processor Clock, in turn, is divided by a programmable value and creates a Master Clock that drives internal buses and all peripherals. The 4MHz clock drives two other functions. It is multiplied and provides clocks (usually 48MHz) for the three USB ports. It also drives programmable output clock signals for use in the user's application.

An onboard 50MHz oscillator drives the Ethernet PHY.

2.10 Power supply / Power Management

The primary module input voltage, VDD, is 3.3VDC +/- 10%. This is used by most of the circuitry and is the standard logic signal level for most of the I/O to the module for compatibility. The 3.3V input is not protected or conditioned for noise, EMI, over-voltage, over-current, or reverse polarity. Protection must be provided by the base platform. High-frequency bypass capacitors and three 100uF bulk capacitors are provided on the VDD rail of the Toolkit module.

The processor core, oscillator, and PLLs require 1.8VDC. This is generated from the 3.3VDC by an on-board, low-dropout, linear voltage regulator. Appropriate capacitors and grounding on the 1.8VDC supply supports the low noise and high transient current requirements of this rail.

The module contains 2 separate grounds. Digital ground, VSS, is the main ground that supports most of the functions on the module. Analog ground (AGND) is the ground for the Ethernet, and is electrically isolated from main Vss. Analog ground is available at the edge connector.

The AT91RM9200 contains programmable hardware that allows optimization of system power consumption by controlling processor mode and peripheral clock speeds. No functions on the module require battery power. However, the low-power modes and power management functions available on the system do support end applications that require battery operation or battery backup.

3 Base PCB Overview

The reference design base platform (X-Slot PCB) consists of:

- 144 pin Toolkit Module connector (used to populate the Toolkit Module)
- 3.3 volt @ 1 amp power supply (used to provide regulated power to the base PCB and Toolkit Module circuitry)
- ST M41T94 Real Time Clock (RTC)/Power On Reset device with a Lithium Snap Hat battery back up system
- SMSC LAN91C113 10/100 Mbit Ethernet MAC/PHY controller (for a second Ethernet port)
- RS-232 transceiver
- Reset switch
- 4 position stacked LED
- 6 position DIP switch
- Piezo Horn
- (1) RJ-45 connector (Configuration Port)
- (2) RJ-45 connectors (Primary and Secondary Ethernet Ports) with integrated magnetics.
- USB Type “B” peripheral pads to support USB connector

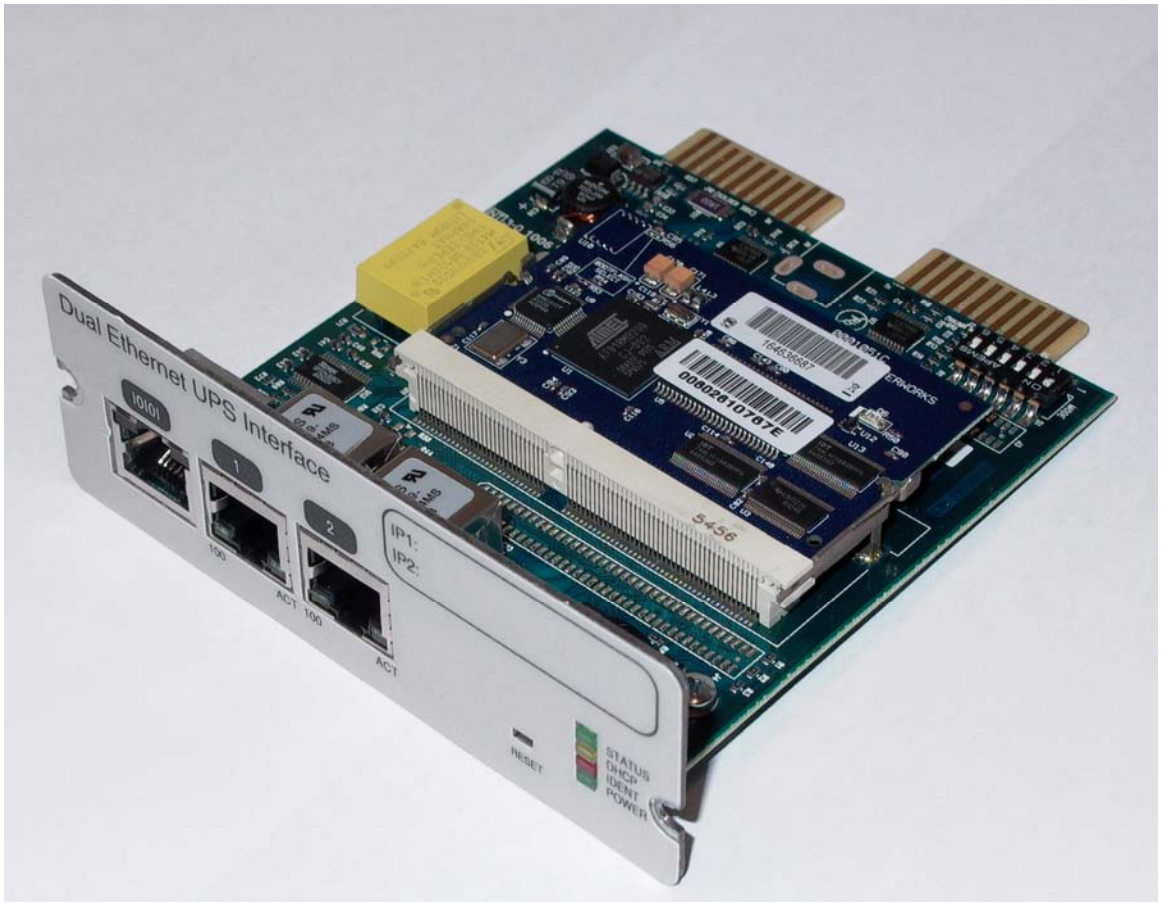


Figure 2. Toolkit Module populated on the X-Slot (UPS-related) Base Platform

The RJ-45 configuration port connector, available on the left front edge of the platform, serves an RS-232 based configuration port, while the (2) adjacent RJ-45 connectors, are used to provide10/100 Mbit Ethernet port interfaces. A four position stacked LED, located at the right hand side of the PCB assembly, is used to advertise system status, while a piezo horn is used to signal alarm conditions. Refer to Figure 2 for the PCB Layout as illustrated above.

3.1 Ethernet Port (Secondary)

The reference design's base platform supports an integrated MAC/PHY combo chip that adds a secondary 10/100BaseT Ethernet channel.

3.2 Unused USB Connection

A footprint to support a (Type "B") USB connector is also provided on the leading edge of the base PCB assembly.

3.3 RTC/Power On Reset/Snap-Hat Battery Back-up Device

The base PCB assembly supports a battery backed ST M41T94 Real Time Clock (RTC) and Power On reset (POR) within a single TSOP28 pin package. The M41T94 is enabled by SPI NPCS1 and provides RTC information to the AT91RM9200 via the SPI interface.

The POR portion of the M41T94 is used to assist in initiating a cold boot process of the Toolkit Module. This process involves the use of a hardware reset switch SW1, AT91RM9200 Interrupt Request (IRQ) input, chip select 7 (NCS7) output signal, M41T94's reset input (/RSTIN1) and output signals (/RST).

Whenever the reset switch is pressed, a logic zero is generated and used to force an interrupt within the AT91RM9200 microprocessor. Software detects this, which forces NCS7 to logic 0. Since NCS7 is tied to the M41T94's reset input signal (/RSTIN1), this causes the M41T94's reset output signal (/RST) to be asserted to a logic low, which forces the M41T94's reset output signal, /RST to be asserted to a logic low for approximately 120 mS. Since /RST is connected to the AT91RM9200 tri-state reset signal, this causes the module to perform a cold reboot.

3.4 Reset Switch

The reset switch (SW-1), located on the leading edge of the base platform is used to initiate the cold boot process. Refer to section 3.3 above for operational details.

3.5 LED Indicators

Four signals, provided at the edge card interface, are tied to connector J11 (69-72) and are buffered by a 74LV06 open collector device. Each LED may be used to advertise system health, Flash operation, etc. and are assignable.

3.6 Piezo Horn

A horn is connected to the module's edge card connector through an open collector device and is attached to edge card connector J11-64.

3.7 Serial Data Buffers

Two tri-state buffers are used on the base PCB assembly to drive off-board TTL devices.

3.8 Unregulated Power Supply Input

Normally, DC power is supplied by the UPS. However, a barrel type power jack (SwitchCraft RAPC712) may be is used to interface unregulated DC power to the base platform PCB

assembly. The reference platform supports a wide input voltage range (4.4-35 volts DC @ 0.5 amp).

The following link illustrates the mechanical specifications of the barrel connector. http://www.switchcraft.com/products/pdf_files/rasm712_cd.pdf. The RAP712 is designed for center positive. To add the power jack, insure that the solder located left in the holes at J7 of the baseboard PCB assembly is removed using a de-soldering tool. Then insert the connector and solder the pins into place.

3.9 Regulated Power Supply and Power Consumption

A 3.3 volt 1 amp switcher type power supply provides power to the base platform and Toolkit Module assemblies. The power supply accepts a wide input voltage range between 4.4 and 35 volts DC as indicated in section 3.8.

The power consumption of the complete reference platform is 0.924 Watts.

Appendix A

Toolkit Module Edge Card 144 Pin Assignments

This section describes external interfaces to the Toolkit Module. Signal names proceeded with # are active low. Software-defined signals are in *italics*. The most common use for these signals is shown. Refer to the AT91RM9200 manual for reprogramming options and limitations.

Pin	Signal Source	Signal Name	I/O	Description
1	U9-7	ETXD+	Output	Ethernet Transmitted Data Positive
2	U9-8	ETXD-	Output	Ethernet Transmitted Data Negative
3	U9-3	ERXD+	Input	Ethernet Received Data Positive
4	U9-4	ERXD-	Input	Ethernet Received Data Positive
5	U9-11	LED_COLL	Output	Ethernet-1 Link LED
6	U9-12	LED_SPD	Output	Ethernet-1 Speed LED
7	U9-13	LED_LNK	Output	Ethernet-1 Data LED
8	VDDA	ETH AVDD	Power	Ethernet Analog VDD
9	AGND	ETH AGND	Power	Ethernet Analog Ground
10	PA17	*TXD0*	Output TTL	Serial Port 0 Transmit Data
11	PA18	*RXD0*	Input TTL	Serial Port 0 Receive Data
12	PA21	*RTS0*	Output TTL	Serial Port 0 Request To Send
13	PA20	*CTS0*	Input TTL	Serial Port 0 Clear To Send
14	PA23	*TXD2/IRQ3*	Output TTL	Serial Port 2 Transmit Data
15	PA22	*RXD2*	Input TTL	Serial Port 2 Receive Data
16	PA31	RTS2/DTxD	Output TTL	Serial Port 2 Request To Send / Debug Port Transmit
17	PA30	CTS2/DRxD	Input TTL	Serial Port 2 Clear To Send / Debug Port Receive
18	PA5	*TXD3/NPCS2*	Output TTL	Serial Port 3 Transmit Data
19	PA6	*RXD3/NPCS3*	Input TTL	Serial Port 3 Receive Data
20	PB0	*RTS3*	Output TTL	Serial Port 3 Request To Send
21	PB1	*CTS3*	Input TTL	Serial Port 3 Clear To Send
22	PB20	*TXD1*	Output TTL	Serial Port 1 Transmit Data
23	PB21	*RXD1*	Input TTL	Serial Port 1 Receive Data
24	PB26	*RTS1*	Output TTL	Serial Port 1 Request To Send
25	PB24	*CTS1*	Input TTL	Serial Port 1 Clear To Send
26	PB25	*DSR1*	Input TTL	Serial Port 1 Data Set Ready
27	PB19	*DTR1*	Output TTL	Serial Port 1 Data Terminal Ready
28	PB23	*CD1*	Input TTL	Serial Port 1 Carrier Detect
29	PB18	*RI1*	Input TTL	Serial Port 1 Ring Indicator
30	ARM9-K3	USB_HDA-	Bi-directional	USB Host A DATA -
31	ARM9-K1	USB_HDA+	Bi-directional	USB Host A DATA +
32	ARM9-K2	USB_DD-	Bi-directional	USB Device DATA -
33	ARM9-K5	USB_DD+	Bi-directional	USB Device DATA +
34	3.3VDD	3.3VDD	Power	VDD 3.3V Power supply
35	PD4	USB_CNX	Bi-directional	USB Device port connection detect
36	GND	GND	Power	Ground
37	PB6	*TIOA3*	Bi-directional	TIOA3
38	ARM9-K5	USB_HDB+	Bi-directional	USB Host B DATA-
39	ARM9-K2	USB_HDB-	Bi-directional	USB Host B DATA+

Pin	Signal Source	Signal Name	I/O	Description
40	PB9	*TIOB4*	Bi-directional	TIOB4
41	ARM9-E5	TCLK	Bi-directional	JTAG Test Clock
42	ARM9-A1	TDI	Input	JTAG Test Data In
43	ARM9-B1	TDO	Input	JTAG Test Data Out
44	ARM9-C1	TMS	Output	JTAG Test Mode Select
45	ARM9-E2	#NTRST	Input	JTAG Test Reset Signal, must be asserted during reset even if JTAG/ETM is not used.
46	ARM9-A2	JTAGSEL	Input	JTAG Select
47	PA0	*MISO*	Input	Master Input Slave Output / SRxD
48	PA1	*MOSI*	Bi-directional	Master Output Slave Input / STxD
49	PA2	*SPCK*	Bi-directional	SPI Clock
50	PA3	*#NPCS0*	Bi-directional	Slave Select / SCHS (SPI CS2)
51	PA4	*#NPSC1*	Output	Slave Select / SCHS (SPI CS3)
52	3.3VDD	3.3VDD	Power	VDD 3.3V Power supply
53	GND	GND	Power	Ground
54	PA24	*SCK2/PCK1*	Bi-directional	Serial Synchronous Clock_2 or programmable Clock
55	PA25	*TWD / IRQ_2*	Input	Two Wire Data or IRQ_2
56	PA26	*TWCLK/IRQ_1*	Input	Two Wire Clock or IRQ_1
57	PA27	*MMCCK*	Input	MMCCK
58	PA28	*MMC_CMD*	Input	MMC_COMMAND
59	PA29	*MCDA0*	Bi-directional	MMC Data0
60	PB2	*LED*	Output	LED
61	PB3	*MCDA1*	Bi-directional	MMC Data1
62	PB4	*MCDA2*	Bi-directional	MMC Data2
63	PB5	*MCDA3*	Bi-directional	MMC Data3
64	PB6	*PB6*	Bi-directional	unused I/O Buzzer
65	PB7	*MMC_TYPE*	Bi-directional	Multi-Media Type
66	PB8	*#CF_CD*	Bi-directional	Compact Flash Card Detect
67	3.3VDD	3.3VDD	Power	VDD 3.3V Power supply
68	GND	GND	Power	Ground
69	PB10	*RK1/TIOA5*	Bi-directional	Receive Clock (unused I/O)
70	PB11	*RF1/TIOB5*	Bi-directional	Receive Frame (unused I/O)
71	PB12	*TF2/ETX2*	Bi-directional	Transmit Frame (unused I/O)
72	PB13	*TK2 /ETX3*	Bi-directional	Transmit Clock (unused I/O)
73	PB14	*TD2/ETXER*	Bi-directional	Transmit Data (unused I/O)
74	PB15	*RD2/ERX2*	Bi-directional	Receive Data (unused I/O)
75	PB16	*RK2/ERX3*	Bi-directional	Receive Clock (unused I/O)
76	PB17	*RF2/ERXDV*	Bi-directional	(unused I/O)
77	PB22	*SCK1*	Output	(unused I/O)
78	PB27	*PCK0*	Output	(unused I/O)
79	PB28	*FIQ*	Input	Fast Interrupt Input
80	PB29	*#IRQ_0*	Input	IRQ_0
81	PC0	*BFCK*	Bi-directional	Burst Flash Clock
82	PC1	*#BFRDY*	Bi-directional	Burst Flash Ready
83	PC2	*BFAVD*	Bi-directional	Burst Flash
84	PC3	*BFBAA*	Bi-directional	Burst Flash
85	PC5	*#CF_ RST*	Output	Compact Flash Reset

Pin	Signal Source	Signal Name	I/O	Description
86	PC6	*# CF_ BSY*	Input	Compact Flash Busy
87	PC10	*#CFCS*	Output	Compact Flash Chip Select
88	PC11	*#CFCE1*	Output	Compact Flash Chip Select 1
89	PC12	*#CFCE2*	Output	Compact Flash Chip Select 2
90	ARM9-T6	#NCS2	Output	Chip Select
91	PC13	*#NCS7*	Output	Chip Select
92	PC14	*Hold*	Bi-directional	unused I/O
93	PD0	*ETX0*	Bi-directional	unused I/O
94	PD1	*ETX1*	Bi-directional	Finger Chip Support
95	PD2	*ETX2*	Bi-directional	Finger Chip Support
96	PD3	*ETX3*	Bi-directional	Finger Chip Support
97	PD7	*PCK0/TSYNC*	Bi-directional	unused I/O
98	PD8	*PCK1/TCLK*	Bi-directional	unused I/O
99	PD9	*PCK2/TPS0*	Bi-directional	MN4.B6 (Unused I/O)
100	PD10	*PCK3/TPS1*	Bi-directional	MN4.C6 (Unused I/O)
101	PD18	*#NPCS_1B*	Bi-directional	MN4.G5 SPI_1_Chip_Select
102	PD19	*#NPCS_2*	Bi-directional	MN4.G1 SPI_2_Chip_Select
103	PD20	*#NPCS_3*	Bi-directional	MN4.H2 SPI_3_Chip_Select
104	3.3VDD	3.3VDD	Power	VDD 3.3V Power supply
105	GND	GND	Power	Ground
106	RST Controller out	#NRST	Open coll	ARM9 reset
107	74ALVC16835-U13-3	AB0	Output	Buffered Address for external devices. Addresses are output even during internal module accesses
108	74ALVC16835-U13-5	AB1	Output	Buffered Address
109	74ALVC16835-U13-6	AB2	Output	Buffered Address
110	74ALVC16835-U13-8	AB3	Output	Buffered Address
111	74ALVC16835-U13-9	AB4	Output	Buffered Address
112	74ALVC16835-U13-10	AB5	Output	Buffered Address
113	74ALVC16835-U13-12	AB6	Output	Buffered Address
114	74ALVC16835-U13-13	AB7	Output	Buffered Address
115	74ALVC16835-U13-14	AB8	Output	Buffered Address
116	74ALVC16835-U13-15	AB9	Output	Buffered Address
117	74ALVC16835-U13-16	AB10	Output	Buffered Address
118	74ALVC16835-U2-23	*#CF_WE*	Output	Buffered CF Write Enable
119	74ALVC16835-U2-24	*#CF_OE*	Output	Buffered CF Output Enable
120	74ALVC16835-U2-20	*#CF_IOR*	Output	Buffered CF I/O Read
121	74ALVC16835-U2-21	*#CF_IOW*	Output	Buffered CF I/O Write
122	74ALVC16835-U2-13	AB25	Output	Buffered CF Read Not Write
123	74ALVC16835-U2-9	AB22	Output	Buffered Compact Flash #REG
124	RST Controller In	#MR	Input	External master reset, pulled up to Vdd through 65k.
125	3.3VDD	3.3VDD	Power	VDD 3.3V Power supply
126	GND	GND	Power	Ground
127	74ALVCH16245-2	DB0	Bi-directional	Buffered Data Bus interface for external devices. A “bus hold” function allows the external bus to float

Pin	Signal Source	Signal Name	I/O	Description
				during a processor read cycle.
128	74ALVCH16245-3	DB1	Bi-directional	Buffered Data BUS
129	74ALVCH16245-5	DB2	Bi-directional	Buffered Data BUS
130	74ALVCH16245-6	DB3	Bi-directional	Buffered Data BUS
131	74ALVCH16245-8	DB4	Bi-directional	Buffered Data BUS
132	74ALVCH16245-9	DB5	Bi-directional	Buffered Data BUS
133	74ALVCH16245-11	DB6	Bi-directional	Buffered Data BUS
134	74ALVCH16245-12	DB7	Bi-directional	Buffered Data BUS
135	74ALVCH16245-13	DB8	Bi-directional	Buffered Data BUS
136	74ALVCH16245-14	DB9	Bi-directional	Buffered Data BUS
137	74ALVCH16245-16	DB10	Bi-directional	Buffered Data BUS
138	74ALVCH16245-17	DB11	Bi-directional	Buffered Data BUS
139	74ALVCH16245-19	DB12	Bi-directional	Buffered Data BUS
140	74ALVCH16245-20	DB13	Bi-directional	Buffered Data BUS
141	74ALVCH16245-22	DB14	Bi-directional	Buffered Data BUS
142	74ALVCH16245-23	DB15	Bi-directional	Buffered Data BUS
143	3.3VDD	3.3VDD	Power	VDD 3.3V Power supply
144	GND	GND	Power	Ground

Appendix B

Toolkit Module Electrical Specifications

ABSOLUTE MAXIMUM RATINGS

The values shown are “stress limits”, and permanent module damage may occur if any of these values are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to absolute maximum ratings for extended periods could affect reliability.

Parameter	Symbol	Value	Unit	Note
Temperature under Bias (Commercial)	Top	0 to 70	°C	
Temperature under Bias (Industrial)	Top	-40 to 85	°C	
Storage temperature	TSTG	-60 to 150	°C	
Supply Voltage	Vdd, AVdd	-0.3 to 3.6	VDC	
Voltage on any pin relative to GND (Except USB Voltage)	VIN, VOUT	-0.3 to 3.6	V	
Voltage on USB Power	VUSB	-0.3 to 5.3	VDC	
Short circuit current (All signals at edge connector except Address and Data)	IOS1	±8	mA	1
Short circuit current (Address and Data bus only)	IOS2	-50 to 50	mA	1
Power dissipation	IOS3	7	W	1

Note 1: Output shorted for no more than one second. No more than one output shorted at a time.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Parameter	Symbol	Min.	Max.	Unit	Note
Operating Temperature (Commercial)	TA	0	70	°C	Ambient Temperature
Operating Temperature (Industrial)	TA	-40	85	°C	Ambient Temperature
Supply voltage	VDD	2.7	3.6	V	
Input Voltage (USB)*	VUSB	4.4	5.25	V	*USB power not required
Input high voltage	VIH	2.0	Vdd+0.3	V	1
Input low voltage	VIL	-0.3	0.8	V	1
Output high voltage	VOH	Vdd-0.4	-	V	IOH = -8mA
Output low voltage	VOL	-	0.4	V	IOL = 8mA
Input leakage current	IIL	-1	1	µA	Input pull-ups disabled
Input pullup current	IPU	-	322	µA	Vdd = 3.6V

Recommended operating conditions (Voltages referenced to GND, TA = 0 to 70°C)

Note 1: VCC = 2.7V to 3.6V
Note 2: 0V $\leq$ VIN $\leq$ VCCQ.

CAPACITANCE (VCC = 3.3V TA = 25°C)

Capacitance values shown are referenced at the module edge connector, and account for PCB trace capacitance.
(TA = +25°C, f = 1 MHz)

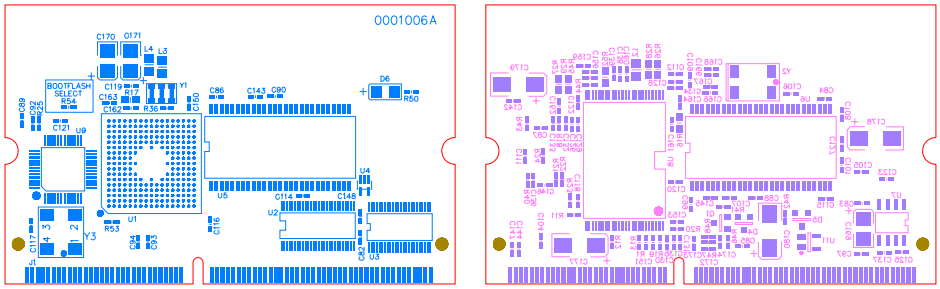
Parameter	Symbol	Min	Max	Unit	Condition	Note
Output capacitance (Address bus)	CIN1	12	14	pF	VIN = 0.0V	1
Input capacitance (#OE, #CE0, #WE, #RESET)	CIN2	29	37	pF	VIN = 0.0V	1
Input / Output capacitance (Data bus)	CI/O	12	14	pF	VOUT = 0.0V	1

Note 1: Sampled, not 100% tested.

Appendix C

Toolkit Module Mechanical Specifications

The edge card connector fingers of the Toolkit Module are gold-plated and should only be used in gold-plated sockets. Using tin-lead socket contacts will result in reliability problems. The connector routes power, buses, and ports to and from the system.



Dimensions:

Module Height:	1.650” (41.91mm)
Module Width:	2.662” (67.61mm)
Module Thickness:	0.660” (16.8mm)
PCB Thickness:	0.039” (1.0mm)
Weight:	0.18 pounds (85g) maximum.

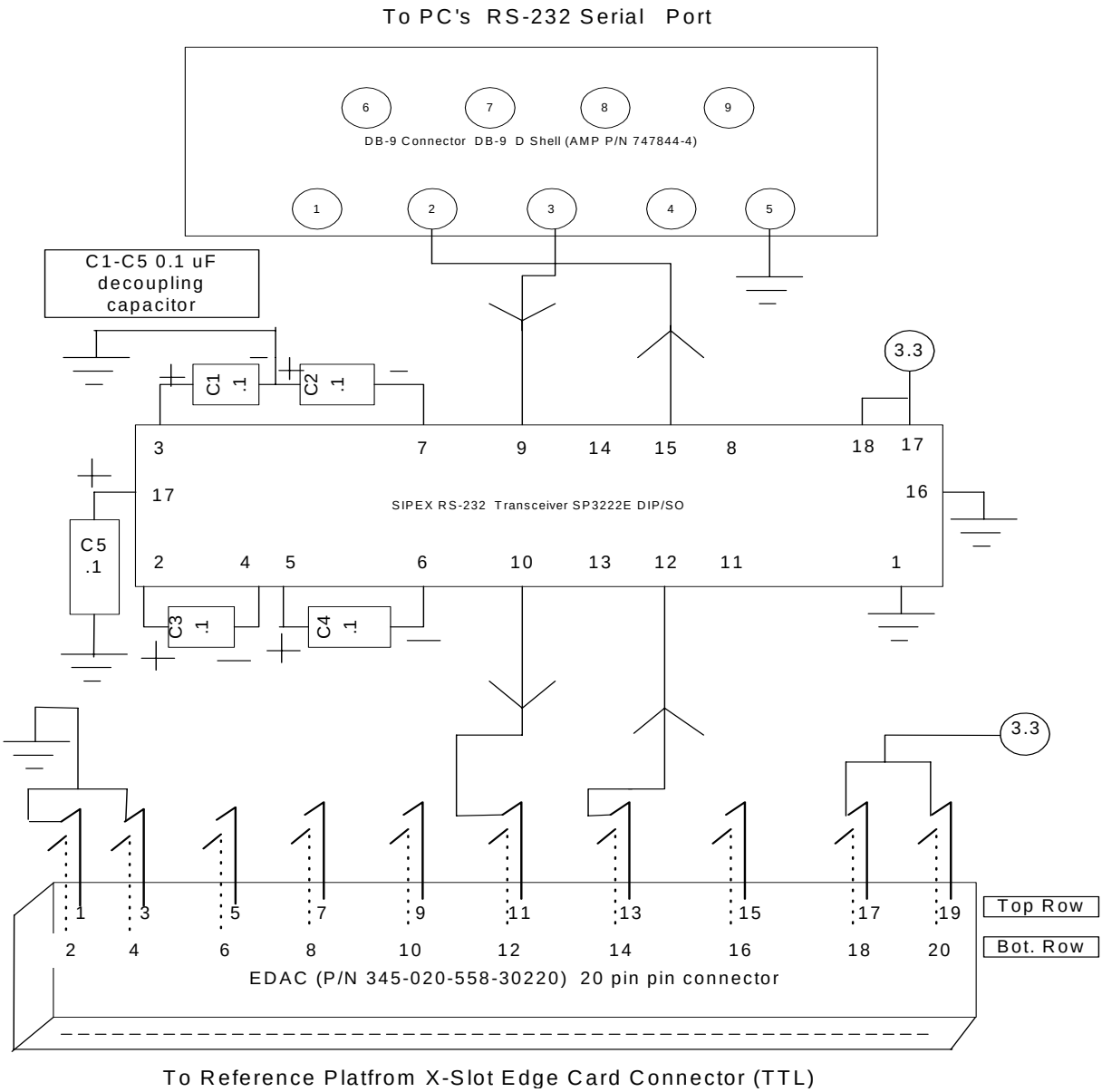
Appendix D

RoHS Compliance

The reference platform conforms to the RoHS directive.

Appendix E

Translator Interface Module Schematic



Note: Insure that a 3.3 volt connection is made on the base platform assembly by soldering a 28 gauge add wire between the positive side of C39 to pins 17 and 19 of the X-Slot 20 pin edge card connector.

Appendix F

Reference Platform Toolkit Module Schematic

Reference file: “Toolkit_Module_Schematic.pdf”, for the Toolkit Module schematic.

Reference Platform Base Platform Schematic

Reference file: “Toolkit_Base_Schematic.pdf”, for the Base Module Schematic.

Reference Platform Web Addresses

The following documents are used in conjunction with the hardware reference platform.

Author	Publication / Hyperlink	Description
Atmel	www.atmel.com/dyn/products/product_card.asp?part_id=2983	ARM9 Datasheets, summaries, reference manuals
ARM	www.arm.com/techdocs/5GWH8V/$File/DDI0180A_9tdmi_trm.pdf	ARM9TDMI Family detailed technical information.
JEDEC	www.jedec.org/download/search/MO-190d.pdf	144 Pin SODIMM Specification