Interface Design Guide for STMicroelectronics Cartesio™ Microprocessor

Micron® 512Mb Mobile DDR SDRAM

Introduction

The STMicroelectronics Cartesio™ STA2062 microprocessor is a highly integrated system-on-chip (SOC) application processor combining host capability with an embedded global positioning system (GPS). The STA2062 target markets include vehicle and portable navigation (PND), telematics, and advanced audio and connectivity systems. The STA2062 features an external dynamic memory bus that can be configured to interface with mobile DDR or SDR memory devices.

This technical note provides guidelines for interconnecting the STA2062 dynamic bus controller to two Micron® 512Mb Mobile DDR SDRAM devices to achieve a 128MB external dynamic memory without series termination resistors other than clock line parallel terminations. This technical note also describes some key features of mobile DDR technology, provides general guidelines for developing the PCB floor plan, and identifies considerations for optimal trace routing and decoupling.

Throughout this document, DRAM is used interchangeably with Mobile DDR SDRAM to improve readability.

STMicroelectronics Cartesio STA2062

The Cartesio STA2062 is a new generation of integrated, single-chip devices developed by STMicroelectronics. It combines the functionality and full peripherals set of the ARM926EJ-S™ 32-bit RISC multipoint control unit (MCU) including:

- 5-stage pipeline
- Harvard architecture (with separated I/O buses)
- 16 Kbyte cache for instructions and 16 KByte for data
- 32-channel high-performance GPS correlation embedded subsystem (RF front end not included)

The Cartesio STA2062 is well suited for portable navigation system applications requiring high performance and a broad range of communication peripherals. It performs at operating frequencies up to 333 MHz. For the current Cartesio STA2062 specifications, refer to the Cartesio STA2062 data sheet.

The Cartesio STA2062 processor interconnects with the ARM926 microcontroller, its peripherals, and the GPS engine, as shown in the top-level block diagram in Figure 1 on page 3.

Cartesio STA2062 Memory Interface

Cartesio features 4GB of linear address space with two external memory buses, managed by a flexible static memory controller (FSMC), and a synchronous DRAM memory controller (SDMC) for Mobile DDR/SDRAM. The Cartesio synchronous DRAM

controller is based on the ARM® PRIMECELL® PL175 multiport memory controller. This is an advanced microcontroller bus architecture (AMBA®) compliant SOC peripheral connecting to the advanced high-performance bus (AHB) that is developed, tested, and licensed by ARM® Limited.

The Cartesio dynamic memory controller provides two CS# pins. The 512Mb parts are addressed by 13 address lines and 2 bank addresses and a 16-bit data bus clocked at 166 Mhz in "overdrive" working conditions (V_{DD} = 1.4 ±5%V, V_{IO} = 1.8 ±10%V).

As shown in Figure 1 on page 3, the external memories connected to the SDMC can be accessed by any of the following:

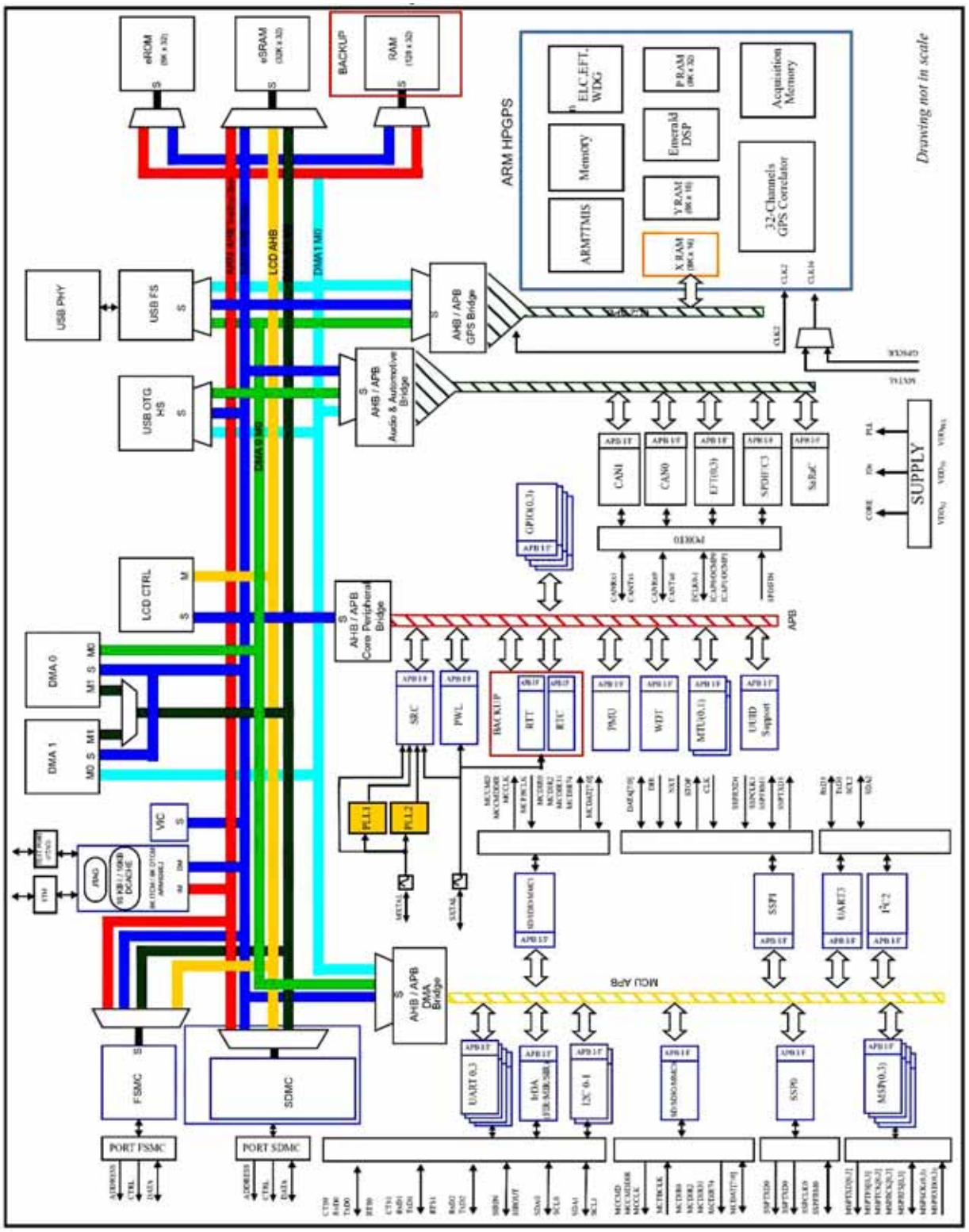
- ARM926EJ CPU instruction fetch bus (attached on AHB bus 5)
- ARM926EJ CPU data bus (attached on AHB bus 4)
- system DMA0 and DMA1 controllers
- LCD controller (attached on AHB bus 1)

Cartesio row-addressing capabilities support a microprocessor connection to monolithic x16 512Mb mobile DDR memory. A total of 128MB of dynamic memory can be accessed by connecting two 512Mb parts to two different chip selects that share the same address, control, and data lines. This configuration requires a strategic bus placement and routing process.

Because Cartesio is designed for use in small systems that typically consist of point-to-point connections, optional drive strength control is provided for the output buffers. Select drive strength based on the expected loading of the memory bus.

The three supported internal impedance settings for the output drivers include $Z_0 < 50\Omega$, $48\Omega < Z_0 < 61\Omega$, and $70\Omega < Z_0 < 80\Omega$. All the Cartesio DDR output buffers also feature an embedded series termination resistor of 20Ω ±25%.

Figure 1: STMicroelectronics Cartesio STA2062 Block Diagram



Notes: 1. Figure 1 is used with permission from STMicroelectronics.

Micron 512Mb Mobile DDR SDRAM

The Micron 512Mb Mobile DDR SDRAM, MT46H32M16LF, is a 536,870,912-bit high-speed CMOS, dynamic random access memory developed for low-power, portable applications. Mobile DDR SDRAM is typically used in point-to-point configurations and features configurable output-buffer drive strength. Four settings for the output drivers are supported: 25Ω, 37Ω, 55Ω, and 80Ω internal impedance, for full, three-quarter, one-half, and one-quarter drive strengths, respectively.

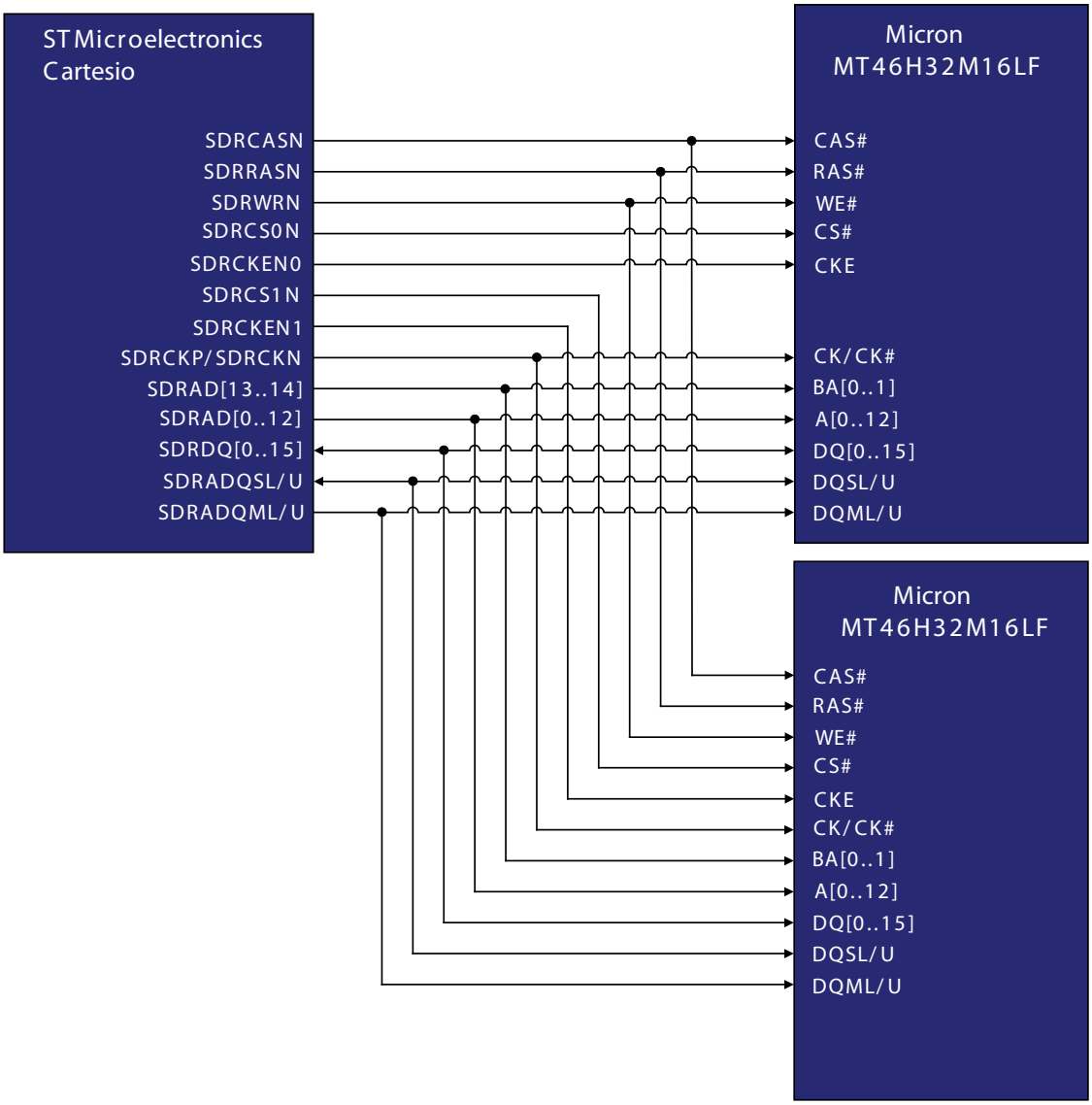
This technical note focuses on the 512Mb Mobile DDR SDRAM device. For more information on the device, refer to the data sheet.

Mobile DDR SDRAM Bus Connections

The two Micron MT46H32M16LF devices must be connected to the dynamic bus and managed by two different CSs; CS and CKE are single point-to-point connections, while data, data strobes, addresses, and control lines connect one point (the microprocessor) to two points (the memory devices). Data input/output and data strobes are also bi-directional lines.

All the connections between the Cartesio STA2062 and the two MT46H32M16LFBF devices are shown in Figure 2 on page 5.

Figure 2: Cartesio STA2062 Connections with Two 512Mb Micron Mobile DDR DRAM Devices



Printed Circuit Board (PCB) Stackup and Geometries

A well-designed PCB stackup is critical for eliminating digital switching noise. The use of FR-4 is the preferred solution for PCBs due to its low cost, low moisture absorption, and low electrical conductivity in board fabrication. FR-4 is a copper-clad laminate that offers exceptional dimensional stability, dielectric thickness control, and high quality manufacturing repeatability.

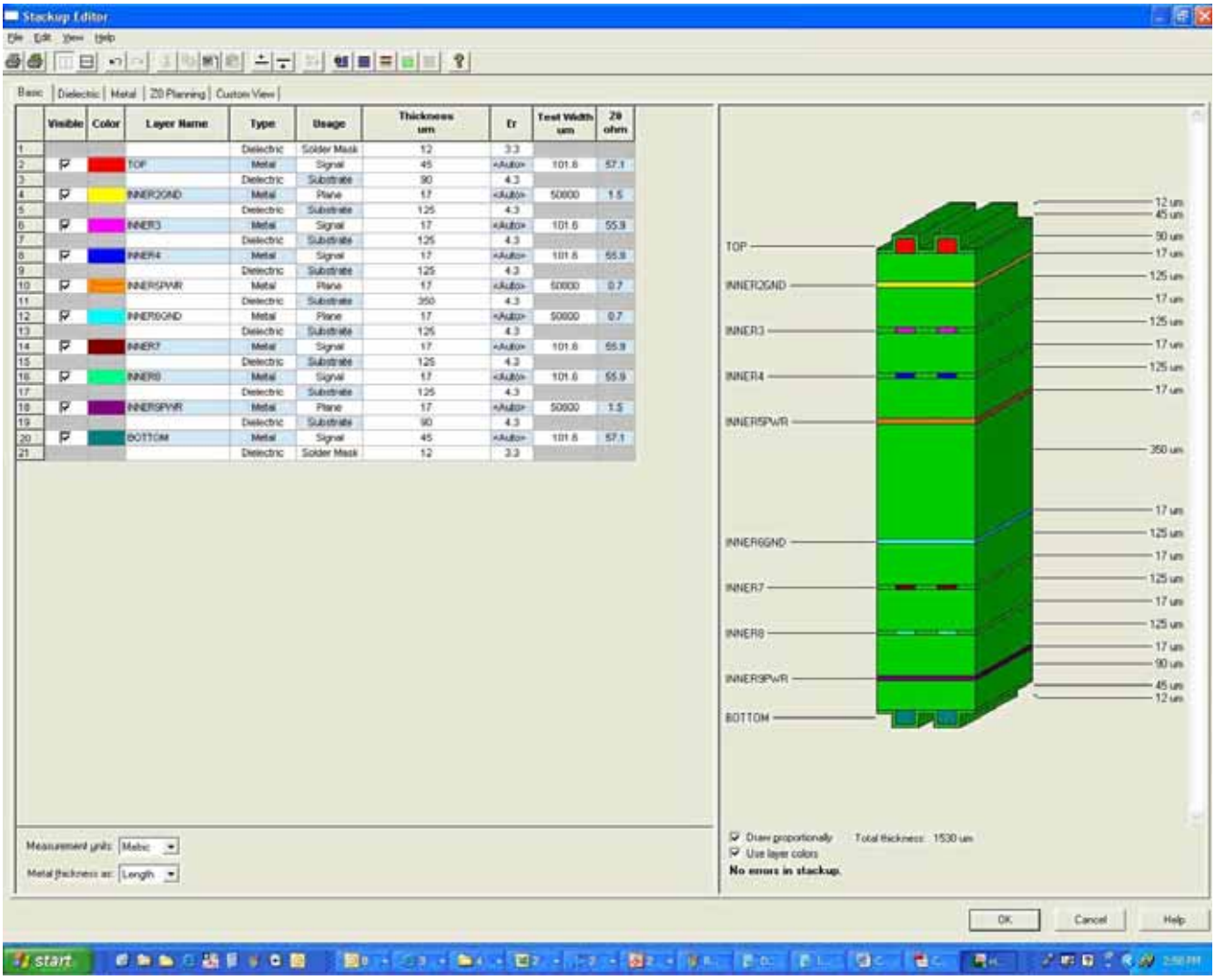
To help ensure signal integrity for this configuration, the best approach is to target a constant characteristic impedance in the Z_0 = 50Ω–55Ω range for all functional signal sets and for all layers.

Although a PCB design with a minimum of six layers is recommended—layers 1 (top), 3, 4, and 6 (bottom) for signals and layers 2 and 5 for ground/power—in this technical note, a 10-layer stackup is used because it is more suitable for automotive applications.

- Layers 1 (top) and 10 (bottom) are only used for fan-out from the microprocessor, DRAM devices, and passives (for example, the fan-out, connecting the ICs' pads to the closest through-hole via, which is hereafter referred to as via)
- Layers 2 and 6 are used for ground
- Layers 5 and 9 are used for I/O and core power
- Layers 3, 4, 7, and 8 are used for signal routing

The recommended 10-layer configuration is shown in Figure 3.

Figure 3: 10-Layer PCB Stackup



With this 10-layer PCB stackup configuration, a constant impedance of $Z_0 = 55 \pm 10\%\Omega$ can only be achieved by adopting a 4-mil trace width on all signal layers. In general, an average distance of 6 mil should be used between two adjacent traces on the same layer.

The only exception is the clock lines (see "Clock Routing" on page 16). A violation of the trace separation can be tolerated for a limited length, providing that the minimum spacing is larger than 4 mils, but only as an exception. Crosstalk is a function of trace spacing and slew rate; slower systems generally provide more timing budget, supporting additional crosstalk without affecting signal integrity.

Vertical crosstalk could occur in a dual stripline configuration as shown in the proposed stackup in Figure 3 on page 6. Take care to use a routing policy to prevent potentially hazardous vertical crosstalk (for example, dedicate a layer of the dual stripline couple [layers inner 3–4 and inner 7–8] as shown in Figure 3 on page 6) for horizontal routing and another for the vertical routing.

The ground plane must provide a low-impedance (Low-Z) return path to guarantee the integrity of high-speed digital signals. The proposed stackup helps minimize the length of this return path (loop area), thus reducing transient currents. This minimal-length return path, in conjunction with keeping most of the signal traces between solid planes, facilitates the containment of electromagnetic interference (EMI).

Return path discontinuities, including holes or splits in the reference planes that could divert the return current path, should be avoided. High-speed return currents should flow directly under the signal line; when the plane has a split, or a slot, the flow is disrupted.

Power and ground nets must be composed only of planes, not traces. To minimize trace inductance for integrated circuits (ICs), terminating resistors, or decoupling capacitors, connections required from power and ground to vias should be as short as possible. Connecting these traces to the closest via, using at least a 10-mil width, and keeping them as short as possible is strongly recommended.

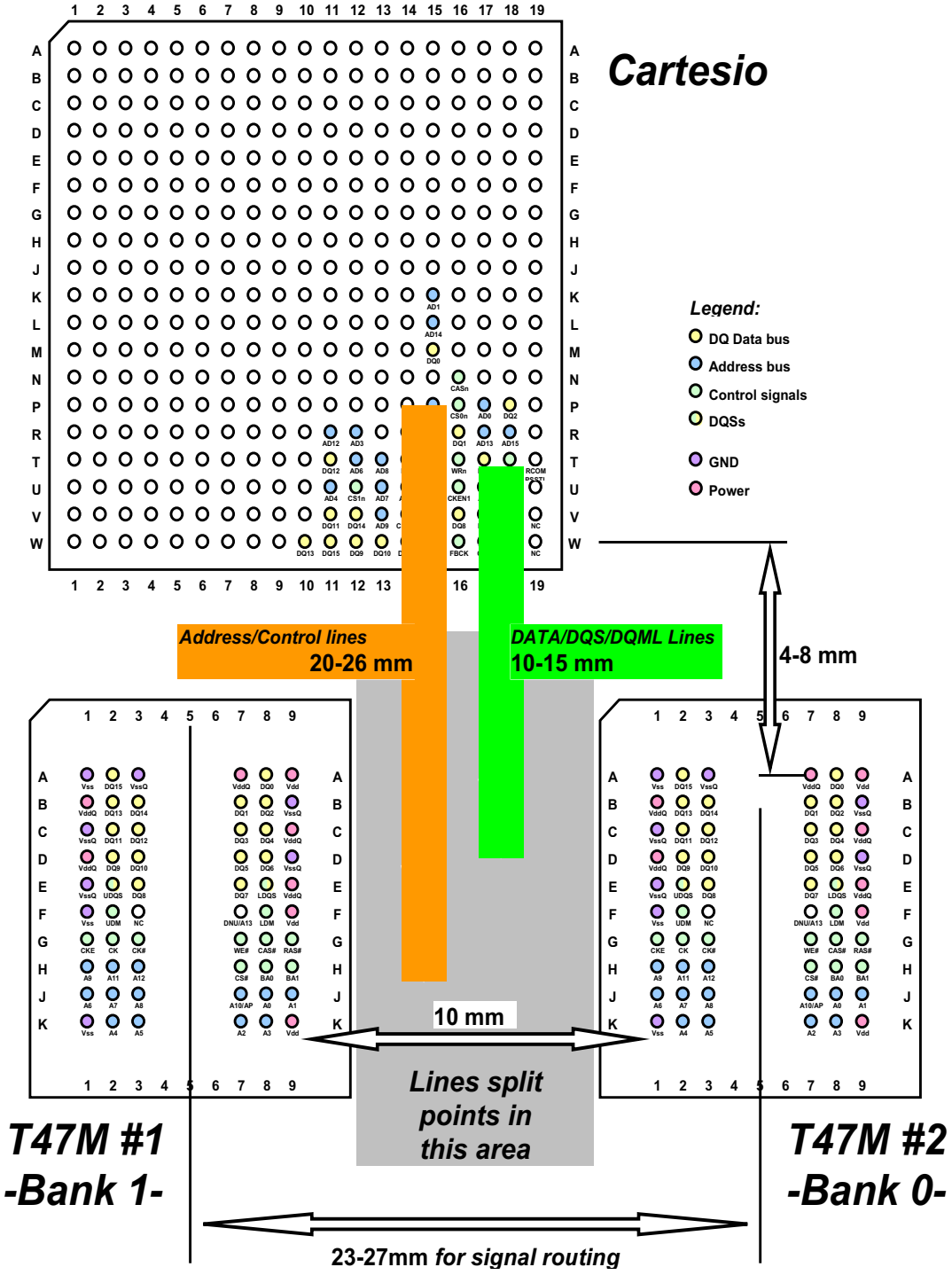
To improve decoupling in the suggested stackup, reducing the thickness of the dielectric stratum between layer 5 (V_{SS}) and layer 6 (V_{DD}) is also strongly recommended.

Mobile DDR SDRAM Placement

When developing the PCB floor plan, the proximity of the DRAM device to the memory controller is an important factor. If the memory is close to the controller, the layout is usually easier. For example, with short traces, the signals may not require series (RS) termination (as in this example), or, at worst case, would require only a small series resistor.

Not all point-to-point designs use a single memory device for each controller; many systems use two multiple memory devices. Quite often 2, 4, or 8 devices are used in parallel to create a wider data bus. In this scenario, the data and strobe connections are point-to-single-point connections; all the other lines are point-to-multiple-point connections. The unique aspect of the Cartesio configuration presented here is that the data and strobe traces must connect more than two ICs while avoiding use of a series-termination resistor. Because placement asserts a significant influence on routing, optimized placement is required to achieve the best performance from the system. Figure 4 on page 8 illustrates the recommended Cartesio and memory device placements.

Figure 4: Suggested Memory Device Placements



Data and strobe balls are all placed in the upper rows of the memory footprint. The configuration shown in Figure 4 on page 8 ensures the shortest path between the Cartesio and memory devices for the data class. Routing should be prioritized to deliver the fastest dynamic. Simulation shows that 10–15mm of additional PCB space provides

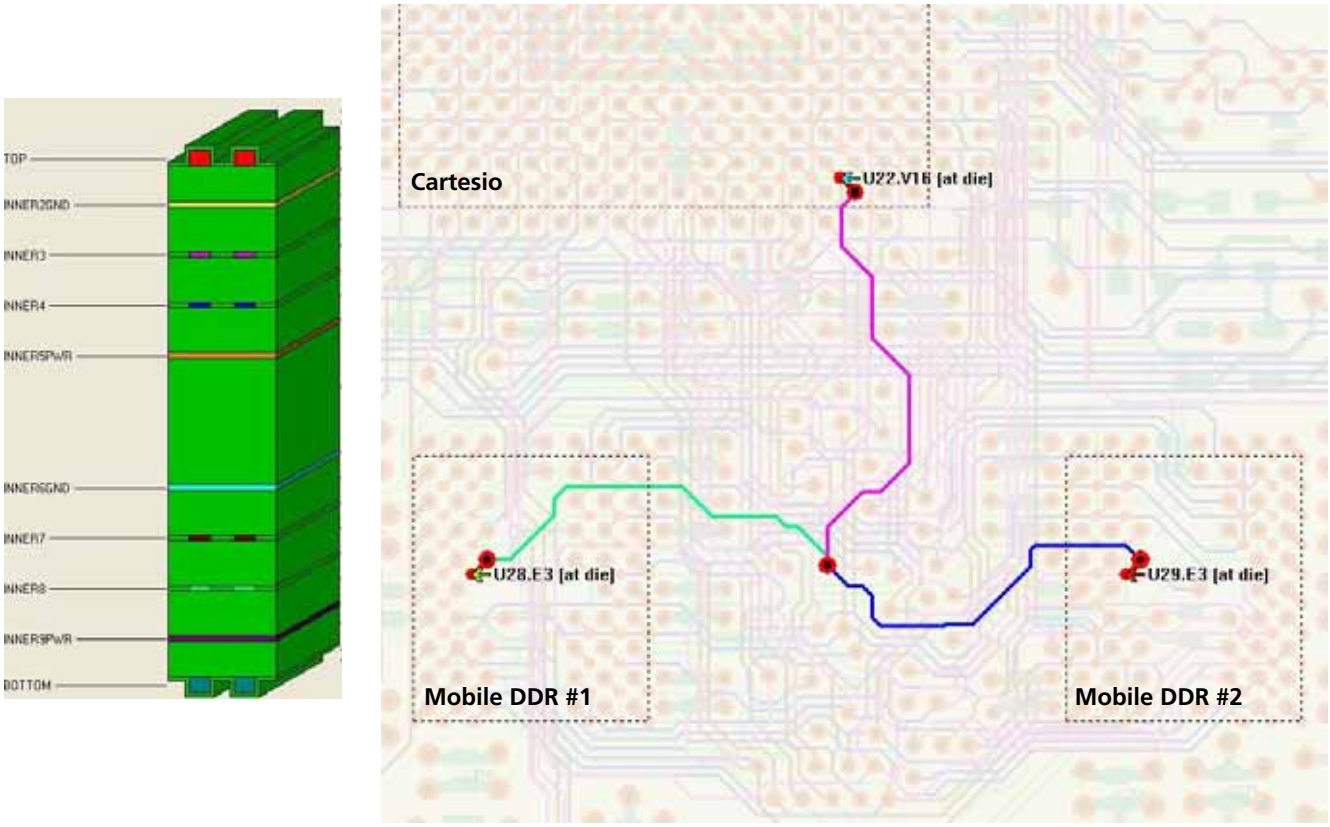
sufficient area for signal routing between the devices and the controller; the T-line split points (a via in most cases) should be placed in the area between the two devices (as shown in the gray area of Figure 4 on page 8).

A data line routing example is shown in Figure 5. Track segment colors indicate the layer used for each section:

- The red short trace reaching the ICs is on the top layer
- The blue trace is on layer inner 4
- The pink trace is on layer inner 3
- The green trace is on layer inner 8

The small, red circles represent the vias used to change layers. The same routing approach has been used for all signal classes.

Figure 5: Cartesio to DRAM T-Line Routing Example

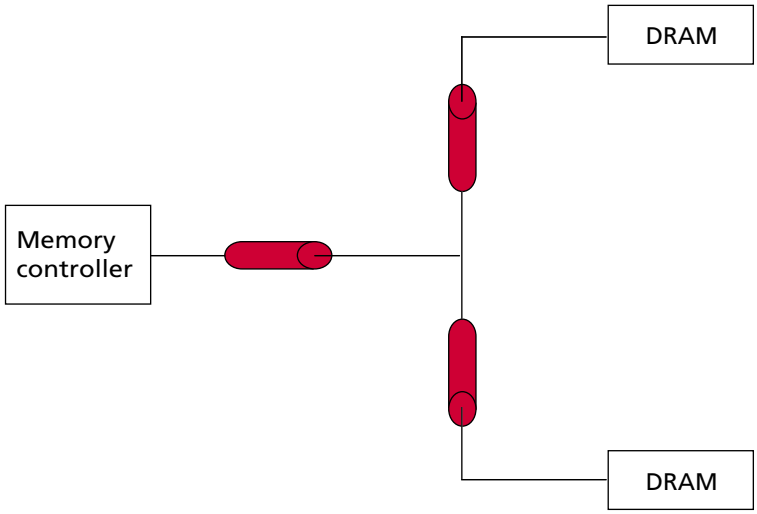


Command, Address, Control, and Data Routing

The mobile DDR device discussed in this technical note is source synchronous. Moving from a synchronous-based architecture to a source-synchronous architecture eliminates the flight-time delay that restricts speed. DRAM devices use bidirectional strobes as a data clock to eliminate flight-time delays. In a source-synchronous architecture, such as DDR, the board skew is a major speed limiter.

As in our example case, when the controller is driving more than one device, a matched tree-type routing pattern should be used (see Figure 6 on page 10).

Figure 6: Matched "Tree" Routing



The advantage of a matched tree topology is that all trace segments are balanced for each path. The total trace length to the first DRAM is identical to the total trace length to the last DRAM, and flight times for each DRAM are also the same. This helps to match timing; it also helps reduce transmission line effects by controlling reflections. In matched tree topologies, the first segment is typically the longest. As the segments get closer to the DRAM, they are shorter (especially in systems with four or more DRAM that require multilevel trees).

Although a memory component has many signals, most of the signals work together and have similar functionality. A group of I/O signals (a class) has one of four purposes:

- Carry a binary address
- Transmit or receive data
- Relay a command to the device
- Latch in address/data or a command

The address group consists of row/column address pins and bank address pins. The command group includes the row address strobe (RAS#), the column address strobe (CAS#), and write enable (WE#). The control group includes chip select (CS#) and clock enable (CKE).

Each data group/lane contains 10 signals: the eight DQ (DQ[7:0]), the strobe (DQS), and the data mask (DM). The system discussed in this technical note has a 16-bit data bus and features two data groups.

Recommendations for data-lane fanout include:

- Place alternate adjacent 10-line data lanes on different PCB stackup layers.
- Place data tracks on different layers from address and control lanes.
- Minimize skew within a signal class.
- Keep traces as short as possible.

If the total trace length is <2in (5cm), routing is simplified, and signal quality usually improves proportionately. In most cases, trace lengths >2in (5cm) lead to increased signal undershoot, overshoot, and ringing—all of which are detrimental to signal integrity (SI). Regardless of bus type, all DRAM signal groups must be properly referenced to a solid V_{SS} or V_{DD} plane. For both READs and WRITEs, the key relationships are among CK/CK#, DQ, DM, and DQS signals (the DRAM data group). This data group operates at twice the speed of other signal groups, making SI more critical.

The skew caused by trace-length mismatch can be calculated by multiplying the distance between the shortest and longest trace in the byte lane by the propagation delay of the trace. For the 10-layer stackup configuration suggested, the propagation delay associated with a microstrip trace (outer layers) or a stripline trace (inner layers) is 150ps or 175ps per inch, respectively, assuming an FR4 substrate (Er = 4.3). The propagation delay can vary depending on the dielectric constant of the PCB and the impedance of the trace.

Design Recommendations for Data, Strobes, Address, and Control-Line Routing

Restrict all traces to 20–25ps, which corresponds to about 3/4mm, within a byte lane to help diminish skew. This applies for all data lines and associated strobes and requires matching trace lengths for data groups within ±70 mil of each other. A 140-mil difference in trace lengths equates to 0.14in × (175ps of propagation delay per 1 inch of trace), or 25ps skew. Serpentine traces (back and forth traces in an “S” pattern to increase trace length) can be used to match lengths.

Timing between different byte lanes can usually be a bit more relaxed, typically within 70–80ps. Different DQ byte lanes should be matched to within 450 mil of each other. Figure 7 on page 12 and Figure 8 on page 13 provide examples of data line routing and data strobe routing, respectively. Match byte lane and clock trace lengths. Route byte lanes so that ±300 mil is the largest trace-length difference relative to the clock trace lengths.

Maintain a solid-ground reference (for example, no splits) for each group to provide a Low-Z return path; high-speed signals must not cross a plane split. DQ, DQS, and clock lines are best referenced to V_{SS} to minimize noise.

Address, command, and control signals are single-ended and are driven exclusively from the controller. Match clock traces to each signal trace in the address and command groups to within ±400 mil. If clock traces cannot be matched to the trace lengths of these groups within 400 mil, then all clock trace lengths must be increased as a group. If the timing budget can absorb this amount of lane-to-lane skew and other routing delays, the system will perform normally. Figure 9 on page 14, Figure 10 on page 15, and Figure 11 on page 16 provide examples of address and control-line routing.

Figure 7: Data Line Routing Example: DQ11 Line

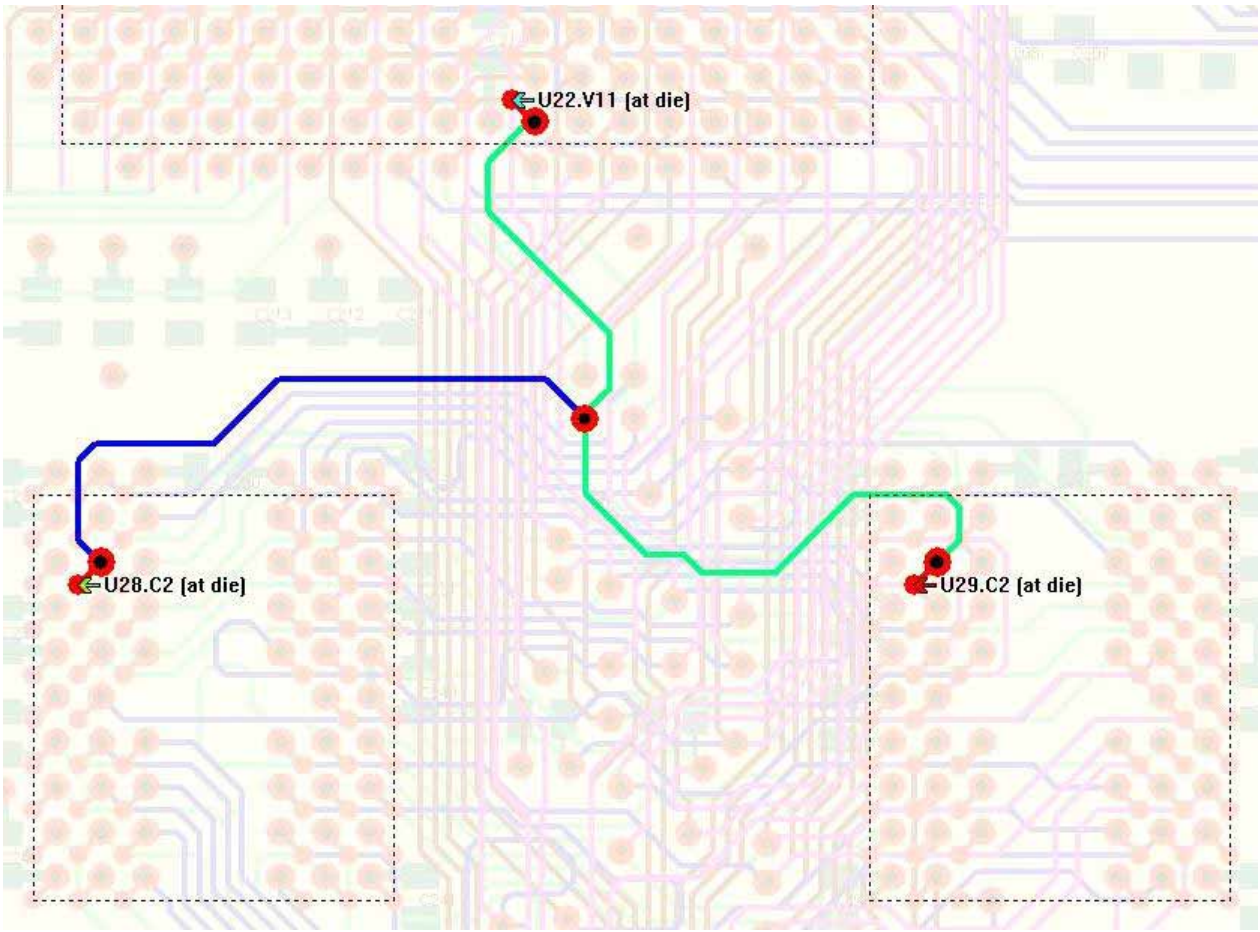


Figure 8: Data Strobe Line Routing Example: DQSU Line

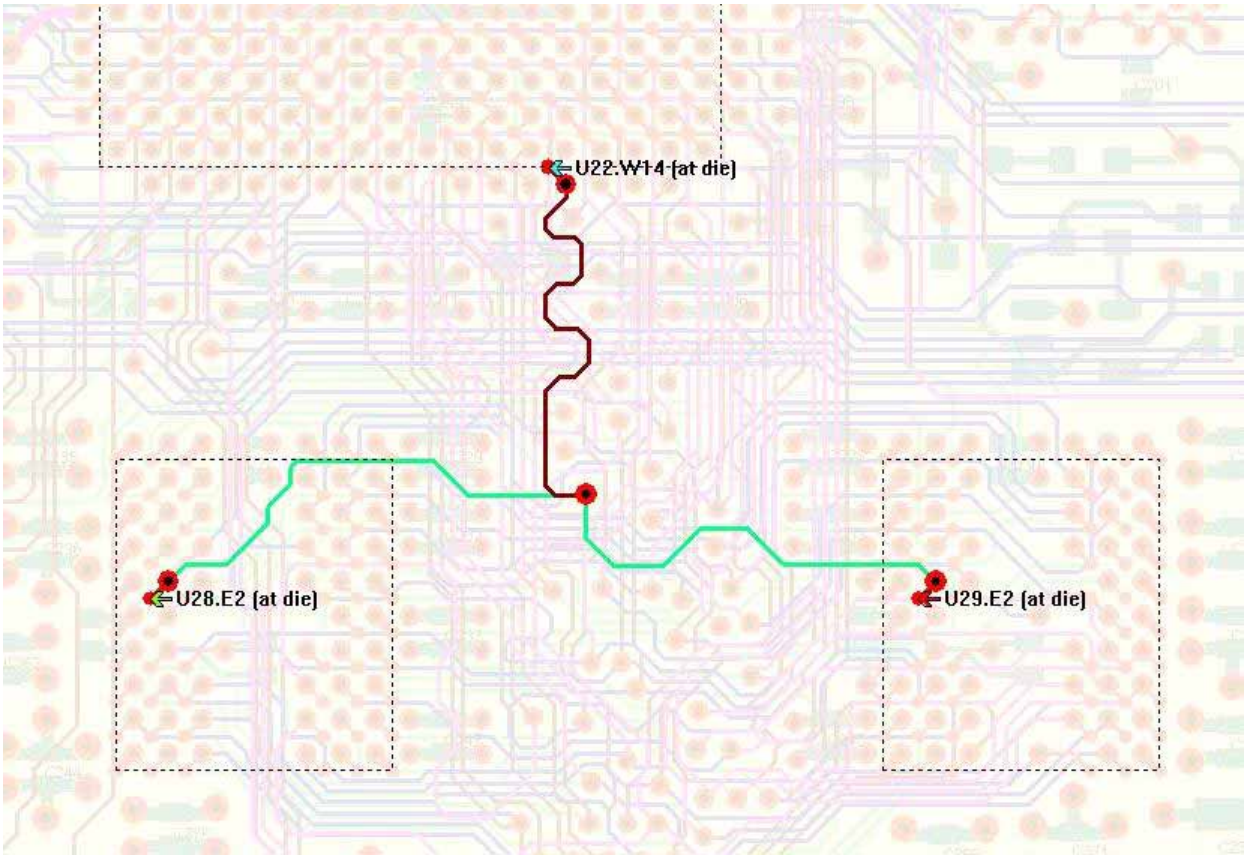


Figure 9: Address Line Routing Example: ADDR6 Line

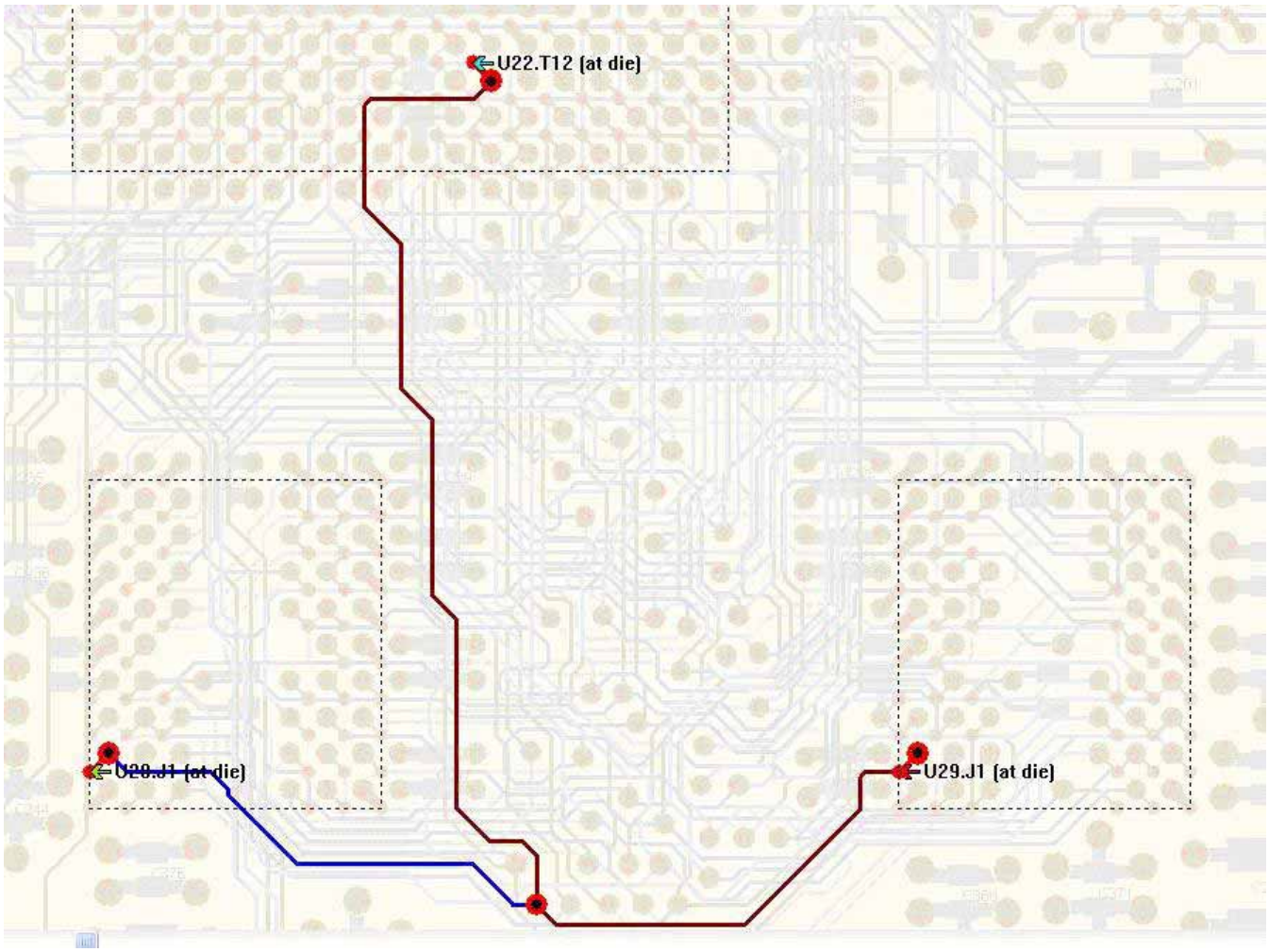


Figure 10: Command Line Routing Example: Single Point to Two Points, RAS# Line

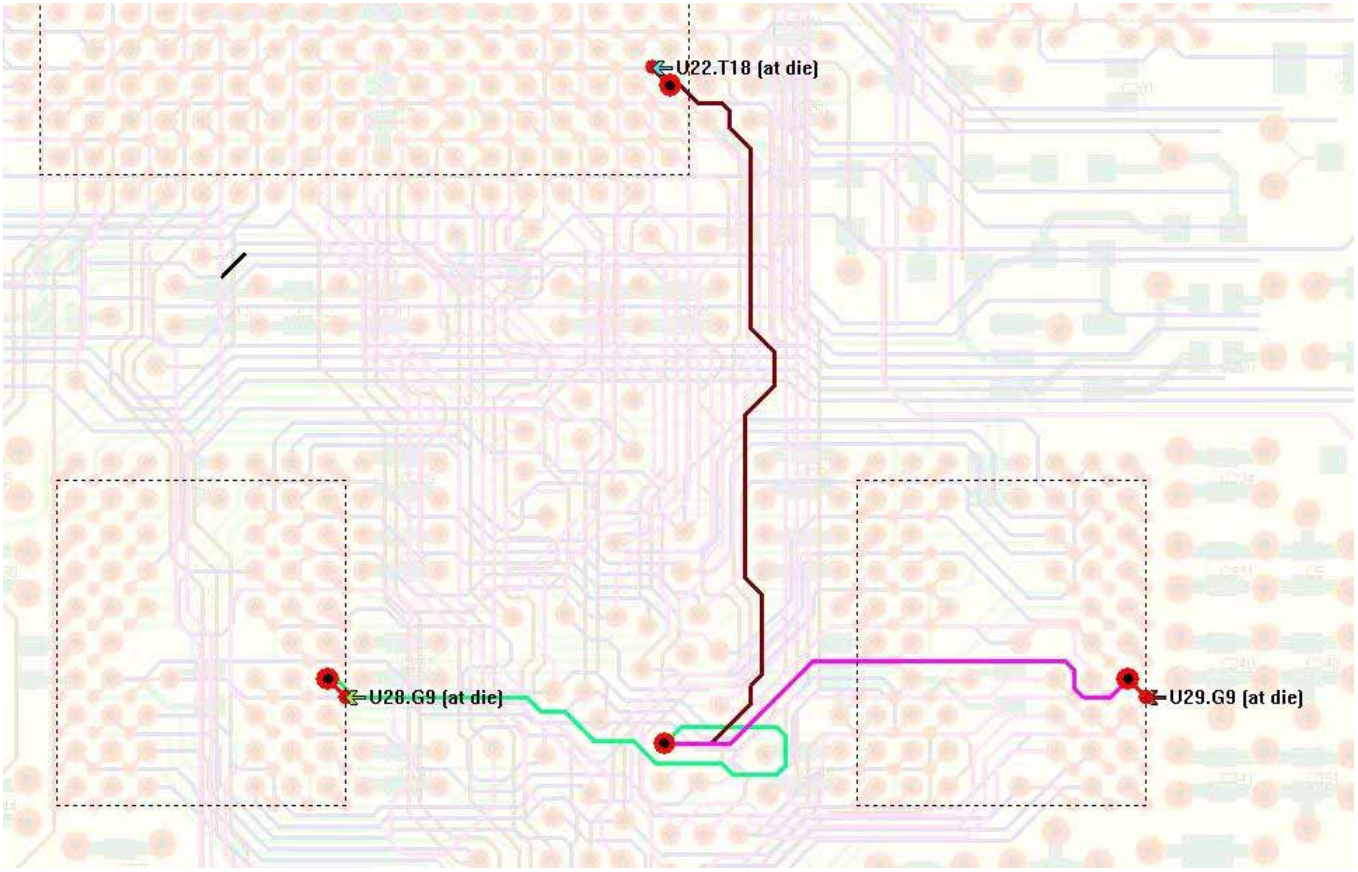
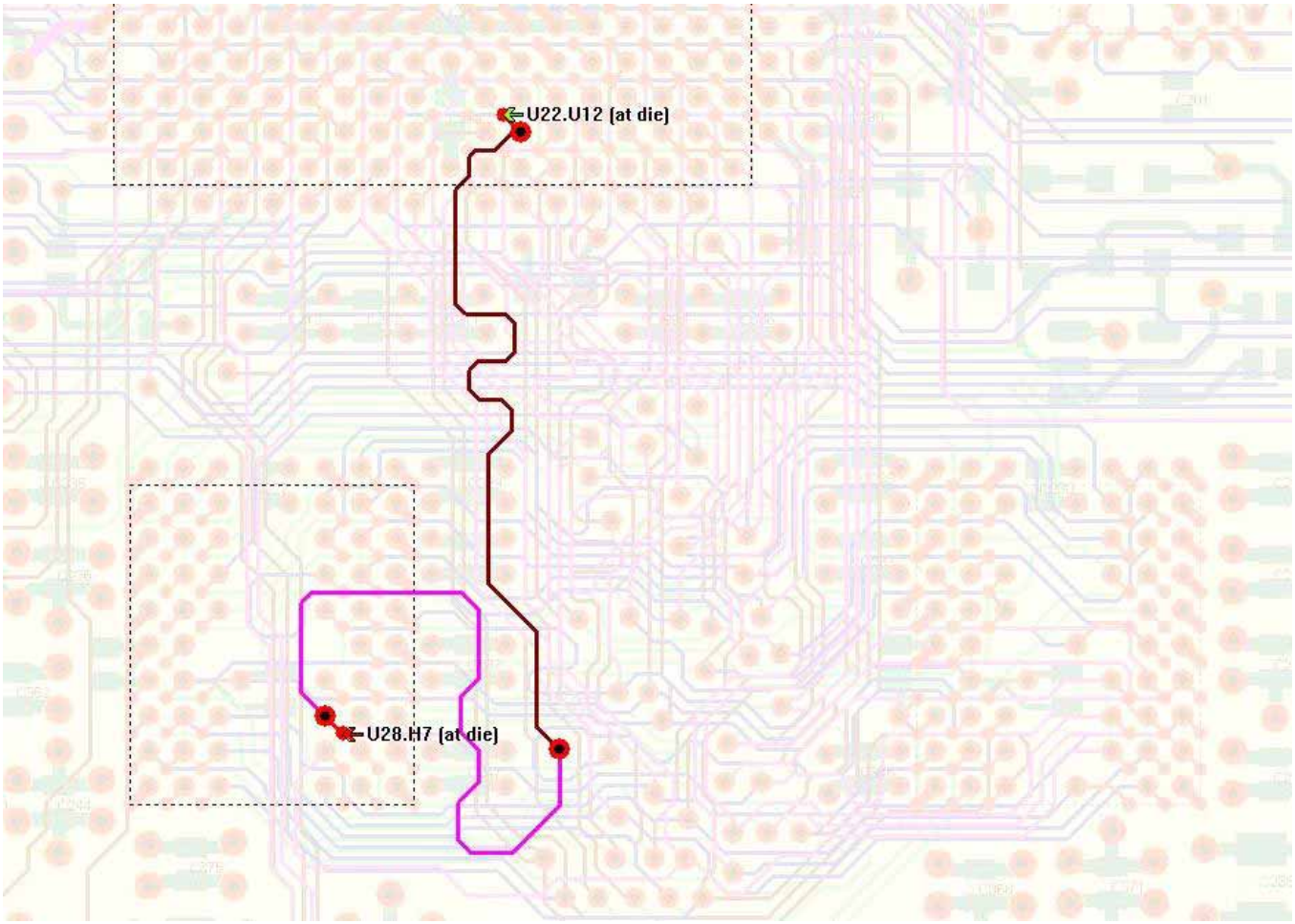


Figure 11: Control Line Routing Example: Point to Point, CS1# Line

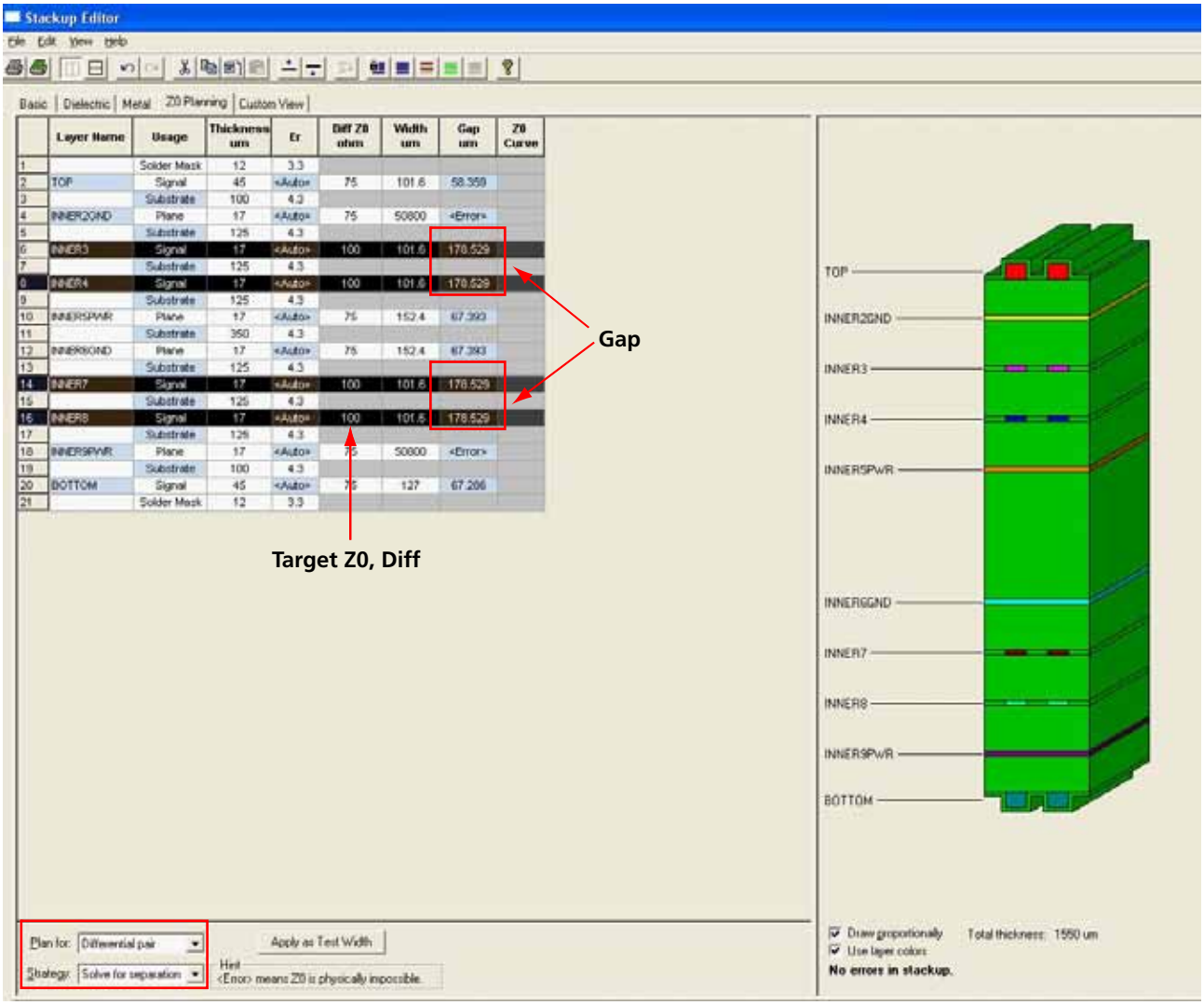


Clock Routing

The Mobile DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH, and CK# going LOW, are referred to as the positive edge of the internal memory device clock. Recommendations for differential clock routing include:

- Route the differential clock pair on the same layer.
- Place the clock signals on an internal layer to minimize noise (EMI).
- Use 4-mil-wide traces for CLK and CLK# signal lines to ensure characteristic impedance (Z_0) of 55Ω for each rail.
- Use a constant 7 mils (180µm) of separation between the two clock rails to ensure a differential characteristic impedance $Z_{0,DIFF}$= 100/120Ω (see inner 3 layer, inner 4 layer, inner 7 layer, and inner 8 layer of the suggested stackup in Figure 12 on page 17).

Figure 12: Stackup of Suggested Clearance Between Clock Rails



Match the CK trace length to the CK# trace length ±40 mil, and match the CK/CK# trace lengths to the DQS trace length ±300 mil. Matching the trace lengths to this level of accuracy helps meet the data sheet specification for clock input midpoint voltage ($V_{MP[DC]}$).

Use a differential termination resistor (R_T) between CK# and CK near the DRAM component input pins. Figure 13 on page 18 shows recommended DRAM clock routing topology and R_T placement for the two clock pairs. Use two resistors located as close as possible to the respective DRAM components. These resistors are in parallel so each R_T should be 200Ω to 240Ω to keep the effective resistance at 100Ω to 120Ω. Figure 14 on page 19 shows an example of clock-line routing.

Figure 13: Differential Resistor Placement for CK/CK# at DRAM Components

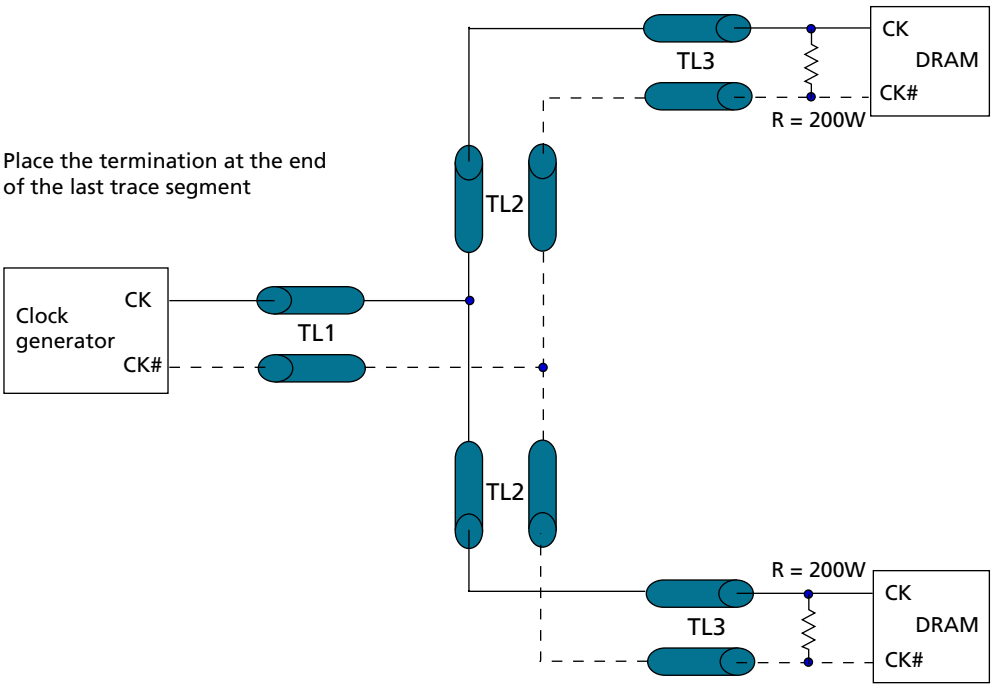
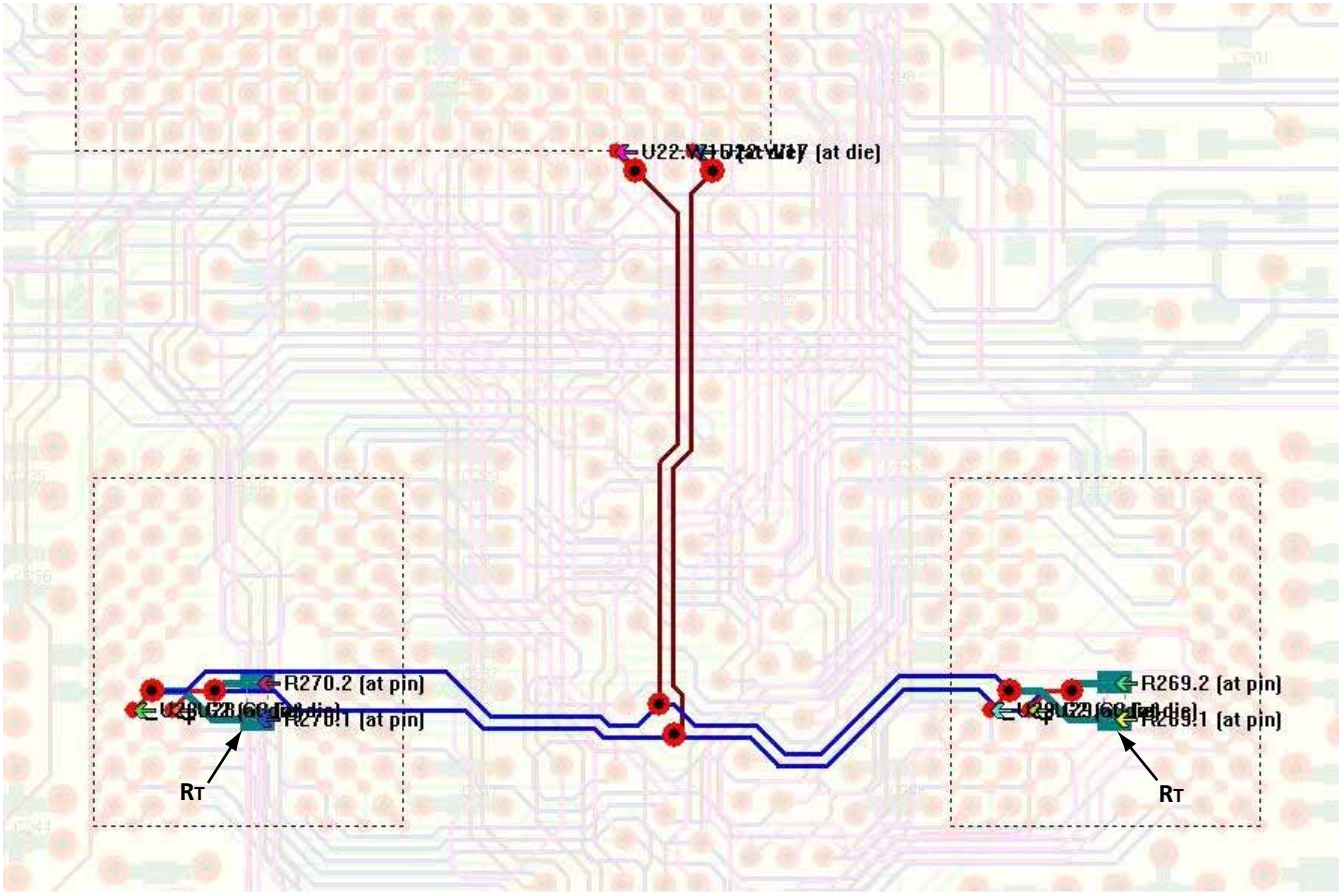


Figure 14: Clock Line Routing Example: Single Point to Two Points



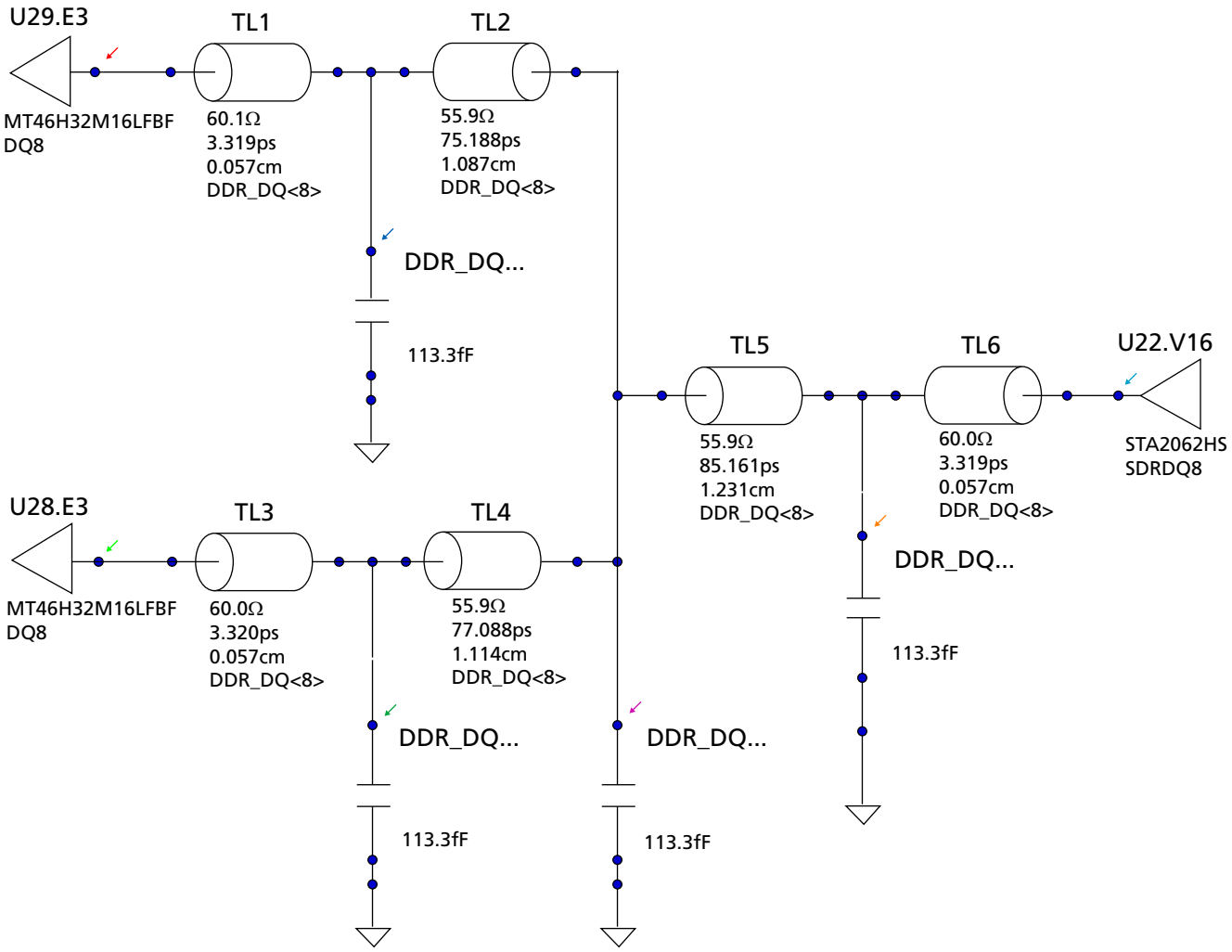
Line-Length Sensitivity Analysis

The initial sizing of a board design under development helps to determine the functional layout, while the sensitivity analysis tests the layout over a wide range of operating conditions. Sensitivity analysis helps locate problems and optimize system performance. Topology is one of the variables usually included in sensitivity analysis because its variations will help determine the effects of possible routing modifications and mismatched trace lengths.

The analysis has been performed by extracting all characteristics and parameters of two nets from a post-layout simulation bench for a real and optimized layout. The analysis uses the dual DRAM configuration for this technical note, together with the proposed 10-layer PCB stackup and requires importing them into a pre-layout simulator.

An address line (ADDR2) and a data line (DQ8) are used as representative samples of all signals driven by the microprocessor (command, controls, and address classes, together with the data class during a WRITE operation) and the memory (data lines during READs), respectively. The example transmission line model of the DQ8 line, as generated by the Hyperlynx simulator, is shown in Figure 15 on page 20.

Figure 15: DQ8 Net Transmission Line Model



In the model in Figure 15, different stubs and trunk-length combinations have been simulated without modifying the track-to-layer assignments or layer sequences. Only matched tree configurations have been analyzed because the equalization of the two stubs is the key element for improved signal quality. Table 1 on page 21 and Table 2 on page 22 show the lengths of the three sections (ADDR2 and DQ8 lines, respectively) and the corresponding layer used for each segment:

- Original corresponds to the net as defined in the actual simulated layout.
- Ideal represents the best (realistic) configuration.
- Configurations A and C use worst-case routing, which is still acceptable for ADDR2 and DQ8 nets, respectively.
- Configurations B and D are the shortest configurations and are not acceptable.

Table 1: Generic Address Line: Simulated Routing Configurations

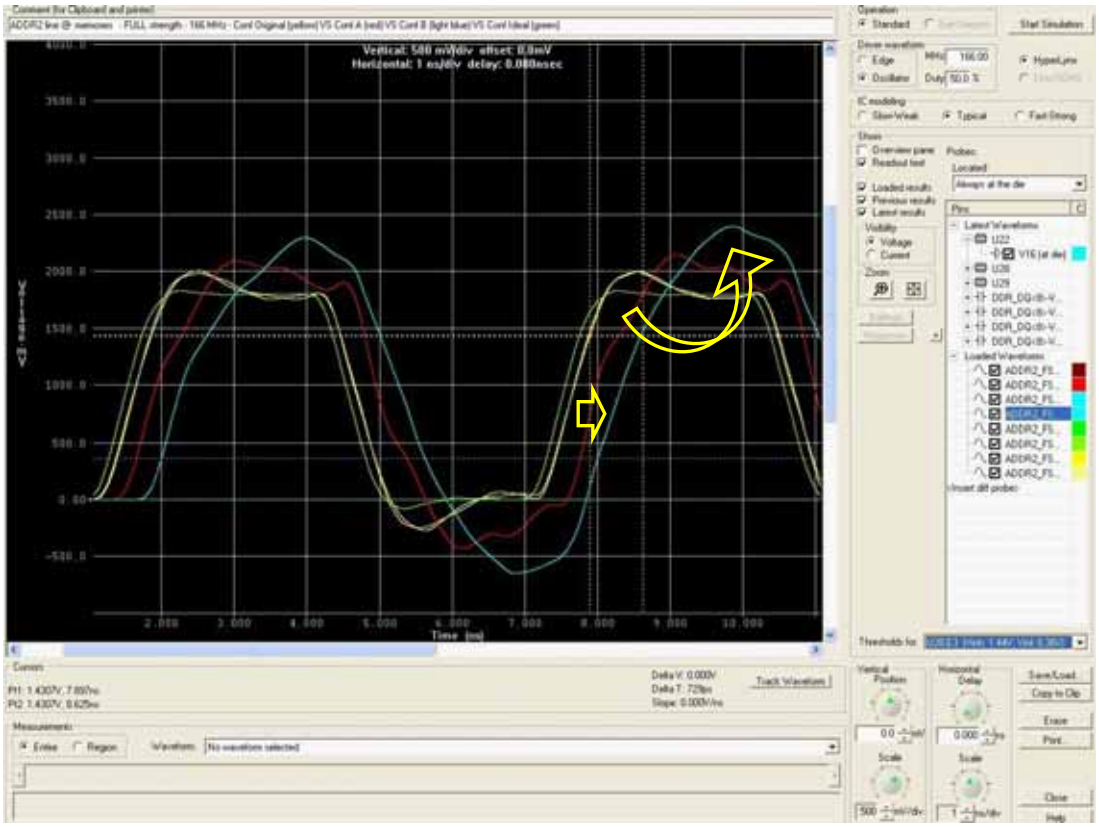
		Stub to DRAM #1	Stub to DRAM #2	Trunk to Cartesio
Layer		**Inner 3**	**Inner 8**	**Inner 7**
Configuration name	**Wave color**	**Length [µm]**	**Length [µm]**	**Length [µm]**
Original	Green	1,123	914	2,880
Ideal	Yellow	1,200	1,200	1,200
Configuration A (max acceptable)	Red	2,880	2,880	5,000
Configuration B (not acceptable)	Light blue	2,880	2,880	10,000

For all configurations shown in Figure 16 on page 22, simulation is at 166 MHz, with the DRAM drive strength set to full. Comparing the green, yellow, and red waveforms (original, ideal, and A configurations), this example shows how doubling both stubs and trunk lengths has a limited impact on the signal quality (the overshoot and delay increase of 150mV and 400ps, respectively). This behavior is probably due to the effect of 20Ω series termination resistors present on all signals on the Cartesio die.

On the other hand, increasing the trunk length to 10cm (4 times the light blue waveform) causes 1ns delay pushes the overshoot to 2.4V, which is an unacceptable overshoot (see arrows in Figure 16). For this reason, configuration A should be considered the worst acceptable case.

Under these conditions, full drive-strength ($Z_0 = 50\Omega$) is the preferred choice for Cartesio I/O buffers because the reduced drive-strength option ($48\Omega < Z_0 < 61\Omega$) causes an unacceptable reduction of the signal margins versus the thresholds for $V_{IH,MAX}[DC]$ and $V_{IL,MAX}[DC]$.

Figure 16: Routing Configuration Comparison



Notes: 1. Figure 16 compares the routing configurations of original, ideal, A, and B; condition of comparison is ADDR2 line, full drive, 166 MHz.

Table 2: Generic DQ Line: Simulated Routing Configurations

		Stub to DRAM #1	Stub to DRAM #2	Trunk to Cartesio
Layer		**Inner 4**	**Inner 8**	**Inner 3**
Configuration name	**Wave color**	**Length [µm]**	**Length [µm]**	**Length [µm]**
Original	Green	1,087	1,114	1,231
Ideal	Yellow	1,000	1,000	1,000
Configuration C (max acceptable)	Red	1,300	1,300	1,300
Configuration D (not acceptable)	Light blue	1,300	1,300	6,000

Figure 17 on page 23 and Figure 18 on page 24 show the results of 166 MHz simulations for the four configurations defined in Table 2, scoped on the Cartesio die, with the DRAM drive-strength set at full and three-quarter drive-strengths, respectively. These figures demonstrate that the differences among original, ideal, and C configurations have only a limited impact on the signal quality (green, yellow, and red waveforms).

Increasing the trunk length to 6cm (light blue waveform) generates 1ns of supplementary delay and causes an unacceptable overshoot of more than 2.5V (see arrows in Figure 17). For this reason, configuration D should be considered unacceptable.

A comparison of Figure 17 and Figure 19 on page 26 also demonstrates the impact of changing the DRAM drive-strength from full to three-quarter drive-strength. The three-quarter setting supports a 200mV decrease of the overshoot and also helps to reduce overshoot, ringing, and margins to the $V_{IH,MIN}$[DC] and $V_{IL,MAX}$[DC] thresholds (see arrows in Figure 18 on page 24). For this reason, the three-quarter drive-strength setting is the optimal choice for all simulated configurations (this is still to be confirmed by measurements on a real platform).

Figure 17: Routing Configuration Comparison of Original, Ideal, A, and B: DQ8, Full Drive-Strength, 166 MHz

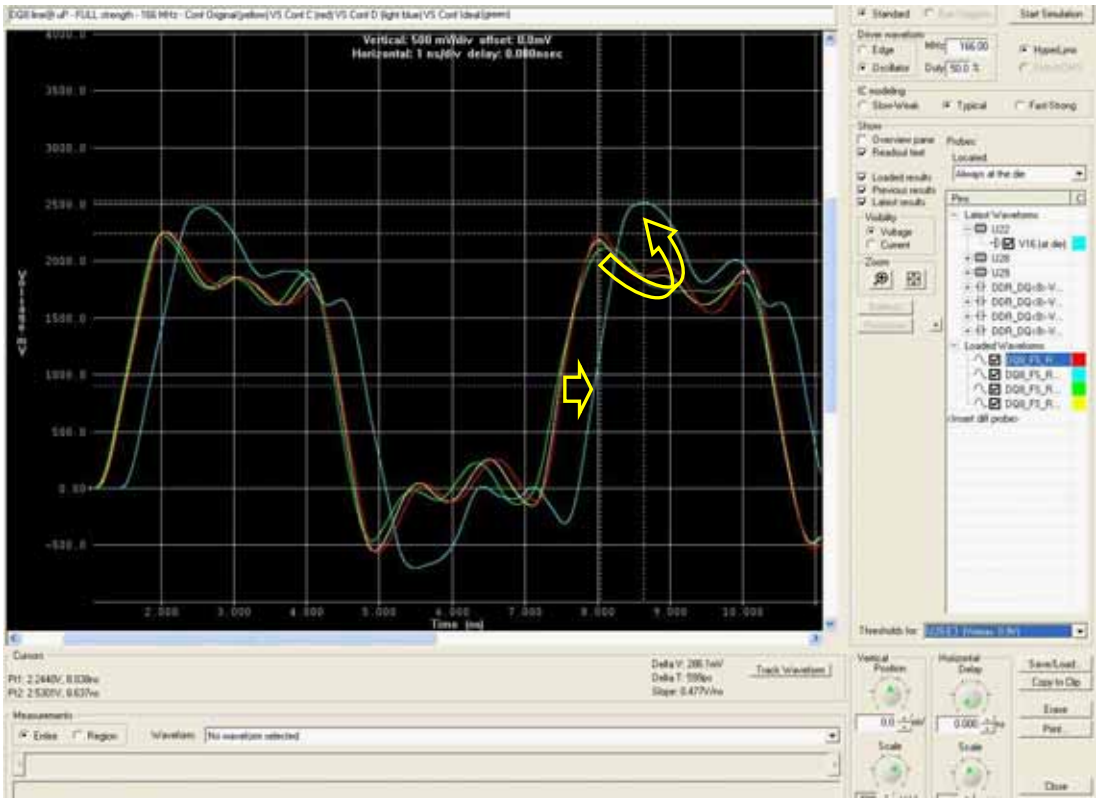
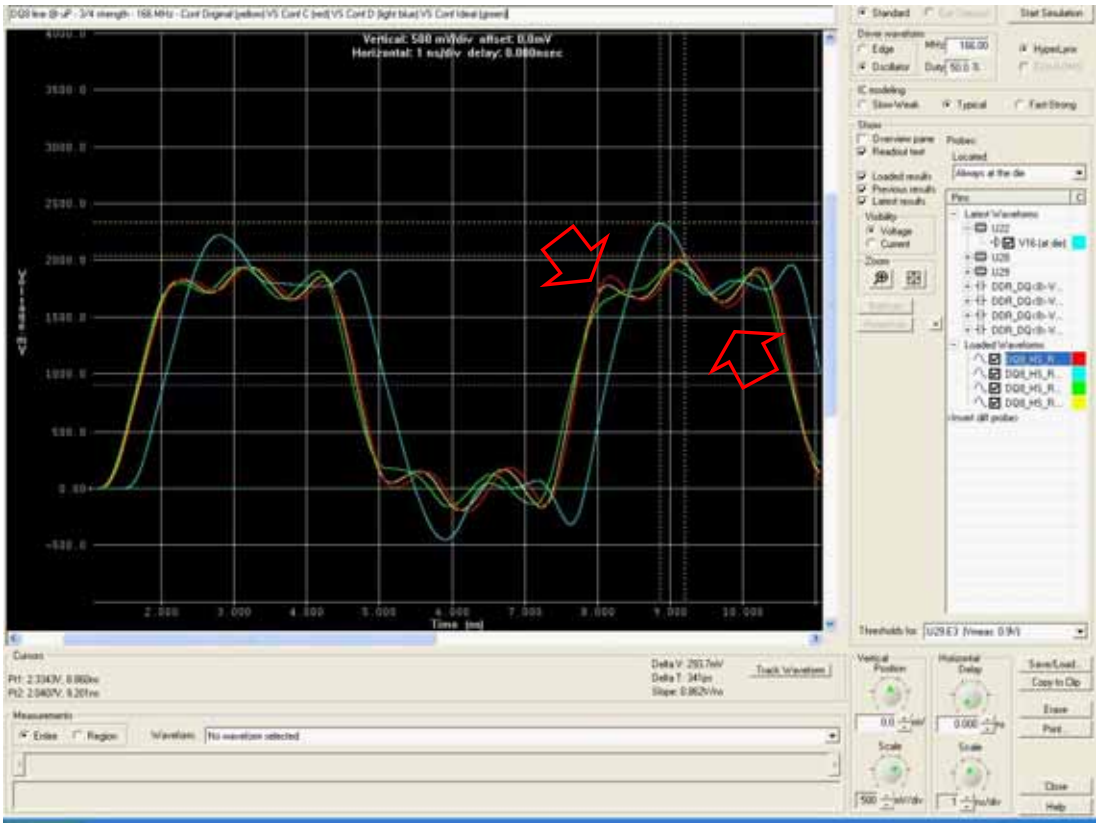


Figure 18: Routing Configuration Comparison for Original, Ideal, A, and B: DQ8, 3/4 Drive-Strength, 166 MHz



Decoupling

Adequate power decoupling on the PCB is necessary to prevent excessive VDD noise and memory errors in a situation where power supply draw can change by magnitudes in a single clock cycle. In the example configuration analyzed, up to 18 drivers (16 data and 2 strobes) could be switching from one state to another state. In a pipelined access, the controller could have an additional 19 signals transitioning at the same time. This large burst current generates noise in the supply voltages as charge is drained from decoupling capacitors. The burst current also causes supply voltages to drop momentarily until the system power supply or voltage regulators can begin recharging the decoupling capacitors.

When designing and setting the dimensions of the decoupling section of a power distribution system (PDS), the critical limiting factor is usually the amount of inductance in the capacitor leads and in the vias connecting the caps to the power and ground planes. It is not the total capacitance.

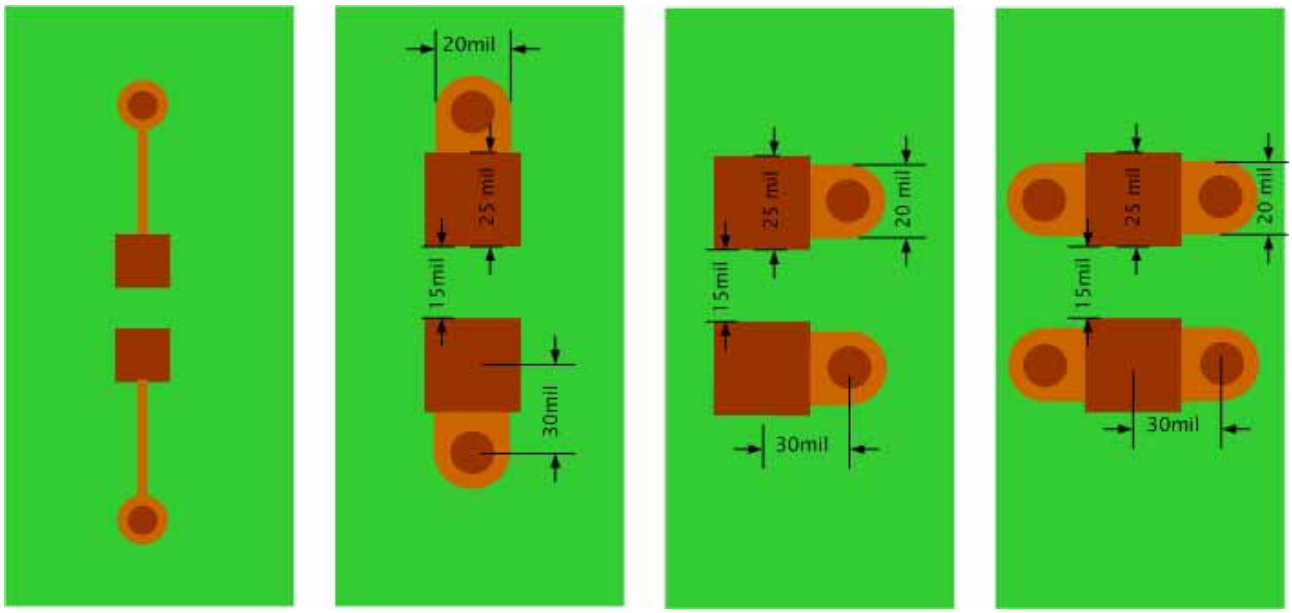
The parasitic inductance of current paths in the PCB originates from two distinct sources: the capacitor mounting and the power and ground planes of the PCB. The mounting comprises the capacitor's solder land on the PCB, the trace between the land and via, and the via itself. The inductance contribution of vias, traces, and pads in a capacitor mounting can be estimated at anywhere from 300pH to 4nH of inductance,

depending on the specific geometry. Minimizing the size of the loop through which the current passes is a key element in designing an effective decoupling system. This is because the parasitic inductance of the current path is proportional to the area of the loop. The loop comprises the path along one power plane, up through one via, through the connecting trace to the land, through the capacitor, through the other land and connecting trace, down through the other via, and along the other plane. The area of the loop can be broadly reduced by minimizing the length of both connecting traces and the via through which the current flows, thus reducing the amount of inductance.

The inductance contribution caused by the length of connecting traces should not be underestimated because it has a significant impact on the parasitic inductance of the mounting. Use of a connecting trace also plays a significant role in the parasitic inductance generated by the mounting. Use of long traces (as in configuration A shown in Figure 19 on page 26) should be avoided wherever possible. The via should be tangent to the land itself (see Figure 19, configuration B). Additionally, the connecting trace should be made as wide as possible. To further reduce parasitic inductance from the mounting, place vias alongside capacitor lands (see Figure 19, configuration C), or double the number of vias (Figure 19, configuration D).

A common practice in PCB layout is to share vias among multiple capacitors to squeeze more parts into a small area. This practice should be avoided. If a second capacitor is connected into the vias of an existing capacitor, it only improves PDS performance by a very small amount, given that the capacitor mounting typically contributes the same amount or more inductance than the parasitic inductance of the capacitor itself. A better option is to reduce the total number of capacitors and maintain a one-to-one ratio of lands to vias (see reference by Xilinx).

Figure 19: 0402 Decoupling Capacitor Layout: 4-Option Comparison



Configuration A
- 0402 land pattern
- End vias
- Long traces
- 4nH

Configuration B
- 0402 land pattern
- End vias
- Short/tick traces
- 0.8nH

Configuration C
- 0402 land pattern
- Side vias
- Short/tick traces
- 0.6nH

Configuration D
- 0402 land pattern
- Side vias
- Short/tick traces
- 0.4nH

Ultralow Inductance Capacitors

The use of multiple vias per land (shown in configuration D in Figure 19) is important when using ultralow inductance capacitors, such as reverse aspect ratio capacitors (AVX's LICC or Murata's LLL series).

Reducing inductance becomes a serious consideration in the effort to improve system performance, particularly when switching speeds increase and pulse rise times decrease. Even the decoupling capacitors that act as a local energy source can cause unacceptable voltage spikes: V = L (di/dt). When the di/dt ratio increases significantly, the size of the voltage spike can only be reduced by reducing L.

Both the length-to-width ratio and the mutual-inductance coupling between electrodes determine the total inductance of a chip capacitor. A 1210 chip size has a lower inductance than a 1206 chip. This design improvement is the basis of ultralow inductance capacitors, where the electrodes are terminated on the long side of the chip instead of on the short side. Terminating on the long side, the 1206 becomes a 0612, the 0805 becomes a 0508, and the 0603 becomes a 0306. This yields an inductance reduction from the 1nH range of normal chip capacitors to less than 0.2nH for low inductance capacitors (source: AVX).

The following design guidelines are strongly recommended:

- Use a low inductance capacitor, preferably in a 0306 package.

- Use enlarged vias (10 mils) both for power and for ground connections to ICs and passives.
- Shorten the traces connecting caps to vias to minimize the inductance of the PDS. Wherever possible, use no connecting trace.
- Do not share power and ground vias between capacitors and IC power and ground terminals; the generated current loops can alter the voltage levels of the power connections.
- Use side-terminating vias rather than end-terminating vias wherever possible.

It is important to note that any power and ground noise is additive to the switching noise caused by impedance mismatching.

The placement of V_{CC} and ground planes in the PCB stackup (layer order) has a significant impact on the parasitic inductance of power current paths. For this reason, high priority supplies should be placed in the top half of the stackup and low priority supplies in the bottom half. Power supplies with high transient current should have their associated V_{CC} planes close to the top surface (decoupled device side) of the PCB stackup to decrease the vertical distance currents travel through V_{CC} and ground vias before reaching the associated V_{CC} and ground planes.

Decoupling Capacitor Requirements Calculation

To estimate the number of decoupling capacitors required (per via) to reduce parasitic inductance, use the parameters provided in Table 1 on page 21.

Table 3: Calculation Parameters

Parameter	Value
DRAM V_{DDQ} = DRAM V_{DD}	1.8V
Via diameter	0.3mm
Via pad diameter	0.7mm
Printed circuit board thickness (via length)	1.506mm
Maximum voltage drop	0.18V (10%)

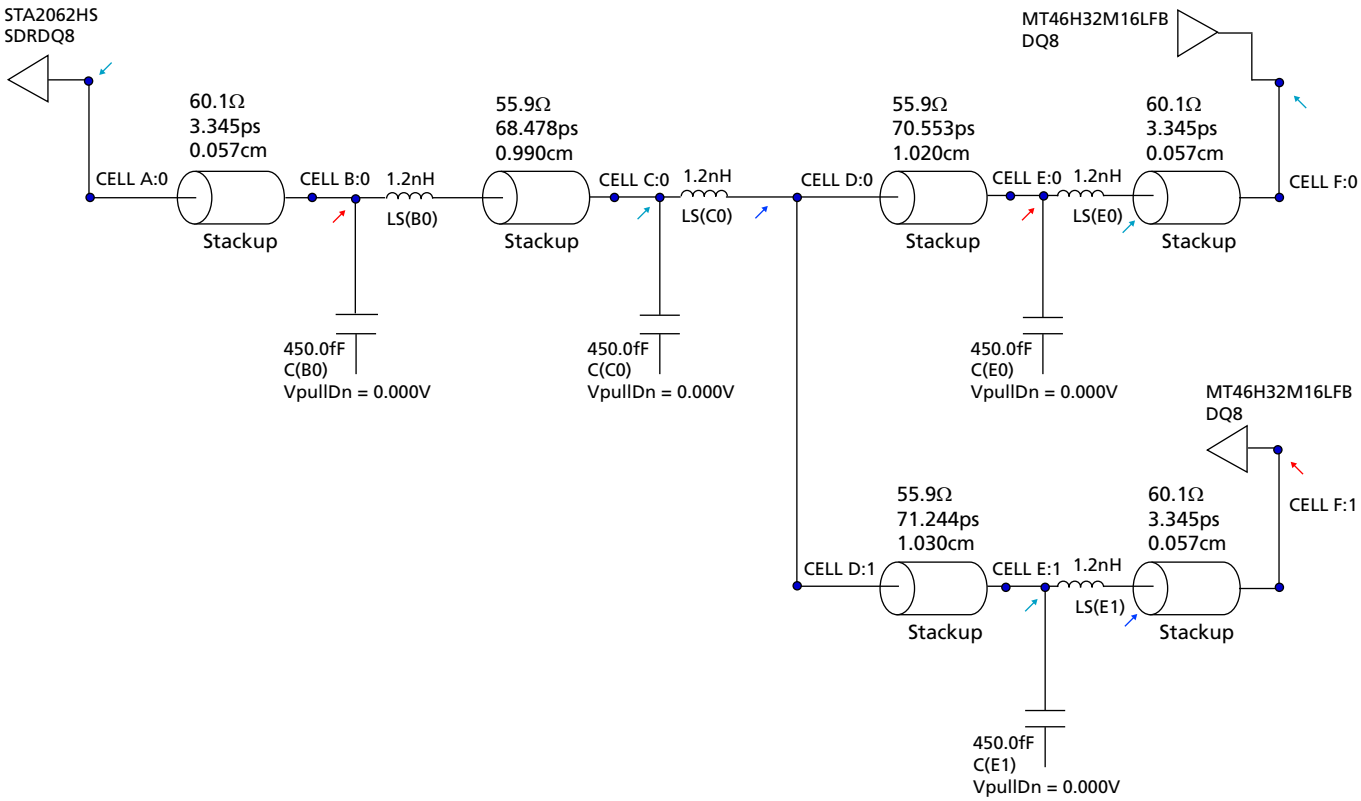
Notes: 1. See H. Johnson, M. Graham, *High-Speed Digital Design: A Handbook of Black Magic*.

Calculation results:

- C_{VIA} (parasitic capacitance of via) = 0.5pF
- L_{VIA} (inductance of via) = 1.2nH

To estimate the signal rise time using a typical net structure for a data line (in this case, DQ8), it is possible to build and import the transmission line model into the prelayout simulator. This model takes into account the inductance, resistance, and capacitance (RLC) parasitics for the DRAM and microprocessor packages (embedded in the IBIS models), the vias parasitic (as previously calculated and added as lumped elements), and the Z_0 and T_{PD} of all line sections (as evaluated by the simulator, considering layout, stackup, and length). The DQ8 transmission line model used is shown in Figure 20 on page 28.

Figure 20: DQ8 Transmission Line Model



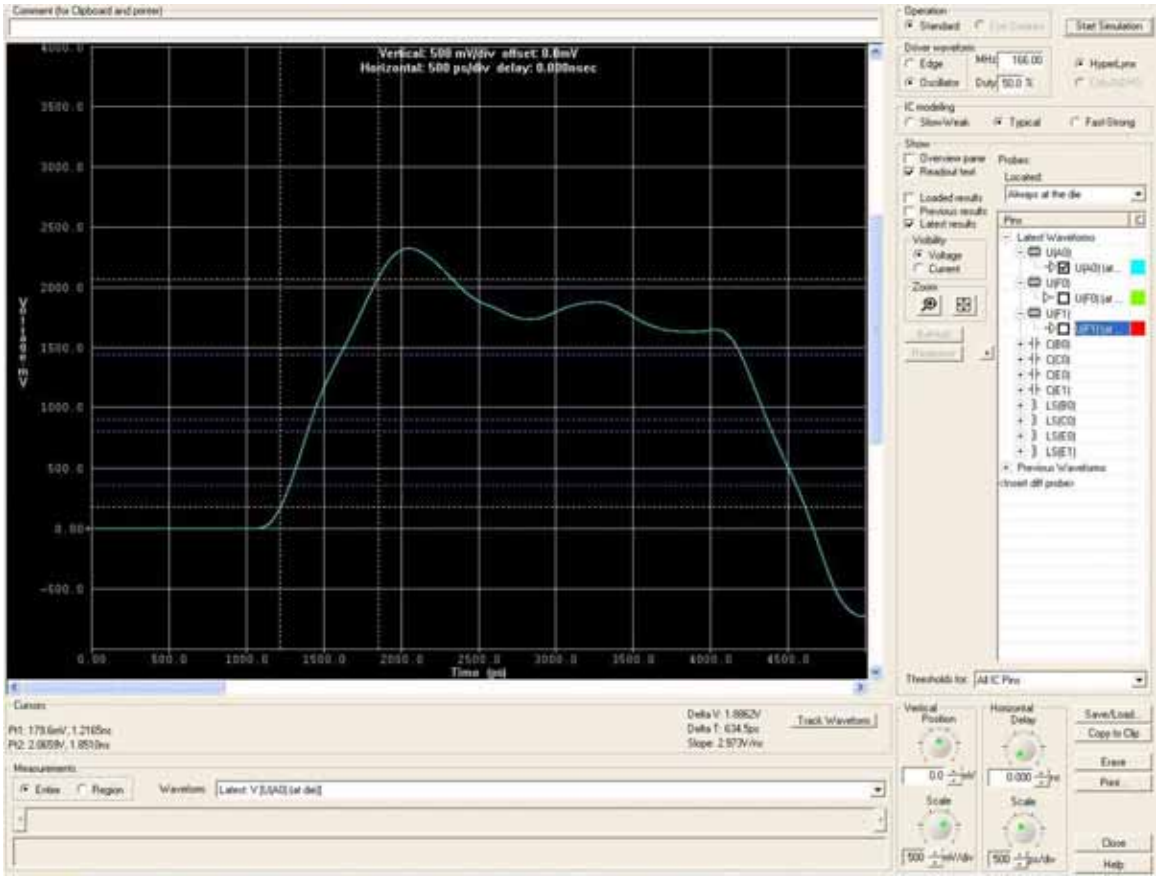
To estimate DQ8 rise time (10% to 90%), the Mentor Graphics Hyperlynx tool was used with the conditions noted in Table 2 on page 22.

Table 4: DQ8 Rise Time Calculation

Contributing Factor	Value
Three dogbones connecting IC pads to the closest vias	155fF
Three vias (as calculated)	1.5pF
Three line sections	4.2pF

With these settings, the DQ8 rise time is TRISE,10% to 90% = 600ps.

Figure 21: DQ8 TRISE,10% to 90% Estimation



Considering the DQ8 line, it is possible to determine the total capacitive load for a given signal line. Table 3 on page 27 defines the contributing factors. In this configuration, 18 DRAM I/Os switch simultaneously (16 DQ and 2 DQS signals).

Table 5: Capacitive Load Factors

Contributing Factor	Value
Three dogbones connecting IC pads to the closest vias	155fF
Three vias (as calculated)	1.5pF
Three line sections	4.2pF

It is possible to estimate ESL = 0.2nH for package and pads of 0306 very low inductance capacitors (AVX catalogue) and ESL = 0.7nH for package and pads of 0402 ceramic capacitors. In addition, for a symmetrical PCB stackup where the same via diameter is used for power and ground, using the length of a single via through the entire thickness of the board can be considered equal to the sum of the via lengths for power and ground. This is because the current flows through a via only to the depth of the plane to which it attaches. In the case of double-sided vias, there are two inductances in parallel; thus, the total ESL contribution for a single capacitor shrinks accordingly.

The total ESL (package + vias + pads) for a single decoupling capacitor with three different configurations can be estimated:

- 1st configuration (0402 single-sided vias) = 1.2nH + 0.7nH = 1.9nH
- 2nd configuration (0402 double-sided vias) = 0.6nH + 0.7nH = 1.3nH
- 3rd configuration (0306 double-sided vias) = 0.6nH + 0.2nH = 0.8nH

Finally, we get:

- 1st configuration needs 18 capacitors to keep the maximum voltage drop lower than 0.18mV.
- 2nd configuration needs 13 capacitors to keep the maximum voltage drop lower than 0.18mV.
- 3rd configuration needs 8 capacitors to keep maximum voltage drop lower than 0.18mV.

Note: See *High-Speed Digital Design: A Handbook of Black Magic*.

Conclusion

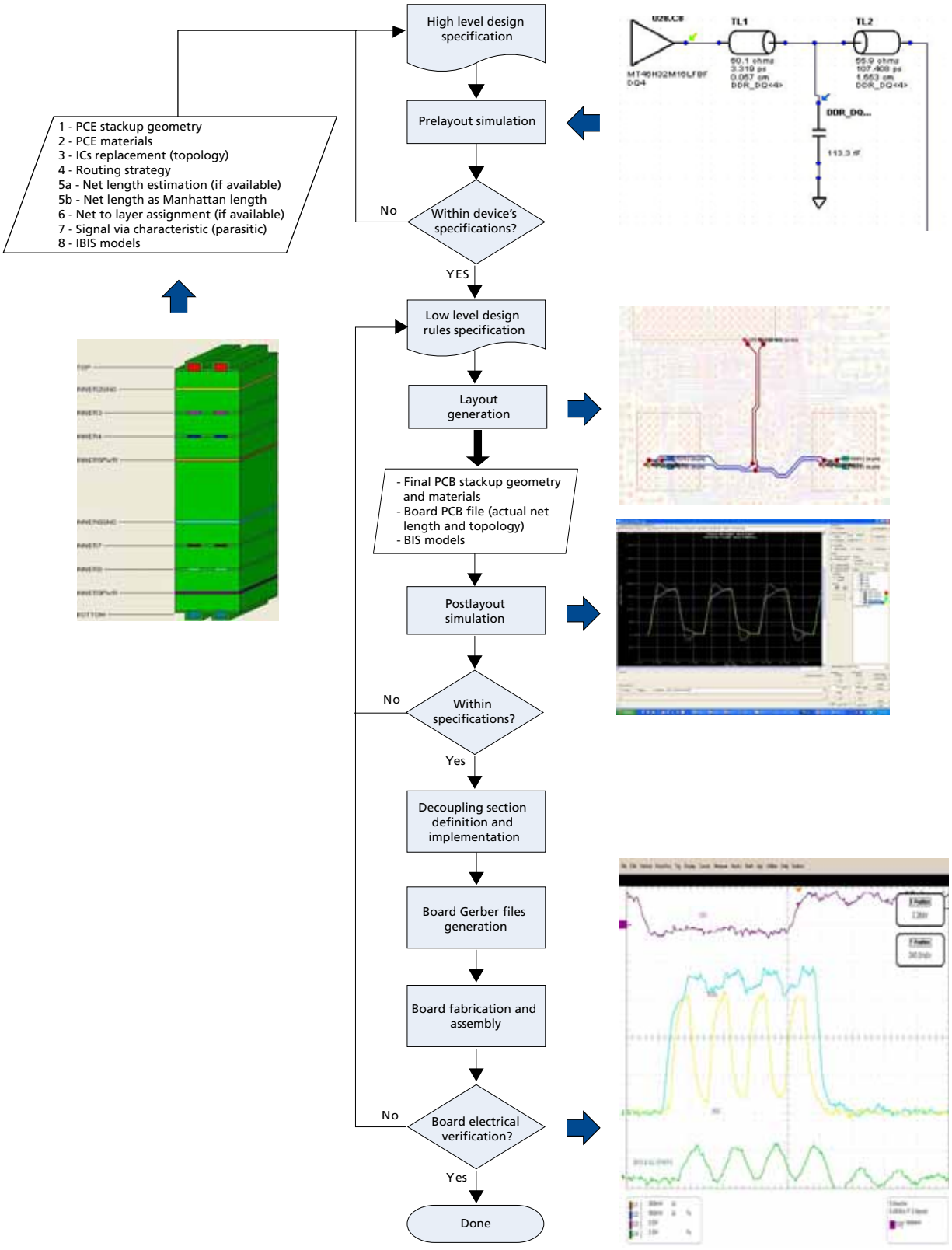
The Cartesio STA2062 microprocessor dynamic external bus interface can support up to 128MB of Mobile DDR SDRAM with 2 CS# at 166 MHz. Using the approach defined here, designers can build a system implementing the Cartesio STA2062 with dual 512Mb Micron Mobile DDR SDRAM devices, which improves signal and power integrity and reduces noise on the DRAM bus, without the use of series termination resistors. This methodology has been shown to be effective in implementing high performance, noise-free memory subsystems, minimizing overall system cost and production yield loss.

Appendix 1: Suggested Board Development Flow

Figure 22 on page 32 shows the suggested flow for digital, high-speed boards. The essential steps include the following:

- Prelayout simulation: Preliminary check performed using transmission line and IBIS models and estimated board/lines parameters
- Postlayout simulation: Final check of the actual board layout, with possible interactions/back annotations with the board layout activity
- Electrical characterization: Use of scope and ad-hoc test suites with the board at ambient temperature to evaluate and to verify signal and power integrity and to correlate simulation results with the actual measurements. Consider checking the functionality of the microprocessor and memory devices over the entire specified temperature range (for example, –40°C to +105°C for AT devices).

Figure 22: Board Development Flowchart



Appendix 2: Cartesio Optimized SDRAM Controller Settings

Table 6: Mobile DDR SDRAM Timing Settings: Device MT46H32M16LF

Parameter	Requirement (Min Value)	Register	Value for 169 MHz T = 5.92ns	Value for 162.5 MHz T = 6.15ns	Calculated Parameter for 169 MHz	Calculated Parameter for 162.5 MHz
^{t}RP	18ns	SDMC_DYRP	0x0000_0003	0x0000_0002	23.67ns	18.46ns
^{t}RFC	70ns	SDMC_DYRFC	0x0000_000B	0x0000_000B	71ns	73.85ns
^{t}MRD	2 tCK	SDMC_DYMRD	0x0000_0001	0x0000_0001	2 tCK	2 tCK
^{t}RAS	42ns	SDMC_DYRAS	0x0000_0007	0x0000_0006	47.34ns	43.08ns
^{t}SREX	120ns	SDMC_DYSREX	0x0000_0014	0x0000_0013	124.26ns	123.08ns
^{t}WR	12ns	SDMC_DYWR	0x0000_0002	0x0000_0001	17.75ns	12.31
^{t}RC	60ns	SDMC_DYRC	0x0000_000A	0x0000_0009	65.09ns	61.54ns
^{t}XSR	120ns	SDMC_DYXSR	0x0000_0014	0x0000_0013	124.26ns	123.08ns
^{t}RRD	12ns	SDMC_DYRRD	0x0000_0002	0x0000_0001	17.75ns	12.31
^{t}WTR	1 tCK	SDMC_DYCDLR	0x0000_0000	0x0000_0000	1 tCK	1 tCK
^{t}RCD	18ns	SDMC_DYRASCASx[1]	0x0000_0304	0x0000_0303	23.67ns	18.46ns

Notes: 1. For SDMC_DYRASCASx, where x = 0, 1 for bank 0 and bank 1.

References

Table 7: References

STMicroelectronics STA2062, CARTESIO data sheet
Micron MT46H32M16LF, 512 Mb Mobile DDR SDRAM data sheet
Micron TN-46-02, “Decoupling Capacitor Calculation for a DDR Memory Channel”
Micron TN-46-11, “DDR SDRAM Point-to-Point Simulation Process”
Micron TN-46-14, “Hardware Tips for Point-to-Point System Design: Termination, Layout, and Routing”
Micron MT46H32M16LFBF-x:B, IBIS Model
STMicroelectronics STA2062, Cartesio IBIS Model
ARM® PrimeCell™ Multiport Memory Controller, “GX175 Technical Reference Manual”
AVX Corp., *Parasitic Inductance of Multilayer Ceramic Capacitor*, J. Cain
AVX Corp., “Low-Inductance Capacitors”
H. Johnson, M. Graham, *High-Speed Digital Design: A Handbook of Black Magic*, Englewood Cliffs, NJ: Prentice Hall
Xilinx XAPP623, “Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors”
Mentor Graphics Corp., Hyperlynx LineSim/BoardSim simulation tool

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992