Migrating to an AT91SAM9G20-based System from an AT91SAM9260-based System

1. Scope

This application note specifies the migration from the AT91SAM9260 to the AT91SAM9G20 microcontroller and describes the differences between them. These variances lie in the Features, Package, Power Supplies, Clock Characteristics, Bus Matrix and Errata. In this document all shaded cells concern AT91SAM9G20.

2. Features

The following list shows the features of the AT91SAM9G20 that differ from the AT91SAM9260.

- **ARM926EJ-S™ ARM® Thumb® Processor with:**
  - **32-KByte Data Cache, 32-KByte Instruction Cache**
  - **CPU Frequency 400 MHz**
- **Additional Embedded Memories**
  - **One 64-KByte internal ROM, Single-cycle Access at Maximum Matrix Speed**
  - **Two 16-KByte internal SRAM, Single-cycle Access at Maximum Matrix Speed**
- **ROM Boot from DataFlash®, NAND Flash, Serial Flash, SD Memory Card and EEPROM**
- **Ethernet MAC**
  - **The RX FIFO and TX FIFO Sizes are Increased to 32 Words**
- **Hardware ECC Controller Enhancement**
- **PDC Channel on TWI controller**
- **Selectable Drive to Control the I/Os Slew Rate on EBI Signals**
- **PIO Controllers**
  - **All the I/O Lines are Schmitt Trigger Inputs.**
- **Required Power Supplies**
  - **0.9V to 1.1V for VDDBU, VDDCORE, VDDPLL**
  - **1.65 to 3.6V for VDDOSC**
  - **1.65V to 3.6V for VDDIOP (Peripheral I/Os)**
  - **3.0V to 3.6V for VDDUSB**
  - **3.0V to 3.6V VDDANA (Analog-to-digital Converter)**

Other than those mentioned here, the features for the two microprocessors are the same.

3. Package

The AT91SAM9G20 is available in a 217-ball LFBGA package 15 x 15 mm (0.8 mm ball pitch). The AT91SAM9G20 and the AT91SAM9260 are pin-to-pin compatible, only power supply pins differ.

AT91 ARM Thumb Microcontrollers

Application Note

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4. Power Supplies

4.1 Power Supply Range

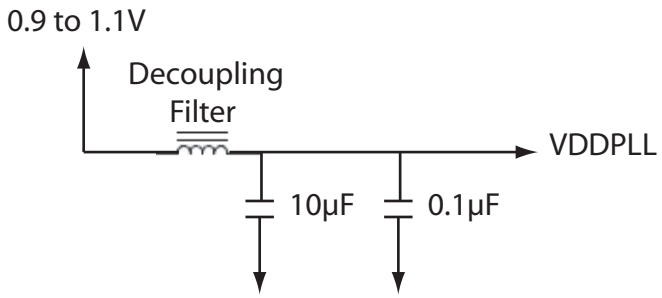
All the power supplies differ except VDDIOM and VDDANA.

Table 4-1. Power Supplies

Power supply domain	AT91SAM9260		AT91SAM9G20	
	Range (V)	What is powered	Range (V)	What is powered
VDDCORE	1.65 - 1.95	Core	0.9 - 1.1	Core
VDDBU	1.65 - 1.95	Backup	0.9 - 1.1	Backup
VDDPLL[1]	1.65 - 1.95	PLL and Oscillator	0.9 - 1.1	PLL
VDDOSC[3]	N/A	N/A	1.65 - 3.6	Oscillator
VDDANA	3.0 - 3.6	Analog	3.0 - 3.6	Analog
VDDIOP0	3.0 - 3.6	Peripherals and USB transceivers	N/A	N/A
VDDIOP1	1.65 - 3.6		N/A	N/A
VDDIOP	-	-	1.65 - 3.6	All peripherals
VDDUSB[3]	-	-	3.0 - 3.6	USB transceivers
VDDIOM	1.65 - 1.95 or 3.0 - 3.6	Memories	1.65 - 1.95 or 3.0 - 3.6	Memories

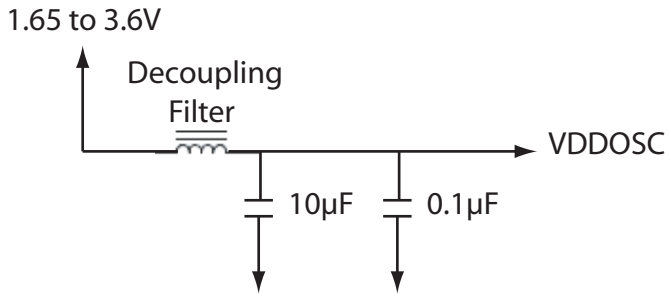
Notes: 1. The VDDPLL power supply pin draws small current, but it is noise sensitive. Care must be taken in VDDPLL power supply routing, decoupling and also on bypass capacitors. The supply ripple is to be limited to 10mV for AT91SAM9G20.

Figure 4-1. VDDPL Power Supply



2. The ball (L4) used for VDDOSC on the AT91SAM9G20 is a VDDIOP0 on AT91SAM9260. The VDDOSC power supply pin draws small current, but it is noise sensitive. Care must be taken in VDDOSC power supply routing, decoupling and also on bypass capacitors.

Figure 4-2. VDDOSC Power Supply



3. On the AT91SAM9260, the USB transceiver is powered by VDDIOP0. VDDUSB is only available on AT91SAM9G20 because VDDIOP could be 1.8V.

4.2 Power Supply Constraints at Startup

The AT91SAM9G20 board design must comply with the power-up and power-down sequence guidelines below to guarantee reliable operation of the device. Any deviation from these sequences may lead to the following situations:

- Excessive current consumption during the power-up phase which, in worse case, can result in irreversible damage to the device.
- Prevent the device from booting.

4.2.1 Power-up Sequence

Table 4-2. Power-on-Reset Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Units
V_{th+}	Threshold Voltage Rising		0.5	0.70	0.89	V
V_{th-}	Threshold Voltage Falling		0.4	0.60	0.85	V
T_{RES}	Reset Time		30	70	130	µs

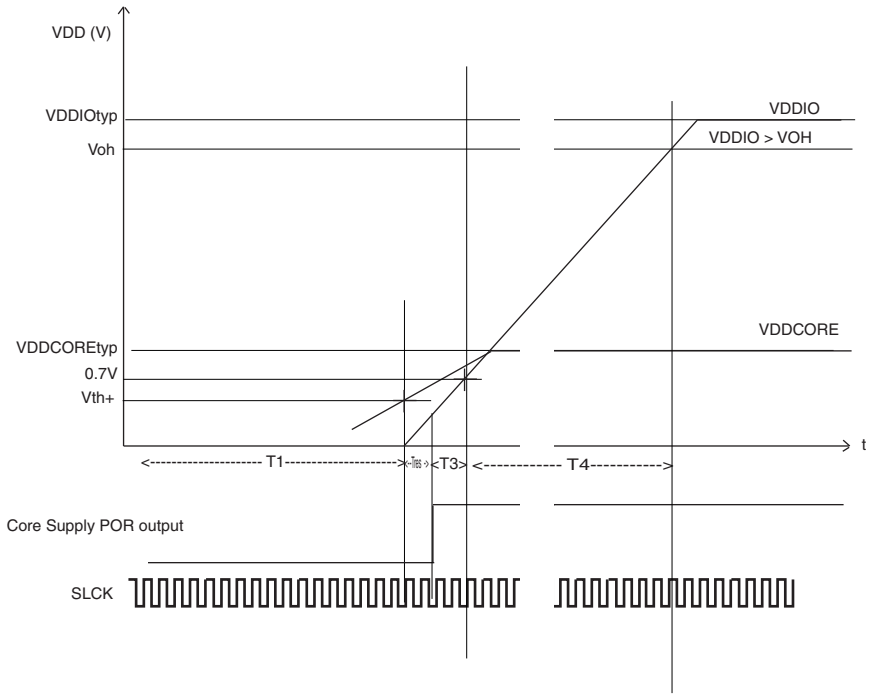
VDDCORE and VDDBU are controlled by internal POR (Power-on-Reset) to guarantee that these power sources reach their target values prior to the release of POR.

- VDDIOM and VDDIOP must NOT be powered until VDDCORE has reached a level superior to V_{th+}.
- VDDIOM and VDDIOP must be >= to 0.7V within (T_{RES}+ T3) after VDDCORE has reached V_{th+}.
- VDDIOM and VDDIOP must reach V_{OH} (2.6V) within (T_{RES} + T3 + T4) after VDDCORE has reached V_{th+}
  - T_{RES} is a POR characteristic
  - T3 = 3 x T_{SLCK}
  - T4 = 16 x T_{SLCK}

The T_{SLCK} min (22 µs) is obtained for the maximum frequency of the internal RC oscillator (44 kHz).

– T_{RES} = 30 µs
– T3 = 66 µs
– T4 = 352 µs

Figure 4-3. $V_{VDDCORE}$ and V_{VDDIO} Constraints at Power-up



4.2.2 Power-Down Sequence

Switch-off the VDDIOM and VDDIOP power supply prior to or at the same time as VDDCORE.

No power-up or power-down restrictions apply to VDDBU, VDDPLL, VDDANA and VDDUSB.

5. Clock Characteristics

5.1 On Chip RC Oscillator

Table 5-1. RC characteristics

RC Characteristics	AT91SAM9260	AT91SAM9G20
Startup time	240 µs	150 µs

5.2 Boot ROM Crystal Frequency Support

5.2.1 With Internal RC Oscillator

The following crystal descriptions only give acceptable USB clock frequency accuracy for the Boot ROM on the AT91SAM9G20.

Table 5-2. Reduced Crystal Table (MHz) OSCSEL = 0

	3.0	8.0	18.432	Other
Boot on DBGU	Yes	Yes	Yes	Yes
Boot on USB	Yes	Yes	Yes	No

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Table 5-3. Reduced Crystal Table (MHz) OSCSEL = 0 and Main Oscillator is Bypassed

	3.0	8.0	20.0	50.0	Other
Boot on DBGU	Yes	Yes	Yes	Yes	Yes
Boot on USB	Yes	Yes	Yes	Yes	No

5.2.2 With External 32768 Hz Crystal

The following crystal descriptions only give acceptable USB clock frequency accuracy for Boot ROM on the AT91SAM9G20.

Table 5-4. Large Crystal Table (MHz) OSCSEL = 1

3.0	3.6864	3.84	4.0	4.9152
5.24288	6.0	6.144	6.4	6.5536
7.3728	8.0	9.8304	10.0	11.05920
12.0	12.288	14.31818	14.7456	16.0
16.367667	17.734470	18.432	20.0	

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Table 5-5. Large Crystal Table (MHz) OSCSEL = 1 and Main Oscillator is Bypassed

3.0	3.6864	3.84	4.0	4.9152
5.24288	6.0	6.144	6.4	6.5536
7.3728	8.0	9.8304	10.0	11.05920

Table 5-5. Large Crystal Table (MHz) OSCSEL = 1 and Main Oscillator is Bypassed

12.0	12.288	14.31818	14.7456	16.0
16.367667	17.734470	18.432	20.0	24.0
24.576	25.0	28.224	32.0	33.0
40.0	48.0	50.0	.	

5.3 PLLA

Table 5-6. PLLA Characteristics

PLLA Characteristics	AT91SAM9260	AT91SAM9G20
Range	80 - 240 MHz	400 - 800 MHz
MULA	1 - 1047	1 - 254
DIVA	1 - 255	1 - 255
Entry frequency	1 - 32 MHz	2 - 32 MHz
Embedded PLL Filter	No	Yes

The PLLRCA pin on the AT91SAM9260 is replaced by an NC (not connected) pin on the AT91SAM9G20. The filter for the PLLA is embedded in this new device. Do not connect this pin.

Table 5-7. AT91SAM9260 PLLA Frequency Regarding ICPPLLA and OUTA

PLL frequency range (MHz)	ICPPLLA	OUTA	
190 - 240	1	1	0
80 - 200	1	0	0

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Table 5-8. AT91SAM9G20 PLLA Frequency Regarding ICPPLLA and OUTA

PLL frequency range (MHz)	ICPPLLA	OUTA	
745 - 800	0	0	0
695 - 750	0	0	1
645 - 700	0	1	0
595 - 650	0	1	1
545 - 600	1	0	0
495 - 550	1	0	1
445 - 500	1	1	0
400 - 450	1	1	1

5.4 PLLB

Table 5-9. PLLB Characteristics

PLLB Characteristics	AT91SAM9260	AT91SAM9G20
Range	70 - 130 MHz	30 - 100 MHz
MULB	1 - 1047	1 - 62
DIVB	1 - 255	1 - 255
OUTB	01	00
Entry frequency	1 - 5 MHz	2 - 32 MHz
Embedded PLL Filter	Yes	Yes

5.5 Processor/Master Clock

A new field (PDIV) has been added to program the processor speed.

Table 5-10. Processor/Master Clock

Characteristics	AT91SAM9260	AT91SAM9G20
Processor Max frequency	180 MHz	400 MHz
Bus Max frequency	90 MHz	133 MHz
Master clock divider MDIV	1, 2, 4	1, 2, 4, 6
Processor clock div. PDIV	N/A	1, 2
Current consumption on VDDCORE in Active Mode	130 mA @ 180 / 90 MHz	50 mA @ 400 / 133 MHz

5.6 SDRAM Clock

Table 5-11. SDRAM clocks

Characteristics	AT91SAM9260	AT91SAM9G20
SDCK Max frequency @ 1.8V (load = 30pF)	100 MHz	133 MHz
SDCK Max frequency @ 3.3V (load = 50pF)	100 MHz	133 MHz

The rising and falling times of the EBI signals can be adapted using the “selectable drive function” located in the EBI_CSA register.

6. Bus Matrix Masters

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Table 6-1. List of Bus Matrix Masters

Master	AT91SAM9260	AT91SAM9G20
Master 0	ARM926™ Instruction	ARM926™ Instruction
Master 1	ARM926 Data	ARM926 Data
Master 2	PDC	PDC
Master 3	USB Host DMA	ISI Controller
Master 4	ISI Controller	Ethernet MAC
Master 5	Ethernet MAC	USB Host DMA

7. ECC Controller

Table 7-1. ECC Controller Connections

Device	ECC Connection
AT91SAM9260	1 ECC per page
AT91SAM9G20	1 ECC per page 1 ECC per 256 bytes of data 1 ECC per 512 bytes of data

8. I/O Considerations

Adaptation serial resistors of 27 or 33 ohms are needed on each data line and address line to limit the following:

- Current flowing (in order to prevent simultaneous switching noise).
- Falling and rising slope (reflection problems and spectral spreading).
- Trace ringing according to the intrinsic trace characteristics.

9. Errata

The following list gives the AT91SAM9260 errata and its status, corrected or not, in the AT91SAM9G20. For a detailed description of the errata, please refer to the errata section in the AT91SAM9260 datasheet.

Errata Section	Errata Description	Status
Analog-to-digital Converter (ADC)	All errata are fixed except Sleep Mode:	Fixed
	Sleep Mode	Not Fixed
Boot ROM	NAND Flash Boot does not work correctly	Fixed
	Problem with RTT	Fixed
EMAC	TX underrun may occur in some cases	Fixed
MCI	Busy signal of R1b responses is not taken in account	Not Fixed
	SDIO interrupt does not work for slot different from A	Not Fixed
	Data Timeout Error Flag	Not Fixed
	Data Write Operation and number of bytes	Not Fixed
	Flag Reset is not correct in half duplex mode	Not Fixed
Oscillators	On-chip RC startup time	Fixed
	Bad sampling of OSCSEL	Fixed
SDRAM Controller	All SDRAMC Errata	Fixed
Serial Peripheral Interface (SPI)	Bad Serial Clock Generation on second chip_select when SCBR = 1, CPOL = 1 and NCPHA = 0	Not Fixed
	Baudrate set to 1	Not Fixed
Serial Synchronous Controller (SSC)	Unexpected RK clock cycle when RK outputs a clock during data transfer	Not Fixed
	Incorrect first RK clock cycle when RK outputs a clock during data transfer	Not Fixed
	Transmitter Limitations in Slave Mode	Not Fixed
	Periodic Transmission Limitations in Master Mode	Not Fixed
Static Memory Controller (SMC)	High Drive Strength	Fixed
System Controller	Possible event loss when reading RTT_SR	Not Fixed
Two-wire Interface (TWI)	Switch from slave to master mode	Fixed
	RXRDY Flag is not reset when a Software reset is performed	Not Fixed

Errata Section	Errata Description	Status
USB Host Port (UHP)	Non-ISO IN transfers	Not Fixed
	ISO OUT transfers	Not Fixed
	Remote Wakeup event	Not Fixed
Universal Synchronous Asynchronous Receiver Transmitter (USART)	TXD signal is floating in Modem and Hardware Handshaking mode	Not Fixed
	DCD is Active High instead of Low	Not Fixed
	RXBRK flag error in Asynchronous Mode	Fixed
	CTS signal in Hardware Handshake	Fixed
	RTS not expected behavior	Fixed
	Two characters sent if CTS rises during emission	Fixed

Revision History

Doc. Rev	Comments	Change Request Ref.
6415A	First issue	
6415B	Section 4.1 “Power Supply Range”, updated with VDDPLL constraints. See Table 4-1 and Figure 4-1	5790

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com
www.atmel.com/AT91SAM

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