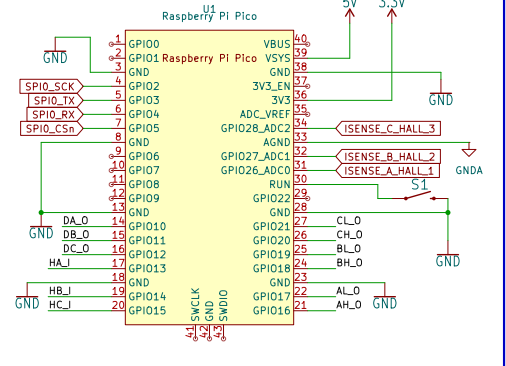
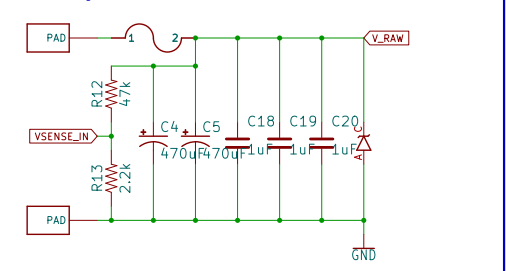


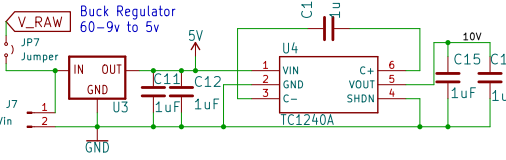
Microcontroller



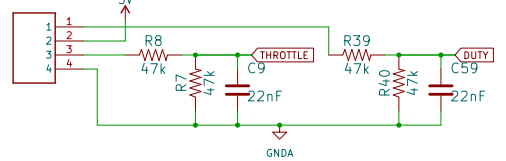
Power Stage



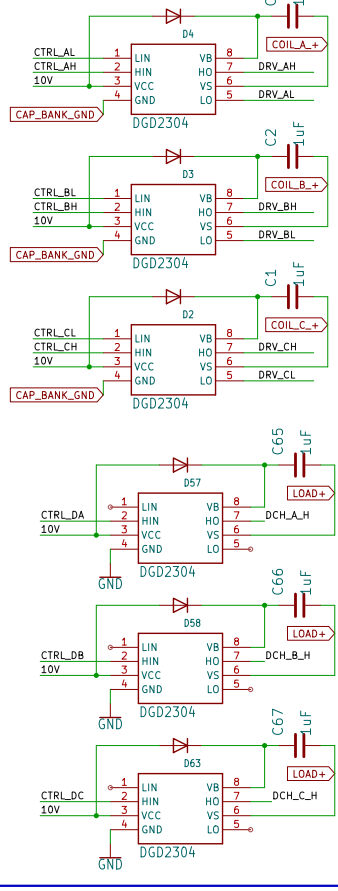
Voltage Regulators



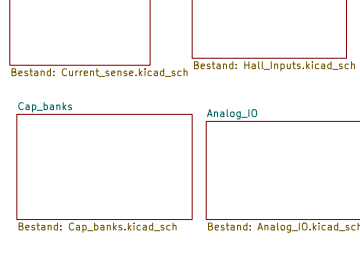
Throttle/Freq and Duty



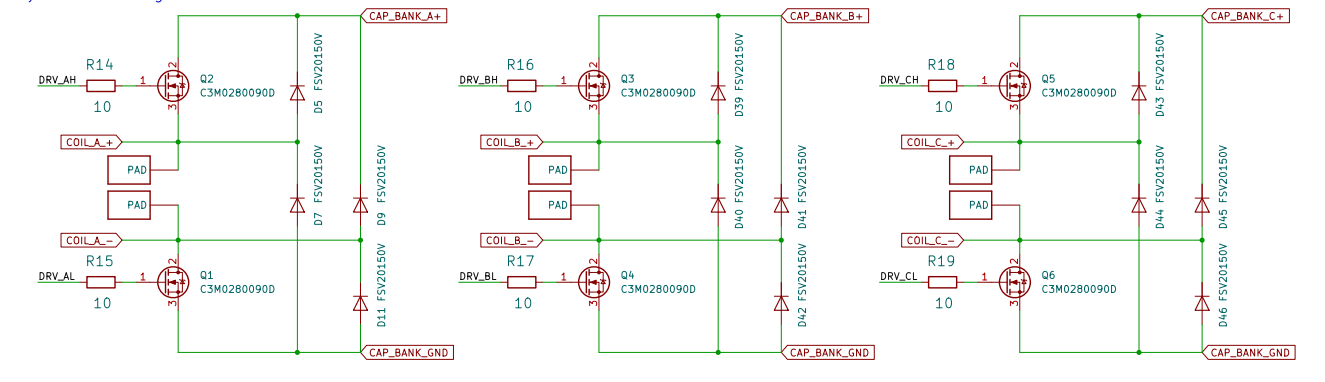
Gate Drivers



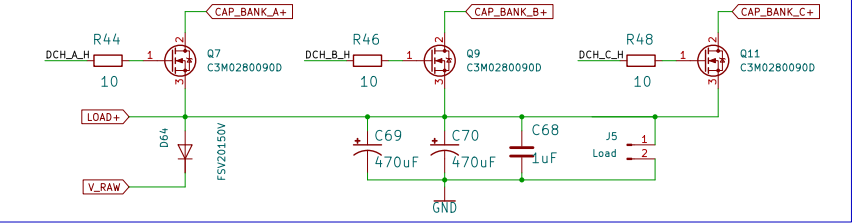
Current_sense



Asymmetric Bridge

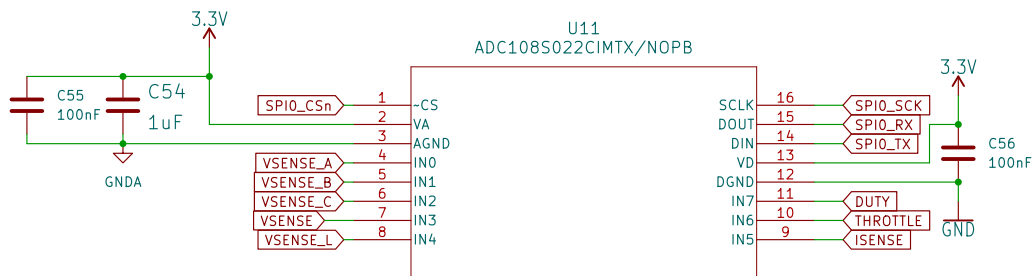
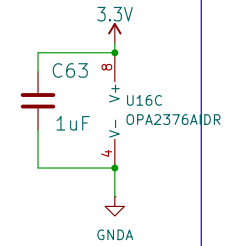
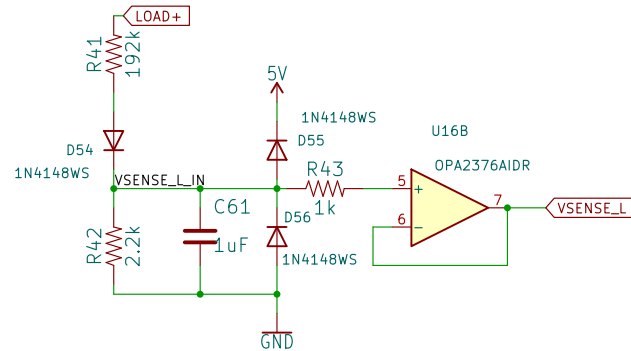
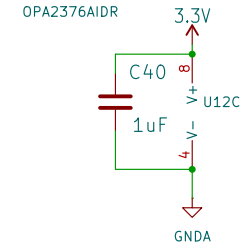
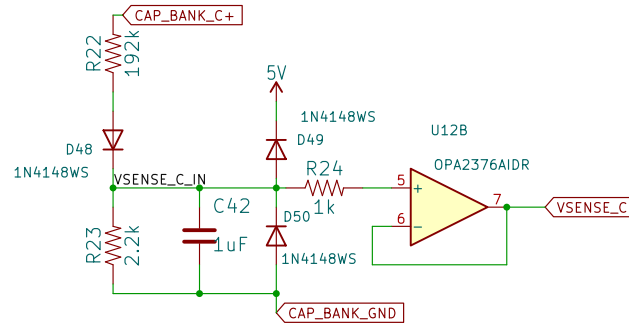
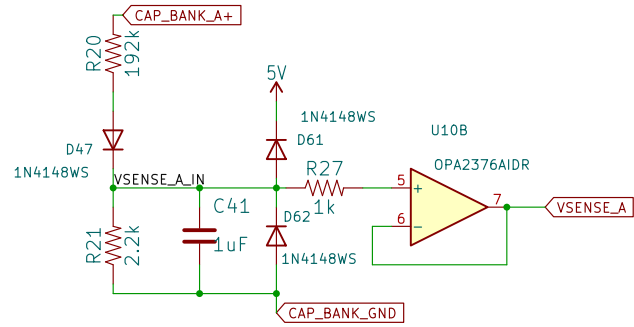
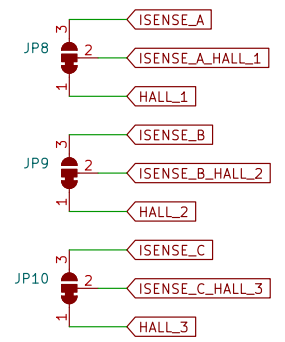
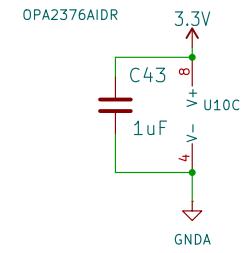
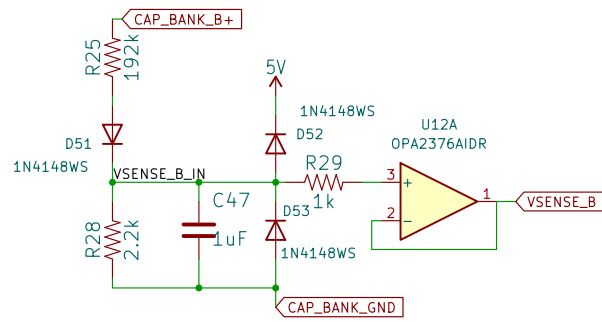
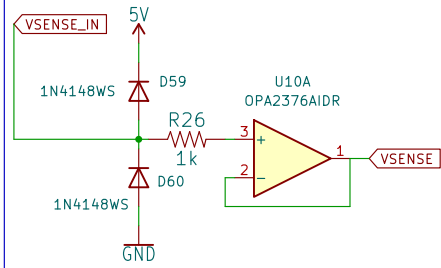


Discharge to load

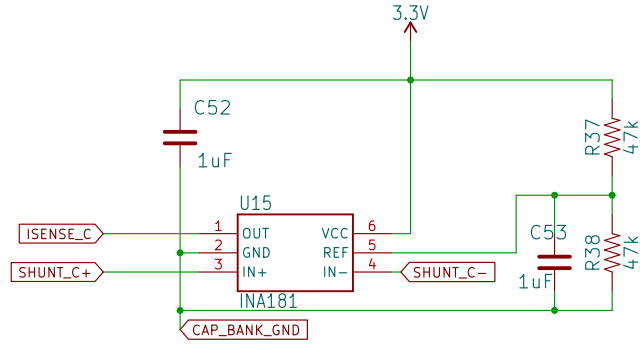
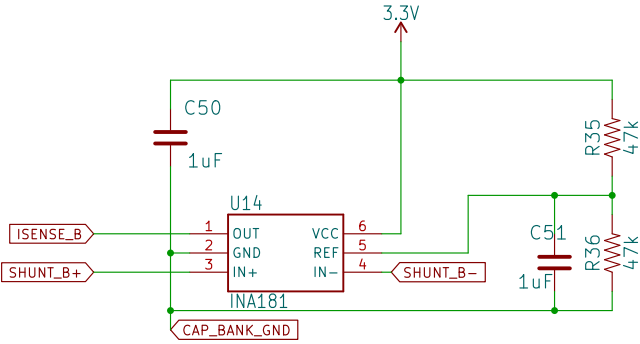
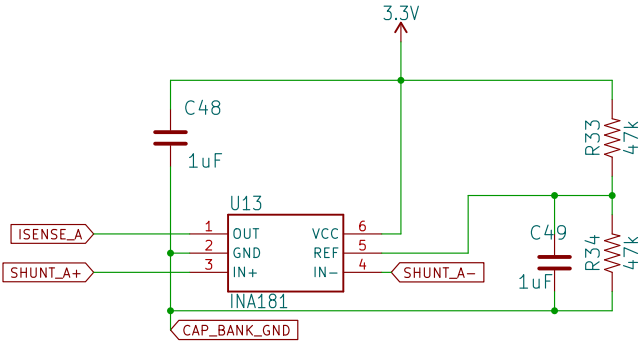
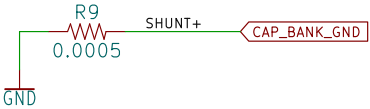
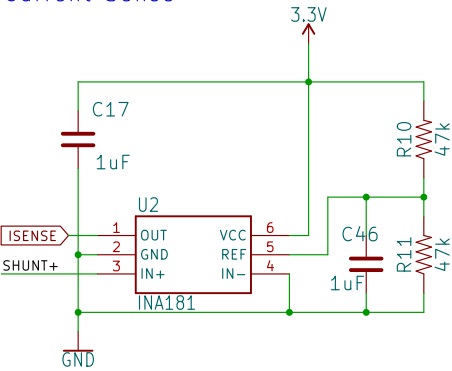


The image displays three circuit diagrams for SHUNT_A+, SHUNT_B+, and SHUNT_C+ channels. Each circuit is powered by V_RAW and includes a diode bridge (D6, D8, D10, D12 for SHUNT_A+; D19, D20, D21, D22 for SHUNT_B+; D29, D30, D31, D32 for SHUNT_C+). The bridge is connected to a network of capacitors (C10, C23, C6, C13, C7, C21, C8, C22 for SHUNT_A+; C27, C30, C24, C31, C25, C28, C26, C29 for SHUNT_B+; C35, C38, C32, C39, C33, C36, C34, C37 for SHUNT_C+) and jumpers (JP1, JP2, JP3, JP4 for SHUNT_A+; JP3, JP4 for SHUNT_B+; JP5, JP6 for SHUNT_C+). The output is connected to SHUNT_A+, SHUNT_B+, and SHUNT_C+ terminals, which are also connected to CAP_BANK_GND. A 0.0005 resistor (R30, R31, R32) is connected to the output terminals.

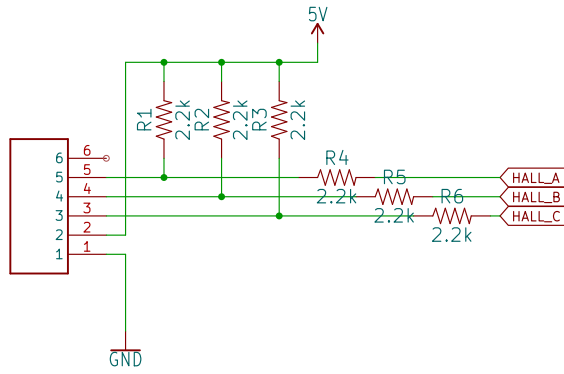
Analog buffers



Current Sense



Digital Hall Inputs for BLDC



Analog Hall Inputs for MEG

