Processing signals received from sensors

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Structure of Computer Systems Project

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# **Introduction**

## Context

This project focuses on processing the signals coming from sensors in real time. This data must be collected and displayed as a histogram.

## Objectives

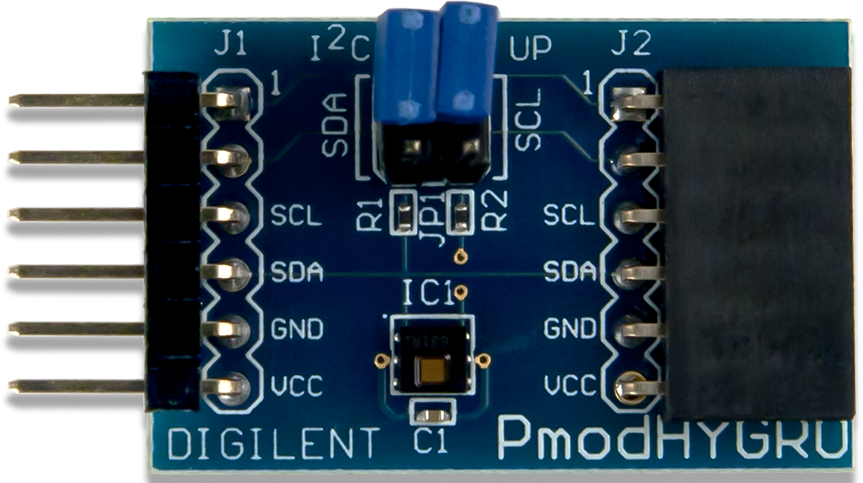
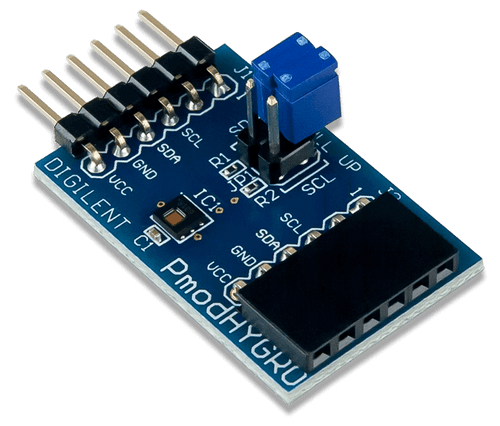
As far as technical stuff goes, a project consisting of a Basys3 FPGA board, a pmod HYGRO and a pmod ESP32 will be assembled. The required software (written in VHDL or other programming languages) will be provided, as well as the results to some test cases that prove the correct functionality of the whole design.

# **Bibliographic Research**

## PMOD HYGRO

Pmod Hygro is a module manufactured by Digilent equipped with the TI HDC1080, a humidity and temperature sensor produced by Texas Instruments.

Figure . PMOD HYGRO



The module offers up to 14 bits of resolution, good stability at high humidity and a great sensitivity – the error is bounded to ±2%, for humidity, and ±0.2ºC, for temperature. An internal resistive heating element is provided to ensure the condensation that may appear when it is used in high humidity environments is driven off. The J2 header passes through all the information in the J1 header to allow daisy chaining.

The Pmod can pe attached to the Basys3 board via the 6-pin connector. The voltage required is between 2.7 and 5.5, providing a 10-400 KHz clock frequency.

### The I²C interface (protocol)[[1]](#footnote-1)

The *Inter-Integrated Circuit* is a synchronous, multi-controller/multi-target, single-ended communication bus, widely used for attaching lower-speed peripheral integrated circuits to processors and microcontrollers in short-distance, intra-board communication.

I²C uses 2 bidirectional, pulled-up with resistors, signals: Serial Data Line (**SDA**) and Serial Clock Line (**SCL**). I²C defines 3 basic types of transactions that all begin with *START* and end with *STOP*:

1. Single message – controller writes data to a target.
2. Single message – controller reads data from a target.
3. Combined format – controller issues at least 2 reads/writes to one or more targets.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| START | First byte | | ACK | I²C message sequence  (X bytes) | STOP |
| I²C address field | Read/Write |
| 7 bits  MSB to LSB | 1 = Read |
| 0 = Write |

Table . I²C 7-bit addressing structure

|  |  |  |  |
| --- | --- | --- | --- |
| First byte | | | Description |
| 7-bit I²C address field | | **R/W value** |
| 0000 | 000 | 0 | General call |
| 0000 | 000 | 1 | Start byte |
| 0000 | 001 | X | CBUS address |
| 0000 | 010 | X | Reserved for different bus |
| 0000 | 011 | X | Reserved for future purpose |
| 0000 | 1XX | X | HS-mode controller mode |
| 1111 | 1XX | 1 | Device ID |
| 1111 | 0XX | X | 10-bit target addressing |

Table . Reserved addresses in 7-bit address space

**The transaction format** of the I²C protocol consists of one or more messages. Each message begins with a *START* and ends with a *STOP*. More *START* symbols placed at the beginning of a transaction are referred to as *repeated start* *symbols*.

A message is either a read or a write. A transaction may consist of a single message (read/write transaction) or multiple messages (combined transaction).

Some limitations of the I²C interface are the *small address space* (the 7-bit protocol is widely used, but does not prevent address collision when thousands of devices are available, while the 10-bit I²C is not supported by many operating systems), *automatic bus configuration* (given addresses may be used by protocol-incompatible devices, device cannot be detected at runtime), *limited range of speeds*, *starving bandwidth* (devices are allowed to stretch clock cycles to suit their particular needs, increasing latencies), being *fault prone* (a fault, error or exception can hang the entire bus, i.e. a device holding *SDL* or *SCL* low will prevent the controller from sending *START* or *STOP* commands).

### Interfacing with the Pmod

The Pmod HYGRO communicates with the host board by means of the I²C interface. Users can both read and configure from the module. Data is sent in such a sequence:

1. the 7-bit I²C address 0x40.
2. a read/write bit.
3. the register address of interest.

Multiple 16-bit registers are accessible: the *configuration register* (address 0x02) allows the user to control the resolution of the measurement, change the acquisition mode, enable or disable the heater etc., the *temperature* (address 0x00) and *humidity* (address 0x01) *registers* are both read-only. The result of the measurement is always stored (regardless of resolution) in the most significant bits, the least 2 significant bits are always 0 for both registers. The higher the resolution the more time the conversion takes.

Upon power-up, the pmod requires 15 ms prior to perform a measurement. To perform a measurement, users need to accept the settings in the *configuration register* and then trigger the measuring process by sending an I²C write transaction paired with the address pointer set to the appropriate register. After waiting for the appropriate time necessary for conversion, users may perform a read transaction. After a read transaction users must wait at least one full second before performing another read transaction to avoid internal heating of the sensor and the distortion of the result. Whenever a write transaction is performed on either *temperature* or *humidity register*, the current conversion will be aborted and a new one started. If a read is performed during the conversion, the pmod will respond back with a ‘unavailable’ signal (NACK).

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit name | Bit number | Bit description | Bit values | Functional description |
| RST | 15 | Reset | 0\* | Normal functioning (self-clearing) |
| 1 | Software reset |
| Reserved | 14 | Reserved | 0 | Must be 0 |
| HEAT | 13 | Heater | 0\* | Heater disabled |
| 1 | Heater enabled |
| MODE | 12 | Acquisition Mode | 0 | Temperature or humidity is acquired depending on which register you choose to read |
| 1\* | Temperature and humidity are acquired in sequence (temperature first) |
| BTST | 11 | Battery Status | 0\* | VDD > 2.8 V (read-only) |
| 1 | VDD < 2.8 V (read-only) |
| TRES | 10 | Temperature Measurement Resolution | 0\* | 14 bit (6.35 ms\*\*) |
| 1 | 11 bit (3.65 ms\*\*) |
| HRES | [9:8] | Humidity Measurement Resolution | 00\* | 14 bit (6.50 ms\*\*) |
| 01 | 11 bit (3.85 ms\*\*) |
| 10 | 8 bit (2.50 ms\*\*) |
| 11 | - |
| Reserved | [7:0] | Reserved | 0 | Must be 0 |

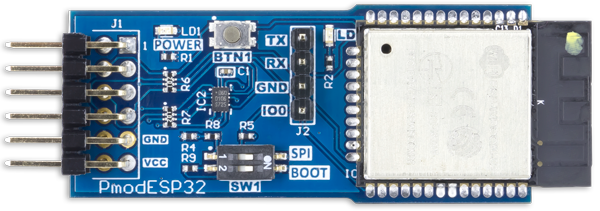
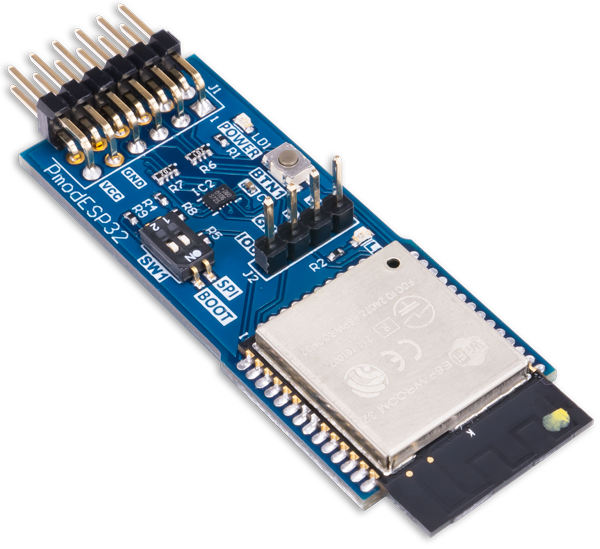
(\* Default value on power-up or reset, \*\* Time required to compute a conversion at that specific resolution)

Table . The Configuration Register (address 0x02)

## PMOD ESP32[[2]](#footnote-2)

The pmod ESP32 contains a Tensilica Xtensa microprocessor that allows operation in target mode over a UART interface. The module can work in a standalone mode as well. An additional UART port is provided on top of the module to make debugging easier.

Figure . PMOD ESP32



The module integrates Wi-Fi and Bluetooth 4.2 on a single chip. It possesses both the ability to be configured as an access point to its own network and to connect to an existing Wi-Fi. In target mode (SPI and GPIO are not used), the pmod responds to a set of AT commands. As a standalone device, a particular application can be uploaded via the J2 header UART connector.

Two switches are placed in the center of the module. The first one (SPI) switches between the SPI and UART interfaces. The second one (BOOT) controls whether the ESP32 boots into an application stored in memory or waits to be flashed with a new one. When the device is powered on, if the BOOT switch is on, the ESP32 will enter a mode where it waits to be flashed with a new application. If the switch is off, the ESP will boot and begin to run whatever application it has stored in memory. The behavior of the SPI switch can be controlled by a host board by means of the SELECT pin in the J1 header (the nineth pin): driving the SELECT pin high causes the top row of the connector to have SPI functionality, regardless of the value of the SPI switch; driving the same pin low causes the top row of the connector to have UART functionality. After flashing the ESP32 with a new application, or when switching between boot modes, RESET must be pressed. Pin 8 on the J1 header controls the functionality of the RESET button (BTN1 on the module).

The module requires between 2.7 and 3.6 V to operate. It offers an SPI serial clock frequency between 2 (typical) and 8.8 MHz and a UART serial clock frequency between 80 – 5 000 000 Baud (typically 115 200). Radio specifications: up to 150 Mbps 802.11 max data rate and up to 4 Mbps Bluetooth HCI max data rate.

|  |  |  |
| --- | --- | --- |
| Pin number | Signal | Description |
| 1 | RTS/SS | UART request to send/SPI target select |
| 2 | RXD/MOSI | UART receive data/SPI controller out target in |
| 3 | TXD/MOSI | UART transmit data/SPI controller in target out |
| 4 | CTS/SCK | UART clear to send/SPI serial clock |
| 5 | GND | Power supply ground |
| 6 | VCC | Power supply (3.3 V) |
| 7 | INT | Configurable GPIO/IO2 |
| 8 | EN | Reset enable |
| 9 | SELECT | UART or SPI mode select |
| 10 | GPIO | Configurable GPIO/IO32 |
| 11 | GND | Power supply ground |
| 12 | VCC | Power supply (3.3 V) |

Table . Pinout table diagram for ESP32

|  |  |  |
| --- | --- | --- |
| Switch | Value | Behavior |
| SPI (SW 1.1) | OFF | UART interface on pins  1 – 4 of Pmod header J1 |
| ON | SPI interface on pins 1 – 4 of Pmod header J1 |
| BOOT (SW 1.2) | OFF | Upon boot, the ESP32 will load the application that is currently stored in memory |
| ON | Upon boot, the ESP32 will not load anything, but wait for a new application to be flashed |

Table . PMOD ESP32 switch behavior

### AT command set[[3]](#footnote-3)

List . The types of AT commands

Rules for creating/using AT commands:

* Not all AT commands support all the above-mentioned four types.
* Only strings and integers are supported as parameters.
* **<>** designate parameters that cannot be omitted.
* []designate optional parameters. If missing, such a parameter is replaced by its default value.
* Multiple parameters are separated by commas.
* Strings need to be included between quotation marks.
* Escape character syntax is required if a string contains special characters.
* Input does not need to be escaped.
* The default baud rate is 115 200.
* The length of a command must not be greater than 256 bytes.
* All commands end with a new line (carriage return + line feed).

|  |  |
| --- | --- |
| ESP-AT response message | Description |
| OK | AT command process done and return OK. |
| ERROR | AT command error or error occurred during execution. |
| SEND OK | Data has been sent to the protocol stack. Data may not have reached the opposite end.  *(specific to AT+CIPSEND and AT+CIPSENDEX)* |
| SEND FAIL | Error occurred during sending the data to the protocol stack.  *(specific to AT+CIPSEND and AT+CIPSENDEX)* |
| SET OK | The URL has been set successfully.  *(specific to AT+HTTPURLCFG)* |
| +<command\_name>: … | Response to the sender that describes the AT command process results in details. |

Table . ESP-AT passive messages

|  |  |
| --- | --- |
| ESP-AT message report | Description |
| ready | The ESP-AT firmware is ready. |
| busy p… | Busy processing. The system is in process of handling the previous command, thus CANNOT accept the new input. |
| ERR CODE:<0x%08x> | Error code for different commands. |
| Will force to restart!!! | Module restart right now. |
| etc. |  |

Table . ESP-AT active messages

### Interfacing with the Pmod

The Pmod ESP32 is shipped to customers with the AT Instruction firmware preloaded into it, in target mode. The top pins are mapped to their UART functionality. It is important to keep in mind that the switches must be off when the device is powered on. To keep the device in target mode the SPI switch must be off. In this mode, AT commands are passed to the pmod via the UART interface on the top row of pins. The UART interface is set to work at 115 200 baud with 8 data bits, 1 stop bit, no parity or hardware control. These settings can be modified by the user.

To make it operate in standalone mode a couple of tools are required: the Xtensa toolchain, the Espressif ESP-IDF, Python and a USB-UART bridge device.

## AXI communication protocol

The AXI (Advanced eXtensible Interface) Stream protocol is used as a standard interface to exchange data between connected devices. It is a point-to-point protocol that connects a single transmitter to a single receiver.

### Glossary of terms

|  |  |
| --- | --- |
| Term | Meaning |
| Data BYTE | A byte transmitted from the source to the destination containing valid information. |
| Position BYTE | A placeholder that does not contain any relevant data, but relative positions of data bytes in the stream. |
| Null BYTE | A byte that is not a data or a position byte. |
| Transfer | A single transfer of data across the AXI-Stream interface. It is defined by a single *TVALID* and *TREADY* signal handshake. |
| Packet | A group of bytes that are transported across an AXI-Stream interface. It consists of a single or multiple transfers. |
| Frame | An integer number (may be very large) of packets. Highest level of byte grouping in AXI-Stream. |
| Data stream | A transport of data from a source to a destination. Can be a series of individual byte or packets transfers. |

# **Analysis**

## Project Proposal

## Project Analysis

# **Design**

# **Implementation**

# **Testing & Validation**

# **Conclusions**

# **Bibliography**

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