Homework

B.8 [5/5/5] <B.3> We want to observe the following calculation

$$d_i = a_i + b_i * c_i, \qquad i : (0 : 511)$$

Arrays a, b, c, and d memory layout is displayed below (each has 512 4-byte-wide integer elements).

The above calculation employs a for loop that runs through 512 iterations.

Assume a 32 Kbyte 4-way set associative cache with a single cycle access time. The miss penalty is 100 CPU cycles/access, and so is the cost of a write-back. The cache is a write-back on hits write-allocate on misses cache (Figure B.32).

a. [5] <B3> How many cycles will an iteration take if all three loads and single store miss in the data cache?

b. [5] <B3> If the cache line size is 16 bytes, what is the average number of cycles an average iteration will take? (Hint: Spatial locality!)

c. [5] <B3> If the cache line size is 64 bytes, what is the average number of cycles an average iteration will take?

d. If the cache is direct-mapped and its size is reduced to 2048 bytes, what is the average number of cycles an average iteration will take?

Mem. address in bytes	Contents
0–2047	Array *a*
2048–4095	Array *b*
4096–6143	Array *c*
6144–8191	Array *d*

Figure B.32 Arrays layout in memory.