Application note

DA14580-01 Cold boot timing and power details

AN-B-011

Abstract

This Application Note describes and explains the power dissipation of the DA14580-01 from power-up to the point that the Bluetooth system starts advertising. It also explains the time intervals in terms of actions performed in the DA14580-01. It concludes with further optimisation proposals for power and timing if cold boot requirements dictate it.

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1 Terms and definitions

DMA	Direct Memory Access
FSM	Finite State Machine
HW	Hardware
LDO	Low Drop-Out (regulator)
OTP	One Time Programmable (memory)
SDK	Software Development Kit
SW	Software

2 References

1. DA14580, Data sheet, Dialog Semiconductor

3 Introduction

The cold boot time and energy used is an important feature of the DA14580-01 since, due to its very good characteristics, it enables the total powering down of the chip in applications with a very large duty cycle. In parallel, the cold boot sequence is optimised to be immune to any voltage drop during booting. Such drops can be generated by poor contact while a battery is being changed or bad debouncing from a power switch.

This application note explains the cold boot sequence with respect to the timing and the charge drawn from a battery. The measurements have been performed using the SmartSnippets v2.2 on a DA14580-01 Development Kit in buck mode. The OTP has been programmed with the Proximity Reporter application which comes with the SDK.

4 Power and timing details

The power profile of the DA14580 from cold boot up to the point of starting to advertise is presented in the following figure:

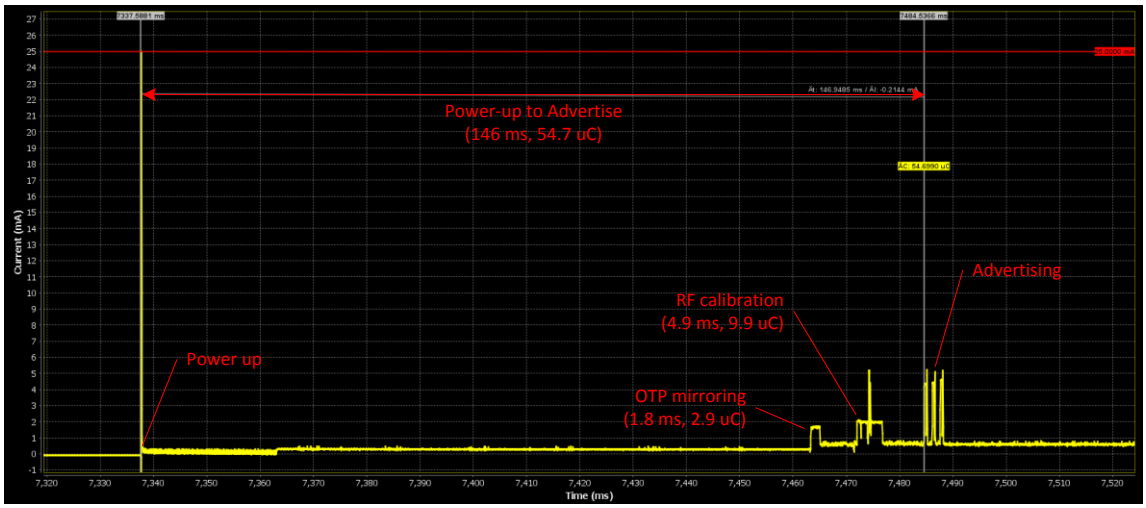

Figure 1: Power up to advertise timing

Figure 1 clearly shows the time required from powering up the system up to the point of advertising. The total time required is 146 ms. The breakdown of this time is presented in the following table:

Table 1: Cold boot timing break down

Interval	Identification	Time/Charge	Description
From Power Up to OTP mirroring	Hardware FSM BootROM	1.2 ms/1.9 µC 124 ms/31 µC	The HW FSM which powers up LDOs and the DC-DC converter. The BootROM code which consists of a delay of 100 ms and the copy of the calibration values from the OTP into the registers.
OTP Mirroring	OTP Mirroring	1.8 ms/2.9 µC	OTP contents are copied into System RAM.
From OTP mirroring to RF calibration	Reset Handler	6.9 ms/4 µC	SW executes the reset handler and initialises 12 kB of exchange memory to zero (EM_MAP=23).
RF Calibration	RF Calibration	4.9 ms/9.9 µC	Radio is trimmed by SW.
From RF calibration to Advertising	Database initialization	7.8 ms/5 µC	SW initialises the descriptors and the database of the system.

The system starts with the hardware state machine which operates on the RC32KHz internal oscillator. This state machine is responsible for starting up the DC-DC converter, the internal LDOs and safely identifying whether the system is in BUCK or BOOST mode. The amount of time for a “clean” run through the state machine (without timeouts) is between 1.2 ms and 1.5 ms, depending on the voltage level at the VBAT3V or VBAT1V pins.

Then the BootROM code will take over, starting with a delay of 100 ms. This delay is protecting the system from continuing to the OTP copy before the voltage has reached a stable level. After this delay, the code switches the clock to the internal RC16 MHz oscillator, which is still untrimmed. This clock is now used to start accessing the OTP and copy the trimmed values stored in the OTP header during production test into the respective registers of the DA14580. The trim values can be found in the DA14580 datasheet.

Next the BootROM code initiates the DMA based OTP mirroring process, which copies the whole OTP memory contents into the System RAM (0x20000000) and requires 1.8 ms. This time is longer than in normal operation[1], since each and every one of the burst copies is protected by a software check on the voltage of the system (using the ADC VBATx channels) and the OTP LDO status. At the end of this interval the BootROM code will switch the clock source to the XTAL16 MHz oscillator and hand over the control to the user’s application.

The first code executed at the end of the BootROM code is the reset handler. This snippet of software is configuring the physical memory mapping with respect to the Bluetooth exchange memory size and then it initialises everything to zero. This takes 7.8 ms considering that there is 12 kB that must be initialised. Following that, the RF calibration process is executed, a necessary function to trim and optimise the radio operation. This process requires 4.9 ms.

The final interval takes 7.8 ms which is used for the initialization of the TX/RX descriptors for the system and the database of the Bluetooth Smart device. Following this action, the system starts advertising, assuming that it is configured as a peripheral.

The total charge required for the cold boot sequence is 54.7 μC and the time needed is 146 ms. This time ensures that the system will automatically identify whether Buck or Boost mode is used and guarantees proper operation, even when severe voltage drops occur during the booting process.

5 Improvement proposals

To further optimise the time elapsed from power-up to advertising, the following amendments may be considered:

- Use a different exchange memory configuration (see GP_CONTROL_REG[EM_MAP]) which results to a smaller allocation and thus the time required for the zero initialization can be further reduced.
- Do not initialise the whole memory to zero but only the section of the variables, to reduce time.

The actual reduction in time is only affecting the interval from the OTP mirroring up to the RF calibration and is heavily dependent on the configuration choices made by the user.

[1] An OTP mirroring action is also triggered every time the system wakes up from the Deep Sleep mode.

6 Revision history

Revision	Date	Description
1.0	04-Mar-2014	Initial version.

Status definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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