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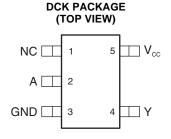
# LOW POWER, 1.8/2.5/3.3-V INPUT, 3.3-V CMOS OUTPUT, SINGLE SCHMITT-TRIGGER INVERTER GATE

Check for Samples: SN74AUP1T14

#### **FEATURES**

- Single-Supply Voltage Translator
- Output Level Up to Supply V<sub>CC</sub> CMOS Level
  - 1.8 V to 3.3 V (at  $V_{CC} = 3.3 \text{ V}$ )
  - 2.5 V to 3.3 V (at  $V_{CC} = 3.3 \text{ V}$ )
  - 1.8 V to 2.5 V (at  $V_{CC} = 2.5 \text{ V}$ )
  - 3.3 V to 2.5 V (at  $V_{CC} = 2.5 \text{ V}$
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity
- I<sub>off</sub> Supports Partial Power Down (V<sub>CC</sub> = 0 V)
- Very Low Static Power Consumption: 0.1 μA
- Very Low Dynamic Power Consumption: 0.9 μA
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Pb-Free Packages Available: SC-70 (DCK)
   2 x 2.1 x 0.65 mm (Height 1.1 mm)

- More Gate Options Available at www.ti.com/littlelogic
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)



#### **DESCRIPTION/ORDERING INFORMATION**

The SN74AUP1T14 performs the Boolean function  $Y = \overline{A}$  with designation for logic-level translation applications with output referenced to supply  $V_{CC}$ .

AUP technology is the industry's lowest-power logic technology designed for use in extending battery-life in operating. All input levels that accept 1.8-V LVCMOS signals, while operating from either a single 3.3-V or 2.5-V  $V_{CC}$  supply. This product also maintains excellent signal integrity (see Figure 1 and Figure 2).

The wide  $V_{CC}$  range of 2.3 V to 3.6 V allows the possibility of switching output level to connect to external controllers or processors.

Schmitt-trigger inputs ( $\Delta V_T = 210$  mV between positive and negative input transitions) offer improved noise immunity during switching transitions, which is especially useful on analog mixed-mode designs. Schmitt-trigger inputs reject input noise, ensure integrity of output signals, and allow for slow input signal transition.

 $I_{off}$  is a feature that allows for powered-down conditions ( $V_{CC} = 0$  V) and is important in portable and mobile applications. When  $V_{CC} = 0$  V, signals in the range from 0 V to 3.6 V can be applied to the inputs and outputs of the device. No damage occurs to the device under these conditions.

The SN74AUP1T14 is designed with optimized current-drive capability of 4 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



#### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACK	(AGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
4000 to 0500	COT (CC 70) DCK	Reel of 3000	SN74AUP1T14DCKR	c.
–40°C to 85°C	SOT (SC-70) – DCK	Reel of 250	SN74AUP1T14DCKT	6F_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) The actual top-side marking has one additional character that designates the water fab/assembly site.

#### **FUNCTION TABLE**

INPUT (Lower Level Input)	OUTPUT (V <sub>CC</sub> CMOS)
Α	Y
Н	L
L	Н

#### Supply $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V } (2.5 \text{ V})$

117	00	<u> </u>
INF V <sub>T+</sub> max V <sub>T-</sub> min	OUTPUT CMOS	
Α	В	Υ
V <sub>IH</sub> =	= 1.1 V	V <sub>OH</sub> = 1.85 V
V <sub>IL</sub> =	0.35 V	$V_{OL} = 0.45 \text{ V}$

#### Supply $V_{CC} = 3 \text{ V to } 3.6 \text{ V } (3.3 \text{ V})$

INP V <sub>T+</sub> max V <sub>T-</sub> min =	OUTPUT CMOS			
Α	В	Y		
V <sub>IH</sub> =	V <sub>IH</sub> = 1.19 V			
V <sub>IL</sub> =	0.5 V	$V_{OL} = 0.45 \text{ V}$		

#### LOGIC DIAGRAM (SCHMITT-TRIGGER INVERTER GATE)



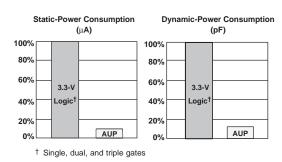


Figure 1. AUP – The Lowest-Power Family

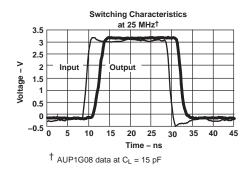


Figure 2. Excellent Signal Integrity

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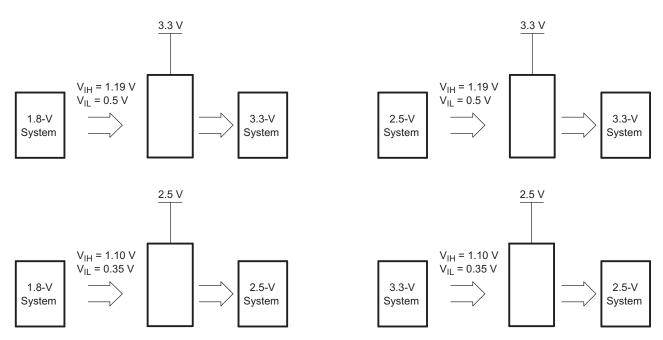


Figure 3. Typical Design Examples

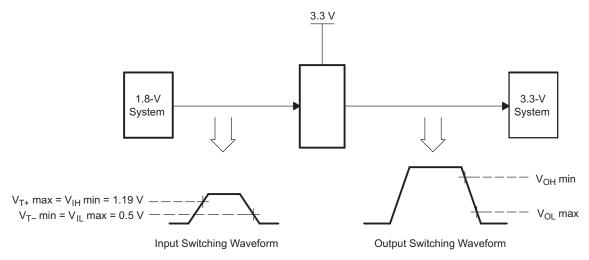


Figure 4. Switching Thresholds for 1.8-V to 3.3-V Translation



#### **ABSOLUTE MAXIMUM RATINGS**(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	4.6	<b>V</b>
VI	Input voltage range <sup>(2)</sup>		-0.5	4.6	V
Vo	Voltage range applied to any output in the high-impedance or power	er-off state <sup>(2)</sup>	-0.5	4.6	V
Vo	Output voltage range in the high or low state (2)	-0.5	$V_{CC} + 0.5$	V	
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		<b>-</b> 50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
Io	Continuous output current			±20	mA
	Continuous current through V <sub>CC</sub> or GND			±50	mA
$\theta_{JA}$	Package thermal impedance (3)	DCK package		259	°C/W
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2.3	3.6	V
$V_{I}$	Input voltage		0	3.6	V
Vo	Output voltage		0	$V_{CC}$	V
	High level output ourset	V <sub>CC</sub> = 2.3 V		-3.1	A
Іон	High-level output current	V <sub>CC</sub> = 3 V		-4	mA
	Lour lovel output ourrent	V <sub>CC</sub> = 2.3 V		3.1	A
IOL	Low-level output current	V <sub>CC</sub> = 3 V		4	mA
T <sub>A</sub>	Operating free-air temperature	·	-40	85	°C

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the TI application report Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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<sup>(2)</sup> The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(3)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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#### **ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIONS	V <sub>cc</sub>	T <sub>A</sub> =	= 25°C	T <sub>A</sub> = -40 to 85°C		UNIT
				MIN	TYP MAX	MIN	MAX	
V <sub>T+</sub>			2.3 V to 2.7 V	0.6	1.1	0.6	1.1	
	e-going input old voltage		3 V to 3.6 V	0.75	1.16	0.75	1.19	V
V <sub>T</sub> _			2.3 V to 2.7 V	0.35	0.6	0.35	0.6	
	ve-going nreshold e		3 V to 3.6 V	0.5	0.85	0.5	0.85	V
$\Delta V_{T}$			2.3 V to 2.7 V	0.23	0.6	0.1	0.6	
Hyster (V <sub>T+</sub> -			3 V to 3.6 V	0.25	0.56	0.15	0.56	V
		I <sub>OH</sub> = -20 μA	2.3 V to 3.6 V	V <sub>CC</sub> - 0.1		V <sub>CC</sub> - 0.1		
		$I_{OH} = -2.3 \text{ mA}$	2.3 V	2.05		1.97		V
$V_{OH}$		I <sub>OH</sub> = -3.1 mA	2.3 V	1.9		1.85		
		$I_{OH} = -2.7 \text{ mA}$	3 V	2.72		2.67		
		$I_{OH} = -4 \text{ mA}$	3 V	2.6		2.55		
		I <sub>OL</sub> = 20 μA	2.3 V to 3.6 V		0.1		0.1	
		I <sub>OL</sub> = 2.3 mA	2.3 V		0.31		0.33	
$V_{OL}$		I <sub>OL</sub> = 3.1 mA	2.3 V		0.44		0.45	V
		I <sub>OL</sub> = 2.7 mA	3 V		0.31		0.33	
		I <sub>OL</sub> = 4 mA	3 V		0.44		0.45	
I	All inputs	V <sub>I</sub> = 3.6 V or GND	0 V to 3.6 V		0.1		0.5	μΑ
$I_{\rm off}$		$V_I$ or $V_O = 0$ V to 3.6 V	0 V		0.1		0.5	μΑ
$\Delta I_{\text{off}}$		$V_I$ or $V_O = 3.6 \text{ V}$	0 V to 0.2 V		0.2		0.5	μΑ
I <sub>CC</sub>		V <sub>I</sub> = 3.6 V or GND, I <sub>O</sub> = 0	2.3 V to 3.6 V		0.5		0.9	μΑ
		One input at 0.3 V or 1.1 V, Other inputs at 0 or $V_{CC}$ , $I_{O} = 0$	2.3 V to 2.7 V				4	μА
ΔI <sub>CC</sub>		One input at 0.45 V or 1.2 V, Other inputs at 0 or $V_{CC}$ , $I_{O} = 0$	3 V to 3.6 V					μΑ
$C_{i}$		$V_I = V_{CC}$ or GND	3.3 V		1.5			pF
Co		V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		3			pF

#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $V_{CC}$  = 2.5 V ± 0.2 V,  $V_I$  = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 5)

PARAMETER	FROM	TO (OUTPUT)	C <sub>L</sub>		T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C	
	(INPUT)			MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>			5 pF	1.8	2.3	2.9	0.5	6.8	
	^	V	10 pF	2.3	2.8	3.4	1	7.9	
	А	Y	15 pF	2.6	3.1	3.8	1	8.7	ns
			30 pF	3.8	4.4	5.1	1.5	10.8	

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#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $V_{CC}$  = 2.5 V ± 0.2 V,  $V_I$  = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 5)

PARAMETER	PARAMETER	FROM	TO (OUTPUT)		CL	T	λ = 25°C		T <sub>A</sub> =	40°C 5°C	UNIT
	(INPUT)	(OUTPUT)	_	MIN	TYP	MAX	MIN	MAX			
t <sub>pd</sub>	А	Y	5 pF	1.8	2.3	3.1	0.5	6			
			10 pF	2.2	2.8	3.5	1	7.1			
			15 pF	2.6	3.2	5.2	1	7.9	ns		
			30 pF	3.7	4.4	5.2	1.5	10			

#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $V_{CC}$  = 2.5 V ± 0.2 V,  $V_I$  = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 5)

PARAMETER	FROM	TO (OUTPUT)		CL	Т,	<sub>A</sub> = 25°C		T <sub>A</sub> = -	40°C 5°C	UNIT
	(INPUT)			MIN	TYP	MAX	MIN	MAX		
t <sub>pd</sub>		Υ	5 pF	2	2.7	3.5	0.5	5.5		
	^		10 pF	2.4	3.1	3.9	1	6.5		
	А		15 pF	2.8	3.5	4.3	1	7.4	ns	
			30 pF	4	4.7	5.5	1.5	9.5		

#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $V_{CC}$  = 3.3 V ± 0.3 V,  $V_I$  = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 5)

PARAMETER	FROM	TO (OUTPUT)	CL	Т,	<sub>A</sub> = 25°C	;	T <sub>A</sub> = -40°C to 85°C		UNIT
	(INPUT)	(OUTPUT)	_	MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	А		5 pF	1.6	2	2.5	0.5	8	
		V	10 pF	2	2.4	2.9	1	8.5	
		Y	15 pF	2.3	2.8	3.3	1	9.1	ns
			30 pF	3.4	3.9	4.4	1.5	9.8	

#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{I} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted) (see Figure 5)

PARAMETER	PARAMETER	FROM TO (INPUT) (OUTP			CL	T	λ = 25°C		T <sub>A</sub> =	40°C 5°C	UNIT
	(INFOT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX			
t <sub>pd</sub>	А	A Y	5 pF	1.6	1.9	2.4	0.5	5.3			
			10 pF	2	2.3	2.7	1	6.1			
			15 pF	2.3	2.7	3.1	1	6.8	ns		
			30 pF	3.4	3.8	4.2	1.5	8.5			

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#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $V_{CC}$  = 3.3 V ± 0.3 V,  $V_I$  = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 5)

PARAMETER	FROM	TO (OUTPUT)	C <sub>L</sub> T <sub>A</sub> = 25°C			T <sub>A</sub> =	40°C 5°C	UNIT		
	(INPUT)	(OUTPUT)		MIN TYP MAX			MIN	MAX		
			5 pF	1.6	2.1	2.7	0.5	4.7		
	^	V	10 pF	2	2.4	3	1	5.7		
t <sub>pd</sub>	A	ř	15 pF	2.3	2.7	3.3	1	6.2	ns	
			30 pF	3.4	3.8	4.4	1.5	7.8		

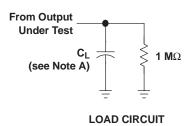
#### **OPERATING CHARACTERISTICS**

 $T_A = 25^{\circ}C$ 

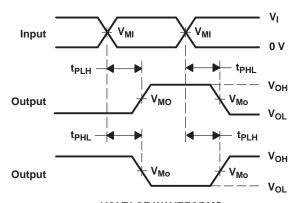
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT	
	PARAMETER	TEST CONDITIONS	TYP	TYP	ONII	
$C_{pd}$	Power dissipation capacitance	f = 10 MHz	4	5	pF	



#### PARAMETER MEASUREMENT INFORMATION



	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V
C <sub>L</sub>	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V <sub>MI</sub>	V <sub>I</sub> /2	V <sub>I</sub> /2
V <sub>MO</sub>	V <sub>CC</sub> /2	V <sub>CC</sub> /2



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \ \Omega$ , slew rate  $\geq$  1 V/ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 5. Load Circuit and Voltage Waveforms

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#### PACKAGE OPTION ADDENDUM

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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins P	ackage Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74AUP1T14DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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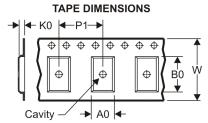
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PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION





1	40	Dimension designed to accommodate the component width
		Dimension designed to accommodate the component length
ŀ	⟨0	Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
T	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T14DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T14DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

## DCK (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



# DCK (R-PDSO-G5)

### PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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