

QFN Layout Guidelines

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1 Introduction

Board layout and stencil information for most Texas Instruments (TI) Quad Flat No-Lead (QFN) devices is provided in their data sheets. This document helps printed-circuit board (PCB) designers understand and better use this information for optimal designs.

The QFN package is a thermally enhanced standard size IC package designed to eliminate the use of bulky heat sinks and slugs. This package can be easily mounted using standard PCB assembly techniques and can be removed and replaced using standard repair procedures.

The QFN package is designed so that the lead frame die pad (or thermal pad) is exposed on the bottom of the IC (see [Figure 1](#)). This provides an extremely low thermal resistance (θ_{JC}) path between the die and the exterior of the package.

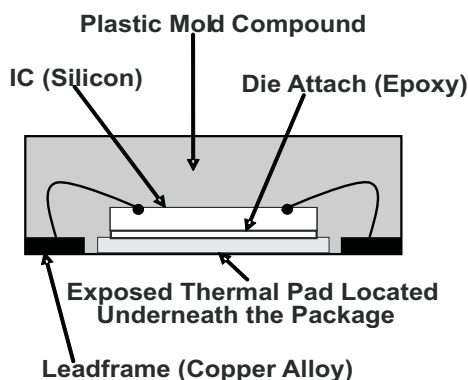


Figure 1. Section View of a QFN Package

2 Board Layout

Figure 2 shows an example of the recommended board layout for an RGZ package.

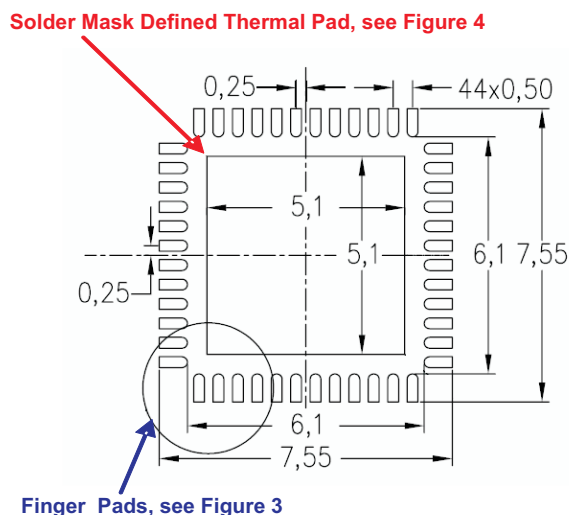


Figure 2. Board Layout for an RGZ Package Finger Pads

TI recommends the use of rounded finger pads to prevent solder bridging. Surround each pad with a 0.07-mm wide solder mask. The recommended dimensions are shown in Figure 3.

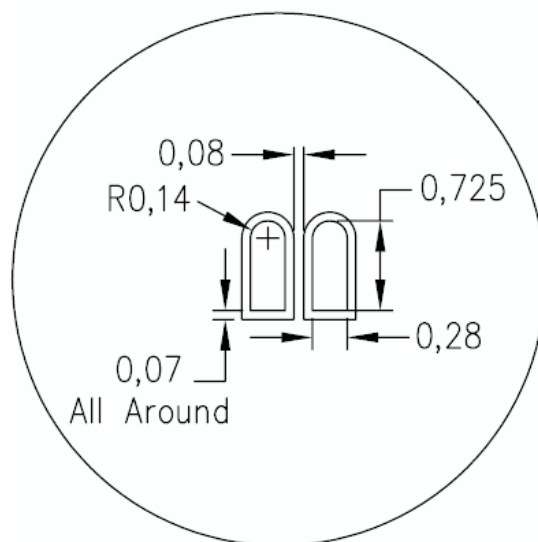


Figure 3. Finger Pads Layout

2.1 Solder Mask Defined Thermal Pad

The solder mask defined thermal pad is the exposed copper area not covered by solder mask. It must be soldered directly to the thermal pad on the bottom of the IC. Figure 2 shows an example of the recommended dimensions.

2.1.1 Copper Areas

Copper areas on and in a PCB act as heat sinks for the QFN device. Top copper areas should be covered with solder mask leaving only the solder mask defined thermal pad exposed. The top copper areas should be made as large as possible.

Inner or bottom layer copper planes also can be connected to thermal pad using vias and should be made as large as possible. The thermal pad is usually tied to ground, and designers should verify the electrical correctness when connecting the copper planes to the thermal pad.

Designers may leave the bottom copper plane exposed. However, studies have shown that this has minimal impact on thermal performance.

2.1.2 Thermal Vias

TI recommends placing thermal vias in the solder mask defined thermal pad to transfer effectively the heat from the top copper layer of the PCB to the inner or bottom copper layers.

TI provides the recommended layout of the thermal vias in most data sheets. The recommended via diameter is 0,3 mm or less, and the recommended via spacing is 1 mm (see [Figure 4](#)).

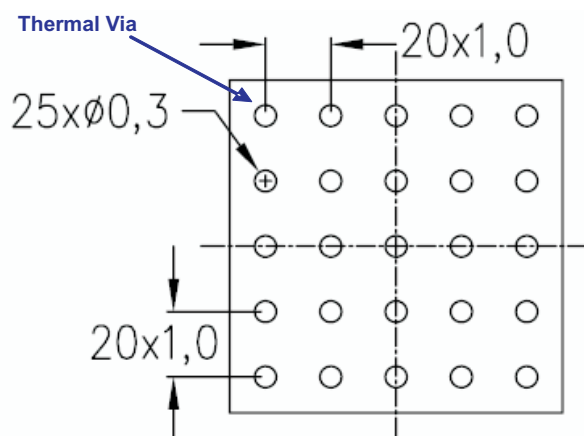


Figure 4. Solder Mask Defined Thermal Pad

The thermal vias should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole. Place a ring of exposed copper (0,05 mm wide) around the vias at the bottom of the copper plane.

Do not cover the vias with solder mask which causes excessive voiding.

Do not use a thermal relief web or spoke connection which impedes the conduction path into the inner copper layer(s) (see [Figure 5](#)).

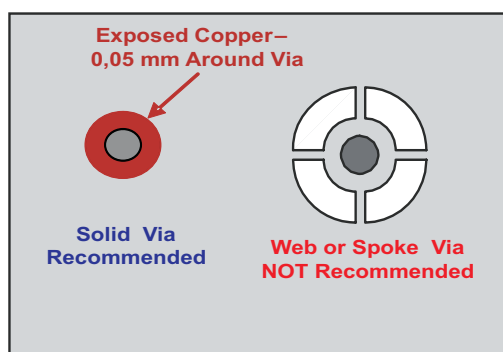


Figure 5. Via Connection at the Bottom of the Copper Plane

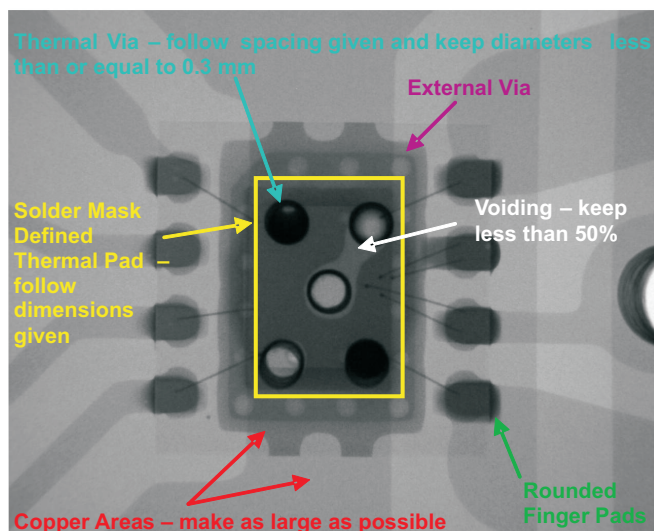


Figure 6. X-Ray – DRB Device

Vias may be plugged to prevent solder loss and protrusions. This often produces the best thermal performances but is not necessary or recommended because of the increased cost of PCBs and because solder tends to wet the upper surface first before filling the vias.

Vias also can be used in the copper area outside the solder mask defined thermal pad to help dissipate heat through bottom or inner planes.

If thin PCBs or vias larger than 0,3 mm are used, designers may use only external vias to prevent solder loss and protrusions (see [Figure 7](#)). Designers should note that this might reduce thermal performance significantly and should be evaluated on their PCBs.

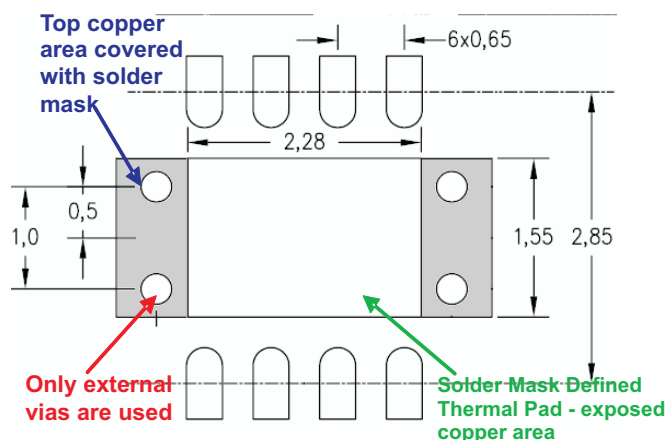


Figure 7. Example of Using Only External Vias in a DRB Package

2.1.3 Solder Loss and Protrusions

Solder loss and protrusions result when excessive solder flowed through internal vias during reflow. These usually happen when incorrect internal vias sizes and stencil openings are used.

Solder loss results in voiding and severely affects thermal conductivity. Designers are encouraged to x-ray their reflowed boards to verify that at least 50% of thermal pad area is soldered (less than 50% voiding) when using 0,127-mm thick stencils.

Protrusions might cause misalignment in stencil on the reverse side of the PCB (see [Figure 8](#)).

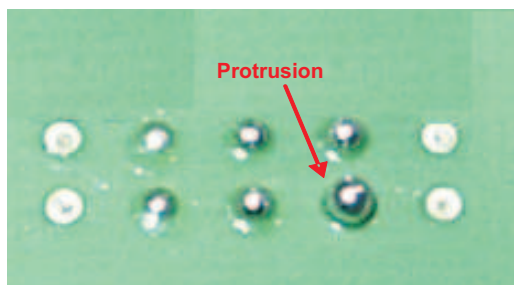


Figure 8. Protrusion at the Other Side of Board

2.1.4 Stencil

Figure 9 shows an example of the recommended stencil openings and thickness. Follow stencil openings and thickness recommended to ensure that the right amount of solder paste is used.

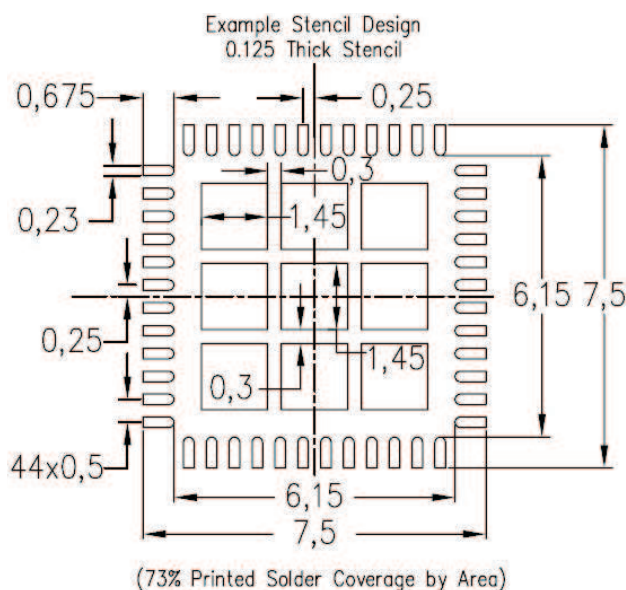


Figure 9. Recommended Stencil Openings and Thickness for RGZ Package

Use cross-hatching in the thermal pad stencil opening of a QFN device. This prevents excessive amount of solder paste applied thus prevents solder bridging (see Figure 10).

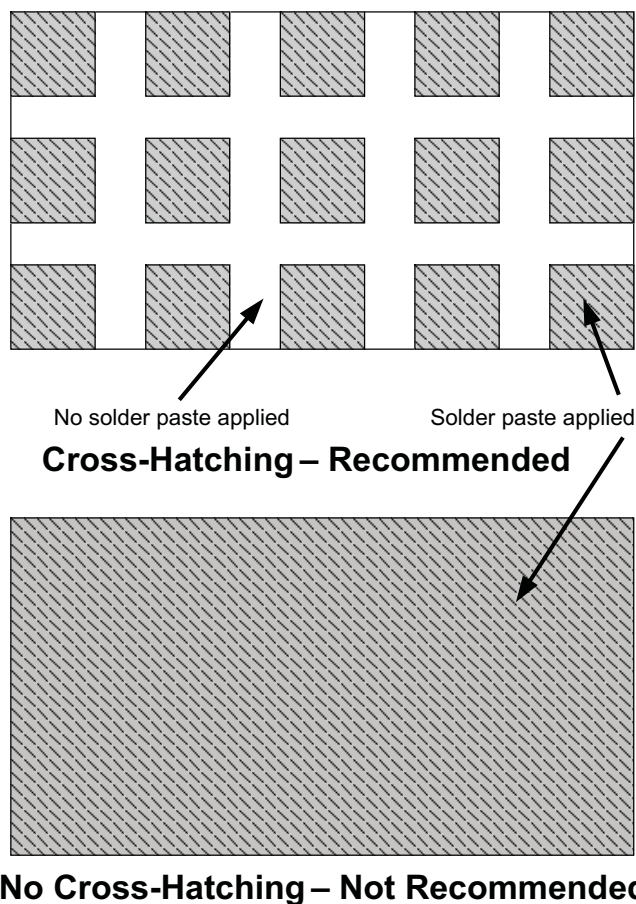


Figure 10. Thermal Pad Stencil Opening

2.1.5 Recommended Solder Paste

TI recommends the use of type 3 or finer solder paste when mounting a QFN.

2.2 Additional Information

For detailed information on the QFN package including thermal modeling considerations and repair procedures, see ([SLUA271](#)) QFN/SON PCB attachment.

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