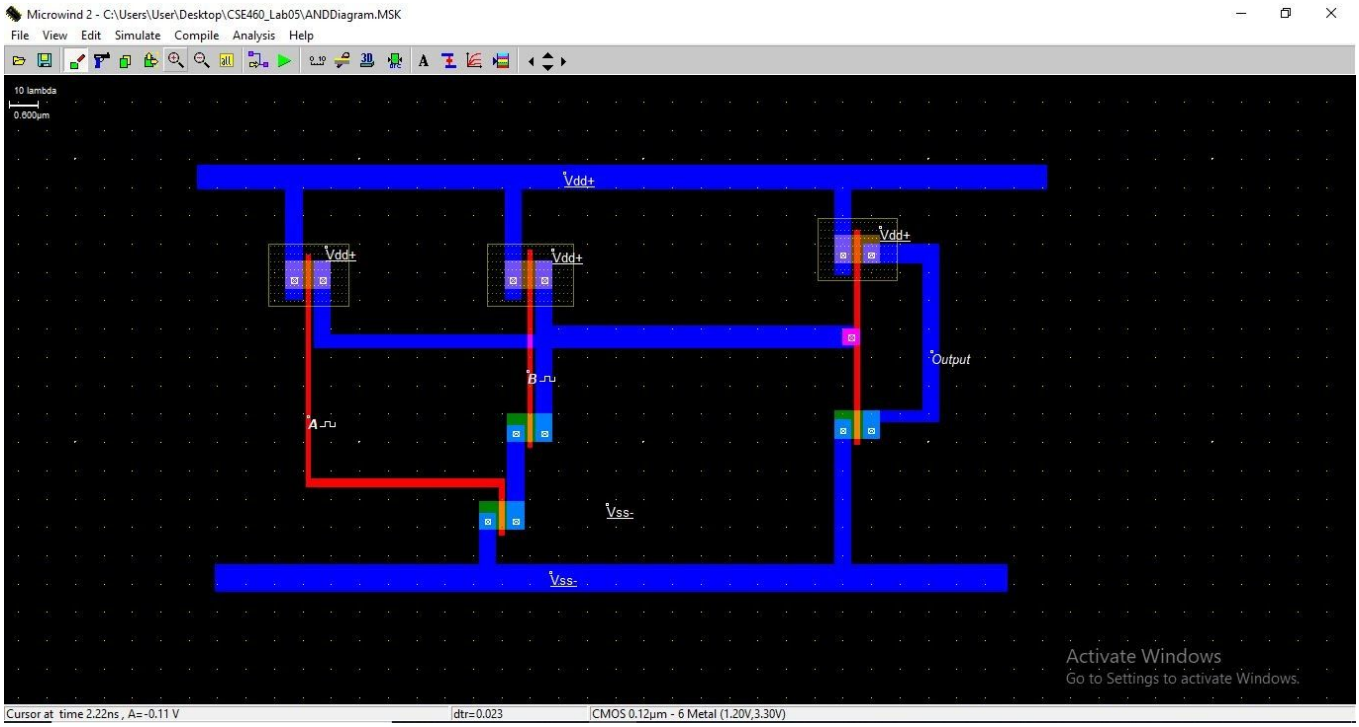
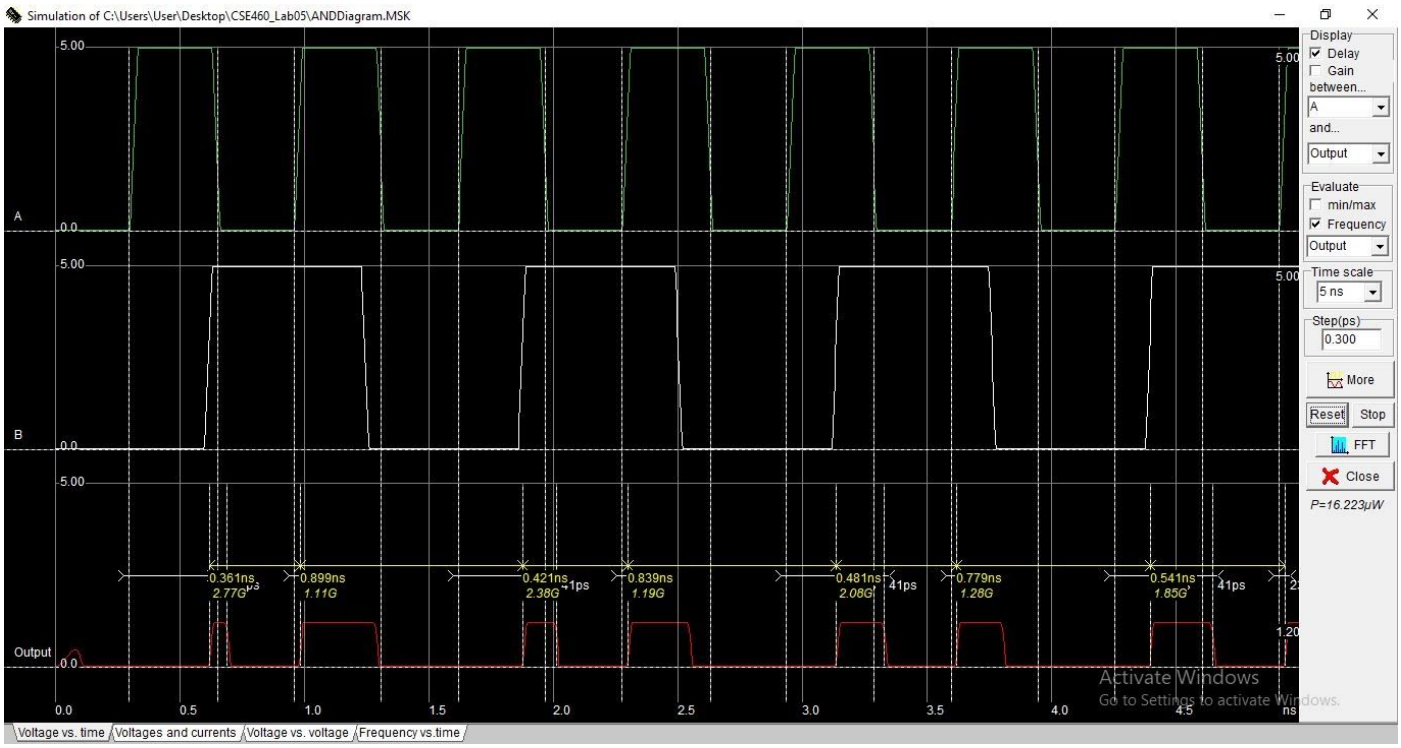
Name: Mashfiq Shahriar Zaman
ID: 17301167
Section: 12
CSE 460 Lab 05

Answer to the Question No: 01

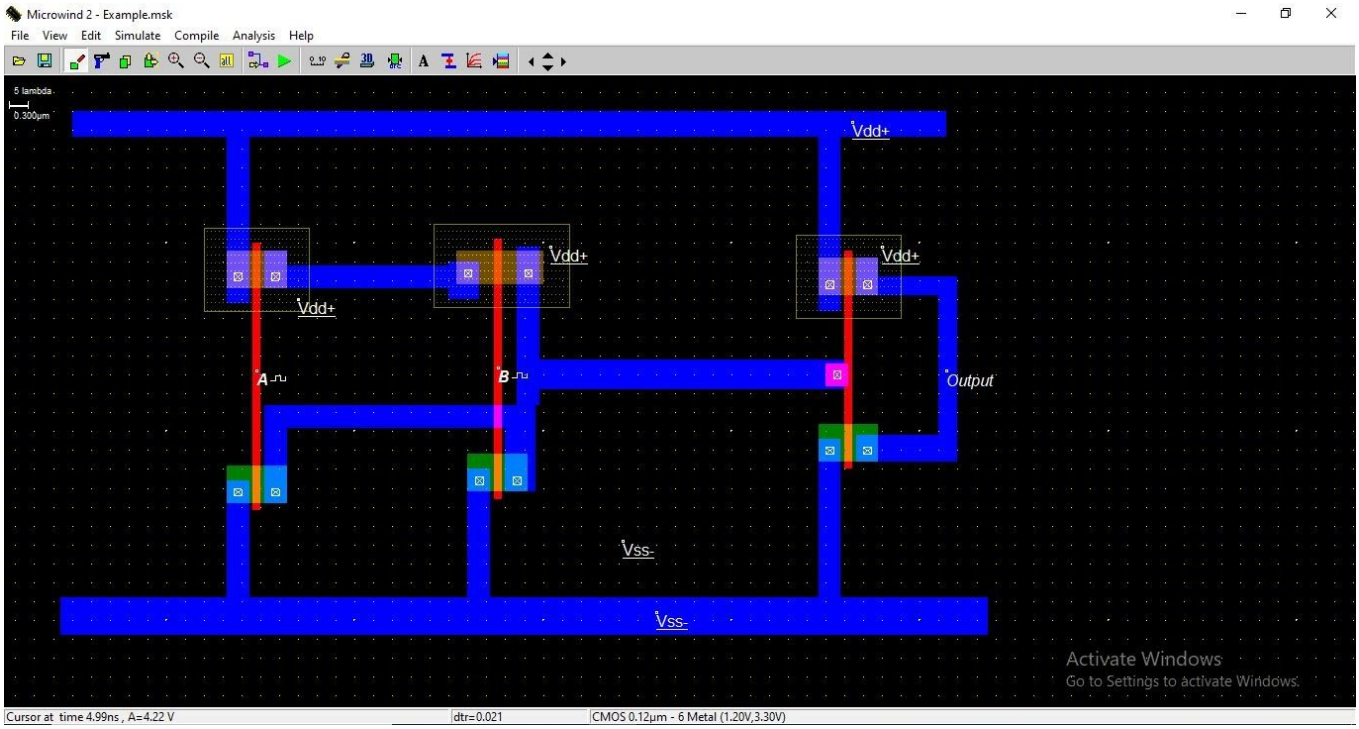
The layout design of AND gate using CMOS gate has given below:

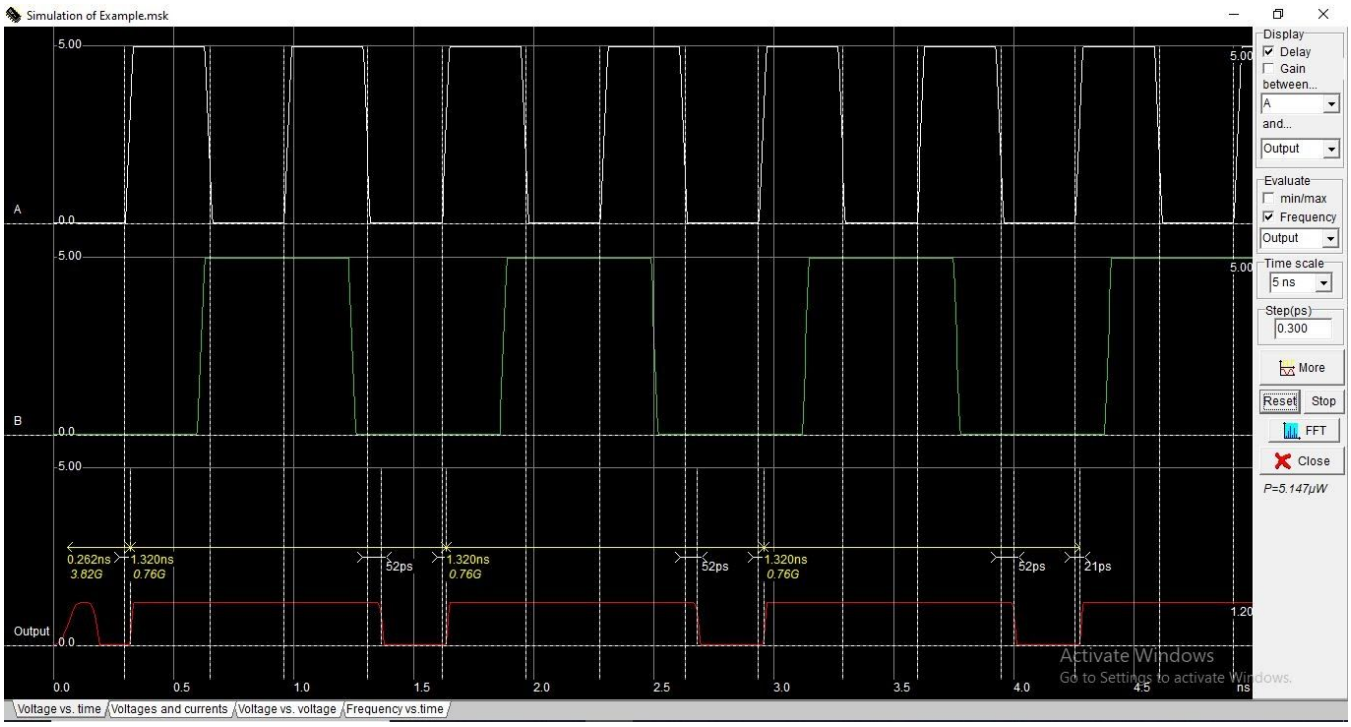




For the AND gate implementation, I have used two inputs A and B. From the simulation, it can be observed that when both inputs A and B are high (1), the output is high(1). When the input of one the gates is low(0), the output will be low(0). Also, the output will be low(0) when the two inputs are low(0). The output will be only high(1) when both or all of the inputs are high(1). As the simulation is showing the signals properly, it can be perceived that the implementation is correct.

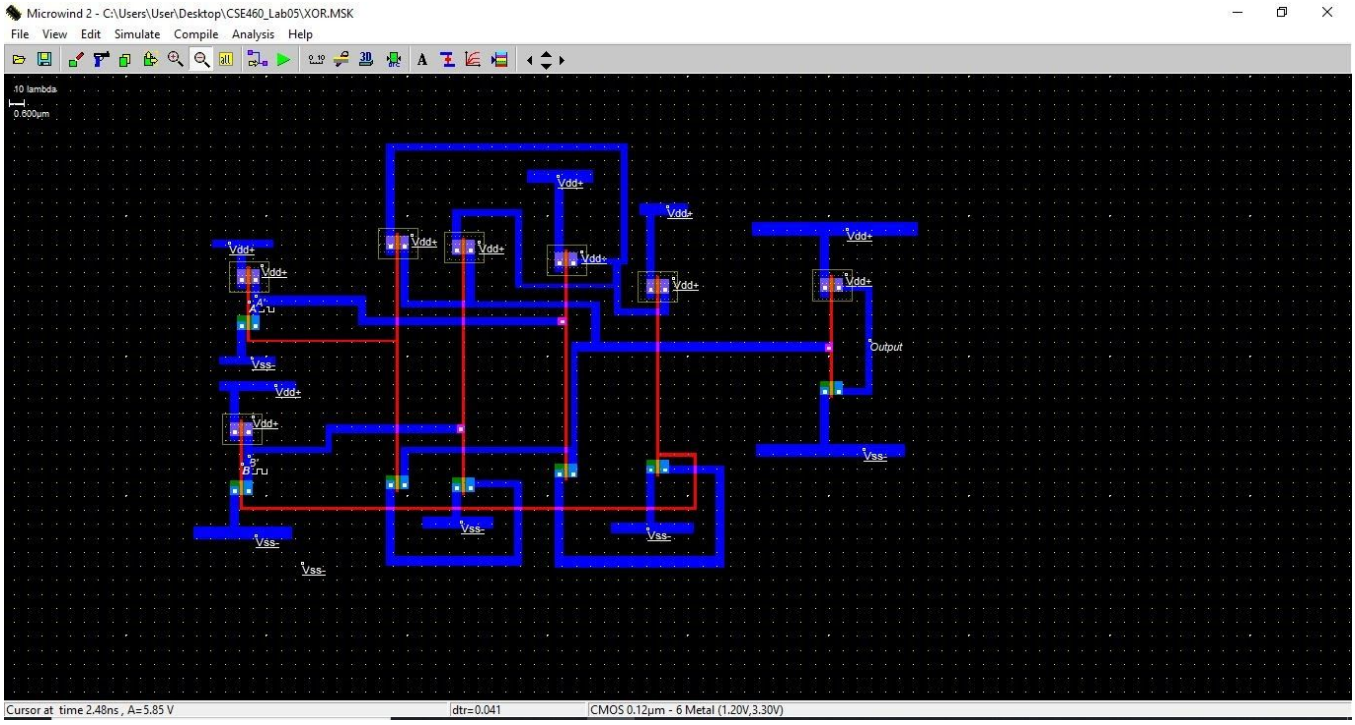
The design layout of OR gate using CMOS has given below:

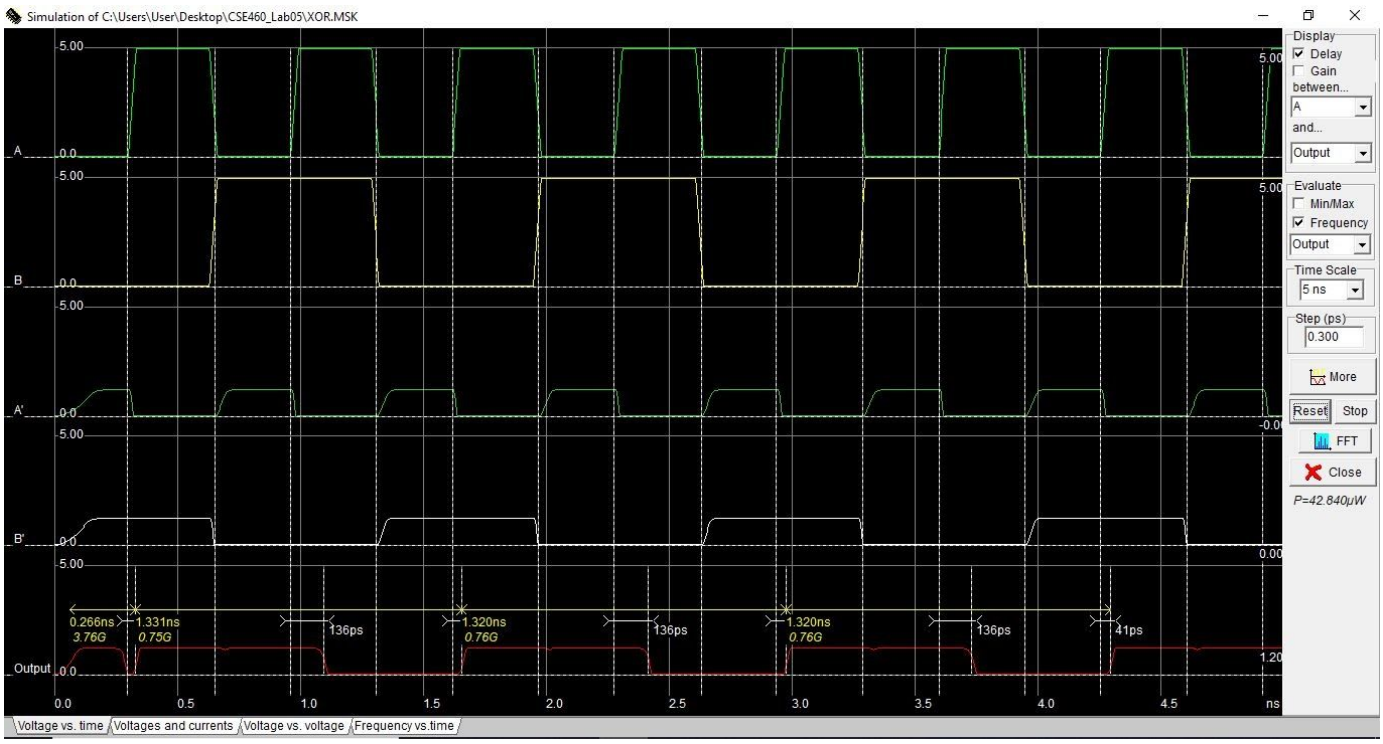




For the OR gate implementation, I have used two inputs A and B. From the simulation, it can be observed that the output will be high(1) if one of the inputs is high(1). The output will only be low(0) when both or all of the inputs are low(0). So, the output will be high(1) if only one input is high(1) and the output of the OR gate will only be low(0) when all of the inputs are low(0).

The layout design of XOR gate using CMOS has given below:

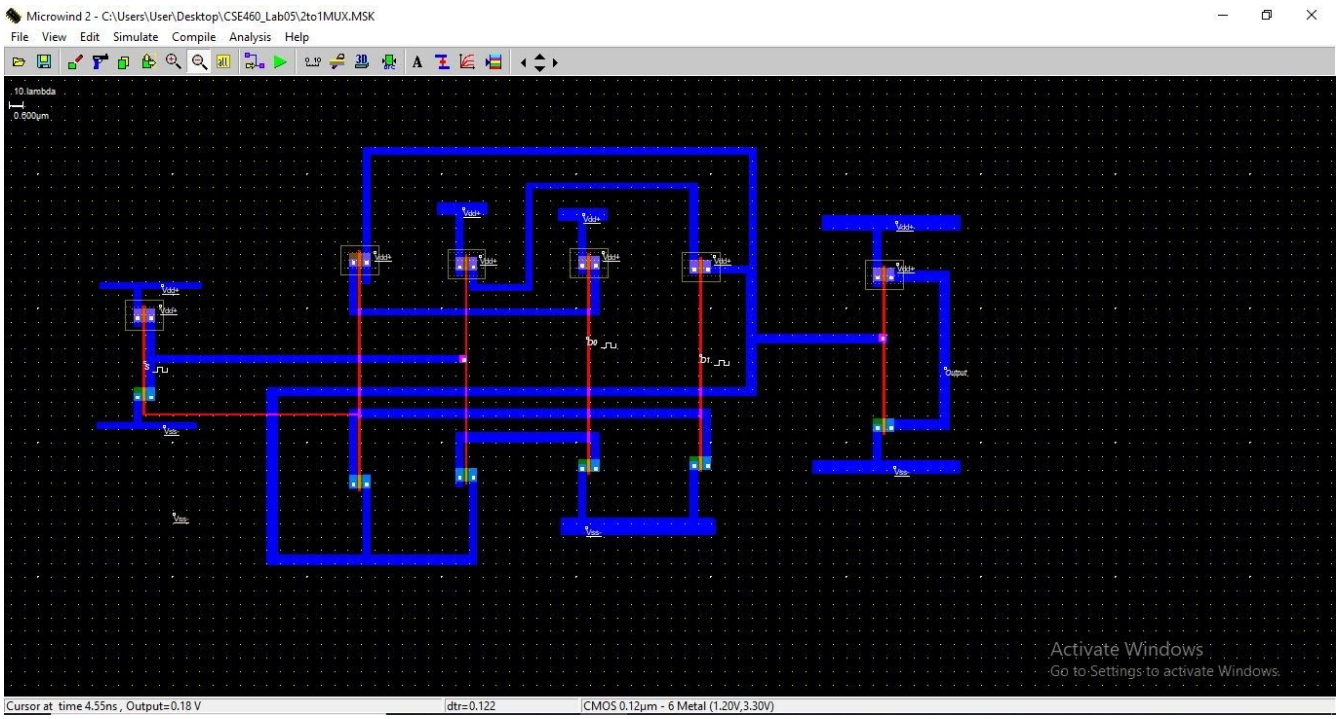


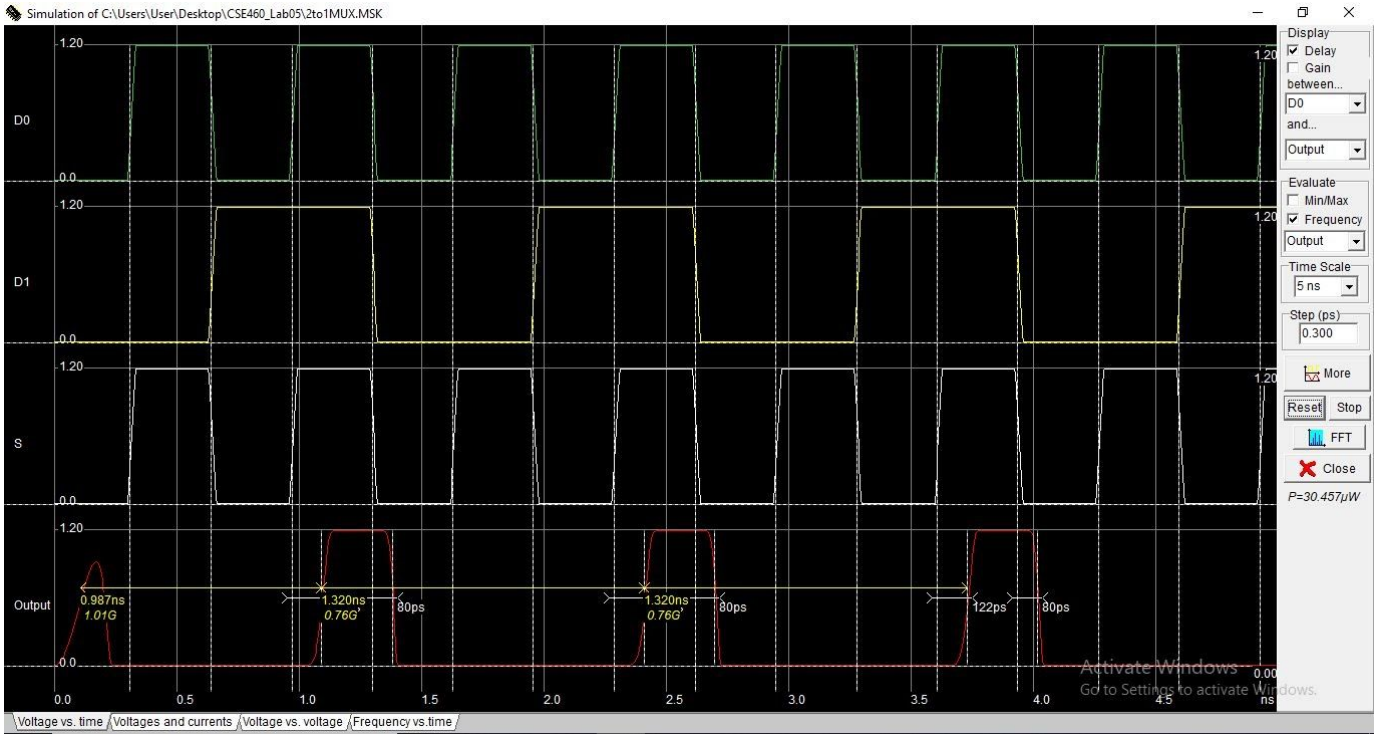


I have used inverter gates to get the inverted values of input A and B. From the simulation, it can be observed that the output will be low(0) when both of the inputs A and B are high(1). When all of the inputs are low(0), the output will be also low(0). The output will be only high(1) if one of the input is high(1) and the other input is low(0).

Answer to the Question No: 02

The layout of 2 to 1 MUX using CMOS has given below:

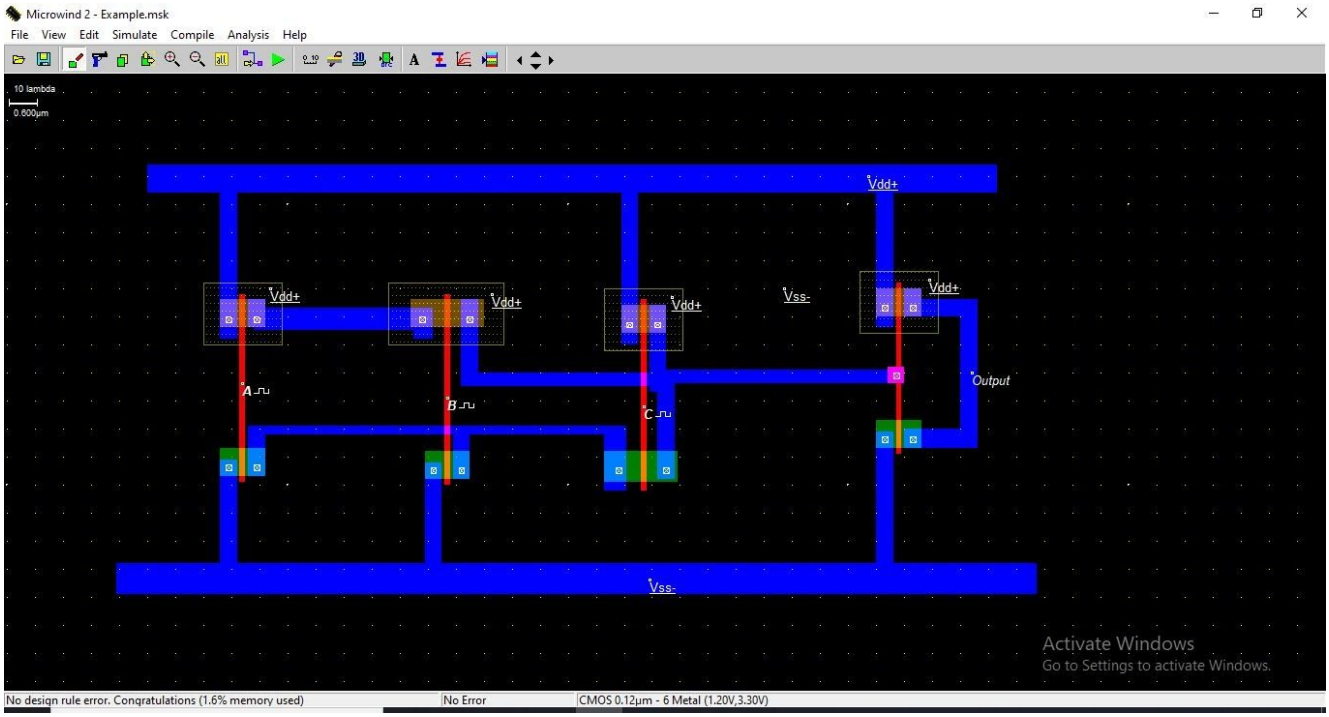


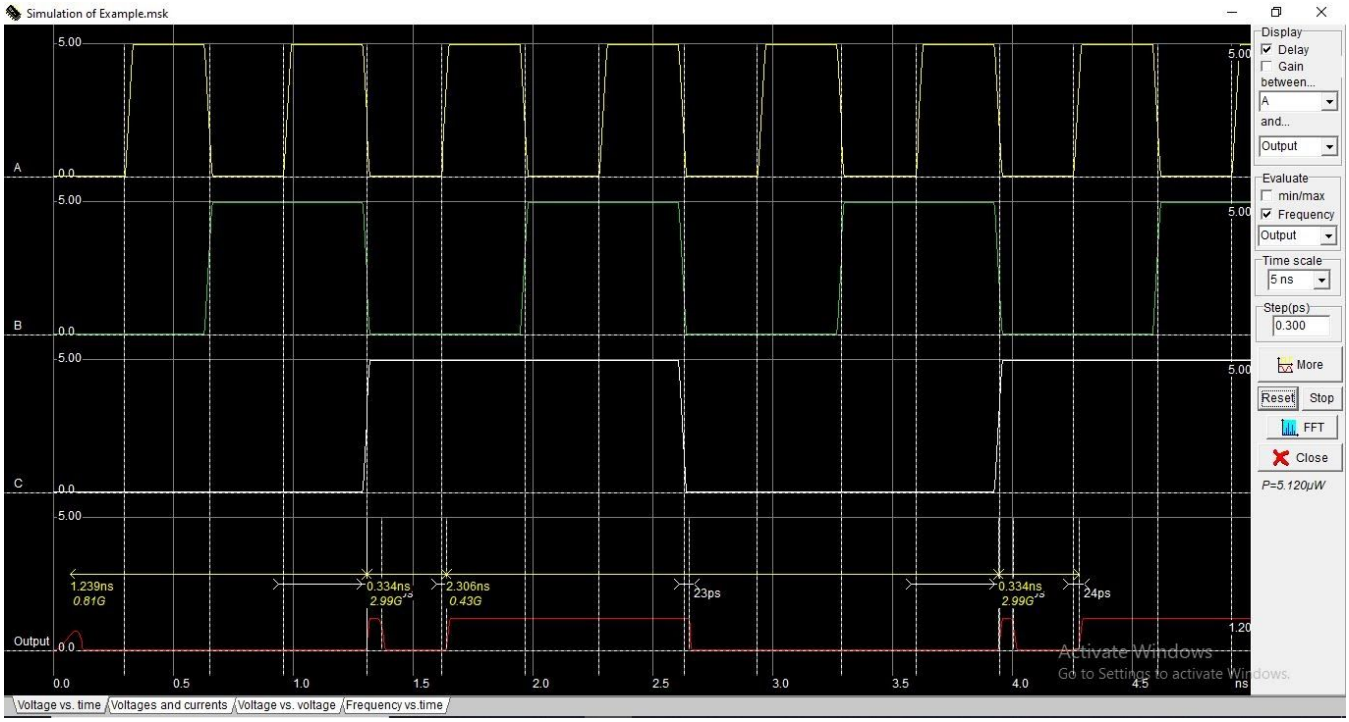


From the 2 to 1 MUX implementation, it can be observed from the simulation that the output depends on the selector pin S. The D0 and D1 are two input data pins. When the S is low(0) the output will be from D0 and when the S is high(1) the output will be from the D1. From the simulation, it can be seen that, when the S is low(0), the output is similar with the values of D0 and if D0 is low(0) the output will also be low(0) and if D0 is high(1) the output will also be high(1). Also, if the S is high, the output will be similar with the values of the D1.

Answer to the Question NO: 03:

The combinational circuit f=(A+B)C has given below:





From the circuit simulation, it can be observed that the output is high(1) when all of the inputs are high(1). When the input value of A is low(0) but the two other inputs B and C are high(1), the output will be high. Moreover, when the value of C is low(0) the output will be low(0) and the output will not depend on the values of A and B whether they are high(1) or low(0). If A and B both are high(1) but C is low(0), the output will be low(0). The output will also be low(0) if all of the three inputs are low(0).
