

# CSE460

## Lab Report 4

Section: 11

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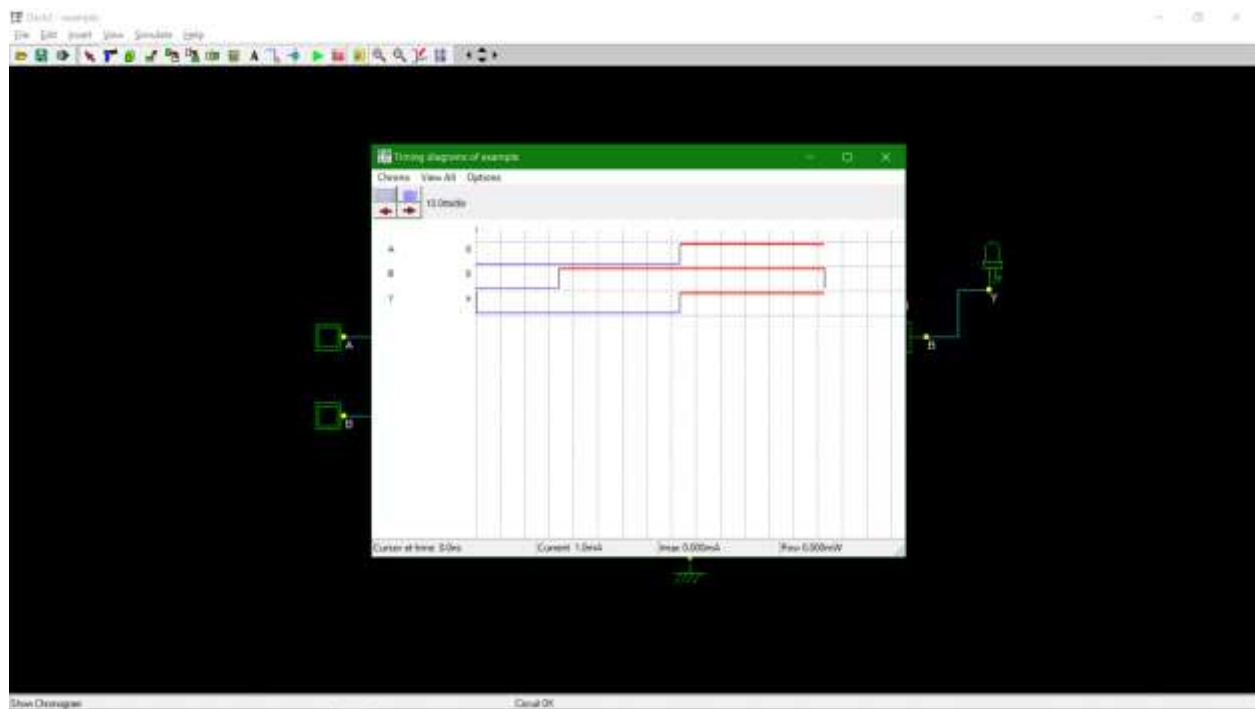
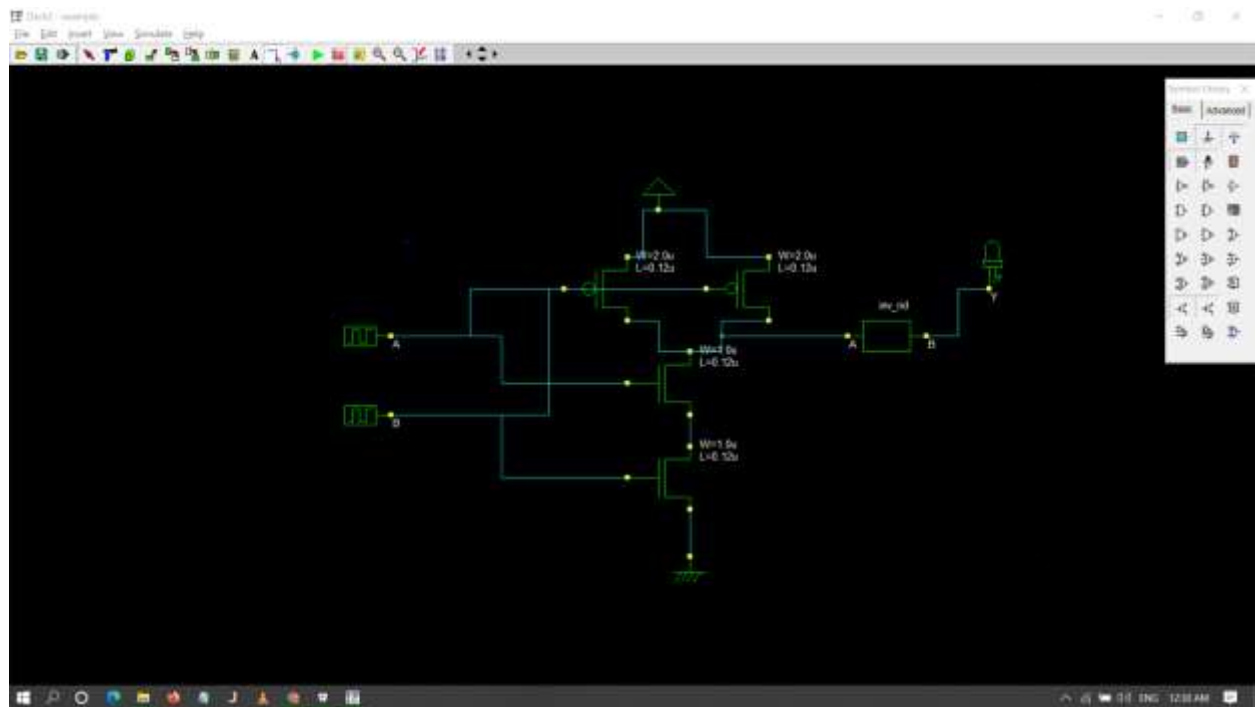


Inspiring Excellence

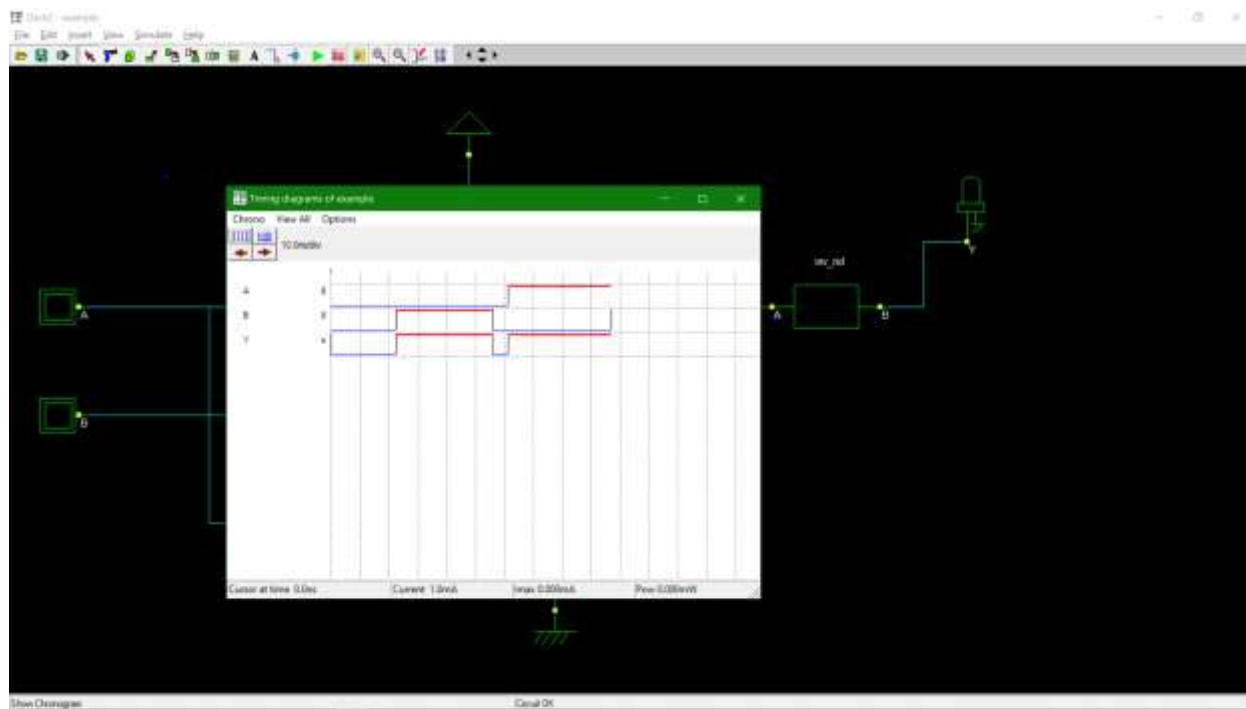
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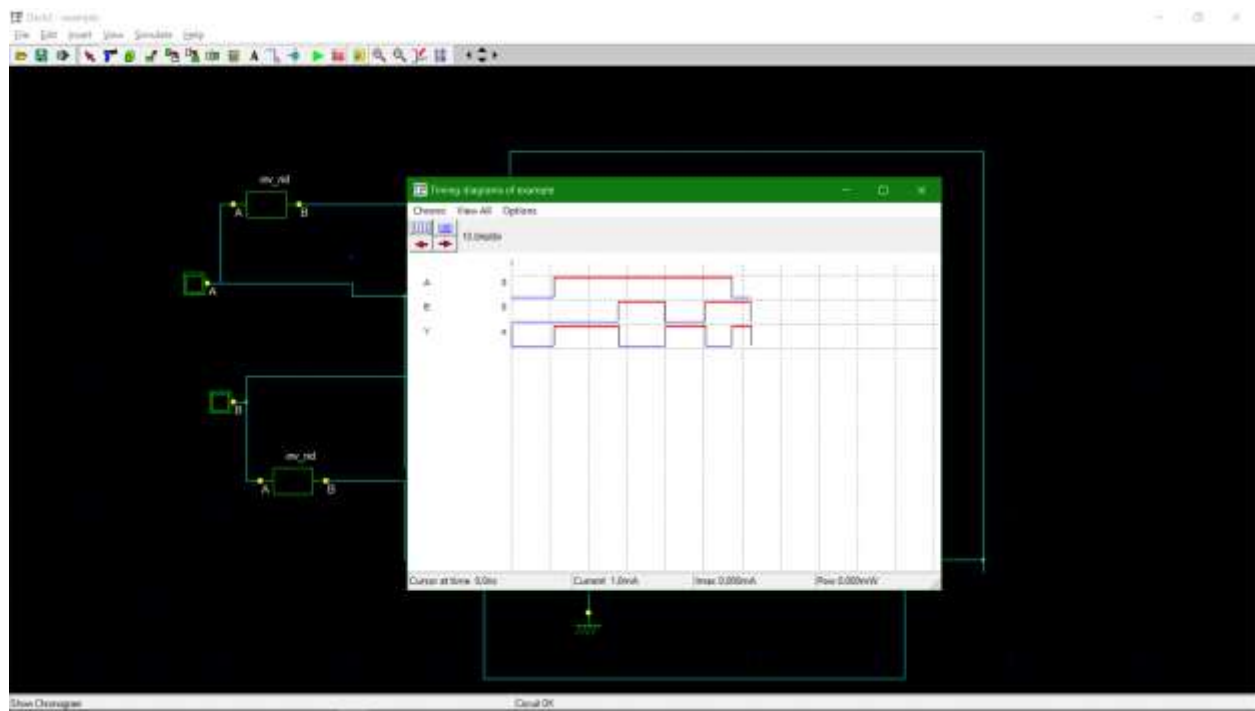
1.



2.



The top screenshot displays a circuit diagram in LTspice. It features two input signals, A and B, connected to a network of four transistors. Two NMOS transistors are in the first stage, with parameters  $W=2.5\mu$  and  $L=0.12\mu$ . Two PMOS transistors are in the second stage, with parameters  $W=1.5\mu$  and  $L=0.12\mu$ . The output of the second stage is connected to a load capacitor, and the output voltage is labeled V. The bottom screenshot shows the same circuit with a timing diagram overlay. The timing diagram displays the waveforms for inputs A and B, and the output voltage V. The waveforms for A and B are square waves, and the output voltage V shows a corresponding step response. The timing diagram includes a cursor at time 0.0ns, a current scale of 1.0mA, a time scale of 0.001ns, and a voltage scale of 0.001V.



The top screenshot displays a circuit schematic for a 4-to-1 multiplexer. The circuit is implemented using CMOS technology, with NMOS and PMOS transistors. The inputs are labeled A and B, and the output is labeled Y. The schematic includes a 200V voltage source and a 100pF capacitor. The transistors are labeled with their dimensions (W and L) and the gate voltage (V<sub>g</sub>). The circuit is connected to a 200V source and a 100pF capacitor.

The bottom screenshot shows the same circuit schematic with a timing diagram overlay. The timing diagram displays the waveforms for inputs A, B, and Y over time. The waveforms are labeled A, B, and Y, and the time axis is marked from 0 to 10.00ns. The timing diagram shows that the output Y follows the input A when B is high and follows the input B when A is high.

