University School of Automation and Robotics
GURU GOBIND SINGH INDRAPRASTHA UNIVERSITY
East Delhi Campus, Surajmal Vihar
Delhi - 110092

| **Paper Code:** ARI 209 | **L** | **T/P** | **Credits** |
|---|---|---|---|
| **Subject:** Switching theory and Logic Design | 4 | - | 4 |

**Marking Scheme**

1. Teachers Continuous Evaluation: 25 Marks
2. End Term Theory Examination: 75 Marks

**INSTRUCTIONS TO PAPER SETTERS:** **Maximum Marks : 75**

1. There should be 9 questions in the end term examination question paper
2. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 15 marks.
3. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 15 marks.
4. The questions are to be framed keeping in view the learning outcomes of course/paper. The standard/ level of the questions to be asked should be at the level of the prescribed textbooks.
5. The requirement of (scientific) calculators/ log-tables/ data-tables may be specified if required

**Course Outcomes:**

| | |
|---|---|
| **CO1:** | Ability of students to implement the fundamental concepts and techniques used in digital electronics along with design of flip flops, registers, counters and their applications as well as the design of digital circuits. |
| **CO2:** | Ability of students to be able to quantitatively identify the fundamentals of computers, including number systems, logic gates, logic and arithmetic subsystems, and integrated circuits. |
| **CO3:** | Ability of students to analyze logic processes and implement logical operations using combinational logic circuits and design sequential circuits |
| **CO4:** | Ability of students to utilize knowledge of different logic families and their characteristics along with the knowledge of different types of memories |

**Course Outcomes (CO) to Programme Outcomes (PO) Mapping** (Scale 1: Low, 2: Medium, 3: High

| CO/PO | PO01 | PO02 | PO03 | PO04 | PO05 | PO06 | PO07 | PO08 | PO09 | PO10 | PO11 | PO12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CO1 | 3 | 3 | 3 | 3 | 3 | - | - | - | 1 | 1 | 1 | 2 |
| CO2 | 3 | 3 | 3 | 3 | 3 | - | - | - | 1 | 1 | 1 | 2 |
| CO3 | 3 | 3 | 3 | 3 | 3 | - | - | - | 1 | 1 | 1 | 3 |
| CO4 | 3 | 3 | 3 | 3 | 3 | - | - | - | 1 | 1 | 1 | 3 |

**Unit I** **[14]**

**Number Systems and Codes:** Decimal, Binary, Octal and Hexadecimal Number systems, Codes- BCD, Gray Code, Excess-3 Code, ASCII, EBCDIC, Conversion between various Codes.

**Switching Theory:** Boolean Algebra- Postulates and Theorems, De' Morgan's Theorem, Switching Functions Canonical Forms- Simplification of Switching Functions- Karnaugh Map and Quine Mc-Clusky Methods.

**Combinational Logic Circuits:** Review of basic gates- Universal gates, Adder, Subtractor, Serial Adder, Parallel Adder- Carry Propagate Adder, Carry Look-ahead Adder, Carry Save Adder, Comparators, Parity Generators, Decoder and Encoder, Multiplexer and De-multiplexer, ALU, PLA and PAL.

**Unit II** **[10]**

**Sequential Logic Circuits:** Latches and Flip Flops- SR, D, T and MS-JK Flip Flops,

Prof. Ajay S. Singholi
Professor In-charge, USAR
Guru Gobind Singh Indraprastha University
(East Delhi Campus)
Surajmal Vihar, Delhi-110092

Asynchronous Inputs.

**Counters and Shift Registers:** Design of Synchronous and Asynchronous Counters- Binary, BCD, Decade and Up/Down Counters, Shift Registers, Types of Shift Registers, Counters using Shift Registers- Ring Counter and Johnson Counter.

**Unit III** [8]

**Integrated circuits:** TTL and CMOS logic families and their characteristics. Brief introduction to RAM and ROM

**Synchronous Sequential Circuits**: State Tables State Equations and State Diagrams, State Reduction and State Assignment, Design of Clocked Sequential Circuits using State Equations.

**Unit IV** [6]

**Finite state machine**: capabilities and limitations, Mealy and Moore models-minimization of completely specified and incompletely specified sequential machines, Partition techniques and merger chart methods, concept of minimal cover table.

**Algorithmic State Machine:** Representation of sequential circuits using ASM charts synthesis of output and next state functions, Data path control path partition-based design.

**Text Books:**

1. Leach and Malvino (2011). *Digital principles and Applications*. Tata McGraw-Hill Education
2. Mano, M. M. (2017). *Digital logic and computer design*. Pearson Education India.
3. Jain, R. P. (2003). *Modern digital electronics*. Tata McGraw-Hill Education.

**Reference Books:**

1. A Anand Kumar. (2016) *Fundamentals of Digital Logic Circuits*, PHI
2. Taub, H., & Schilling, D. L. (1977). *Digital integrated electronics*. McGraw-Hill College.

Prof. Ajay S. Singholi
Professor In-charge, USAR
Guru Gobind Singh Indraprastha University
(East Delhi Campus)
Surajmal Vihar, Delhi-110092