

# **Homework 1**

EE330 - Analog Electronics

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(SETA)

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# 1 Circuit Design

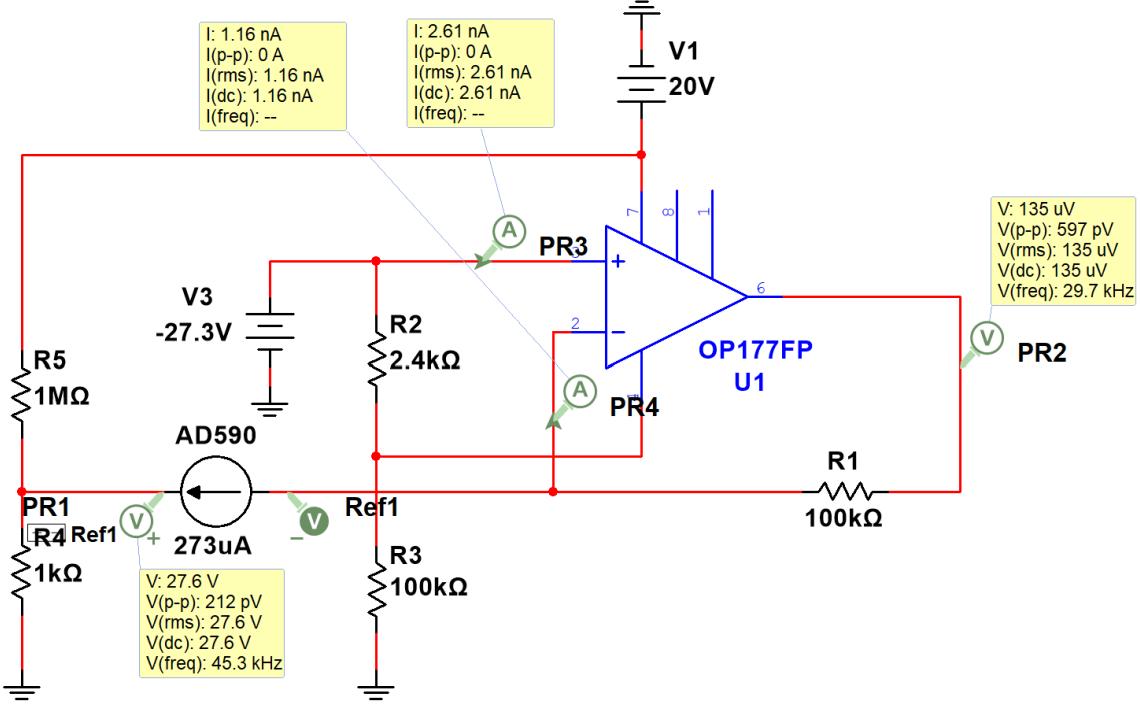


Figure 1: Sensor Interfacing Circuit

The AD590 produces a current proportional to the absolute temperature at a rate of  $1\mu\text{A}/\text{K}$ . Therefore, the current at  $0^\circ\text{C}$  is  $273\mu\text{A}$  and at  $50^\circ\text{C}$  is  $323\mu\text{A}$ .

We use superposition to analyze the output of this circuit. Deactivating the AD590 sensor, we see a voltage follower configuration with  $-27.3\text{V}$  at the non-inverting input. Therefore,  $V_o = -27.3\text{V}$ .

Now, considering the negative voltage reference at the non-inverting input deactivated, we have a transresistance amplifier. Then  $V_o = 100\text{k}\Omega \cdot I_S$ , where  $I_S$  is the current output from the AD590 sensor. Using superposition, we know that,

$$V_o = 100\text{k}\Omega \cdot I_S - 27.3\text{V}.$$

At 0°C,

$$V_o = 100\text{k}\Omega \cdot 273\mu\text{A} - 27.3\text{V} = 0\text{V}.$$

And at 50°C,

$$V_o = 100\text{k}\Omega \cdot 323\mu\text{A} - 27.3\text{V} = 5\text{V}.$$

Figure 1 verifies that the voltage across the AD590 is within the operating conditions of the sensor (4 – 30V). At  $323\mu\text{A}$ , the voltage across the AD590 is 27.7V. This was also verified via simulation.

## 2 Op Amp Choice

I chose the OP177F op-amp for this circuit due to its low offset voltage and low input bias/offset currents.

The following circuit was used to measure the input offset voltage for the OP177F op-amp using a sweep simulation.

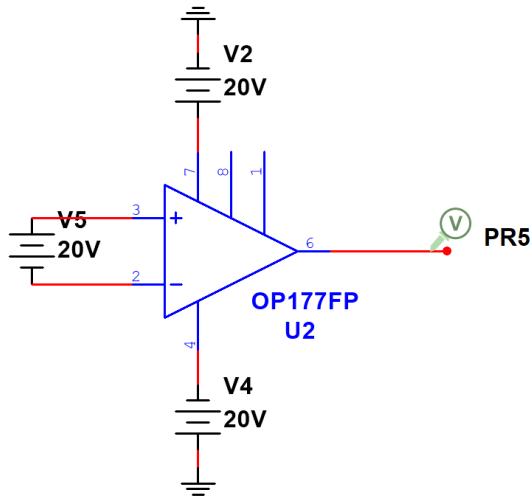


Figure 2: OP177F Voltage Offset Simulation Circuit

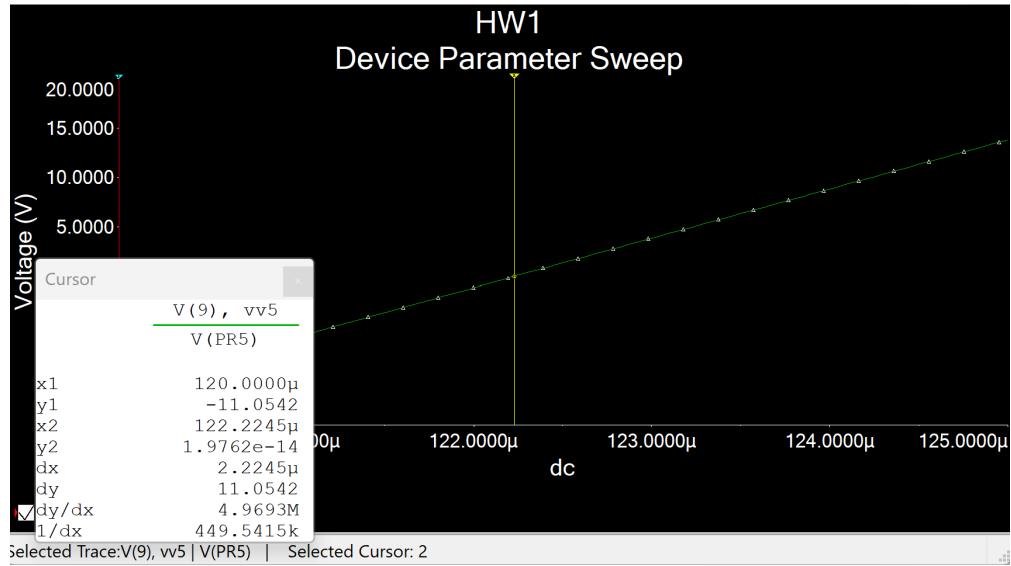


Figure 3: OP177F Voltage Offset Simulation Results

Simulation results indicate that the input offset voltage is about  $122\mu\text{V}$ . Figure 1 shows input bias currents of  $1.16\text{nA}$  and  $2.61\text{nA}$ . Thus, the simulation is accounting for these non-idealities, and explicit models do not need to be added.

# 3 Monte Carlo Simulations

## 3.1 Before Accounting for Non-idealities

After completing a Monte Carlo simulation for this circuit with 1% resistor values at 0°C, the mean output value was  $354.569\mu\text{V}$  with a standard deviation of 90mV. Going out to  $3\sigma$ , at 0°C, we expect our output to be between  $-270\text{mV}$  and  $270\text{mV}$ .

HW1 Monte Carlo Analysis					
	# of runs	time (s)	output value	sigma	parameters
1	V(PR2), Nominal Run		134.58595		
2	V(PR2), Run #1	87.49496 m			
3	V(PR2), Run #2	134.99712			
4	V(PR2), Run #3	80.78294 m			
5	V(PR2), Run #4	134.31815 m			
6	V(PR2), Run #5	17.06066 m			
7	V(PR2), Run #6	134.70063 m			
8	V(PR2), Run #7	155.84104 m			
9	V(PR2), Run #8	101.41800 m			
10	V(PR2), Run #9	261.86458 m			
11	V(PR2), Run #1	24.46281 m			
					Run Log Descriptions
1	Nominal Run (Mean: 0.00035459, Standard Deviation: 0.0900)	0.000134586 (same as nominal, lower than mean by -0.000219 4983)	0.002443	r4 resistance=1000	
2				r1 resistance=100000	
3				r2 resistance=2400	
4				r3 resistance=100000	
5				r5 resistance=1e+06	
6	Run #1	0.087495 (64910.5% higher than 0.567889)		r4 resistance=1001.45	
7				r1 resistance=100320	
8				r2 resistance=2404.09	
9				r3 resistance=99857.4	
10				r5 resistance=1.00066e+06	
11	Run #2	0.134997 (100206% higher than 1.49551)		r4 resistance=995.729	
12				r1 resistance=100494	
13				r2 resistance=2398.48	
14				r3 resistance=100432	

Figure 4: Monte Carlo Simulation Results - 0°C

After completing a Monte Carlo simulation for this circuit with 1% resistor values at 50°C, the mean output value was 4.99375V with a standard deviation of 0.112248V. Going out to  $3\sigma$ , at 50°C, we expect our output to be between 4.66V and 5.33V.

HW1 Monte Carlo Analysis				
Run Log Descriptions				
# of run	time (s)	output value	sigma	parameters
1	Nominal Run (Mean: 1.99375, Standard Deviation: 0.11248)	5.00013 (same as nominal, higher than mean by 0.00638415)	0.056875	r1 resistance=1000
2				r11 resistance=100000
3				r2 resistance=2400
4				r22 resistance=100000
5				r3 resistance=1e+06
6	Run #1	4.98696 (0.263562% lower than nominal)	0.060529	r4 resistance=999.497
7				r11 resistance=9999.2
8				r2 resistance=405.62
9				r22 resistance=100040
10				r3 resistance=1.00186e+06
11	Run #2	4.88208 (2.36107% lower than nominal)	0.994876	r4 resistance=1002.02
12				r11 resistance=99634.5
13				r2 resistance=2398.92
14				r22 resistance=99487.9

Figure 5: Monte Carlo Simulation Results - 50°C

### 3.2 Accounting for Non-idealities

To account for input bias current, a resistor was added to the non-inverting input of the OP177F op-amp. The optimal resistor value was identified using a sweep simulation, such that the output voltage would be 0V at an AD590 current of  $273\mu\text{A}$ . The update circuit is below.

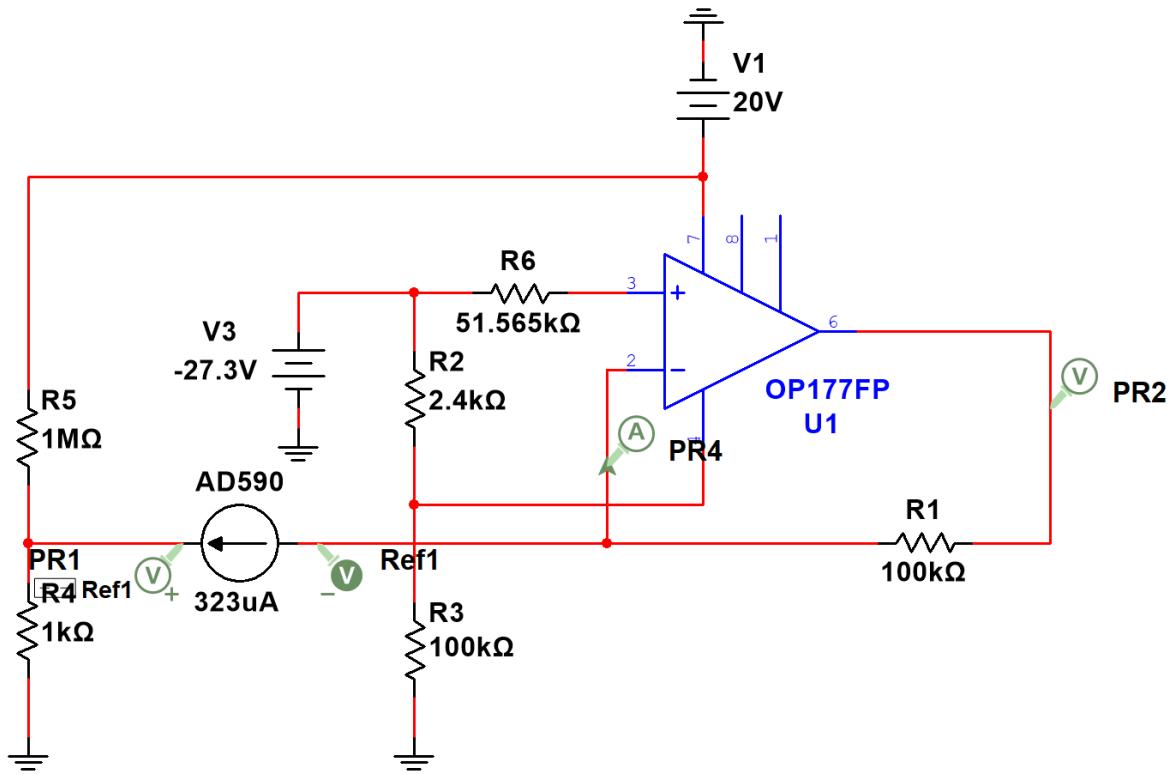


Figure 6: Updated Circuit to Account for Non-idealities

After completing a Monte Carlo simulation for this circuit with 1% resistor values at 0°C, the mean output value was 1.90105mV with a standard deviation of 92.98mV. Going out to  $3\sigma$ , at 0°C, we expect our output to be between -277mV and 280mV. This is slightly worse than the original circuit.

Run Log Descriptions				
# of run	time (s)	output value	sigma	parameters
1 Nominal Run (Mean: 0.00190105, Standard Deviation: 0.05298)		L61598e-08 (Same as nominal, lower than mean by -0.00190107)	0.020445	r44 resistance=1000
2				r11 resistance=100000
3				r22 resistance=2400
4				r33 resistance=100000
5				r55 resistance=1e+05
6 Run #1	-0.0994545 (6.15482e+08% low) 1.09008			r44 resistance=995.94
7				r11 resistance=99635.7
8				r22 resistance=2419.14
9				r33 resistance=99508.5
10				r55 resistance=99727.2
11 Run #2	0.0251161 (1.55433e+08% high) 0.249677			r44 resistance=999.559
12				r11 resistance=100092
13				r22 resistance=2394.75
				r33 resistance=999.559

Figure 7: Monte Carlo Simulation Results - 0°C - Account for Non-idealities

After completing a Monte Carlo simulation for this circuit with 1% resistor values at 50°C, the mean output value was 5.00079V with a standard deviation of 0.108457V. Going out to  $3\sigma$ , at 50°C, we expect our output to be between 4.68V and 5.33V. This is slightly better than the original circuit.

HW1 Monte Carlo Analysis			
#	Run #	Value	Sigma
875	V(PR2), Run #8	4.75394	
	r1	7.41	
876	V(PR2), Run #8	5.04813	
	r2	7.5	
877	V(PR2), Run #8	5.13437	
	r3	7.6	
878	V(PR2), Run #8	5.04910	
	r4	7.8	
879	V(PR2), Run #8	4.87335	
	r5	7.8	
880	V(PR2), Run #8	4.91137	
	r6	7.9	
881	V(PR2), Run #8	4.98104	
	r7	8.0	
882	V(PR2), Run #8	5.00129	
	r8	8.1	
883	V(PR2), Run #8	5.18023	
	r9	8.2	
884	V(PR2), Run #8	4.96166	
	r10	8.3	
885	V(PR2), Run #8	5.07138	
	r11	8.4	

Figure 8: Monte Carlo Simulation Results - 50°C - Account for Non-idealities

The OP177F op-amp is a high precision op-amp with very minimal offset voltage and input bias current. Because of this, our circuit only performs marginally better when accounting for these non-idealities, and we likely would be okay without accounting for them.

	0°C	50°C
3 $\sigma$ lowest	-277mV	4.68V
3 $\sigma$ highest	280mV	5.33V

Table 1: Summarized Results of Monte Carlo Simulations - Accounting for Non-idealities

# **Homework 2**

EE330 - Analog Electronics

Dillon Labonte

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(SETA)

Submitted: February 2025

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(NOTE: I have met all specs and considered all non-idealities, other than only having one voltage source. I was unable to make one voltage source work, and would require more time to go to office hours and/or research which I do not have.)

# 1 Triangle Wave Generator

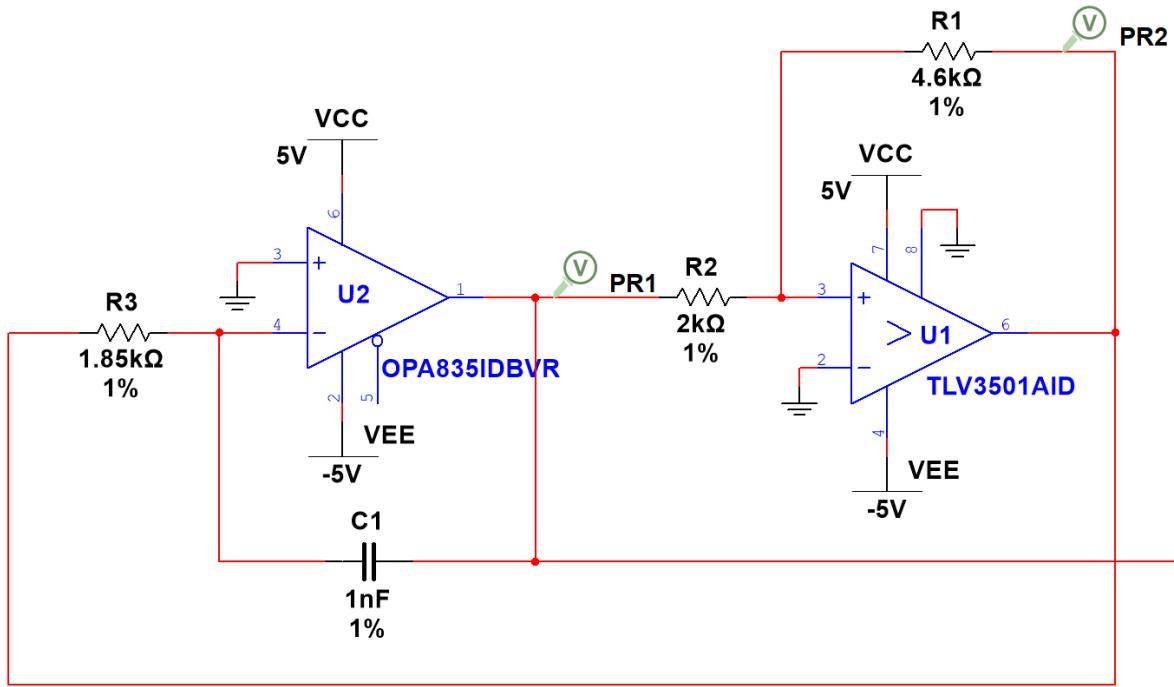


Figure 1: Triangle Wave Generator Circuit

Figure 1 shows a circuit that produces a 300kHz triangle wave at voltage probe 1. It is composed of an integrator op-amp circuit (left side, with OPA835) and a Schmitt Trigger (right side, with TLV3501). The OPA835 op-amp was chosen for its high slew rate (needed for 300kHz wave), and minimal voltage offset and input bias currents. Similarly, the TLV3501 comparator

was chosen due to its high speed operation and minimal offset voltage and input bias currents.

## 1.1 Schmitt Trigger

The Schmitt trigger operates with hysteresis, producing two outputs close to  $VCC$  or  $-VEE$ . The thresholds were designed to be at  $\pm 2V$ , however since the comparator is not exactly rail to rail, the resistor values in the positive feedback loop were manually adjusted until threshold voltages were correct. This resulted in the values of  $2k\Omega$  and  $4.6k\Omega$ , as seen in figure 1.

## 1.2 Integrator

The integrator circuit uses the output of the Schmitt Trigger as an input, and utilizes a resistor and capacitor in negative feedback to integrate the input. This creates a ramp, which is fed back to the Schmitt Trigger. Once the output of the integrator has reached  $\pm 2V$ , the Schmitt Trigger will flip to its other state and invert the ramp output of the integrator.

The  $RC$  time constant of the integrator circuit was designed such that it would provide a  $4V$  swing from  $-2V \rightarrow 2V$  in  $1.67\mu s$ . This is half the period for a  $300kHz$  wave. The other half would come from the ramp being inverted, therefore producing a period of  $3.34\mu s$ , and a frequency of  $300kHz$ . The values for  $R$  and  $C$  were originally calculated by hand, and then adjusted manually to account for nonidealities. The result was,

$$R = 1.85k\Omega,$$

$$C = 1\text{nF}.$$

The resulting triangle wave is seen below in figure 2.

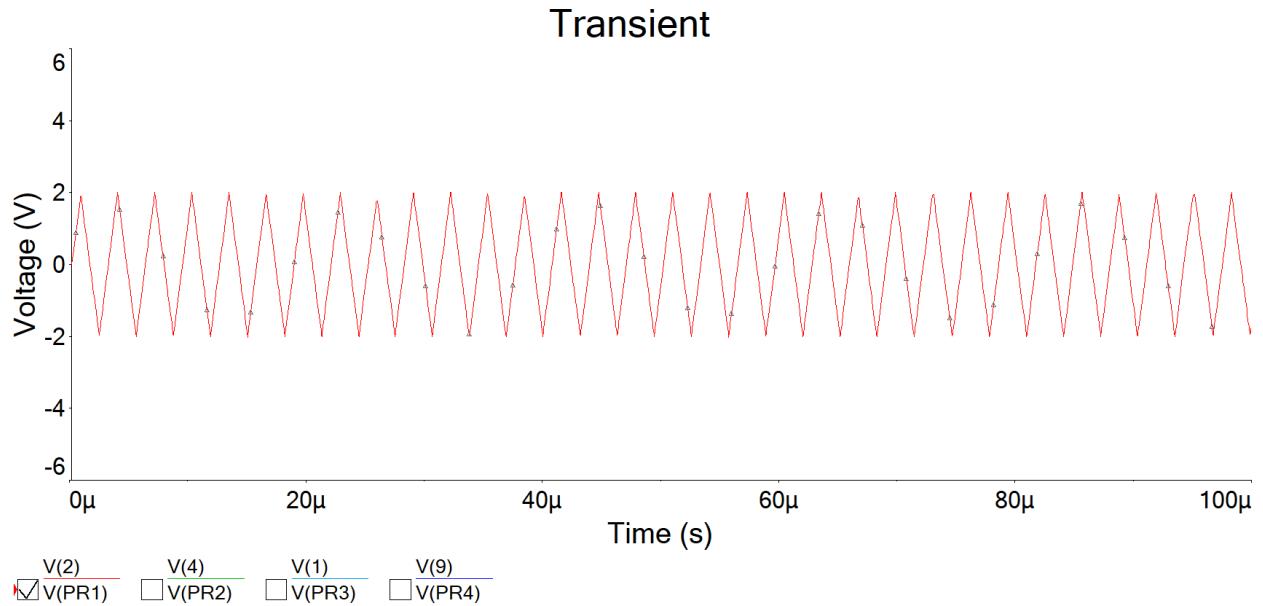


Figure 2: Triangle Wave Output

Now that a triangle wave of the desired frequency was produced, this was fed as an input to the next section of the circuit.

## 2 Voltage Correction

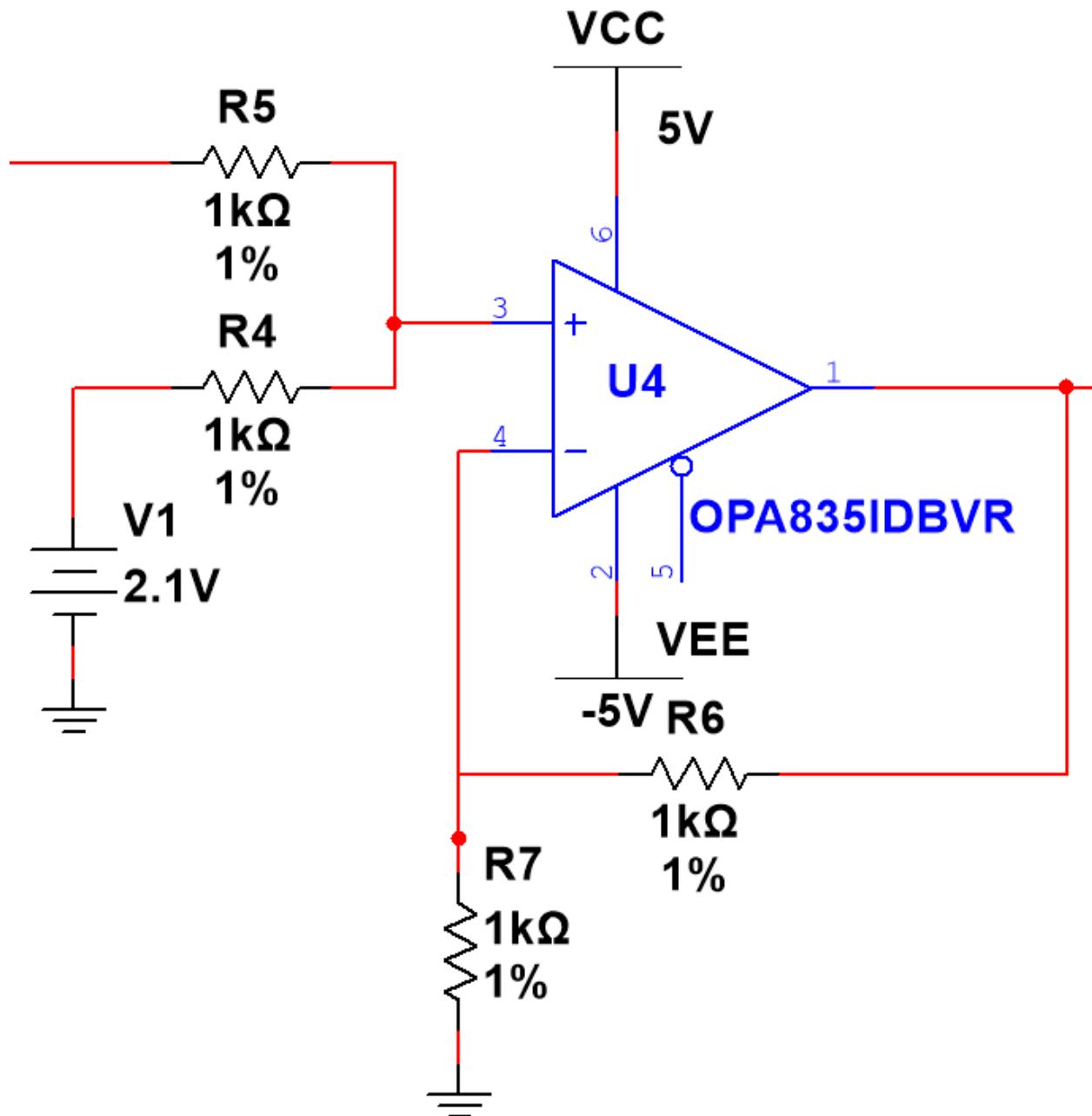


Figure 3: Voltage Correction Circuit

Figure 3 depicts a noninverting summing amplifier used to correct our signal. The eventual input to our comparator is in the range of 0–4V, so the triangle wave should match this. The summing amplifier is designed to have a gain of 1 for each input signal, thus the output is truly the sum of the two inputs.

The resulting triangle wave, compared to the original, is seen below in figure 4.

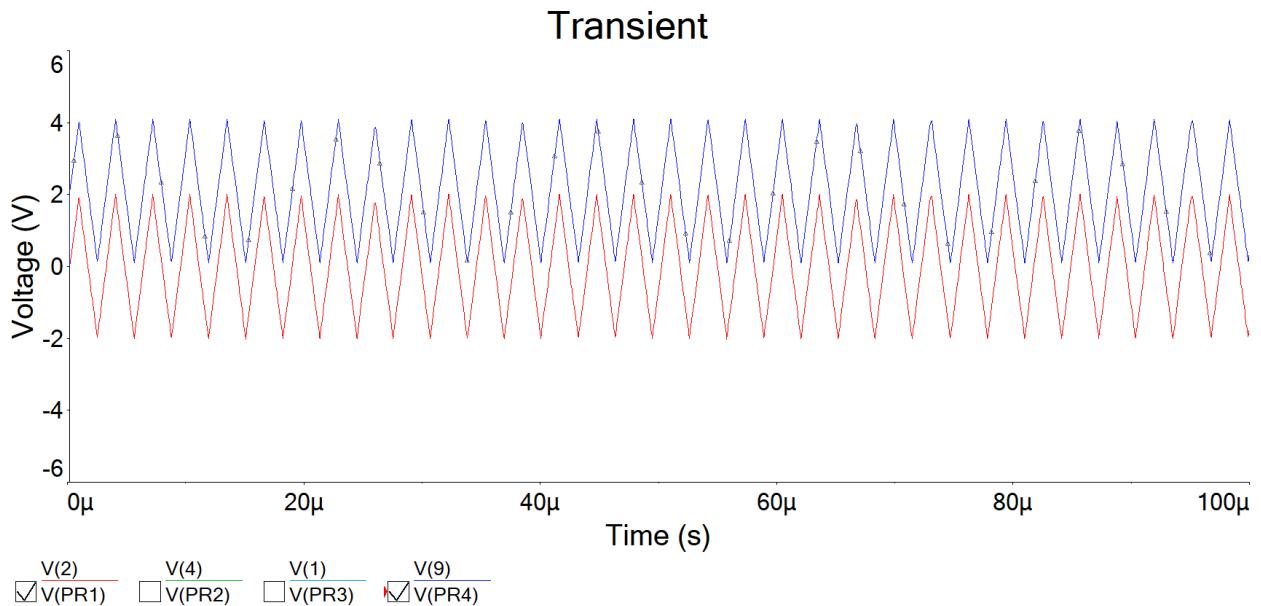


Figure 4: Corrected Triangle Wave Output

The red waveform shows the original triangle wave, and the blue waveform shows the corrected triangle wave, shifted up to the proper range.

Now that the triangle wave is in the proper range, we can feed it into the next part of the circuit.

### 3 Comparator Generating PWM

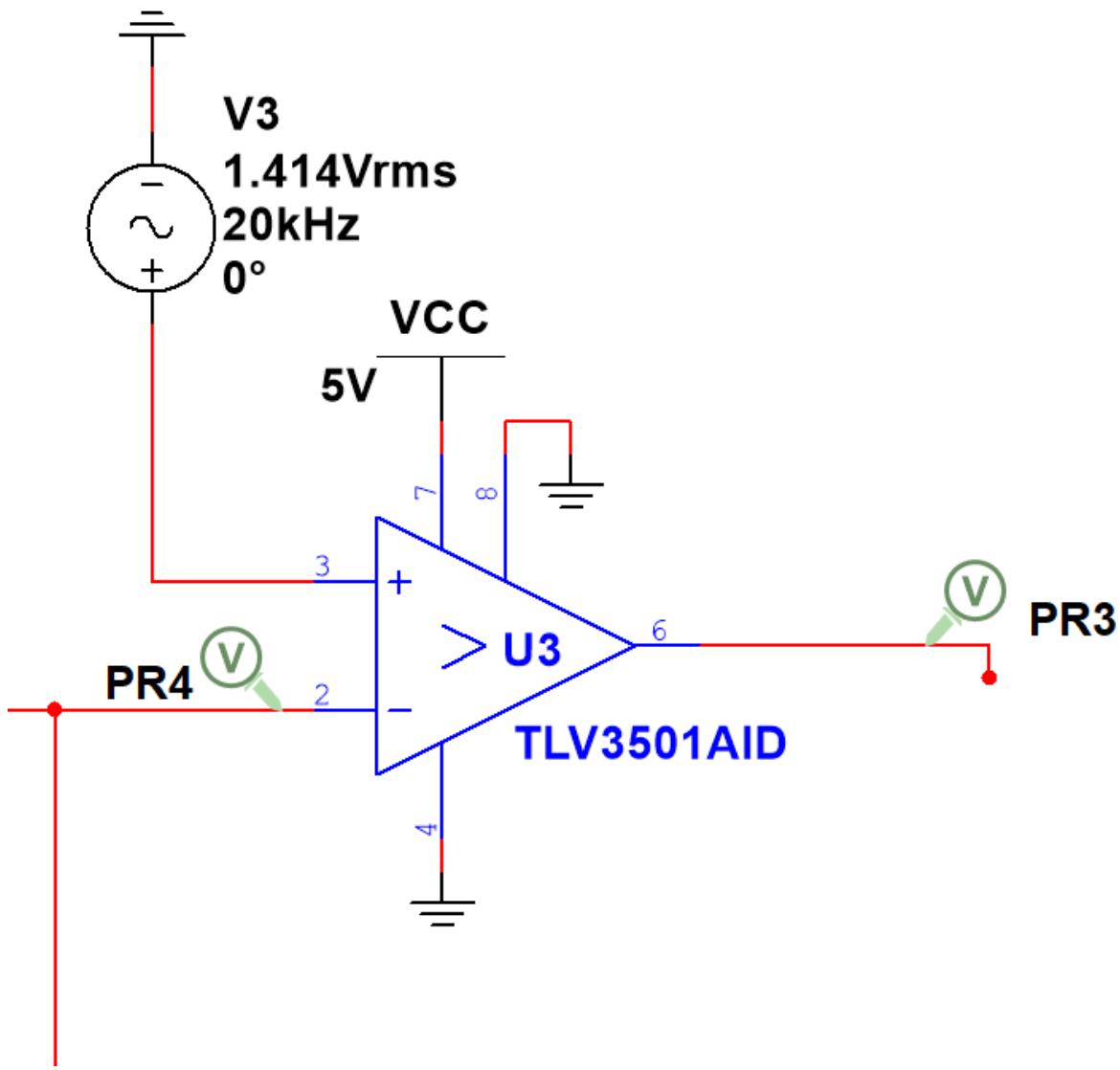


Figure 5: Comparator Circuit to Generate PWM

The circuit above in figure 5 shows a comparator circuit used to generate a PWM output at voltage probe 3. The corrected triangle wave from the previous step in the circuit is used as the input at the inverting terminal of the comparator. The input to our circuit is connected to the noninverting

terminal. While the input voltage is higher than the triangle wave, the comparator will output a high value (5V). When the input voltage is lower than the triangle wave, the comparator will output a low value (0V). Using a sinusoidal input, we can see the PWM output across the entire input voltage range. This is seen below in figure 6.

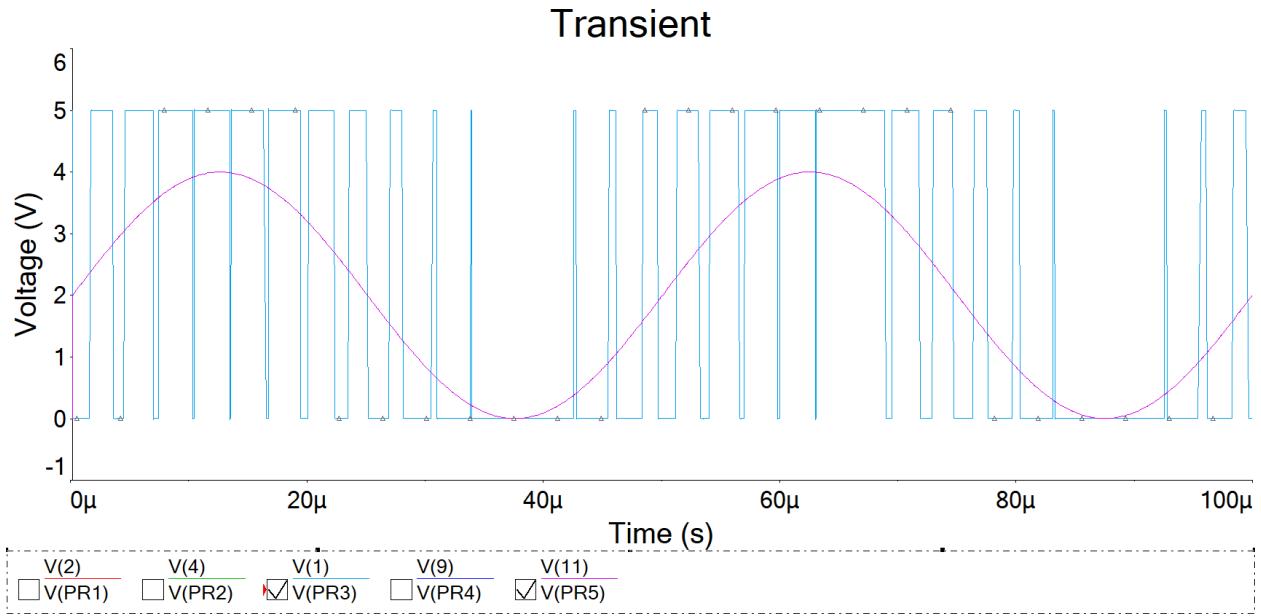


Figure 6: PWM Output for Sinusoid Input

The purple waveform depicts the input sinusoid, and the blue waveform depicts the output PWM signal. We see that when the input signal is higher, we have a larger duty cycle, and when the signal is lower, we have a shorter duty cycle.

The following image shows the PWM output when a constant 2V input is applied.

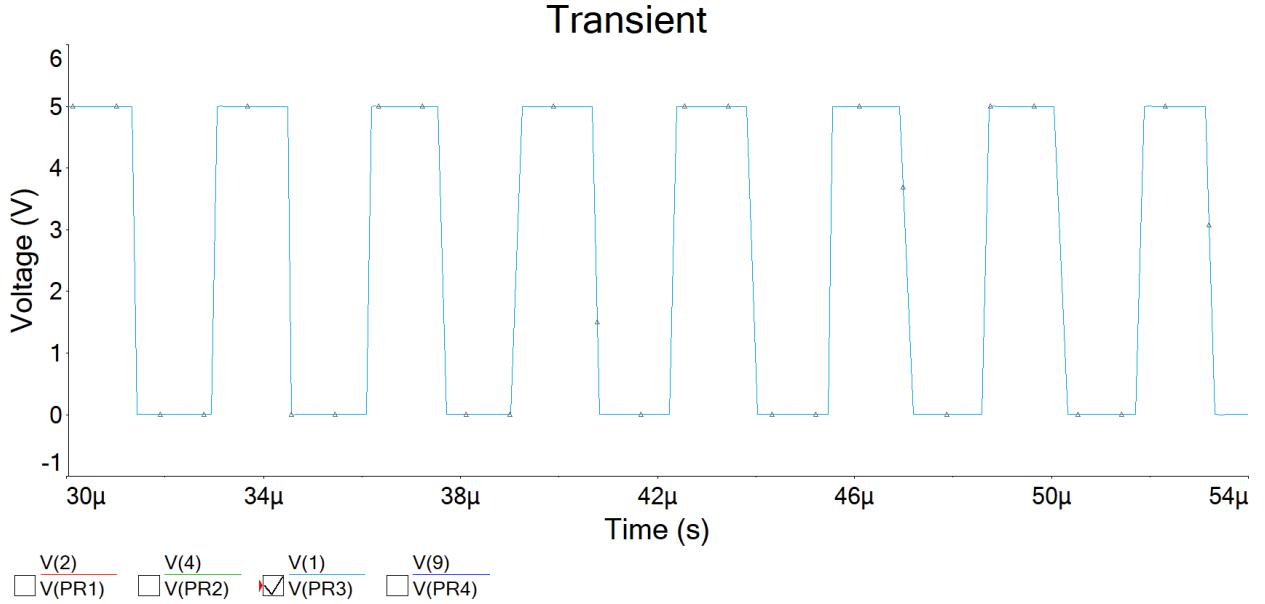


Figure 7: PWM Output for 2V Input

Using the Multisim cursors, the duty cycle of this waveform is measured to be about 50.4%. Compared to the expected 50% duty cycle for a 2V input, this is well within spec of  $\pm 5\%$ .

## 4 Component Tolerances

### 4.1 Triangle Wave Generator

This section explores the use of 1% tolerances for the resistors and capacitors in the triangle wave generating circuit. We will use the worst case to determine the effects on a PWM signal for a 2V input.

The resistor and capacitor of the integrator circuit will affect the frequency of our triangle wave. The worst case arises when they are both 1% higher or 1% lower.

When both resistor and capacitor are 1% higher, we measure a triangle wave frequency of 312kHz.

When both resistor and capacitor are 1% lower, we measure a triangle wave frequency of 325kHz.

The worst case for the Schmitt Trigger arises when the two resistors in the feedback path have errors in different directions. Meaning, if one resistor is 1% higher, and the other is 1% lower, we will get the worst case. This arises from the equations for the threshold voltages.

When the  $4.6\text{k}\Omega$  resistor is 1% higher and the  $2\text{k}\Omega$  resistor is 1% lower, our triangle wave output changes to  $-1.95\text{V} \rightarrow 1.97\text{V}$ .

When the  $4.6\text{k}\Omega$  resistor is 1% lower and the  $2\text{k}\Omega$  resistor is 1% higher, our triangle wave output changes to  $-2.03\text{V} \rightarrow 2.03\text{V}$ .

## 4.2 Voltage Correction

The worst case for the voltage generation circuit is when the two feedback resistors are wrong in different directions, and the input resistors are wrong in the same direction.

When the input resistors are both 1% higher, the feedback resistor is 1% higher, and the resistor to ground is 1% lower, the corrected triangle wave has a range of  $0.10\text{V} \rightarrow 4.09\text{V}$ .

When the input resistors are both 1% higher, the feedback resistor is 1% lower, and the resistor to ground is 1% higher, the corrected triangle wave has a range of  $0.16\text{V} \rightarrow 4.05\text{V}$ .

When the input resistors are both 1% lower, the feedback resistor is 1% higher, and the resistor to ground is 1% lower, the corrected triangle wave

has a range of  $0.12V \rightarrow 4.11V$ .

When the input resistors are both 1% lower, the feedback resistor is 1% lower, and the resistor to ground is 1% higher, the corrected triangle wave has a range of  $0.11V \rightarrow 4.05V$ .

### 4.3 Total Circuit With Worst Case

The comparator circuit does not have any passive components, thus we have covered all the circuits that do and their worst cases. Note that we will also not consider the affect of the  $RC$  error in the integrator circuit, as this only affects the frequency of our signals throughout the circuit. Any error in frequency is well within the slew rate limitations of the chosen op-amps and comparators.

We want to consider when the triangle wave generator produces a wave that is too high in amplitude, with the voltage correction circuit that also increases the amplitude of the triangle wave.

This configuration arises when the  $4.6k\Omega$  resistor is 1% lower, the  $2k\Omega$  resistor is 1% higher, the input resistances to the summing amplifier are 1% higher, the feedback resistor is 1% lower, and the resistor to ground is 1% higher. The output of this configuration when a sinusoidal input is applied is seen below in figure 8.

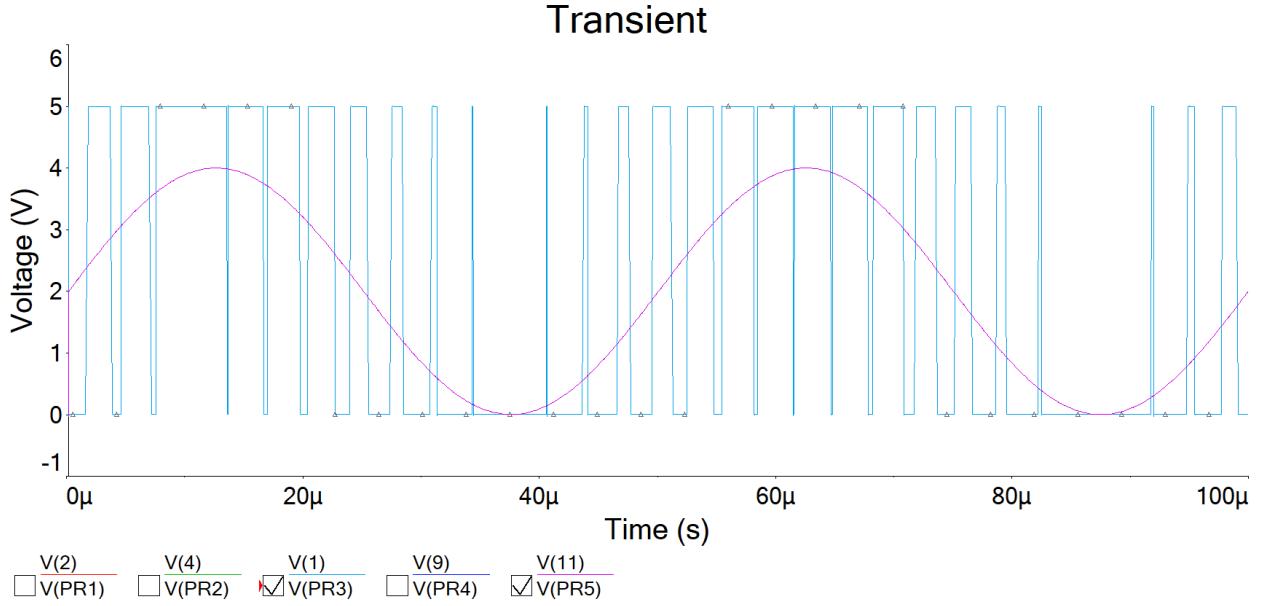


Figure 8: High Worst Case Output

This produces a good output, indicating that this worst case does not affect our PWM output substantially.

We now want to consider when the triangle wave generator produces a wave that is too low in amplitude, with the voltage correction circuit that also decreases the amplitude of the triangle wave.

This configuration arises when the  $4.6k\Omega$  resistor is 1% higher, the  $2k\Omega$  resistor is 1% lower, the input resistances to the summing amplifier are 1% lower, the feedback resistor is 1% lower, and the resistor to ground is 1% higher. The output of this configuration when a sinusoidal input is applied is seen below in figure 9.

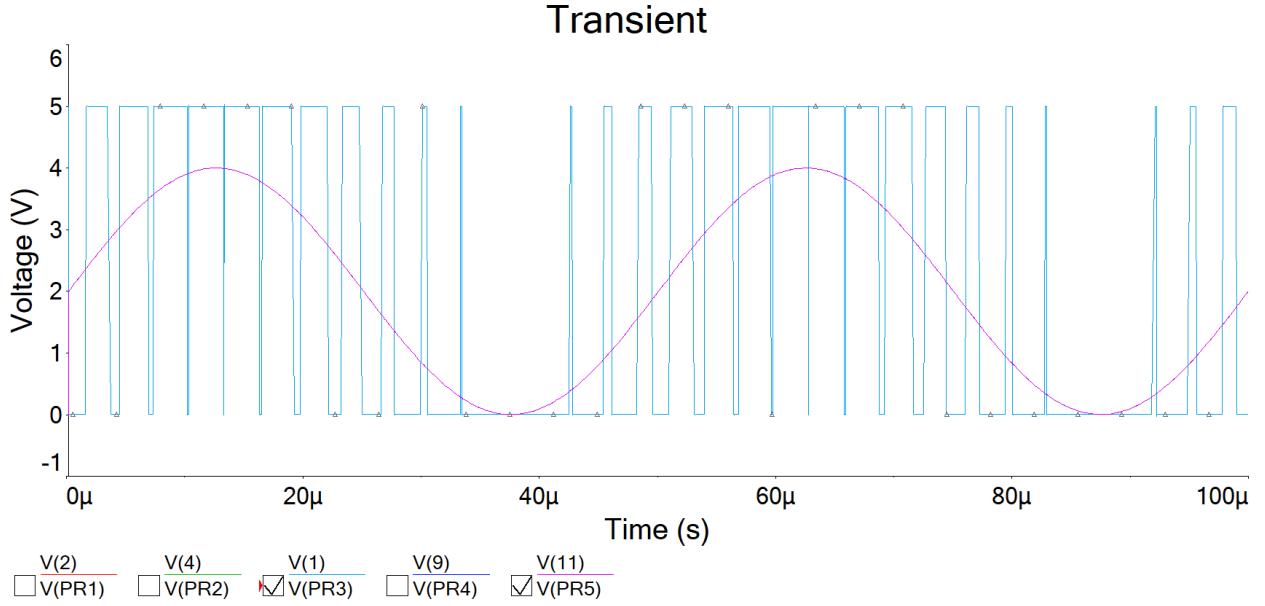


Figure 9: Low Worst Case Output

Again, we see a good output. From both of these results, we conclude that passive component tolerances do not substantially impact our PWM generator circuit. This is likely due to corrections made in earlier steps of the design process, specifically in the voltage correction circuit where a 2.1V source is added to the triangle wave rather than a 2V source. This was added to reduce impacts of poor peaks in the triangle wave.

# **Homework 3**

EE330 - Analog Electronics

Dillon Labonte

Southern New Hampshire University  
School of Engineering, Technology, and Aeronautics  
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# 1 General Approach

The general approach for this homework was to use a super-diode peak rectifier circuit, into a low-pass filter to remove IF content, and a third stage for driving a  $20\text{k}\Omega$  load.

The peak-rectifier circuit was modeled after the reference in the textbook. A super-diode was used to increase accuracy. I used a low-pass filter with a cutoff frequency of 50kHz to smooth out the message signal. The output of the filter was fed into the load. Each circuit was separated by a voltage follower to eliminate interactions between circuits.

## 2 Peak Rectifier

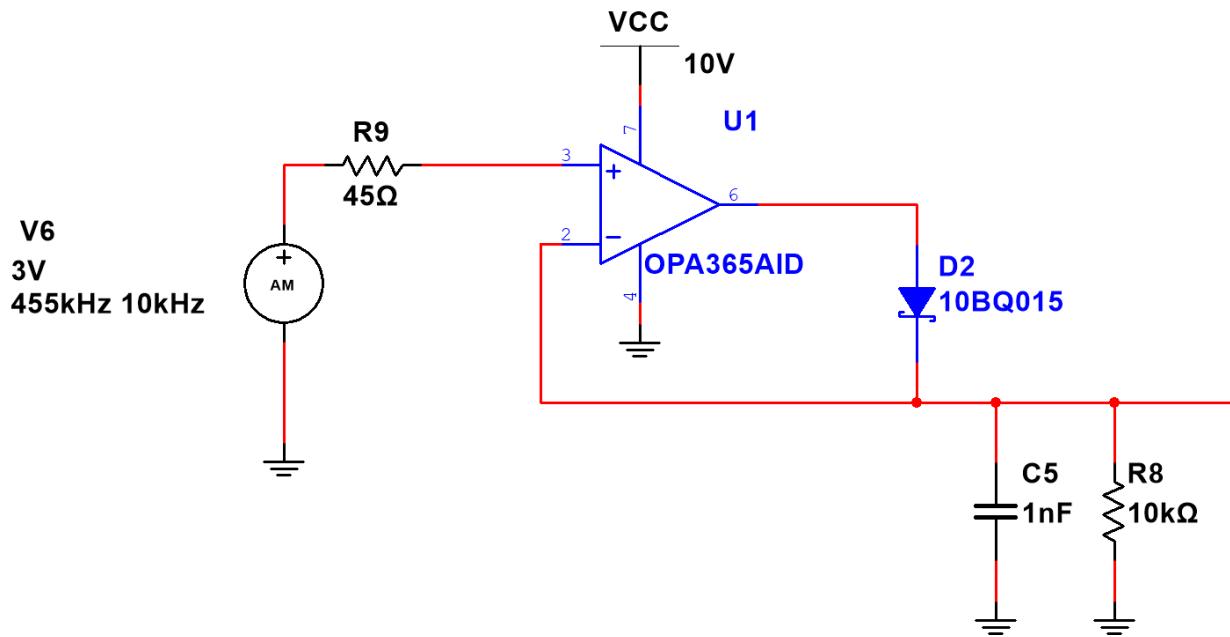


Figure 1: Peak Rectifier Circuit

The Multisim AM voltage source was used as an input to this circuit, along with a  $45\Omega$  source resistance. The modulation for design was set to 0.5, with an IF amplitude of 3V. A super-diode was built using an OPA365 op-amp and 10BQ015 Schottky diode. The OPA365 op-amp was chosen for its

relatively high slew rate, needed to accurately pass the 455kHz IF signal. The 10BQ015 Schottky diode was used in the previous iteration, and is not necessarily needed for this design.

To calculate the resistor and capacitor values for the peak rectifier, the following inequality was used from the textbook.

$$2\pi f_m < \frac{1}{RC} < 2\pi f_c$$

Where  $f_m$  and  $f_c$  are the message and carrier (IF) frequencies, respectively.

I chose the exact middle value of this range, which produced a capacitor value of 1nF and a resistor value of  $684.5\Omega$ . This combination produced a very poor peak-rectifier output. I messed with the resistor value until I had an acceptable output at the highest message frequency (10kHz). This resulted in a resistor value of  $10k\Omega$ .

The following figures show both the input to the circuit and the output of the peak-rectifier circuit.

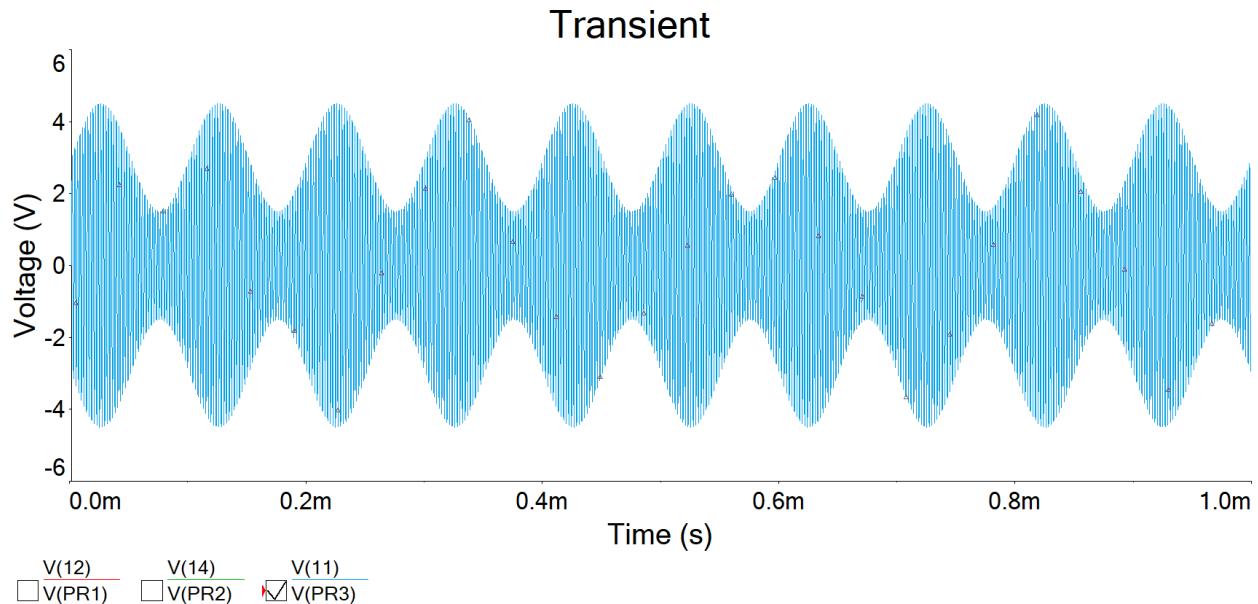


Figure 2: Circuit Input

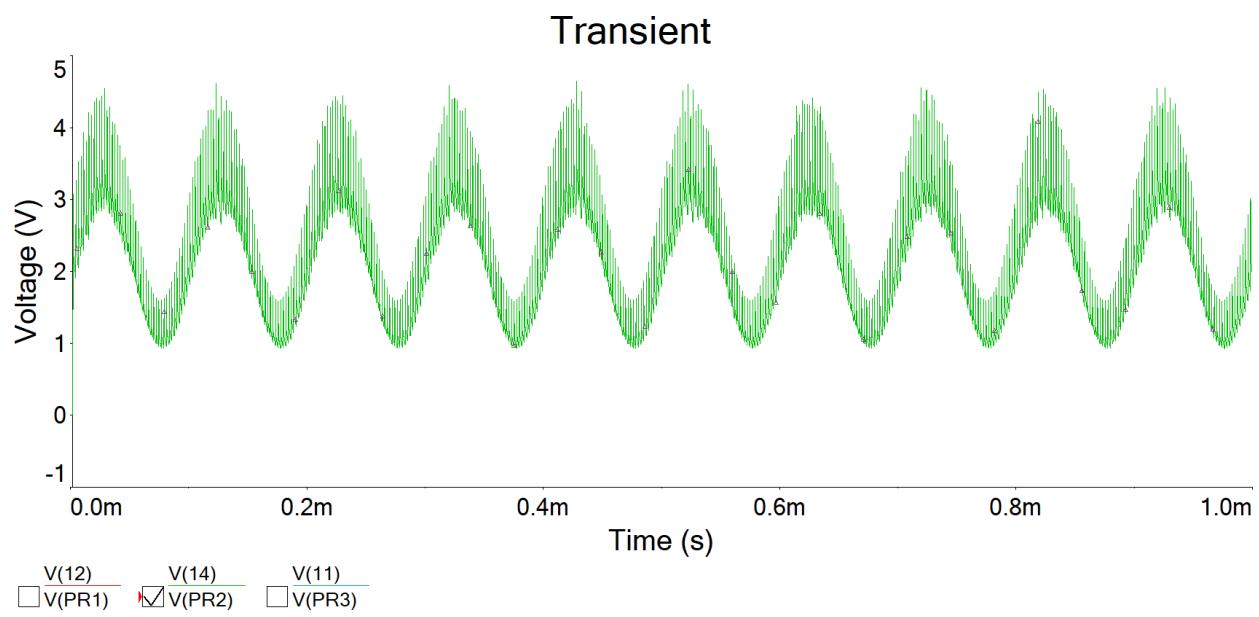


Figure 3: Peak-Rectifier Output

### 3 Low Pass Filter

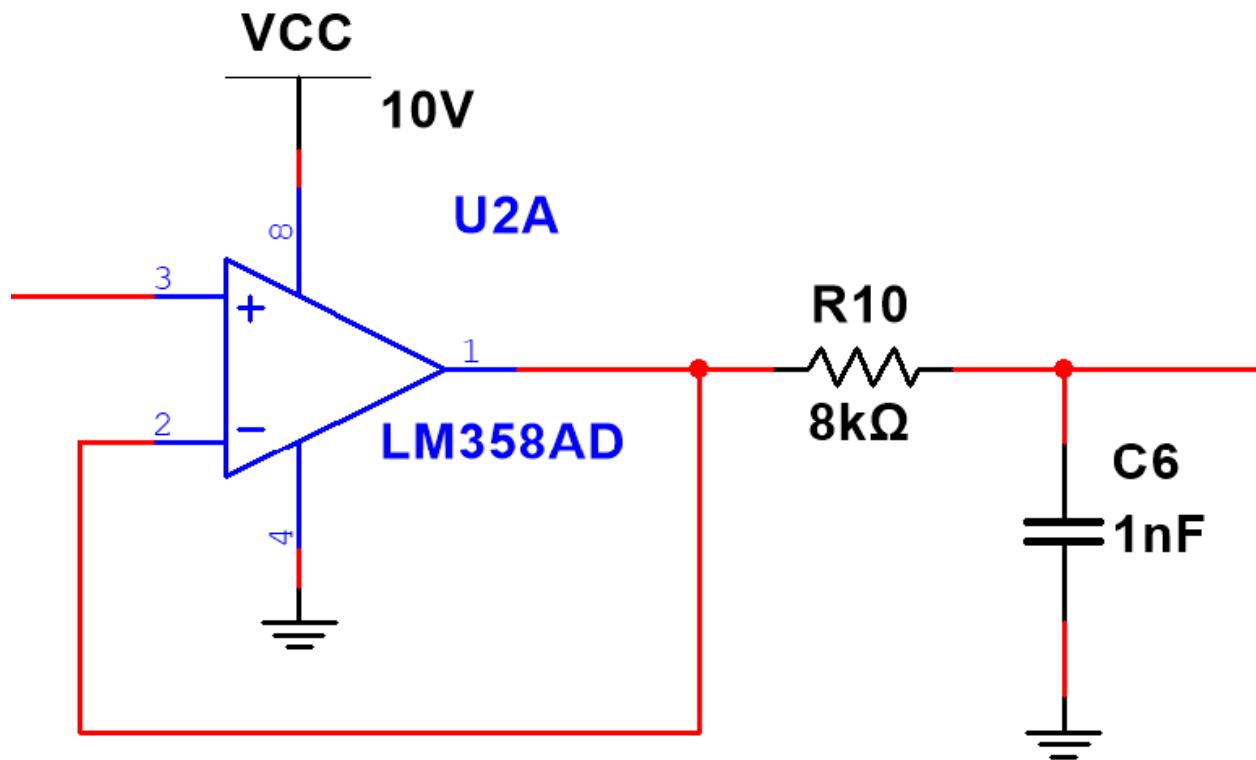


Figure 4: Low Pass Filter Circuit

The input of this circuit is the output of the peak-rectifier. There is a voltage follower buffer between the two circuit to prevent interactions between the two circuits. An LM358 op-amp was chosen, as the message signal contains much smaller frequencies than the IF, so we won't have issues with slewing. If any IF is present in the peak-rectifier output, the LM358's slew rate may actually help us in this instance, by slewing when encountered with IF.

I derived the transfer function of a low pass circuit as:

$$H(S) = \frac{1}{RCs + 1}$$

and a frequency response of:

$$H(\omega) = \frac{1}{j\omega RC + 1}$$

The 3dB bandwidth of the circuit is at  $f_c = \frac{1}{2\pi RC}$ . This cutoff frequency was chosen as 50kHz to allow for the message signal to get through with minimal attenuation, and to mostly cut out the IF. This resulted in a capacitor value of 1nF and a resistor value of 8kΩ.

The following figure shows the output of the low-pass filter compared to the input (peak-rectifier output).

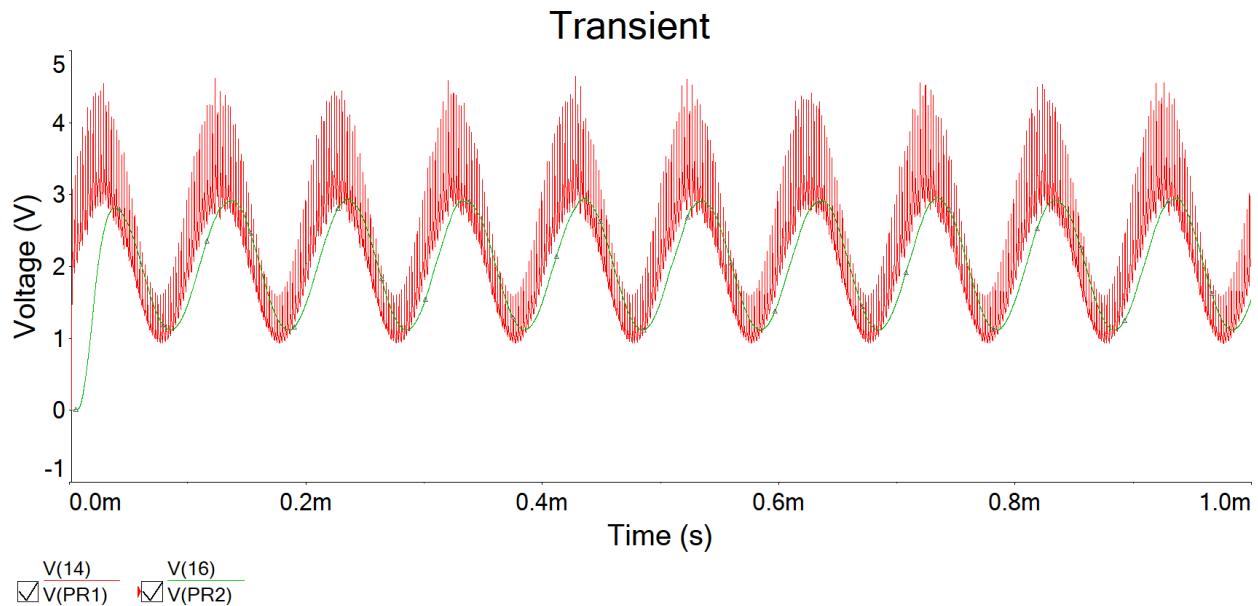


Figure 5: Low Pass Filter Output Compared to Input

## 4 Load Stage

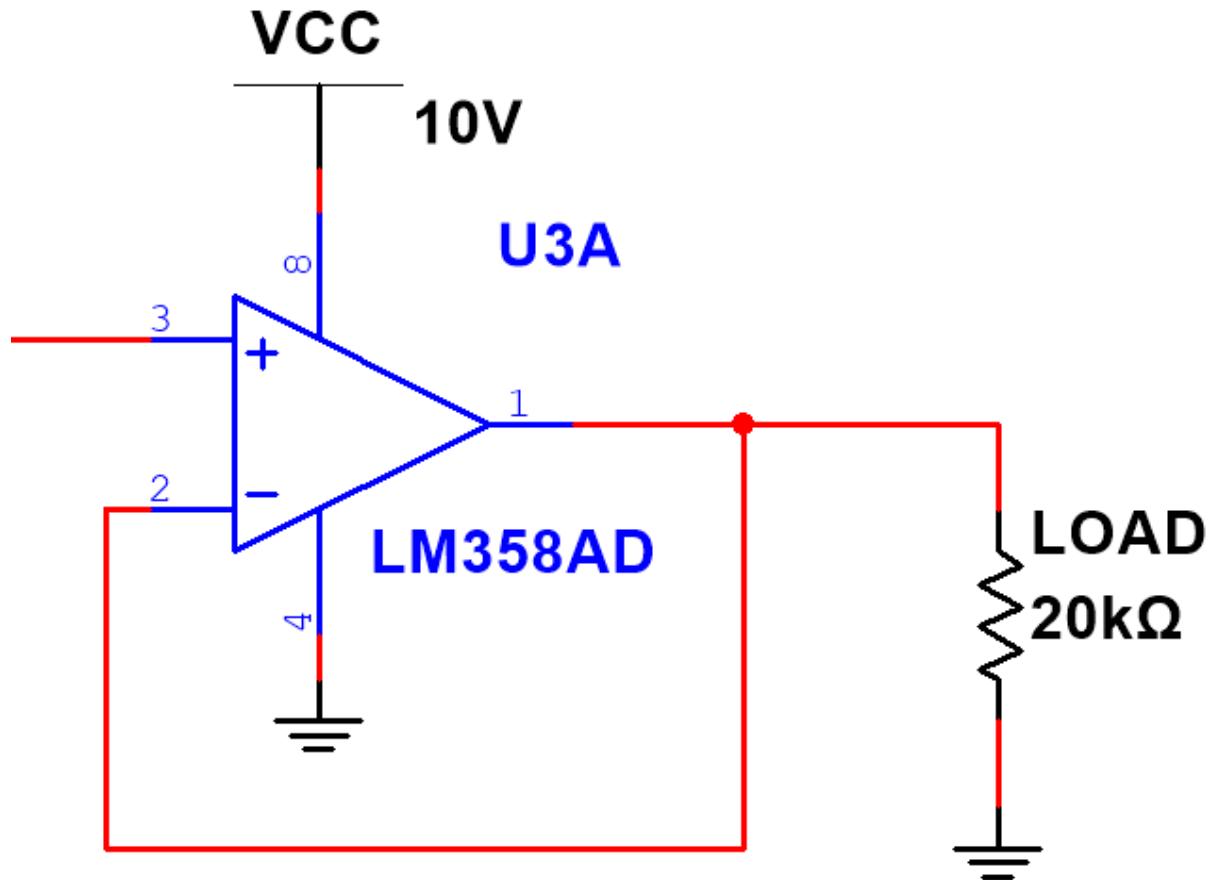


Figure 6: Load Stage Circuit

Again, a voltage follower using the LM358 op-amp was used to isolate the load, without worrying about the low LM358 slew rate. This stage was incorporated to provide a stable output over the load.

The following figure shows the output voltage of the load compared to the AM input signal, for the following frequencies: 20Hz, 5kHz, and 10kHz.

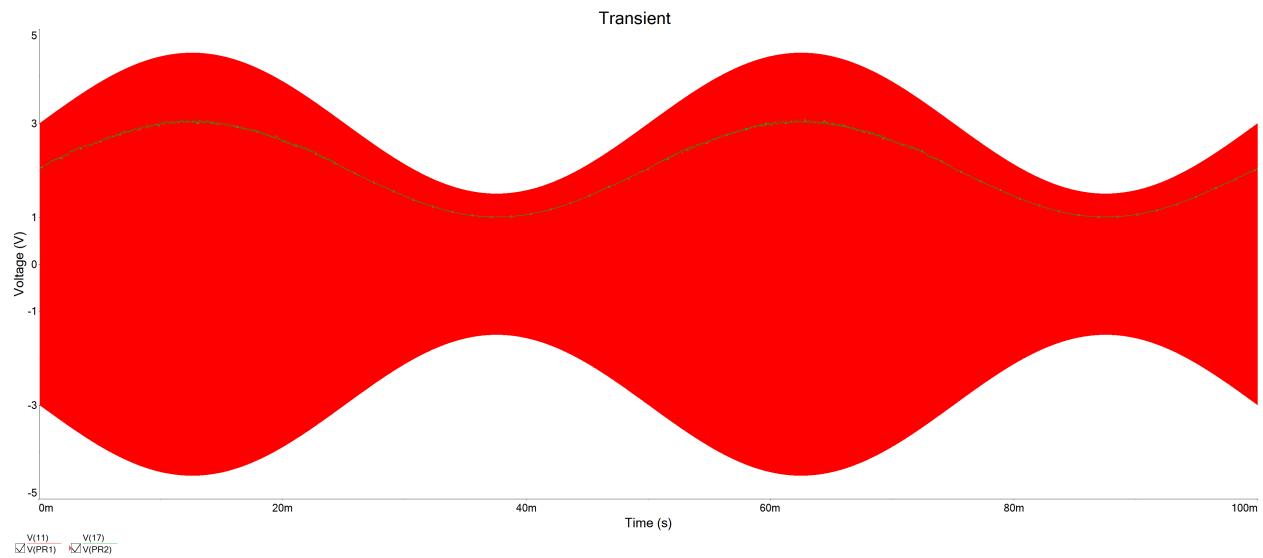


Figure 7: 20Hz Message Output Compared to AM Input

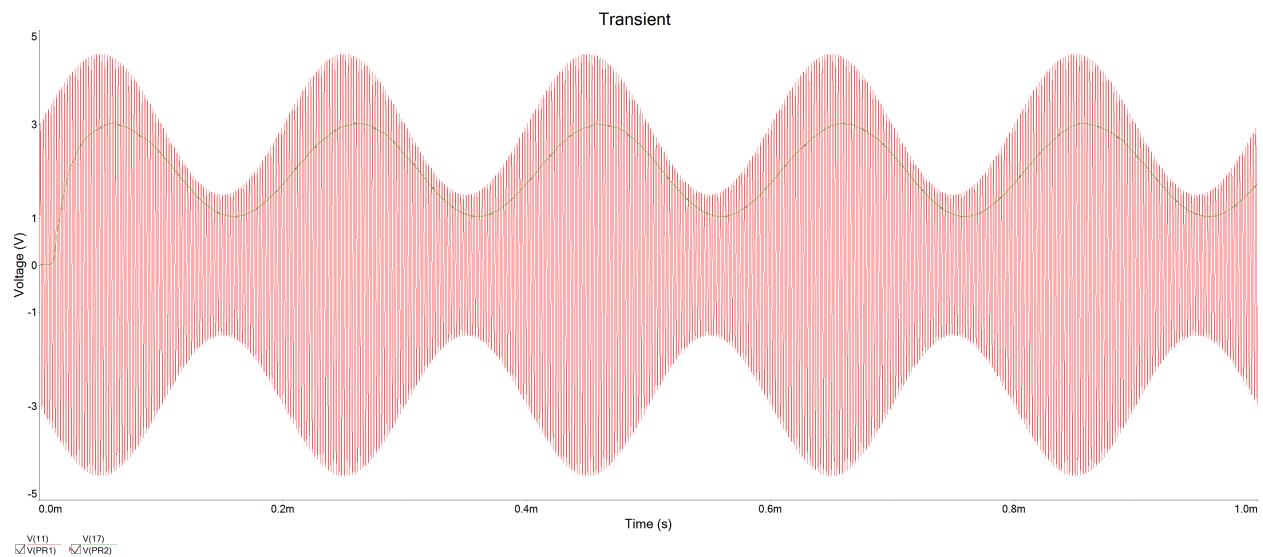


Figure 8: 5kHz Message Output Compared to AM Input

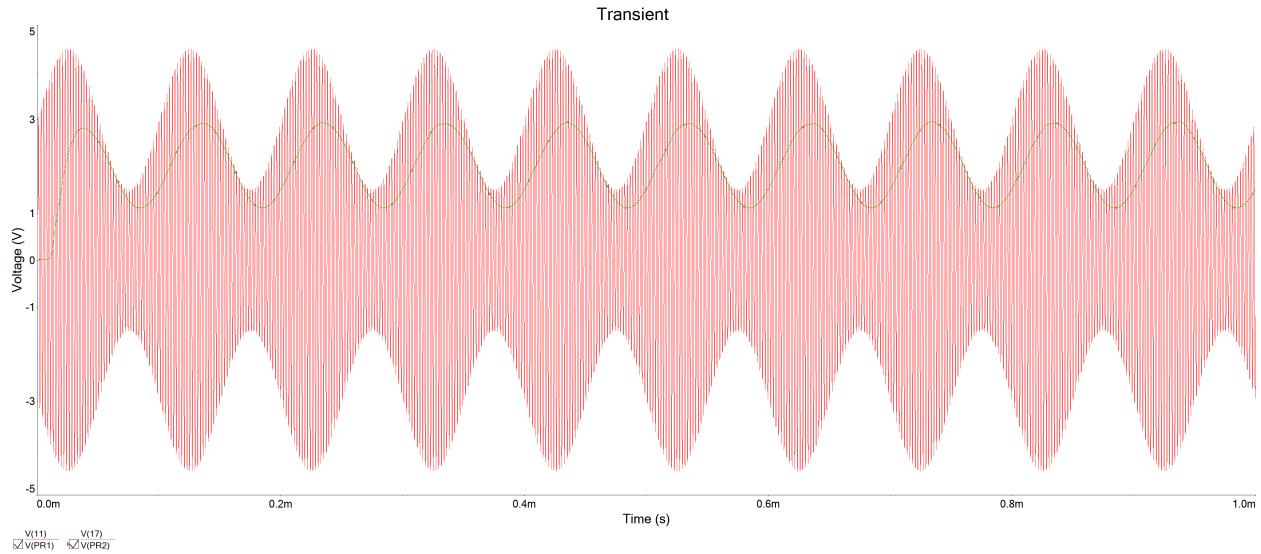


Figure 9: 10kHz Message Output Compared to AM Input

For the above frequencies, we see that the green output signal is the same shape as the envelope of the red AM signal input. There is a small phase shift present and some signal attenuation that could be restored from an amplifier stage.

## 5 Complete Circuit

The following figure shows the complete circuit.

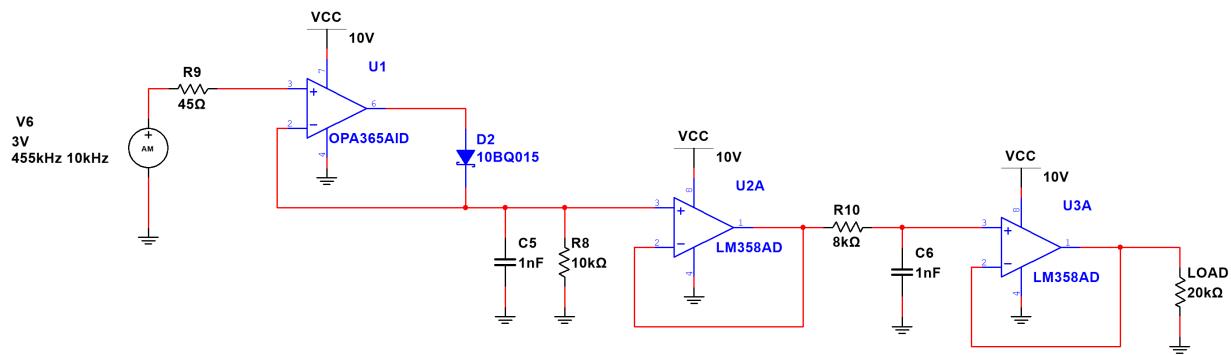


Figure 10: Complete Circuit

# 6 Circuit Performance

## 6.1 Modulation Index of 1

Thus far we have used an AM source with a modulation index of 0.5. In this section, we explore the circuit's performance with a modulation index of 1.

The following figure shows the circuit output for a 10kHz message signal with a modulation index of 1.

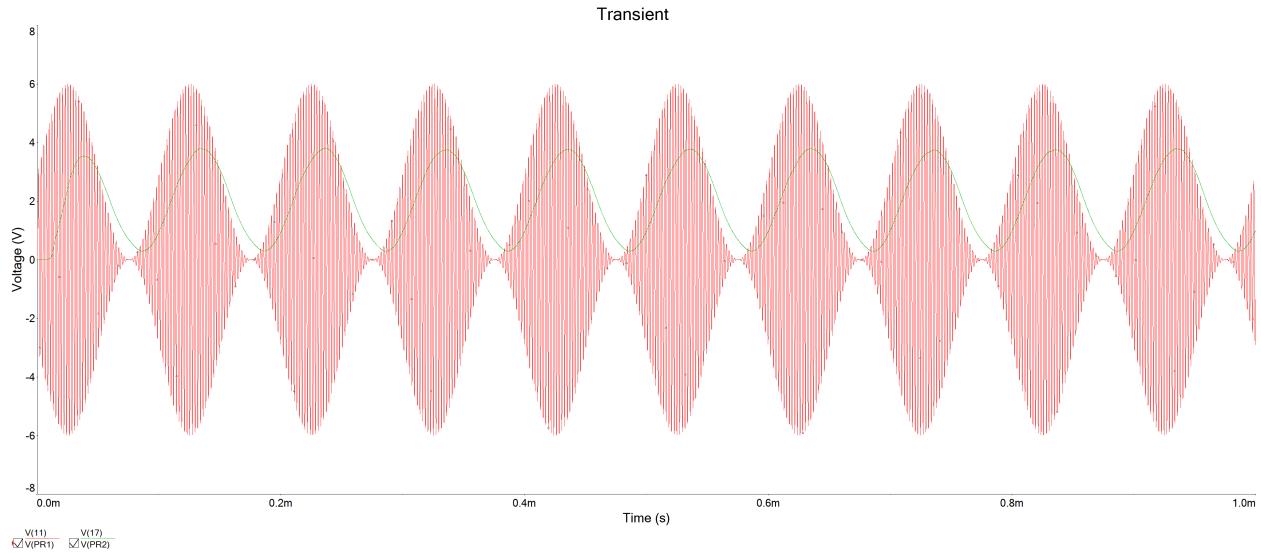


Figure 11: 10kHz message: Output for Modulation Index of 1

This result indicates that this circuit can handle a modulation index of 1 and still produce a good output.

## 6.2 Total Harmonic Distortion

To quantify harmonic distortion of the message signal, we use a Fourier analysis in Multisim. These analyses were conducted after reverting the modulation index back to 0.5.

The following figure shows the output of the Fourier analysis using a 10kHz message signal.

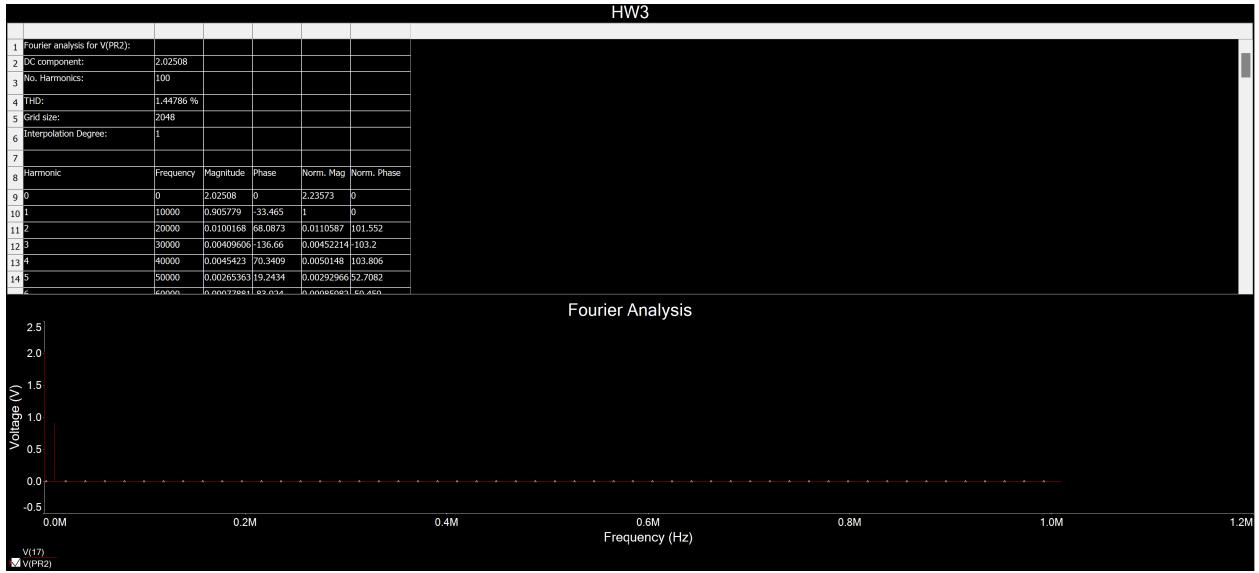


Figure 12: Fourier Analysis for 10kHz Message

I used 100 harmonics, which produced a total harmonic distribution (THD) of 1.44786%. This seems pretty good, and indicates that our circuit is performing well with message signals at 10kHz. The following table summarizes THD measured for other message signal frequencies.

Message Frequency (Hz)	THD (%)
20	2.04183
1000	2.18547
2500	2.19772
5000	2.00702
10000	1.44786

Table 1: Message Frequency vs THD

This circuit performs fairly well across the entire input message frequency range.

### 6.3 Carrier Feedthrough

We also quantify carrier feedthrough using Fourier analysis by setting the fundamental frequency to the IF (455kHz).

1	Fourier analysis for V(PR2):						
2	DC component:	1.47999					
3	No. Harmonics:	1					
4	THD:	0 %					
5	Grid size:	64					
6	Interpolation Degree:	1					
7							
8	Harmonic	Frequency	Magnitude	Phase	Norm. Mag	Norm. Phase	
9	0	0	1.47999	0	47.8846	0	
10	1	455000	0.0309074	-178.92	1	0	
11							

Figure 13: Carrier Feedthrough

From this Multisim Fourier analysis, we see that the carrier has a very small feedthrough to the output, with a magnitude of 0.0309074 which is about 30 times smaller than the message signal amplitude from figure 12.

## 6.4 Component Tolerances

Component tolerances were adjusted to be both high and low and the THD was measured using a message signal of 5kHz. Resistors used a tolerance of 1% and capacitors with a tolerance of 5%. At nominal values of components, the THD for a 5kHz signal was 2.00702%.

### 6.4.1 Input

On the input side, we only have a  $45\Omega$  resistor to change.

When the resistor is 1% higher, we have a THD of 1.50036%, which is quite a bit better.

When the resistor is 1% lower, we have a THD of 1.93745%, which is still slightly better than the nominal run.

Therefore, the tolerance of our input source resistance will not make our THD worse.

#### 6.4.2 Peak Rectifier

In the peak rectifier, we have a resistor and capacitor to change. These values represent a time constant, so the worst effect will be when they are both higher or both lower.

When both the  $10k\Omega$  resistor and  $1nF$  capacitor are higher (1% for resistor and 5% for capacitor), we have an output THD of 2.91919%. This is a bit worse than the nominal run.

When both the  $10k\Omega$  resistor and  $1nF$  capacitor are lower (1% for resistor and 5% for capacitor), we have an output THD of 1.8111%. This is a bit better than the nominal run.

Therefore, if our resistor and capacitor are higher than nominal value, we will expect a worse output.

#### 6.4.3 Low Pass Filter

Similar to the peak-rectifier, in the low pass filter we also have a resistor and capacitor. These values multiply together to affect the cutoff frequency, thus the worst case will be when both are higher or both are lower than nominal value.

When both the  $8k\Omega$  resistor and  $1nF$  capacitor are higher (1% for resistor and 5% for capacitor), we have an output THD of 1.76942%. This is a bit better than the nominal run.

When both the  $8k\Omega$  resistor and  $1nF$  capacitor are lower (1% for resistor and 5% for capacitor), we have an output THD of 2.65866%. This is a bit worse than the nominal run.

Thus, if our resistor and capacitor of the low-pass circuit are lower than nominal value, we will expect a worse output.

#### 6.4.4 Load Stage

The load stage consists of a single  $20k\Omega$  resistor.

When this resistor is 1% higher, we have an output THD of 1.94551%. Which is a little better than the nominal run.

When this resistor is 1% lower, we have an output THD of 2.08792%. This is a little bit worse than the nominal run.

#### 6.4.5 Worst Case

The worst case arises when the peak-rectifier resistor and capacitor are higher than nominal value, the low pass filter resistor and capacitor are lower than nominal value, and the load resistor is lower than nominal value.

Applying this worst case situation to the circuit, we have an output THD of 2.55784%. This is still fairly decent, so our component tolerances do not have a large effect on the circuit output.

#### 6.4.6 Modifying Circuit

By replacing the LM358 op-amps with OPA365 op-amps, we can reduce the output THD in the worst case to 2.13117% and 1.73773% for the nominal run. This modification also reduced the carrier feedthrough to a magnitude of 0.0294026, compared to the previous magnitude of 0.0309074. This modification improves the performance noticeably.

# **Homework 4**

EE330 - Analog Electronics

Dillon Labonte

Southern New Hampshire University  
School of Engineering, Technology, and Aeronautics  
(SETA)

Submitted: March 2025

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# 1 General Approach

The general approach for this voltage regulator circuit is to use a 5V Zener diode as a reference voltage. A resistor is added in series between the voltage input and the Zener to limit the current through the Zener and the power dissipated in the Zener. The Zener voltage reference was isolated from the load using an op-amp voltage follower with low input bias current.

# 2 Circuit Design

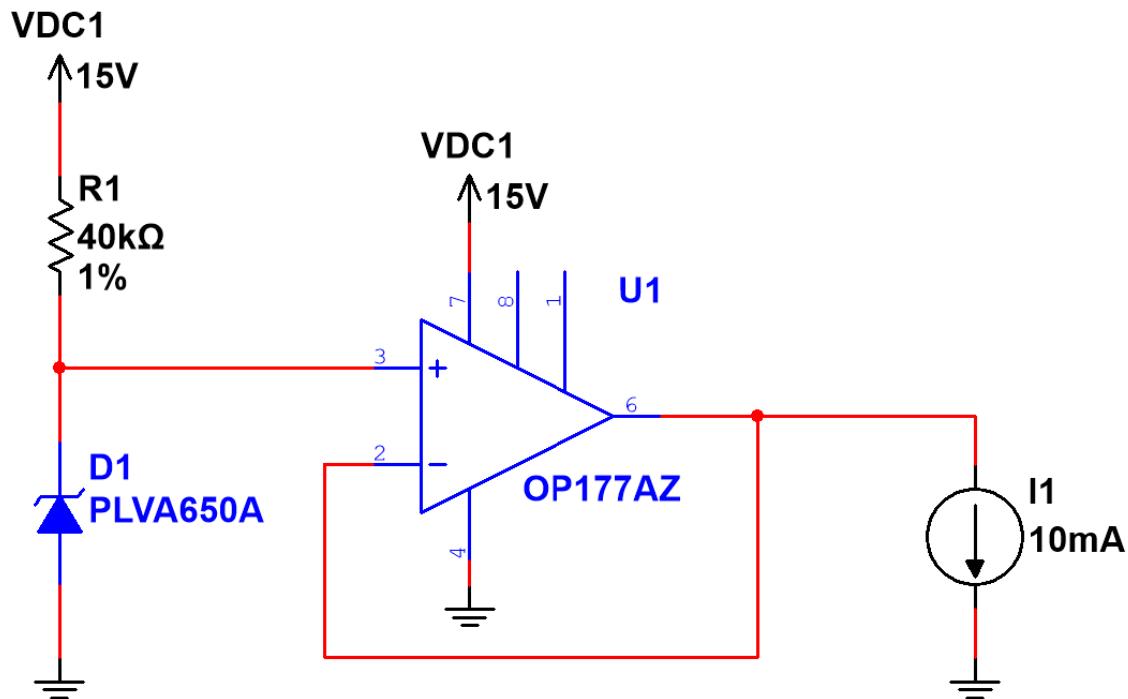


Figure 1: Original Circuit Design

The PLVA650A Zener diode was chosen for its 5V Zener voltage, as well as meeting specifications of power dissipation and temperature requirements. This particular Zener diode produces a Zener voltage of 5V at a test current of  $250\mu\text{A}$ . Setting the input voltage to the middle of the specified range (15V), the resistance value needed can be calculated.

$$R = \frac{15V - 5V}{250\mu A} = 40k\Omega$$

In the operating range of this circuit, the Zener will be dissipating about  $5V \cdot 250\mu A = 1.25mW$ , which is well within the 250mW specification of the diode.

An op-amp was used as a voltage follower to isolate the load from the Zener diode. The OP177AZ op-amp was chosen for its low input bias current, about 1nA. This results in a minimal effect on the Zener voltage. The negative supply rail of the op-amp was connected to ground, while the positive supply voltage was connected to the input of the circuit (the unregulated voltage). A current source was added to the output of the op-amp to simulate a load.

## 2.1 Modification

The  $40k\Omega$  resistor was chosen to limit the current through the Zener and produce an output of 5V. However, the output voltage was actually 5.01488V. This is well within the 5% tolerance of the assignment, but I decided to improve upon this using a parameter sweep of the resistor value. For this simulation, the input voltage was set to 15V and the load current was set to 10mA, both values set to the middle of the range for this assignment. The results of this simulation are seen below.

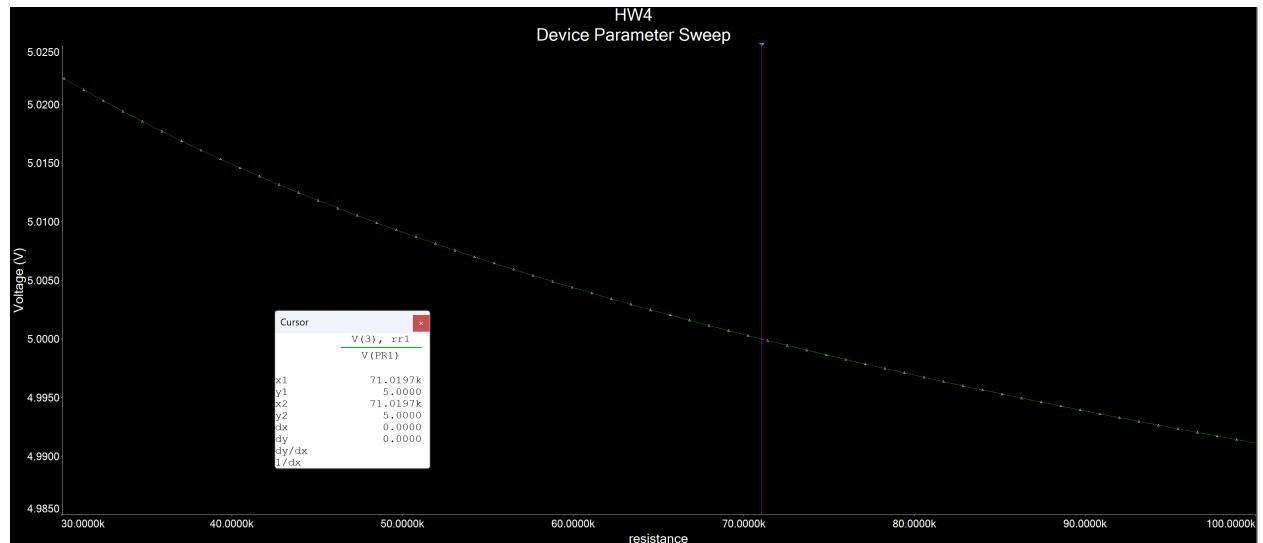


Figure 2: Resistor Sweep Simulation

From this simulation, we see that a resistor value of  $71.0197\text{k}\Omega$  produces an output voltage of exactly 5V in this configuration. I chose to use a  $70\text{k}\Omega$  resistor, which produced an output voltage of 5.00037V in this particular configuration.

### 3 Performance Over Specified Range

Before considering any non-idealities of this circuit, we want to look at the performance of the regulator over the range of possible input voltage values, as well as output load currents.

First we consider the input voltage range of 10 – 20V. By holding the output current constant in the middle of the range at 10mA, we can observe the effect of changing the input voltage. This was completed using a DC sweep simulation and the results can be seen below.

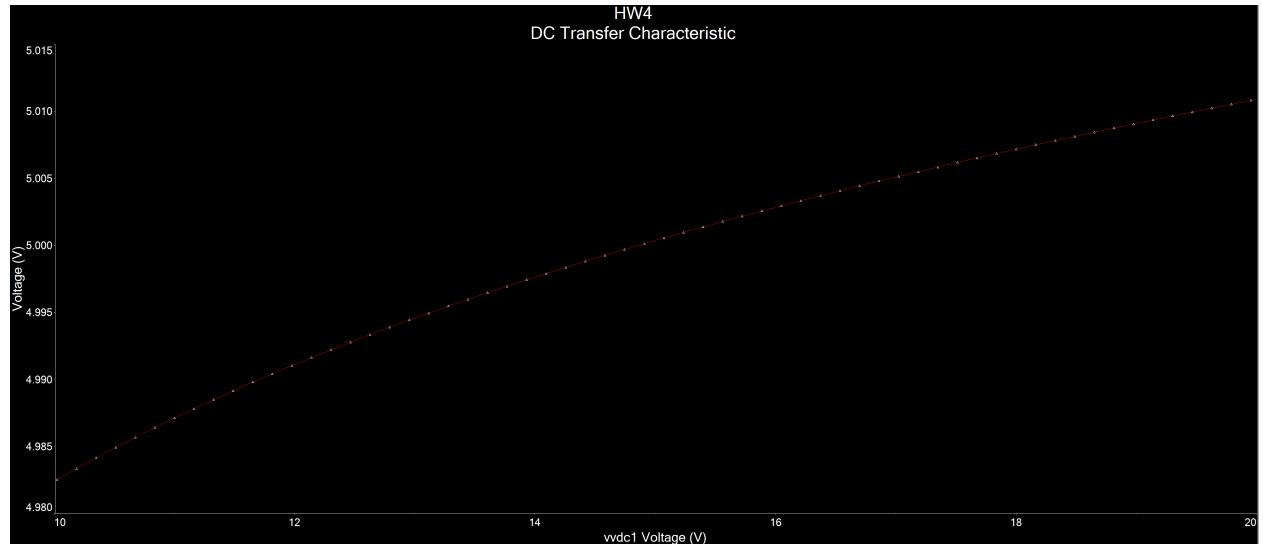


Figure 3: Input Voltage Sweep Simulation

We see that as the input voltage increases, so does the output voltage slightly. Across the input voltage range, the output voltage ranges from 4.9824 – 5.0109V. This slight variation is well within the 5% tolerance as outlined by the assignment.

Next we look at the impact of the load current on the output voltage. The same approach as above was used, with a constant input voltage of 15V and a load current range of 0 – 20mA. The results of the simulation are seen below.

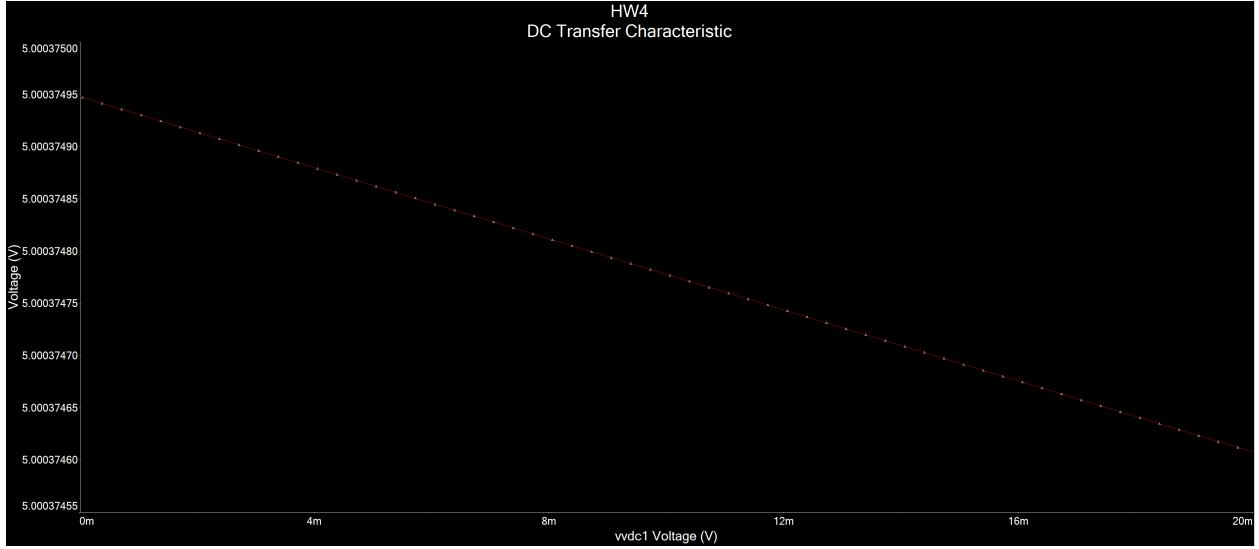


Figure 4: Load Current Sweep Simulation

From this simulation, we observe that as the load current increases, the output voltage decreases. Over the range of load currents, the output voltage has such a small range that the cursor cannot pick up such precision. Thus, our load current has practically no affect on our output voltage.

From this analysis, we see that the regulator circuit is performing exceptionally well under the specified conditions, before considering non-idealities.

## 4 Non-Idealities

In this section we will consider different non-idealities of this circuit. First, we discuss the worst output voltage case with regards to the input voltage and load current as discussed in the previous section. Next, we discuss impacts of passive component tolerances, and finally we will look at temperature effects over the specified conditions of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### 4.1 Worst Case

First we will look at the low worst case of the circuit; the lowest voltage it will produce in the specified ranges of input voltage and load current. From figures 3 and 4, we see that this will occur when the input voltage is 10V and the load current is 20mA.

In this configuration, a DC operating point simulation indicates an output voltage of 4.98244V. This is well within the 5% tolerance.

Next we will look at the high worst case of the circuit; the highest voltage it will produce in the specified ranges of input voltage and load current. From figures 3 and 4, we see that this will occur when the input voltage is 20V and the load current is 0mA.

In this configuration, a DC operating point simulation indicates an output voltage of 5.01089V. Again, this is well within the 5% tolerance.

## 4.2 Passive Component Tolerances

Next we consider the impact of passive component tolerances. Since Multisim does not allow access to passive component tolerances inside the op-amp, the only passive component we need to worry about is the  $70\text{k}\Omega$  resistor. Using a 1% tolerance resistor, the possible values of this resistor range from  $69.3\text{k}\Omega$  to  $70.7\text{k}\Omega$ .

Configuring the circuit using a 15V input voltage, 10mA load current, and  $69.3\text{k}\Omega$  resistor, the output voltage is 5.00064V. This output is slightly higher than the nominal run of 5.00037V.

Configuring the circuit using the same input voltage and load current but with a resistance of  $70.7\text{k}\Omega$ , the output voltage is 5.00012V. This is slightly lower than the nominal run.

From this analysis, we see that the impact of passive component tolerances on the output voltage is very minimal.

## 4.3 Temperature Effects

Next we consider the impact of temperature over the range  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  using the temperature sweep simulation in Multisim.

Configuring the circuit using the same 15V input and 10mA load current, the results of the temperature sweep simulation can be seen below.

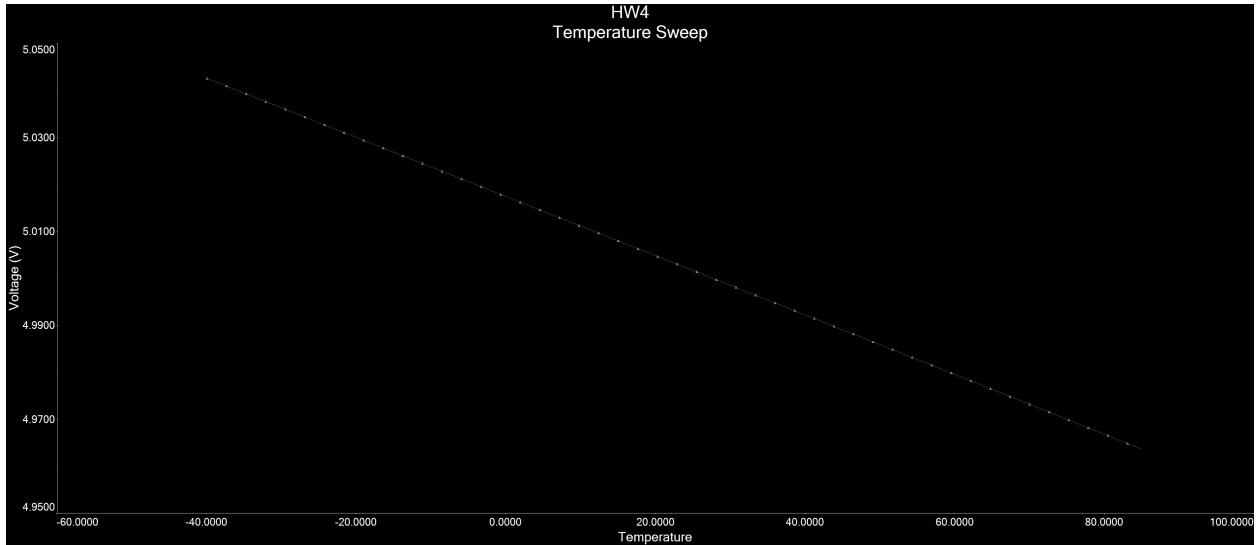


Figure 5: Temperature Sweep Simulation

At  $-40^{\circ}\text{C}$ , we see the highest output voltage of 5.0425V. At  $85^{\circ}\text{C}$ , we see the lowest output voltage of 4.9636V. Both of these output voltages are well within the 5% tolerance.

#### 4.4 Absolute Worst Case

From the analysis of different non-idealities, we want to look at the absolute worst case for both lowest and highest output voltages.

The lowest output voltage occurs when we have a 10V input, 20mA load current,  $70.7\text{k}\Omega$  resistance, and  $85^{\circ}\text{C}$ . This produces an output voltage of 4.9417V. This produces an error of

$$\% \text{ error} = \frac{5\text{V} - 4.9417\text{V}}{5\text{V}} \times 100\% = 1.17\%.$$

This is a very small error and well within the 5% tolerance, as per the requirements of the assignment.

The highest output voltage occurs when we have a 20V input, 0A load current,  $69.3\text{k}\Omega$  resistance, and  $-40^{\circ}\text{C}$ . This produces an output voltage of 5.0509V. This produces an error of

$$\% \text{ error} = \frac{5.0509\text{V} - 5\text{V}}{5\text{V}} \times 100\% = 1.02\%.$$

This is a very small error and well within the 5% tolerance, as per the requirements of the assignment.

# **Homework 5**

EE330 - Analog Electronics

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Southern New Hampshire University  
School of Engineering, Technology, and Aeronautics  
(SETA)

Submitted: March 2025

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# 1 General Approach

The op-amp based multiplier architecture was used to design this circuit. After scaling the  $0 - 1V$  control voltage to a range of  $1 - 5V$ , this signal can then be multiplied by the input voltage signal to produce the desired gain of  $1000 - 5000V/V$ . Figure 1 below shows a high level block diagram of the system. Note that the AD633 multiplication IC was used, which multiplies the two input signals and scales by a factor of  $1/10$ .

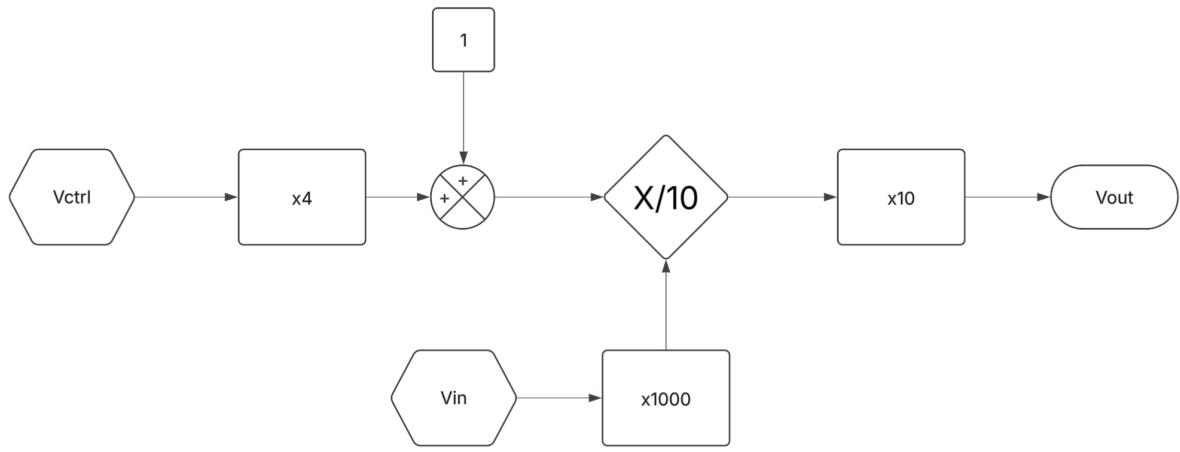


Figure 1: Circuit Block Diagram

Non-inverting amplifiers were used to amplify and add signals together due to their high input impedance. The following sections will go into detail on how each component of the system operates.

## 2 Scaling Control Voltage

In this section, the scaling of the control voltage is analyzed. This step was necessary to change the range of the control voltage from  $0 - 1V$  to  $1 - 5V$ . By scaling the control voltage, the multiplier will be able to multiply the input signal by the proper amount to produce the desired gain, as set by the control voltage.

## 2.1 Amplifying Control Voltage

To amplify the control voltage, a non-inverting amplifier was used with a gain of 4V/V. This changes the range of the control voltage to 0 – 4V. Figure 2 below shows this amplification.

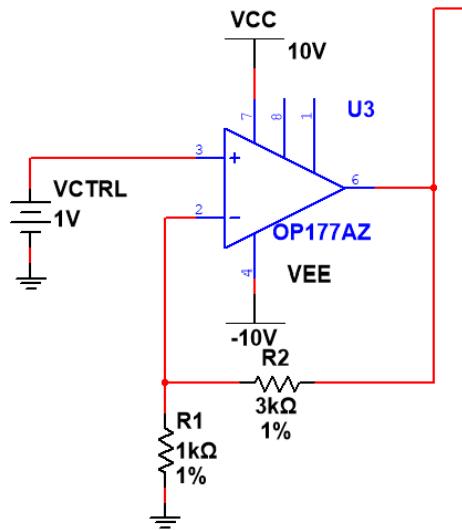


Figure 2: Amplifying Control Voltage

## 2.2 Summing Control Voltage

With the control voltage now in the range of 0 – 4V, 1V must be added to reach the desired range. This is accomplished using a weighted non-inverting summer with a weight of 1.

Due to the assignment requirement of using only two ideal voltage sources, and both being used for op-amp supplies, an alternative method to create a 1V reference was used. Using the 10V  $V_{CC}$  supply from the op-amp, a voltage divider was created to produce 1V. To isolate this voltage reference from the rest of the circuit, op-amp  $U4$  in figure 3 below acts as a buffer amplifier.

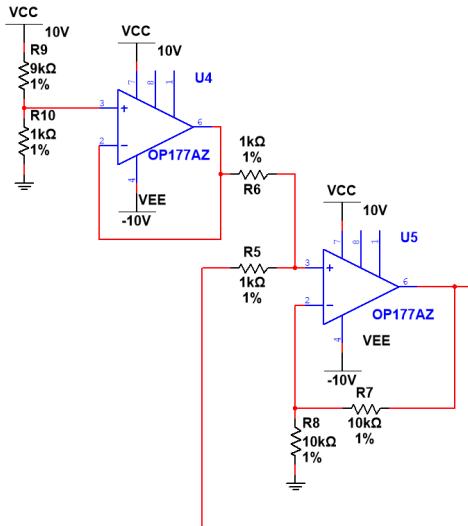


Figure 3: Non-Inverting Summer

By setting  $R5 = R6 = 1\text{k}\Omega$  and  $R7 = R8 = 10\text{k}\Omega$ , the weighting on this summer is 1. Thus, the amplifier will sum the two voltage inputs as is, the 1V reference and the scaled control voltage from the previous section. Thus, the range of the control voltage is now 1 – 5V, as desired.

### 3 Amplifying Input Voltage

This section will analyze the amplification of the input voltage signal. Due to small imperfections in the AD6333 multiplication IC, such as offset voltage, a more accurate and precise output is achieved when the two inputs to the multiplier are of the same magnitude. Since the control voltage is now on a range of 1 – 5V and  $|V_{in}| \leq 5\text{mV}$ , an amplification with gain of 1000V/V is needed. This is accomplished using a non-inverting amplifier as seen in figure 4.

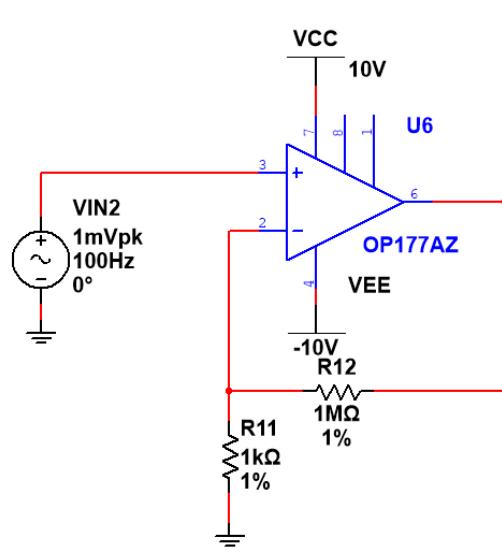


Figure 4: Input Voltage Amplifier

Note that the gain of a non-inverting amplifier is

$$A_v = 1 + \frac{R_2}{R_1}.$$

For this particular amplifier, this results in a gain of 1001V/V which is marginally higher than the desired 1000V/V and can be ignored.

Now that the input voltage has been amplified to the same order of magnitude as the control voltage, they can more accurately be multiplied together using the AD6333 IC.

## 4 Signal Multiplication

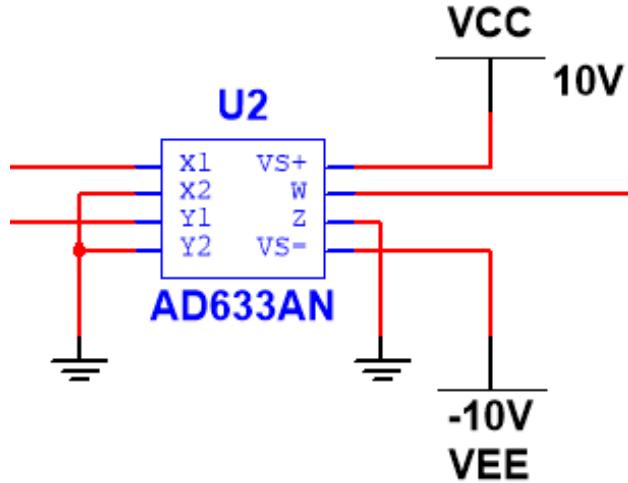


Figure 5: AD633 Multiplication IC

Figure 5 above shows the AD6333 multiplication IC. This IC works by the following equation,

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z.$$

By connecting  $X_2$ ,  $Y_2$ , and  $Z$  to ground, the equation simplifies to,

$$W = \frac{X_1 Y_1}{10},$$

where  $X_1$  and  $Y_1$  are the scaled control voltage and amplified input voltage signals, respectively.

Now that the scaled control voltage and amplified input voltage have been multiplied together, the product can then be amplified in another stage to produce the final output voltage.

## 5 Final Amplifying Stage

The AD633 multiplication IC scaled the product of the scaled voltage control and amplified input voltage by a factor of 1/10. To combat this, a non-

inverting amplifier with a gain of 10V/V was placed after the multiplication to recover the gain to the desired level. Figure 6 below shows this final amplifying stage, where  $PR_1$  is the output voltage.

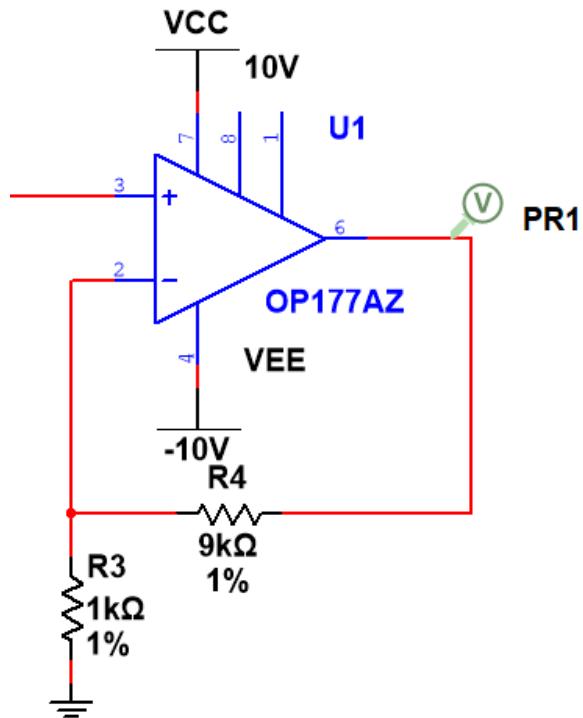


Figure 6: Final Amplifying Stage

## 6 Complete Circuit

Figure 7 below shows the complete circuit.

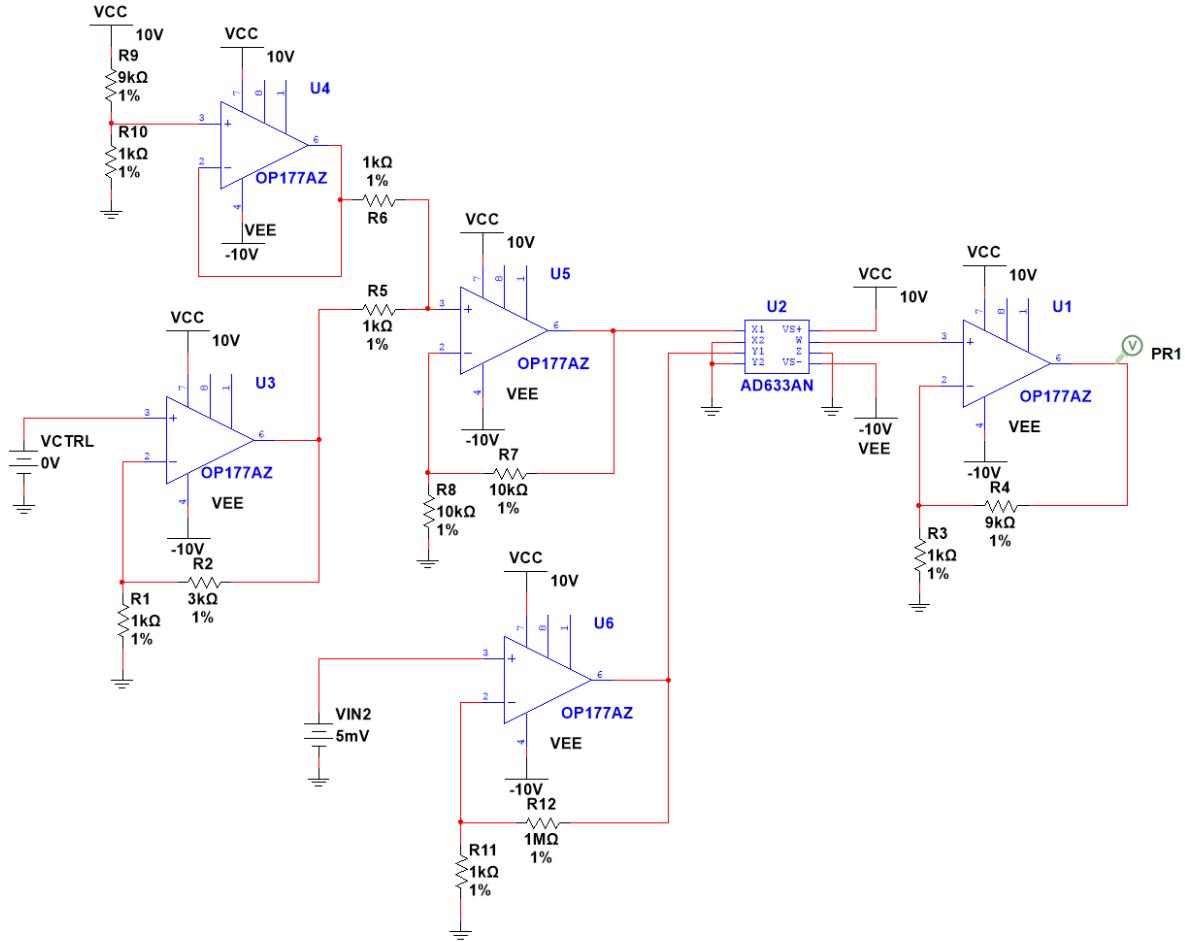


Figure 7: Complete Circuit

# 7 System Performance

This section will analyze different aspects of the circuit in terms of its performance.

## 7.1 Gain Accuracy

### 7.1.1 Positive Input Voltages

The following plot shows the output voltage as a function of the control voltage for a constant input voltage of 1mV.

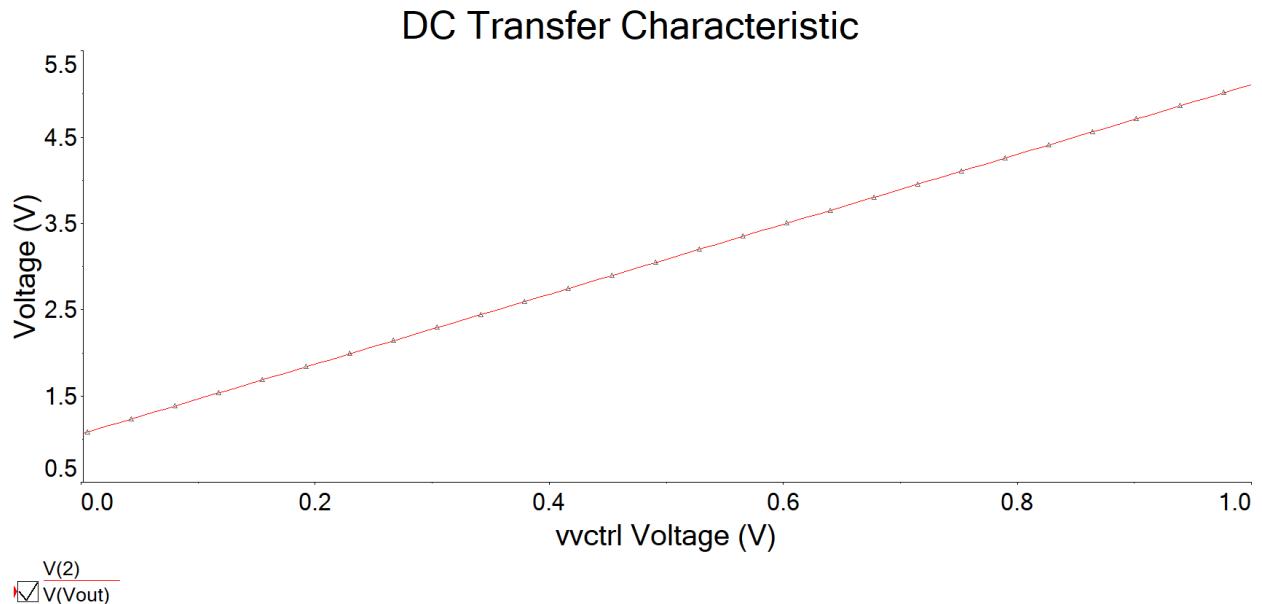


Figure 8: Control Voltage Sweep for 1mV Input

At a control voltage of 0V, the output voltage is 1.0655V. This indicates a gain of

$$G|_{V_{CTRL}=0} = \frac{1.0655V}{1mV} = 1065.5V/V.$$

Relative to the desired 1000V/V, this is an error of,

$$\% \text{ error} = \frac{1065.5V/V - 1000V/V}{1000V/V} \cdot 100\% = 6.55 \% \text{ error.}$$

At a control voltage of 0.5V, the output voltage is 3.0864V. This indicates a gain of

$$G|_{V_{CTRL}=0.5} = \frac{3.0864\text{V}}{1\text{mV}} = 3086.4\text{V/V}.$$

Relative to the desired 3000V/V, this is an error of,

$$\% \text{ error} = \frac{3086.4\text{V/V} - 3000\text{V/V}}{3000\text{V/V}} \cdot 100\% = 2.88 \% \text{ error}.$$

At a control voltage of 1V, the output voltage is 5.1072V. This indicates a gain of

$$G|_{V_{CTRL}=1} = \frac{5.1072\text{V}}{1\text{mV}} = 5107.2\text{V/V}.$$

Relative to the desired 5000V/V, this is an error of,

$$\% \text{ error} = \frac{5107.2\text{V/V} - 5000\text{V/V}}{5000\text{V/V}} \cdot 100\% = 2.14 \% \text{ error}.$$

The voltage gain is predominantly a linear function of control voltage as seen in figure 8 and through this analysis. At 0V control voltage, the gain was within the spec of 1000V/V  $\pm$  10%. At 1V control voltage, the gain was within the spec of 5000V/V  $\pm$  10%. In fact, as control voltage increased, the gain error decreased.

The following plot shows the output voltage as a function of the control voltage for a constant input voltage of 5mV.

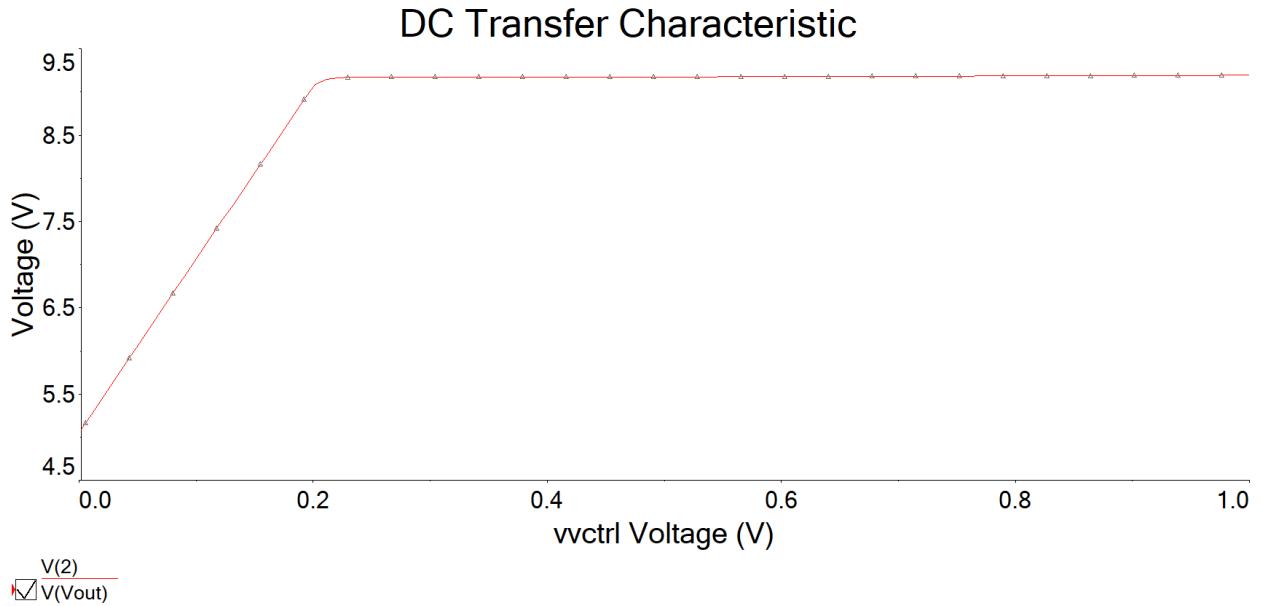


Figure 9: Control Voltage Sweep for 5mV Input

The output voltage begins as a linear function of the control voltage, however it quickly saturates as the various non-inverting amplifiers saturate. However, this saturation limit is well above the required output voltage range as per the requirements of the assignment.

### 7.1.2 Negative Input Voltages

The range of input voltages is  $\pm 5\text{mV}$ , so a similar analysis can be conducted for negative input voltages.

The following plot shows the output voltage as a function of the control voltage for a constant input voltage of  $-1\text{mV}$ .

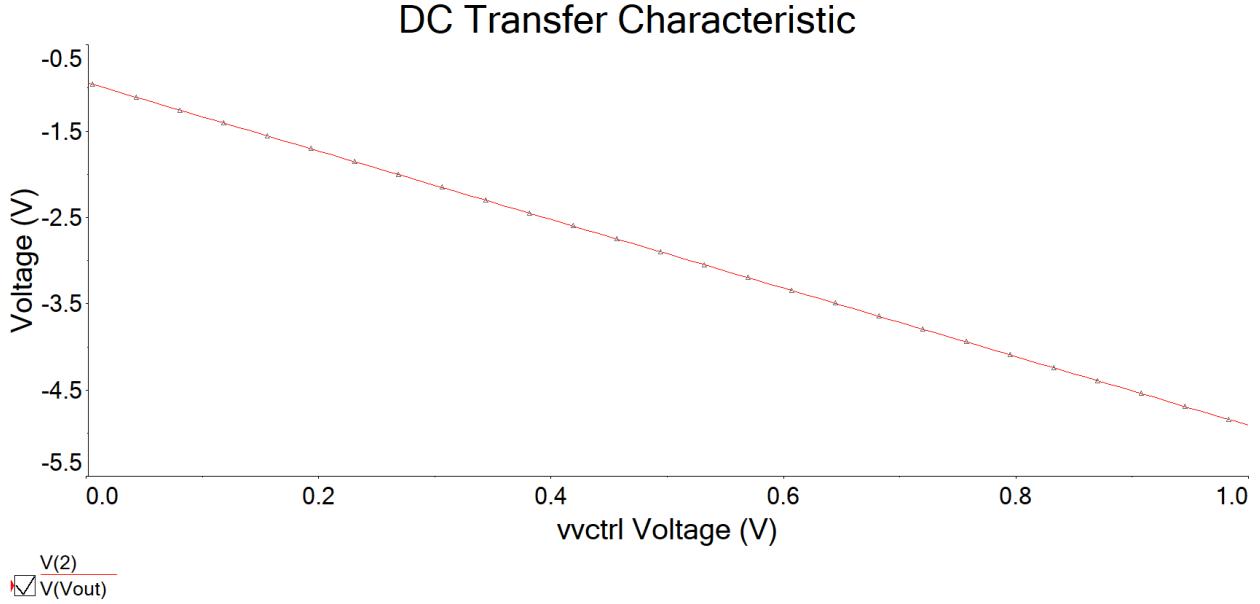


Figure 10: Control Voltage Sweep for  $-1\text{mV}$  Input

At a control voltage of  $0\text{V}$ , the output voltage is  $-945.7907\text{mV}$ . This indicates a gain of

$$G|_{V_{CTRL}=0} = \frac{-945.7907\text{mV}}{-1\text{mV}} = 945.7907\text{V/V}.$$

Relative to the desired  $1000\text{V/V}$ , this is an error of,

$$\% \text{ error} = \frac{945.7907\text{V/V} - 1000\text{V/V}}{1000\text{V/V}} \cdot 100\% = -5.42 \% \text{ error.}$$

At a control voltage of  $0.5\text{V}$ , the output voltage is  $-2.9273\text{V}$ . This indicates a gain of

$$G|_{V_{CTRL}=0.5} = \frac{-2.9273\text{V}}{11\text{mV}} = 2927.3\text{V/V}.$$

Relative to the desired  $3000\text{V/V}$ , this is an error of,

$$\% \text{ error} = \frac{2927.3\text{V/V} - 3000\text{V/V}}{3000\text{V/V}} \cdot 100\% = -2.42 \% \text{ error.}$$

At a control voltage of  $1\text{V}$ , the output voltage is  $-4.9088\text{V}$ . This indicates a gain of

$$G|_{V_{CTRL}=1} = \frac{-4.9088V}{-1mV} = 4908.8V/V.$$

Relative to the desired 5000V/V, this is an error of,

$$\% \text{ error} = \frac{4908.8V/V - 5000V/V}{5000V/V} \cdot 100\% = -1.82 \% \text{ error.}$$

The voltage gain is predominantly a linear function of control voltage as seen in figure 10 and through this analysis. At 0V control voltage, the gain was within the spec of 1000V/V  $\pm$  10%. At 1V control voltage, the gain was within the spec of 5000V/V  $\pm$  10%. In fact, as control voltage increased, the gain error decreased. These results align with the results seen in the positive input voltage section.

The following plot shows the output voltage as a function of the control voltage for a constant input voltage of  $-5mV$ .

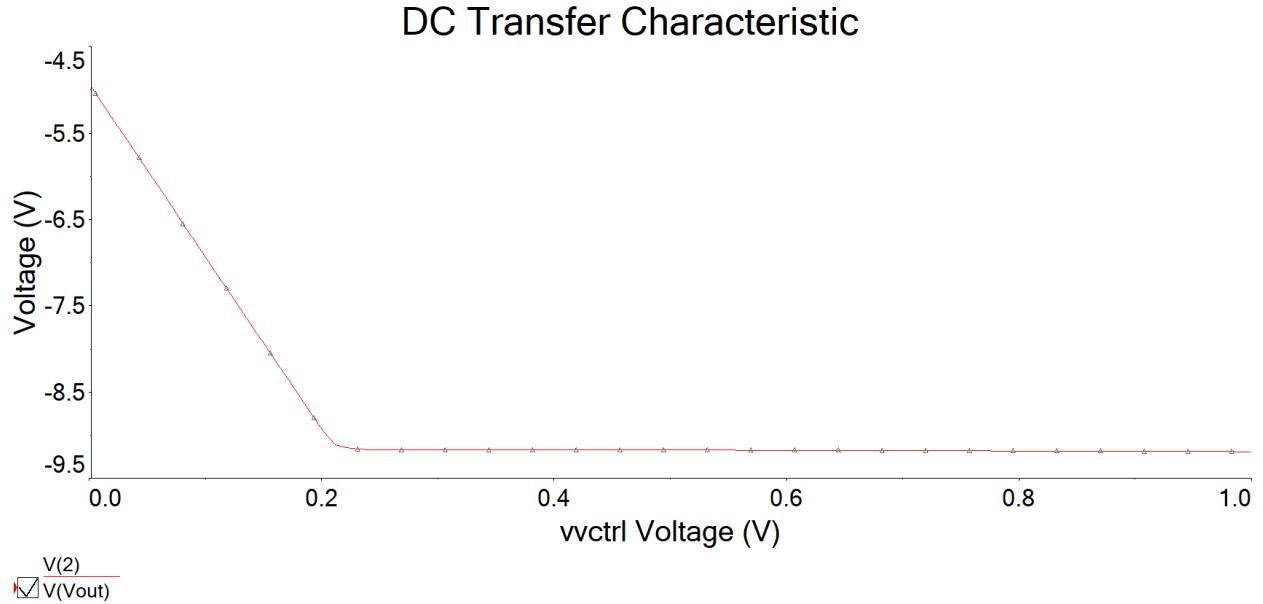


Figure 11: Control Voltage Sweep for  $-5mV$  Input

Similar to that of the positive input voltages, the output voltage quickly saturates as the various op-amps throughout the circuit saturate. However, this is not an issue since the output voltage should be  $\pm 5V$  as per the requirements of the assignment.

## 7.2 Sinusoidal Inputs and THD

In this section, sinusoidal inputs are explored and distortion is quantified using total harmonic distortion (THD) as part of the Fourier analysis in Multisim.

The OP177 op-amps have very small input bias current and offset voltage, however they are lacking in terms of slew rate. Due to this, the gain of the system is diminished as input frequency increases. Thus, a low frequency signal will be used to test for harmonic distortion. A 100Hz, 1mVp signal was chosen.

The following plot shows a transient simulation of the output voltage when the system is subjected to this test signal.

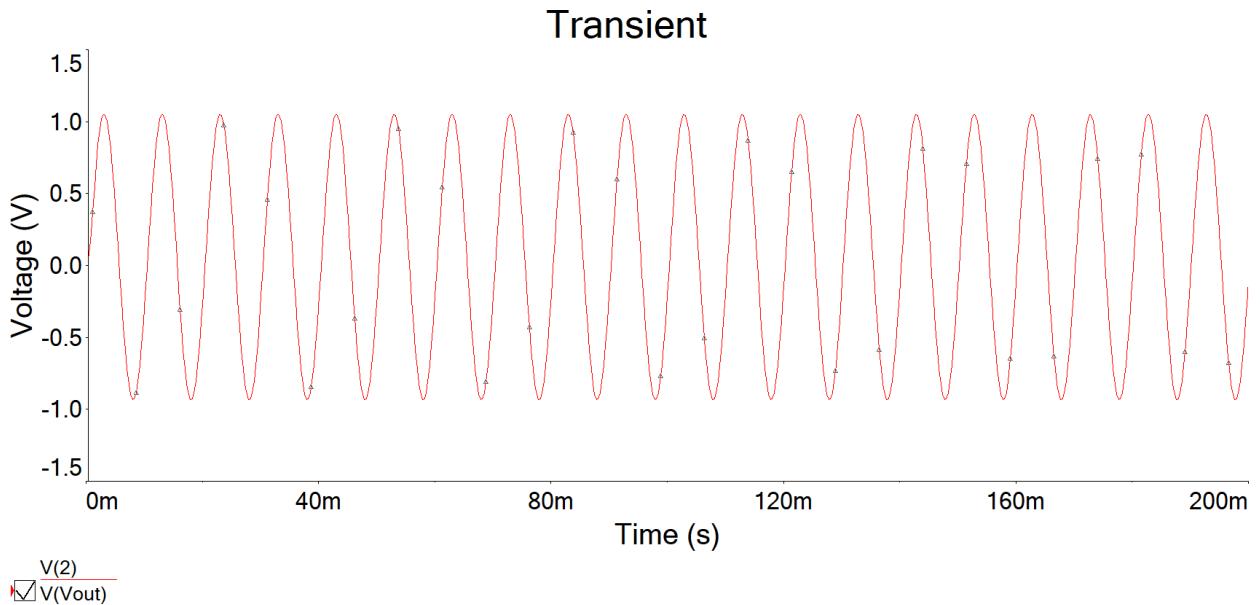


Figure 12: Transient Simulation for  $V_{in} = 1\text{mV} \cdot \sin(2\pi \cdot 100\text{Hz} \cdot t)$

A Fourier analysis is conducted to quantify the total harmonic distortion present in the output. The results are shown below in figure 13.

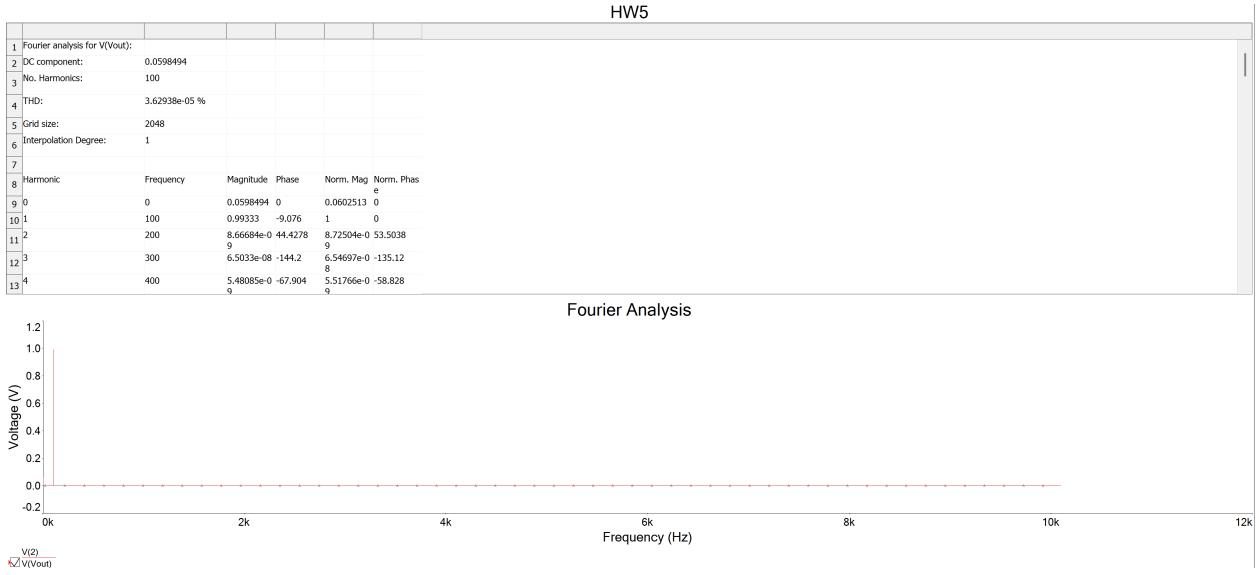


Figure 13: Fourier Analysis for  $V_{in} = 1\text{mV} \cdot \sin(2\pi \cdot 100\text{Hz} \cdot t)$

This analysis results in a THD of  $3.63 \times 10^{-5}\%$ , or 0.0000363%. This is quite minimal, and is acceptable for this assignment.

### 7.3 Passive Component Tolerances

To analyze the impact of passive component tolerances on the system, various control voltages are used along with a constant 1mV input signal. The following table summarizes these results.

Control Voltage (V)	Expected Output (V)	Nominal Run (V)	Worst Case (V)
0	1	1.06549	1.14624
0.25	2	2.07593	2.21154
0.5	3	3.08636	3.29842
0.75	4	4.09680	4.38531
1	5	5.10724	5.47219

Table 1: Worst Case Runs for Various Control Voltages:  $V_{in} = 1\text{mV}$

It appears as though the nominal run and worst case run both consistently amplify the input signal too much. A logical next step would be to decrease the gain of the final amplifying stage, however negative input voltages must first be analyzed. The following table summarizes the results when a constant  $-1\text{mV}$  input is applied.

Control Voltage (V)	Expected Output (V)	Nominal Run (V)	Worst Case (V)
0	-1	-0.94579	-0.87390
0.25	-2	-1.93655	-1.81343
0.5	-3	-2.92732	-2.73441
0.75	-4	-3.91808	-3.65540
1	-5	-4.90884	-4.57638

Table 2: Worst Case Runs for Various Control Voltages:  $V_{in} = -1\text{mV}$

Opposite to what happened with a 1mV input, a  $-1\text{mV}$  input is consistently under-amplified over the control voltage range. This would require the gain of the final amplifying stage to increase. However, since the gain of the final amplifying stage can not both increase and decrease, the consequences of passive component tolerances can not be dealt with.

From table 1 and table 2, a percentage error between the measured and desired gain can be calculated. In both instances, the highest percent error is at a control voltage of 0V. For a 1mV input, the worst case percent error is 14.62%. For a  $-1\text{mV}$  input, the worst case percent error is  $-12.61\%$ . This is outside the  $\pm 10\%$  gain tolerance as per the requirements of the assignment. However, it is extremely unlikely that the worst case scenario will actually occur in practice, and thus a Monte Carlo simulation will give a better approximation as to how passive component tolerances will affect the performance of the system.

The following table summarizes the results of the Monte Carlo simulation. Note that 500 runs were used.

Input (mV)	Mean $\mu$ (V)	Std. Dev. $\sigma$ (mV)	$\mu - 3\sigma$	$\mu + 3\sigma$	% Error Range
1	1.06523	8.06927	1.0411	1.0895	4.11% – 8.95%
-1	-0.946459	8.4814	-0.971903	-0.921015	-2.81% – -7.90%

Table 3: Monte Carlo Simulation Results

Approximately 99.7% of data falls within 3 standard deviations from the mean, thus this metric is used to more accurately depict the performance of the system with non-ideal components. The results as shown in table 3 indicate that the system is performing within the  $\pm 10\%$  gain tolerance, despite having passive component tolerances.

## 8 Conclusion

The variable gain amplifier analyzed in this report was a success as per the requirements of the assignment, however this system still has room for improvement. The AD633 multiplication IC introduced a voltage offset of more than a few millivolts, and this error is then amplified. This IC was chosen for its simplicity and that it was one of few multiplication ICs in Multisim. To further improve this system and implementing this architecture, a better designed multiplication circuit would be necessary. Further improvements may be made by considering other architectures, such as a voltage controlled resistor.

# Power Conversion Project Summary

Dillon Labonte and Sam Norton

# Contents

- Introduction
- Rectifier Circuit
- Boost Converter Circuit
- Complete Power Converter Circuit
- Conclusion

# Introduction

Power grids operate with alternating current (AC) for efficient distribution. Converting AC to direct current (DC) allows electronics to operate more safely and more reliably.

Household outlets provide 120V, but many electronics require much less. In order for these devices to get power from the supply inside the outlet, this energy needs to be converted from this 120V AC to the desired DC.

# Rectifier Circuit

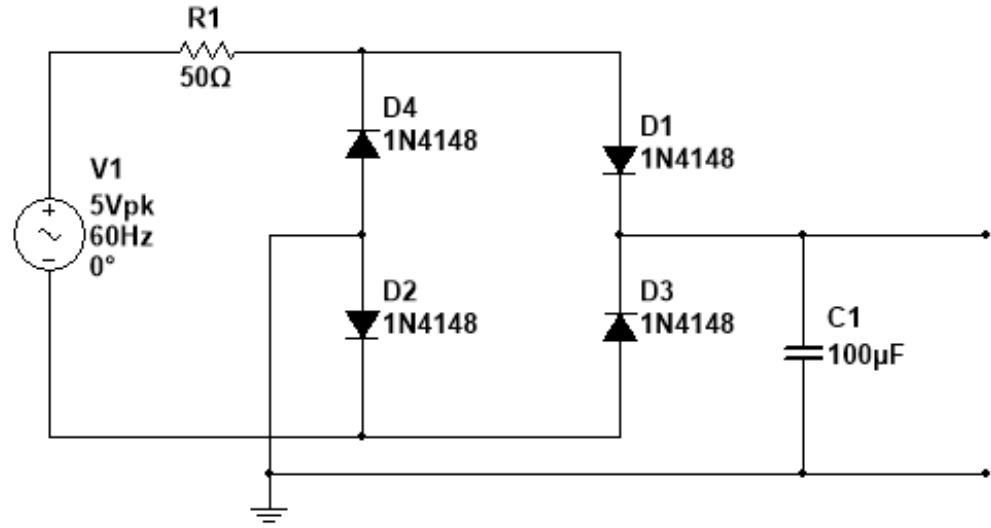


Figure ?. Rectifier Circuit

- A rectifier is a device that converts AC to DC
  - Diodes allow current to flow in only one direction
  - When voltage changes the current will charge and discharge the capacitor
  - Capacitor smooths ripple effect on output voltage

# Testing Rectifier Circuit

Tested using a 5Vpk 60Hz input signal

Oscilloscope measurements taken at various points to confirm proper operation

Comparison with simulation

Tested output voltage and ripple as a function of load resistance

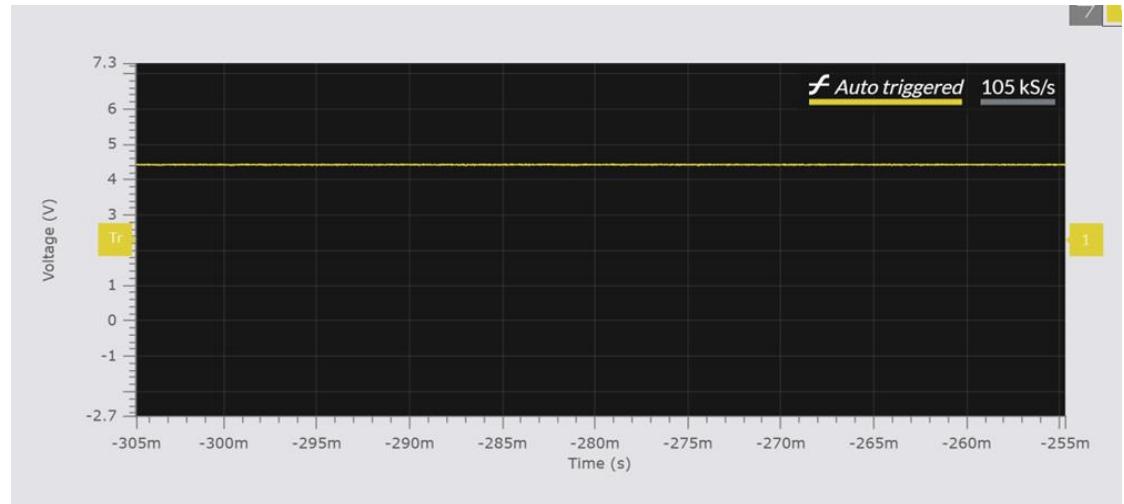


Figure 1. Rectifier Output with No Load

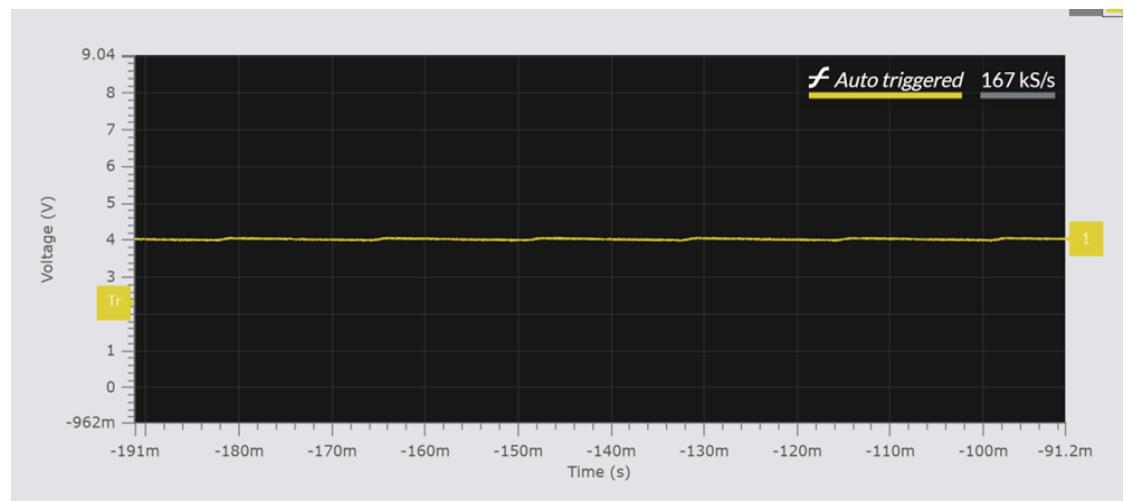


Figure 2. Rectifier Output with 10k $\Omega$  Load

# Rectifier Circuit Results

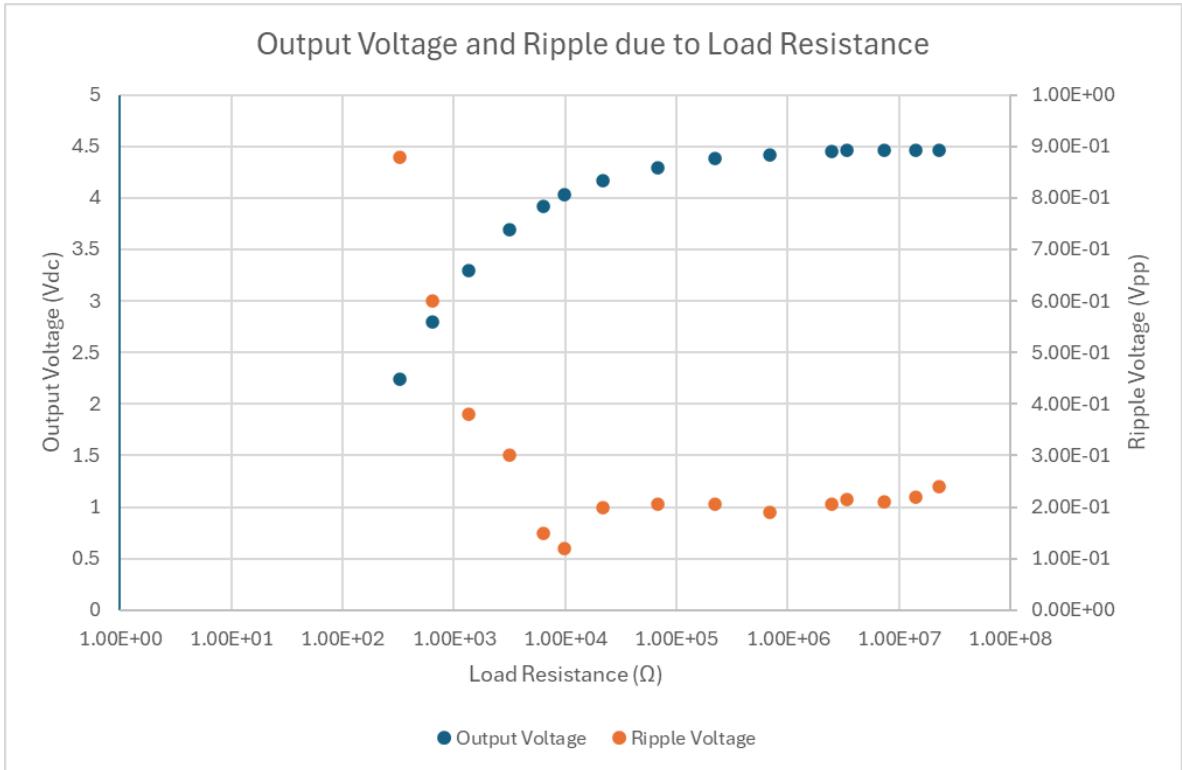


Figure 3. Rectifier Circuit Results

- Output voltage increased as load resistance increased
- Ripple voltage decreased as load resistance increased
- Ripple voltage not very accurate due to noise and fluctuations

# Boost Converter Circuit

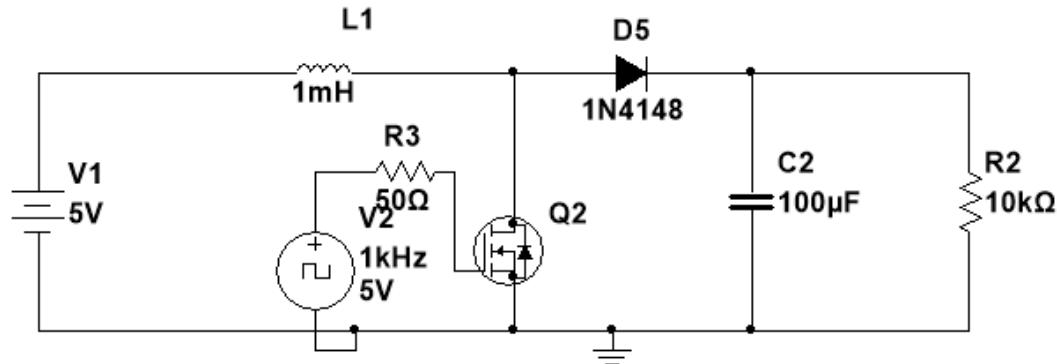


Figure 4. Boost Converter Circuit

- A boost converter steps up DC voltage
  - Energy is stored up in the inductor when the switch is closed
  - Stored energy is released into the load when the switch opens, adding to the input voltage

# Testing Boost Converter

Tested using a 5Vdc input

1kHz 5V square wave used as MOSFET signal

Oscilloscope measurements taken at various points to confirm proper operation

Comparison with simulation

Tested output voltage and ripple as a function of load resistance

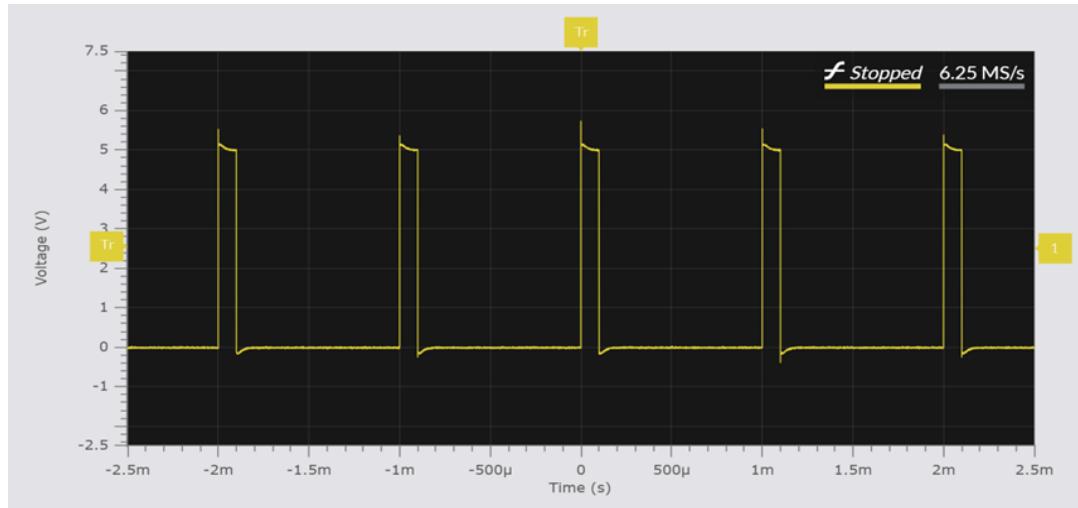


Figure 5. MOSFET Gate Signal



Figure 6. Boost Converter Output with 10k $\Omega$  Load

# Boost Converter Results

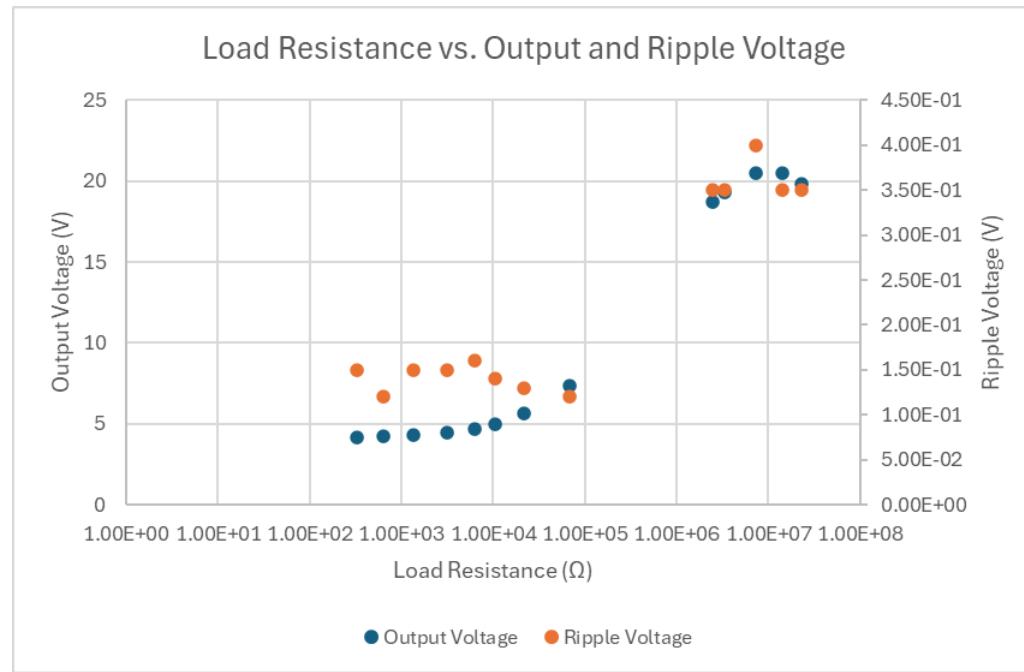


Figure 7. Boost Converter Results

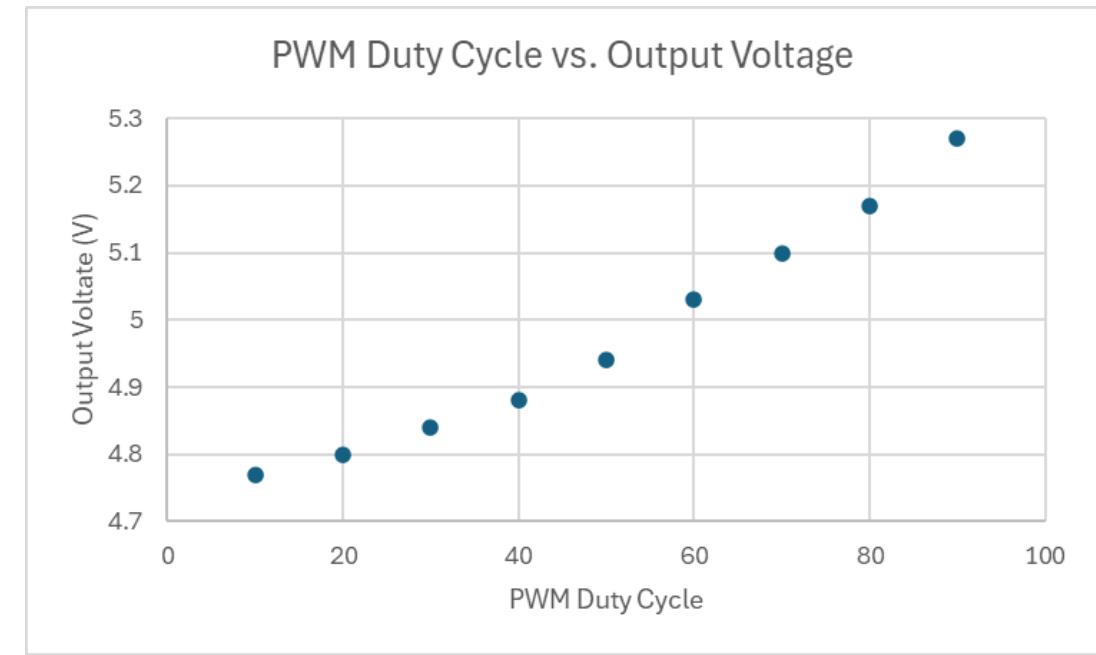


Figure 8. Boost Converter Output vs PWM Duty Cycle

- Output voltage and ripple voltage increased as load resistance increased
- Ripple voltage not very accurate due to noise and fluctuations
- Output voltage increased as duty cycle increased

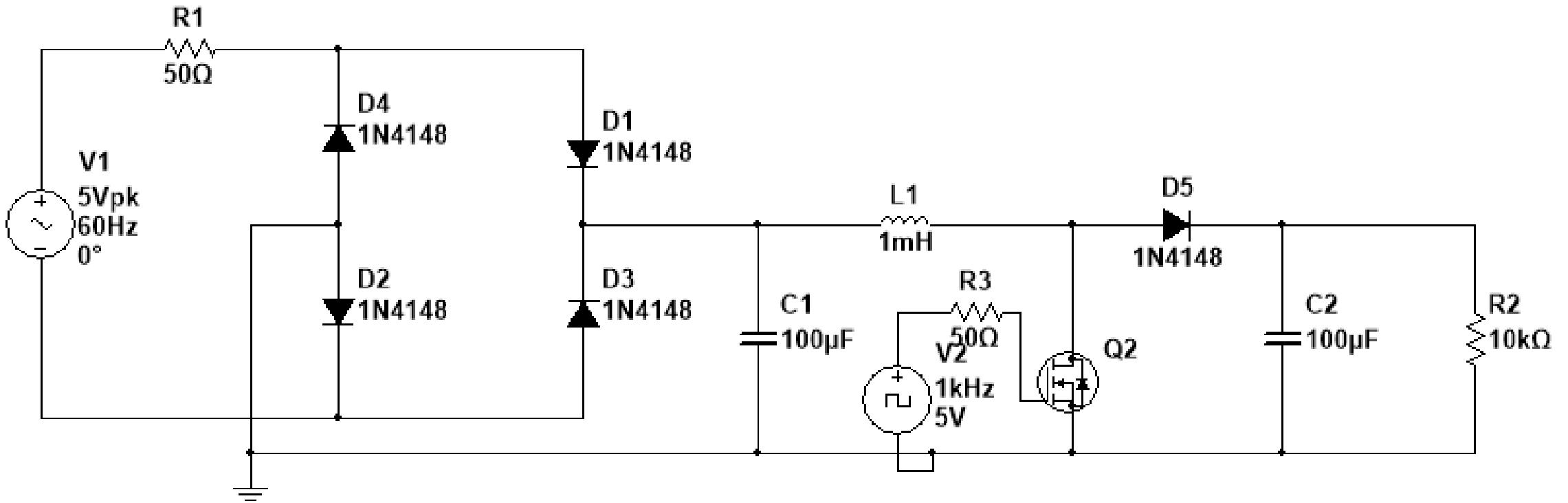


Figure 9. Complete Power Converter Circuit

Combined Circuit – Power  
Conversion

# Testing Complete Circuit

Tested using a 5Vpk 60Hz input to rectifier

1kHz 5V square wave used as MOSFET signal

Oscilloscope measurements taken at various points to confirm proper operation

Comparison with simulation

Tested output voltage and ripple as a function of load resistance

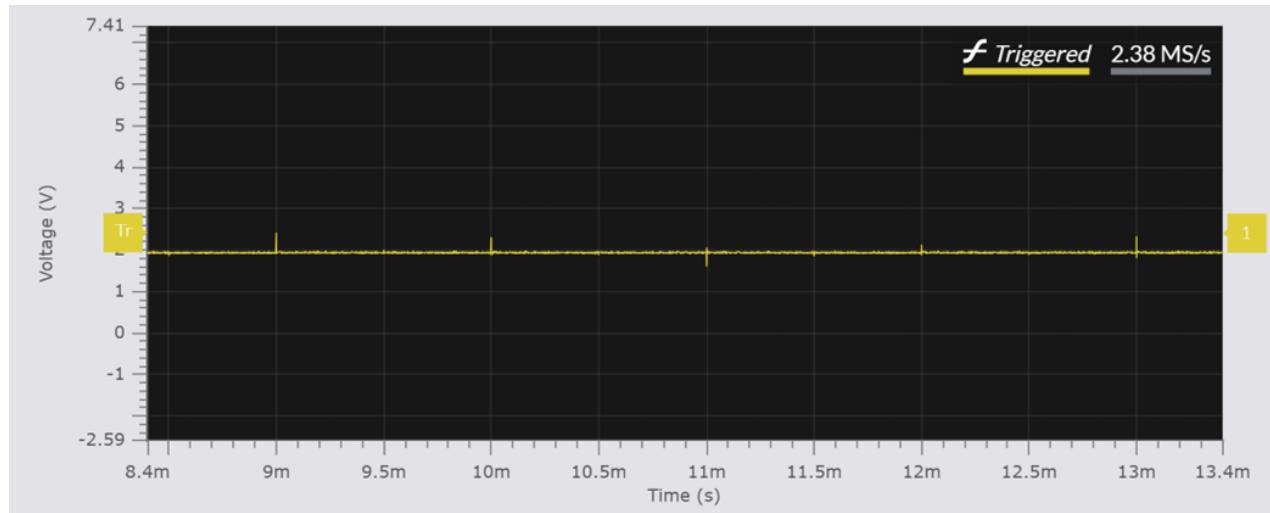


Figure 10. Complete Circuit Output with 10k $\Omega$  Load

# Complete Circuit Results

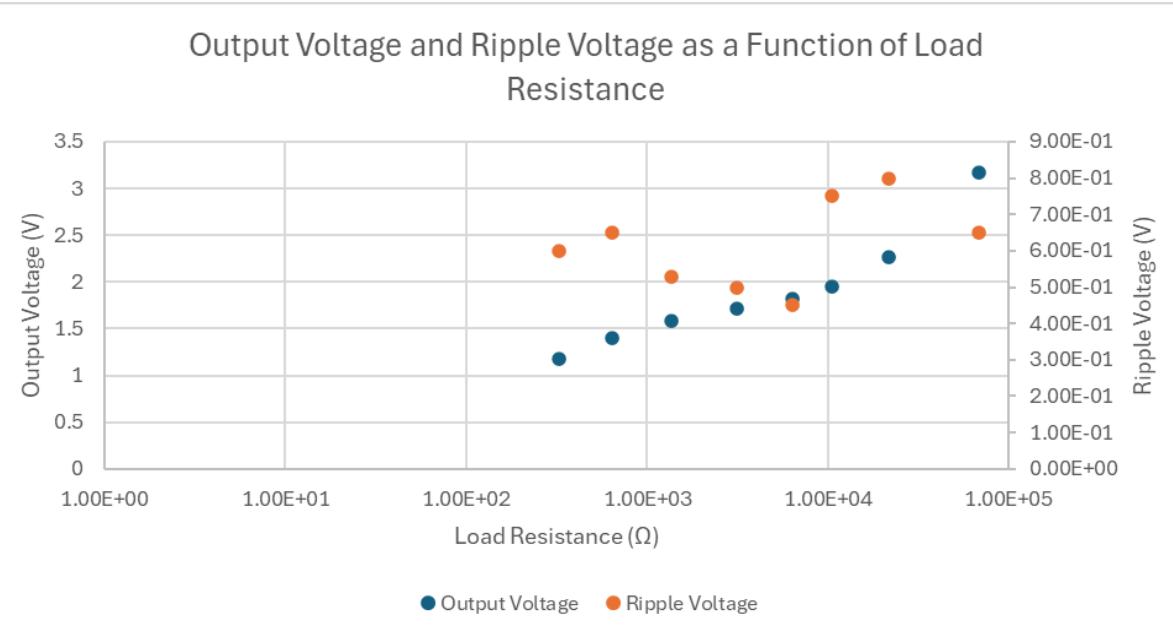


Figure 11. Complete Circuit Results

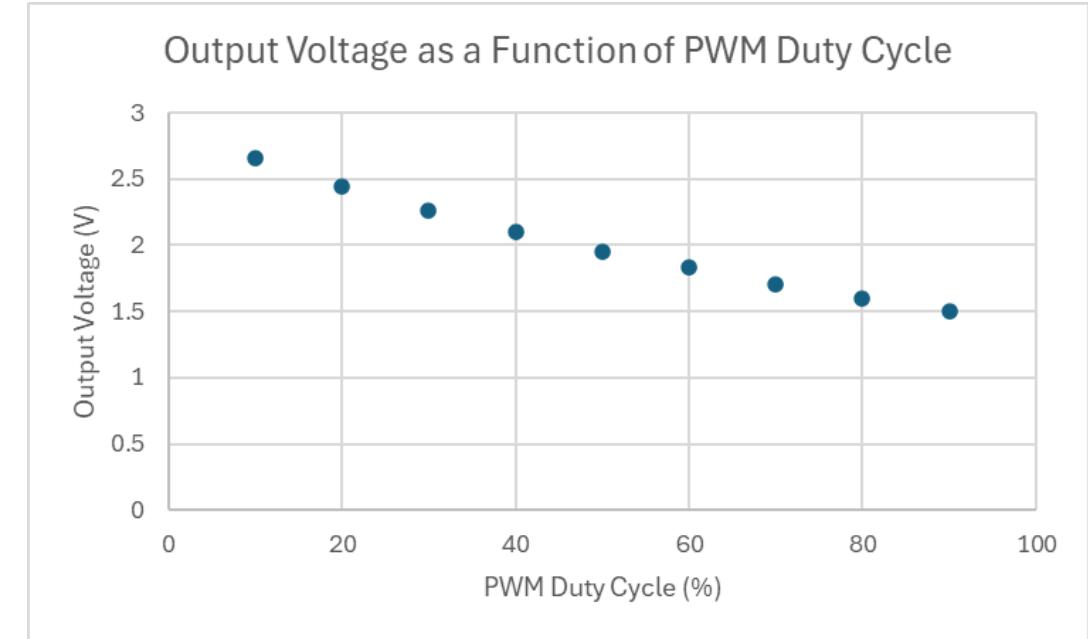


Figure 12. Complete Circuit Output vs PWM Duty Cycle

- Output voltage and ripple voltage increased as load resistance increased
- Ripple voltage not very accurate due to noise and fluctuations
- Output voltage decreased as duty cycle increased

# Conclusion

- Introduction to power converter circuits
- Practice with Measurements Live
- Practice with lab troubleshooting