



Chair of High-Power Converter Systems
TUM School of Engineering and Design
Technical University of Munich
Prof. Dr.sc. ETH Zürich Marcelo Lobo Heldwein

Research and Development of Power Control Middleware Algorithms (PLL, MPPT)

Haoheng Li



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Report of Research Internship

to pass the research internship

Master of Science
(M.Sc.)

in Power Engineering

at Technical University of Munich

Submitted by Haoheng Li
Matriculation Number: 03797669
haoheng.li@tum.de

on Friday 24th October, 2025

Supervisor: Maia de Sousa, Dr. Gean
Chair of High-Power Converter Systems
Technical University of Munich
gean.sousa@tum.de

Declaration

The work in this report is based on research carried out at the Chair of High-Power Converter Systems, Technical University of Munich (TUM) supervised by Maia de Sousa, Dr. Gean. No part of this report has been submitted elsewhere for any other academic degree or qualification and it is all my own work unless referenced to the contrary in the text.

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Abstract

This report presents the research and development of power control middleware algorithms, specifically focusing on Phase-Locked Loop (PLL) and Maximum Power Point Tracking (MPPT) techniques. The research internship was conducted at Infineon Technologies AG, under the supervision of Dr. Gean Maia de Sousa at the Chair of High-Power Converter Systems, TUM. The objective of this research is to design and evaluate the performance of PLL and MPPT algorithms in power electronic systems, which will finally outcome a repository containing the developed algorithms using Model Based Design (MBD) approach. The outcome can be seen in the GitHub repository: <https://github.com/labourer-Lucas/Research-Inernship-PLL-and-MPPT>.

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CHAPTER 1

Introduction

1.1 Background of the Internship

I have been a research intern at Infineon Technologies AG since July, 2025, working as a Power Control Algorithm Intern. I was responsible for developing and implementing middleware control algorithms for power electronics systems, specifically focusing on PLL and MPPT algorithms using Model Based Design (MBD). With aid of MATLAB/Simulink, I designed the algorithms and tested them in a simulated environment. Finally, I generated C code from the Simulink models using Embedded Coder.

1.1.1 Company Overview

Infineon Technologies AG is a global leader in semiconductor solutions, providing innovative technologies for various applications, including automotive, industrial, and consumer electronics.

I was working in the Power & Sensor Systems (PSS) division, which focuses on developing advanced sensor solutions and power management technologies. The PSS division powers Infineon's decarbonization and digitalization vision with a wide range of energy-efficient and digital solutions.

1.1.2 Project Overview

The project "Power Control Middleware" aims to develop and implement middleware control algorithms for power electronics systems, such as PLL, MPPT, Kalman Filter, and 3-zero-3-pole filters. During my internship, I focused on the PLL and MPPT algorithms.

1.2 Objective of the Internship

The main objectives of my internship were to:

- Develop and implement PLL and MPPT algorithms using MBD
- Test the algorithms in a simulated environment using MATLAB/Simulink and evaluate their performance
- Generate C code from the Simulink models using Embedded Coder
- Document the development process and results in a comprehensive report

1.2.1 Phase-Locked Loop (PLL)

Grid synchronization is the process by which power converters, especially those connected to renewable energy sources, ensure that the power injected by the inverter is aligned with the grid. This includes estimating and matching the phase angle, frequency, and voltage magnitude.

Grid synchronization can be achieved using various control techniques. The primary tool for achieving this is PLL. The latter consists of a feedback control loop that follows the frequency and phase of its input signal. In grid-tied applications, the PLL input is the grid voltage. Moreover, some advanced grid synchronization methods combine the PLL with filters applied to the input voltage. Such a combination allows for robust and precise estimation of the above-mentioned grid parameters even under unbalanced voltages, harmonic distortions, or voltage sags.

In my internship, I developed and implemented synchronous reference frame PLL (SRF-PLL), Double Decoupled Synchronous Reference Frame (DDSRF) PLL, Second-Order Generalized Integrators (SOGI) PLL, Dual-Second-Order Generalized Integrators (DSOGI) PLL, and Multiple Second-Order Generalized Integrators (MSOGI) PLL.

1.2.2 Maximum Power Point Tracking (MPPT)

MPPT is a family of control algorithms that aims at optimizing the use of a power source that possesses a fluctuating power profile.

In my research internship, I focus on developing the MPPT algorithms for DC optimizers, which are power electronic devices that are connected to individual solar panels in a photovoltaic (PV) system. I developed and implemented Perturb and Observe (P&O) and Incremental Conductance (InC) MPPT algorithms.

1.3 Structure of the Report

The first chapter introduces the background and objectives of the internship. The second chapter provides a detailed overview of the PLL and MPPT algorithms, including their principles, types, and applications. The third chapter describes the design and implementation of the PLL and MPPT algorithms using MBD, including the Simulink models. The fourth chapter presents

the testing and evaluation of the algorithms in a simulated environment, including performance analysis and results. Finally, the fifth chapter concludes the report with a summary of the work done, challenges faced, and future work suggestions.

CHAPTER 2

Algorithm Development for PLL

2.1 Overview of PLL and its Applications and Development

The increasing penetration of renewable energy into the grid necessitates the employment of grid synchronization techniques to ensure proper integration and stability of the system. Several grid synchronization techniques are available, among which the PLL method has proven to be the more employed one owing to its simplicity and robustness.

Despite being able to provide effective operation of the system under variable grid conditions this technique faces certain technological challenges. This paper studies, in detail, the various PLL techniques that are implemented in the Renewable Energy Sectors such as Synchronous Reference Frame (SRF-PLL), Decoupled Double Synchronous Reference Frame (DDSRF-PLL), Second Order General Integrator (SOGI-PLL), Dual Second Order General Integrator (DSOGI-PLL), and Multi Second Order General Integrator (MSOGI-PLL). The different techniques of the PLL are compared and analyzed based on their efficiency, response to voltage and frequency deviations, complexity, and stability. SRF-PLL gives excellent response under balanced grid conditions, but E-PLL, FLL and SOGI based PLLs are more efficient to address unbalanced grid conditions. The limitations of the PLL technique such as reduced stability margin and manufacturing costs, has lead to the development of improved and new PLLs, which are under research.

2.2 Synchronous Reference Frame PLL

2.2.1 SRF-PLL concept

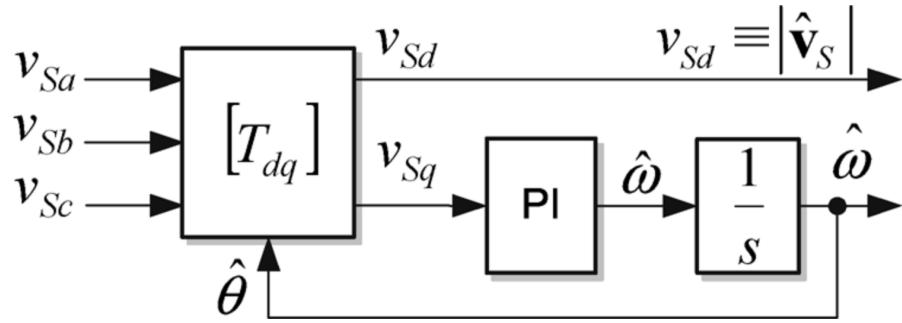


Figure 2.1: Block diagram of a typical SRF-PLL

A synchronous reference frame PLL is a basic type of phase-locked loop based on the Park transform [1]. In a nutshell, the SRF PLL is built using a Park transformation that acts as a phase detector, a low-pass filter (LPF) usually in the form of a PI regulator, and a voltage-controlled oscillator (VCO) typically made from an integrator. The objective of this PLL is then to minimize either the direct or quadrature axis reference voltage. This will then ensure that the phase angle of the rotating reference frame of the park transformation matches the phase angle of the utility grid voltage vector. The block diagram of a typical SRF-PLL is shown in

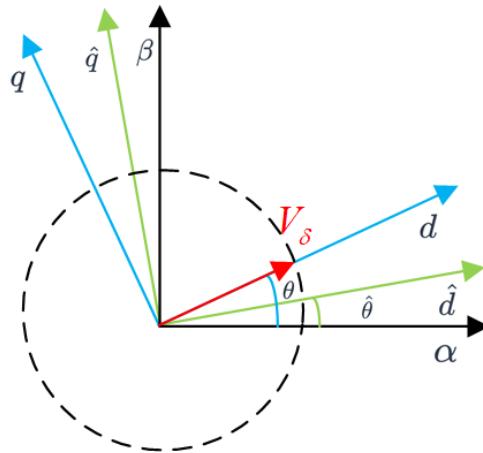


Figure 2.2: $d - q$ and $\hat{d} - \hat{q}$ Frame

Fig. 2.1. In the conventional SRF-PLL, the three-phase voltage vector is translated from the abc reference frame to the dq reference frame using the Park transformation. The angular position of this dq reference frame is controlled by a feedback loop which regulates the q component to

zero. Therefore in steady-state, the d component depicts the voltage vector amplitude and its phase is determined by the output of the feedback loop.

As shown in Figure 2.2 ,the actual phase angle of V_δ is θ , and the phase angle estimated by the PLL is $\hat{\theta}$. The corresponding $d - q$ and $\hat{d} - \hat{q}$ are rotating coordinate systems. Define $\delta = \theta - \hat{\theta}$, then

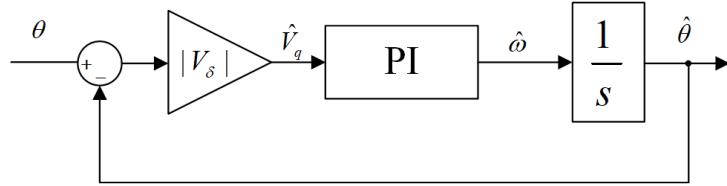


Figure 2.3: Block diagram of SRF-PLL in small signal model

$$\hat{V}_q = V_\delta \cdot \sin(\delta) \quad (2.1)$$

When δ is very small, $\sin(\delta) \approx \delta = \theta - \hat{\theta}$, and thus the control block diagram of the PLL can be depicted.

Figure 2.3 shows the small signal model of the SRF-PLL. However, in practical applications, this model is sensitive to the variation of the grid voltage amplitude. Thus, in order to compensate for that, we are going to design a normalized PLL in this section. The block diagram of normalized PLL is shown in Figure 2.4.

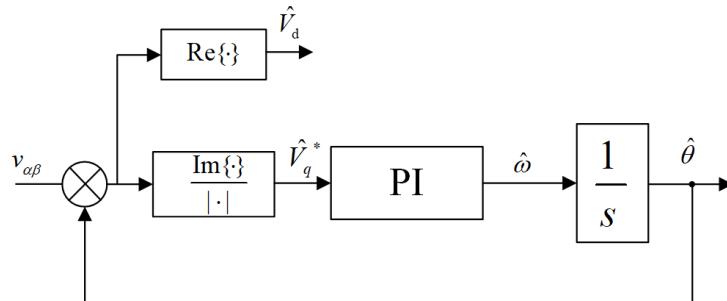


Figure 2.4: Block diagram of normalized SRF-PLL

Therefore, the close loop transfer function of the system can be written as:

$$G_{cl}(s) = \frac{\hat{\theta}(s)}{\theta(s)} = \frac{K_p s + K_i}{s^2 + K_p s + K_i} \quad (2.2)$$

where K_p and K_i are the proportional and integral gains of the PI controller, respectively. The natural frequency ω_n and damping ratio ζ of the system can be defined as:

$$\omega_n = \sqrt{K_i} \quad (2.3)$$

$$\zeta = \frac{K_p}{2\sqrt{K_i}} \quad (2.4)$$

In practical applications, the SRF-PLL is usually designed with a damping ratio of $\zeta = 0.707$ to ensure a good dynamic response without overshoot. The natural frequency ω_n is typically chosen to be around 30Hz. A higher value of ω_n results in a faster dynamic response but may also lead to increased sensitivity to noise and harmonics in the grid voltage.

2.2.2 SRF-PLL under different grid conditions

To simply test the performance of the SRF-PLL under different grid conditions, a simulation is carried out in MATLAB/Simulink. The parameters of the SRF-PLL are chosen with a natural frequency of $\omega_n = 50\text{Hz}$ and a damping ratio of $\zeta = 0.707$.

The result of SRF-PLL under balanced grid conditions with a phase shift of 180° at $t = 0.1\text{s}$ is shown in Figure 2.5. It can be observed that the SRF-PLL can quickly track the phase angle of the grid voltage.

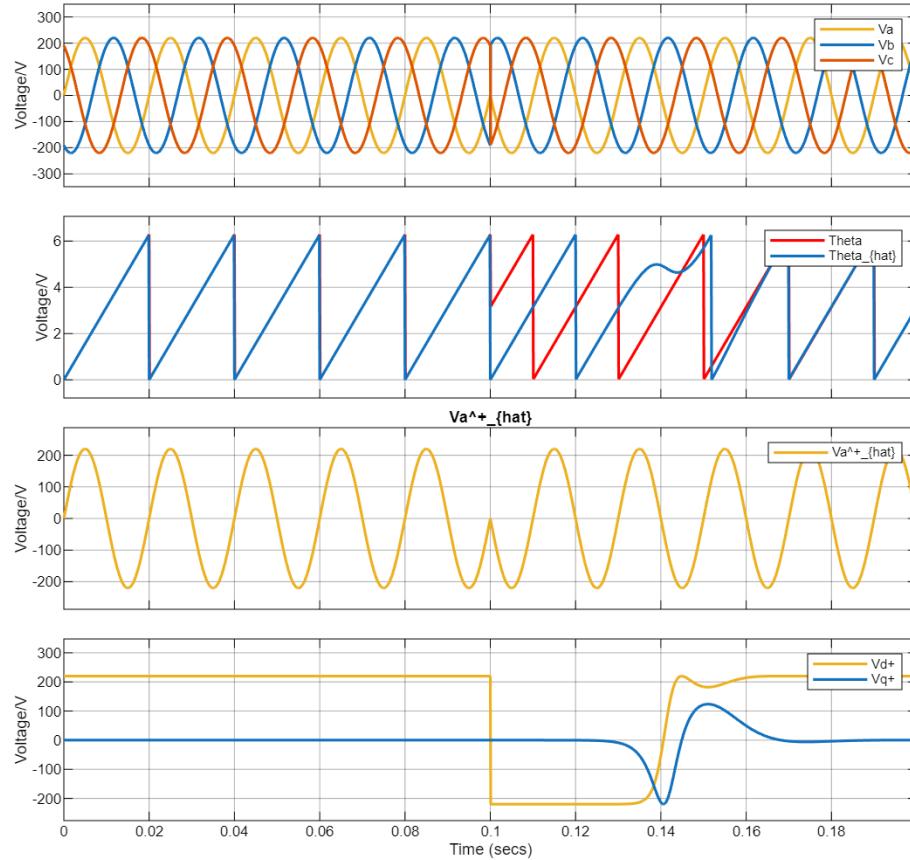


Figure 2.5: Response of the SRF-PLL with a phase shift at $t=0.1\text{s}$ under balanced conditions. Utility voltage [V], Detected phase angle [rad], Fundamental voltage [V] and SRF axes voltage [V]

The result of SRF-PLL under unbalanced grid conditions with a negative sequence component of 30% and a phase shift of 180° at $t = 0.1\text{s}$ is shown in Figure 2.6. It can be observed that the SRF-PLL can still track the phase angle of the grid voltage, but with some oscillations

in the detected phase angle due to the unbalance in the grid voltage. In addition, the d and q axis voltages also show oscillations at twice the fundamental frequency, which can affect the performance of the PLL.

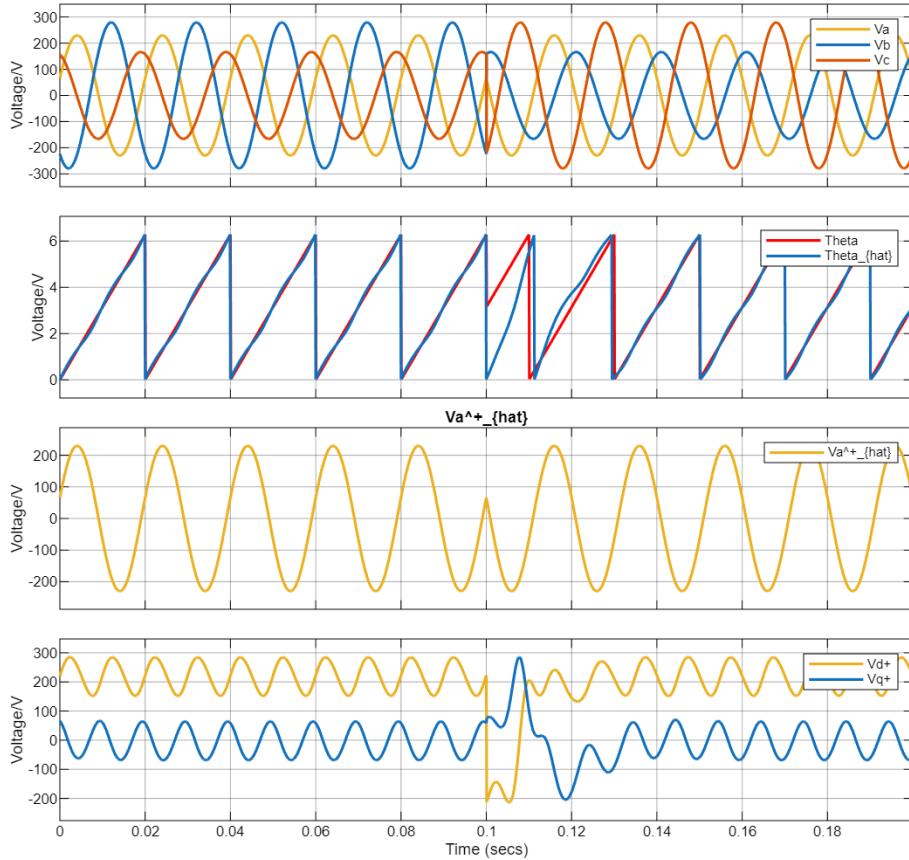


Figure 2.6: Response of the SRF-PLL with a phase shift at $t=0.1s$ under unbalanced conditions. Utility voltage [V], Detected phase angle [rad], Fundamental voltage [V] and SRF axes voltage [V]

The result of SRF-PLL under grid conditions with 30% of the 5th harmonics and a phase shift of 180° at $t = 0.1s$ is shown in Figure 2.7. It can be observed that the SRF-PLL can still track the phase angle of the grid, but with some oscillations in the detected phase angle due to the presence of harmonics in the grid voltage. The d and q axis voltages also show oscillations at the harmonic frequencies, which can affect the performance of the PLL.

In conclusion, the SRF-PLL is a simple and effective method for grid synchronization under balanced grid conditions. However, its performance can be affected by unbalanced grid conditions and the presence of harmonics in the grid voltage. Therefore, for applications where the grid conditions are expected to be unbalanced or distorted, more advanced PLL techniques should be discussed in the following sections.

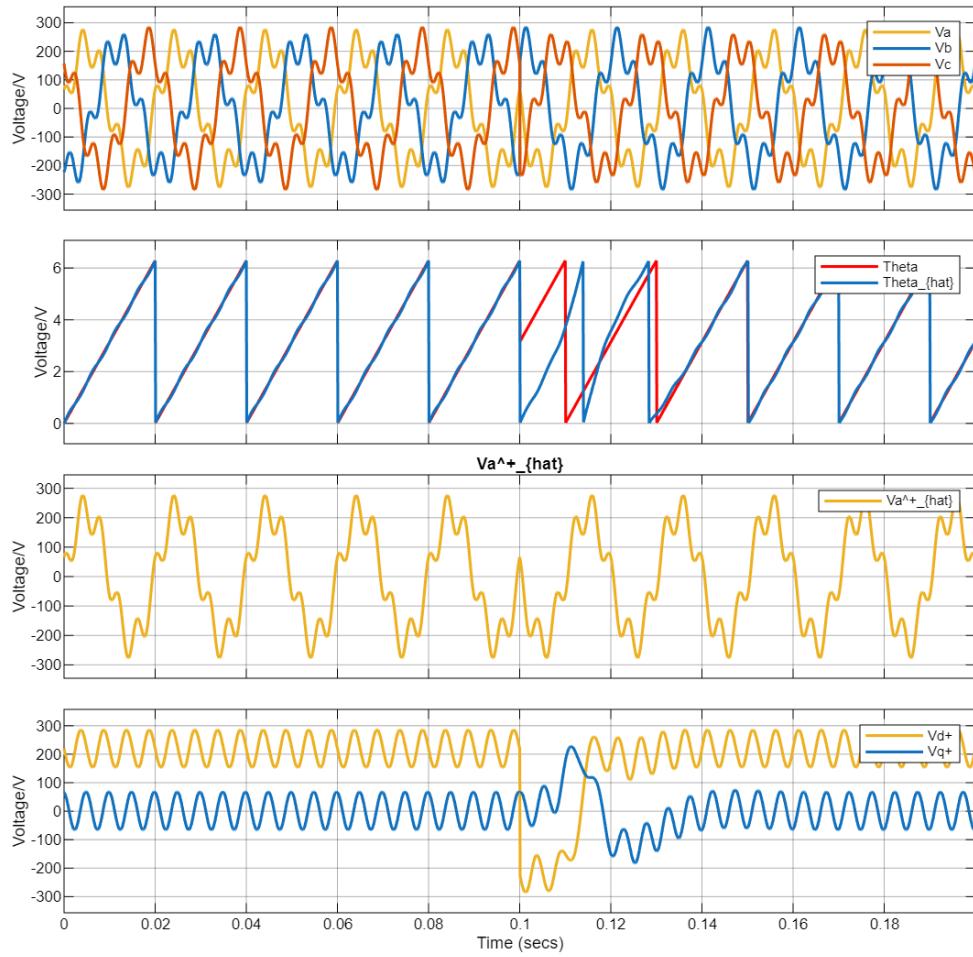


Figure 2.7: Response of the SRF-PLL with a phase shift at $t=0.1\text{s}$ under grid conditions with 30% of the 5th harmonics. Utility voltage [V], Detected phase angle [rad], Fundamental voltage [V] and SRF axes voltage [V]

2.3 Decoupled Double Synchronous Reference Frame PLL

2.3.1 DDSRF-PLL concept

Thanks to its simplicity and performance under nominal conditions, the SRF-PLL has become the PLL of choice for applications where robustness against disturbances is not required. However, in the presence of unbalance in the grid voltage, an oscillating term at twice the fundamental frequency appears after the Park transform. The DDSRF-PLL effectively addresses this issue by using a decoupling network to separate the positive and negative sequence components, ensuring accurate detection even under unbalanced voltages [2].

The grid is subject to varying conditions which result in imbalances in the phase voltages. From the theory of symmetrical components we know that any unbalanced three phase system can be reduced to two symmetrical systems and zero component. The behavior of unbalanced voltages on park and clark transform is analyzed in section below.

Now an unbalanced three phase system can be written as summation of balanced three phase

systems; one rotating with the sequence of the three phase quantities called the positive sequence and one rotating in the opposite sequence called the negative sequence, which is shown in Figure 2.8.

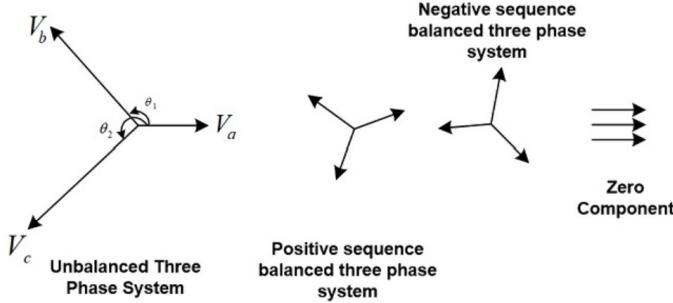


Figure 2.8: Unbalanced and balanced Three Phase Systems

The mathematical representation of the unbalanced three phase system is given as:

$$v = V^{+1} \begin{bmatrix} \cos(wt) \\ \cos(wt - 2\pi/3) \\ \cos(wt - 4\pi/3) \end{bmatrix} + V^{-1} \begin{bmatrix} \cos(wt) \\ \cos(wt - 4\pi/3) \\ \cos(wt - 2\pi/3) \end{bmatrix} + V^0 \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (2.5)$$

If we apply the Clark transformation to the symmetrical components, we get the following results:

$$\nu_{\alpha\beta} = T_{abc \rightarrow \alpha\beta} \cdot v = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot v = V^{+1} \begin{bmatrix} \cos(wt) \\ \sin(wt) \end{bmatrix} + V^{-1} \begin{bmatrix} \cos(-wt) \\ \sin(-wt) \end{bmatrix} \quad (2.6)$$

Taking the projections on the rotating reference frame, we observe that any negative sequence component appears with twice the frequency on the positive sequence rotating frame axis and vice versa.

$$\left\{ \begin{array}{l} \nu_{dq+} = T_{abc \rightarrow dq0+}^* \nu_{\alpha\beta} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} = V^{+1} \begin{bmatrix} 1 \\ 0 \end{bmatrix} + V^{-1} \begin{bmatrix} \cos(-2\omega t) \\ \sin(-2\omega t) \end{bmatrix} \\ \nu_{dq-} = T_{abc \rightarrow dq0-}^* \nu_{\alpha\beta} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} = V^{+1} \begin{bmatrix} \cos(-2\omega t) \\ \sin(-2\omega t) \end{bmatrix} + V^{-1} \begin{bmatrix} 1 \\ 0 \end{bmatrix} \end{array} \right. \quad (2.7)$$

This can cause errors in the control loop and estimation of the grid angle and needs to be taken into account while designing a phase locked loop for three phase grid connected application, like shown in Figure .

Hence assuming the instance just before the PLL is locked to the positive vector, the grid voltages can be written as :

$$v = V^{+1} \begin{bmatrix} \cos(\omega t + \phi_1) \\ \cos(\omega t - 2\pi/3 + \phi_1) \\ \cos(\omega t - 4\pi/3 + \phi_1) \end{bmatrix} + V^{-1} \begin{bmatrix} \cos(\omega t + \phi_{-1}) \\ \cos(\omega t - 4\pi/3 + \phi_{-1}) \\ \cos(\omega t - 2\pi/3 + \phi_{-1}) \end{bmatrix} + V^0 \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (2.8)$$

Figure 2.9 shows the positive and negative sequence components in the alpha-beta frame. The positive sequence vector rotates in the positive direction while the negative sequence vector rotates in the negative direction.

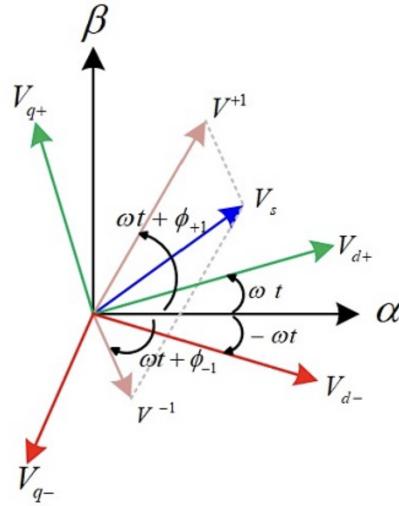


Figure 2.9: Positive and Negative sequence in alpha-beta frame

Taking the clark transform and ignoring the zero component and the zero sequence, we have:

$$V_{\alpha\beta} = V^{+1} \begin{bmatrix} \cos(\omega t + \phi_{+1}) \\ \sin(\omega t + \phi_{+1}) \end{bmatrix} + V^{-1} \begin{bmatrix} \cos(-\omega t + \phi_{-1}) \\ \sin(-\omega t + \phi_{-1}) \end{bmatrix} \quad (2.9)$$

If we take park transform and lock the angle by the positive sequence component, we have:

$$v_{dq+} = \left(V^{+1} \begin{bmatrix} \cos(\omega t + \phi_{+1}) \\ \sin(\omega t + \phi_{+1}) \end{bmatrix} + V^{-1} \begin{bmatrix} \cos(-\omega t + \phi_{-1}) \\ \sin(-\omega t + \phi_{-1}) \end{bmatrix} \right) \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \quad (2.10)$$

By solving the above equation we can get the decoupled value of v_{dq+} as:

$$\begin{cases} v_{d+_{decoupled}} = V^{+1} \cos(\phi_{+1}) = v_{d+} - \bar{v}_{d-} \cos(2\omega t) - \bar{v}_{q-} \sin(2\omega t) \\ v_{q+_{decoupled}} = V^{+1} \sin(\phi_{+1}) = v_{q+} + \bar{v}_{d-} \sin(2\omega t) - \bar{v}_{q-} \cos(2\omega t) \end{cases} \quad (2.11)$$

Therefore, the block diagram of the DDSRF-PLL with decoupling network is shown in Figure 2.10.

The low pass filter (LPF) is used to eliminate the high frequency components in the decoupled voltage signals, which is the 2ω ripple. A common choice for the LPF is a first-order filter as:

$$G_{LPF}(s) = \frac{\omega_c}{s + \omega_c} \quad (2.12)$$

where ω_c is the cut-off frequency of the filter. The cut-off frequency should be chosen to be low enough to attenuate the 2ω ripple, but high enough to ensure a fast dynamic response of the PLL. A typical value for ω_c is around 30rad/s.

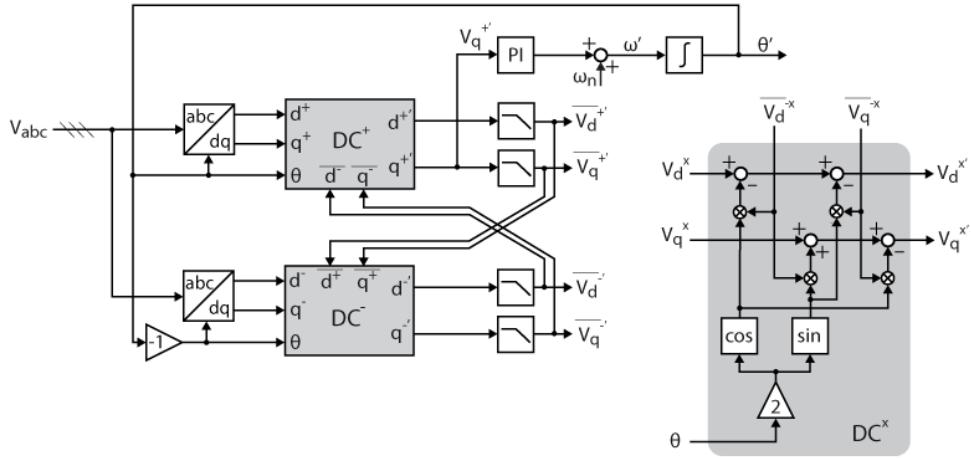


Figure 2.10: Block diagram of DDSRF-PLL with decoupling network

2.3.2 DDSRF-PLL under different grid conditions

To simply test the performance of the DDSRF-PLL under different grid conditions, a simulation is carried out in MATLAB/Simulink. The parameters of the DDSRF-PLL are chosen with a natural frequency of $\omega_n = 50Hz$ and a damping ratio of $\zeta = 0.707$. The cut-off frequency of the low pass filter is chosen to be $\omega_c = 30rad/s$.

The result of DDSRF-PLL under balanced grid conditions with a phase shift of 180° at $t = 0.1s$ is shown in Figure 2.11. It can be observed that the DDSRF-PLL can quickly track the phase angle of the grid voltage.

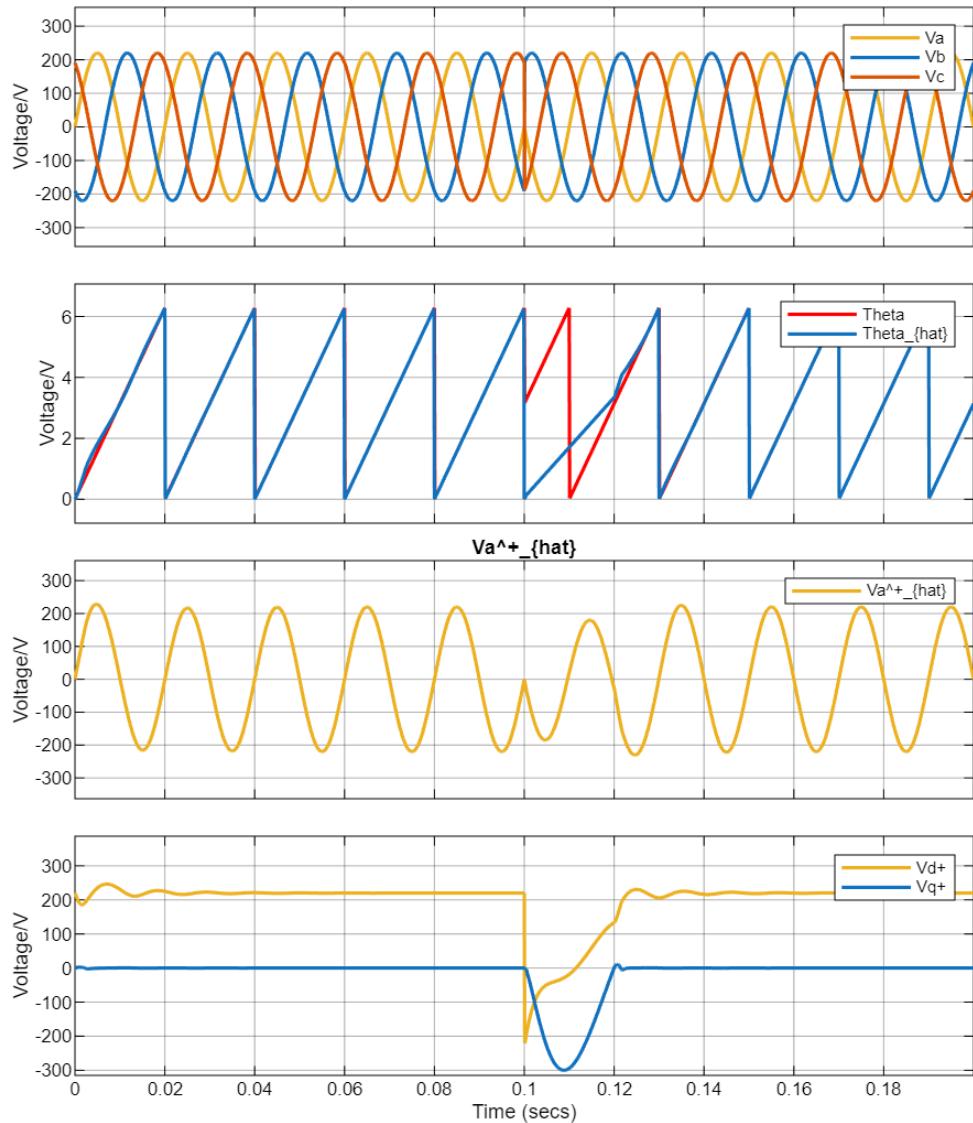


Figure 2.11: Response of the DDSRF-PLL with a phase shift at $t=0.1s$ under balanced conditions. Utility voltage [V], Detected phase angle [rad], Fundamantal voltage [V] and SRF axes voltage [V]

The result of DDSRF-PLL under unbalanced grid conditions with a negative sequence component of 30% and a phase shift of 180° at $t = 0.1s$ is shown in Figure 2.12. It can be observed that the DDSRF-PLL can still track the phase angle of the grid voltage without any oscillations in the detected phase angle, thanks to the decoupling network that effectively separates the positive and negative sequence components. The d and q axis voltages also show no oscillations at twice the fundamental frequency, which indicates that the PLL is robust against unbalanced grid conditions.

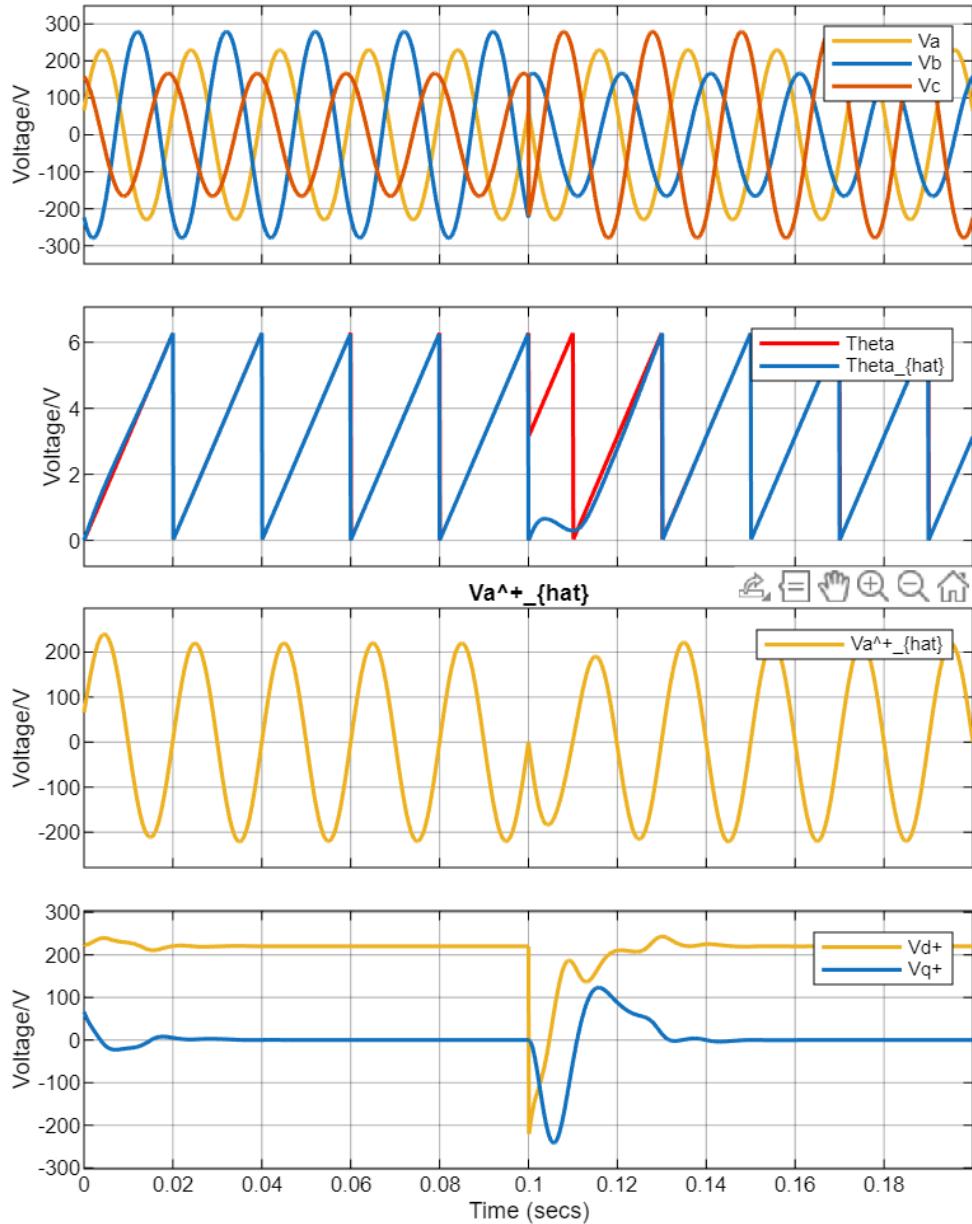


Figure 2.12: Response of the DDSRF-PLL with a phase shift at $t=0.1s$ under unbalanced conditions. Utility voltage [V], Detected phase angle [rad], Fundamental voltage [V] and SRF axes voltage [V]

The result of DDSRF-PLL under grid conditions with 30% of the 5th harmonics and a phase shift of 180° at $t = 0.1s$ is shown in Figure 2.13. It can be observed that the DDSRF-PLL can still track the phase angle of the grid voltage without any oscillations in the detected phase angle, thanks to the decoupling network that effectively separates the positive and negative sequence components. The d and q axis voltages show oscillations at the harmonic frequencies, which indicates that the DDSRF-PLL is still sensitive to harmonics in the grid voltage.

In conclusion, the DDSRF-PLL is an effective method for grid synchronization under unbalanced grid conditions. The decoupling network effectively separates the positive and negative

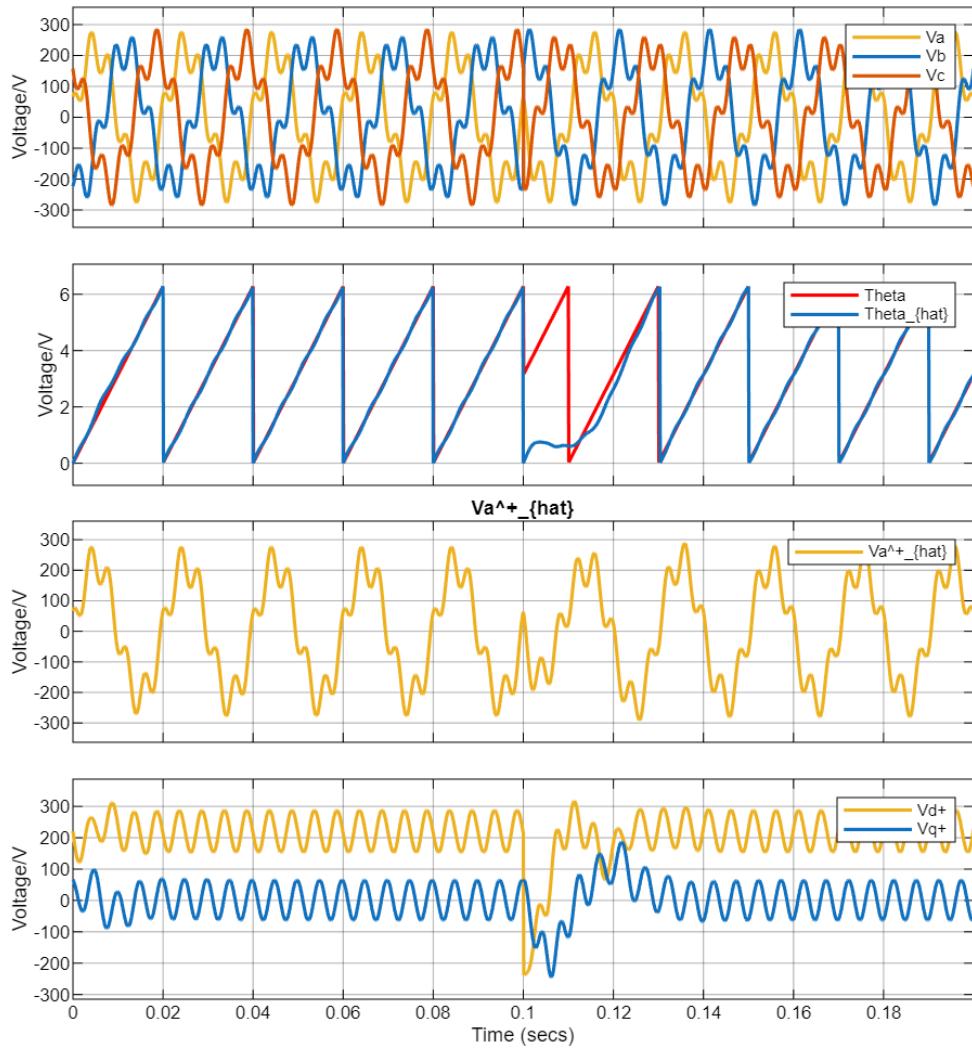


Figure 2.13: Response of the DDSRF-PLL with a phase shift at $t=0.1\text{s}$ under grid conditions with 30% of the 5th harmonics. Utility voltage [V], Detected phase angle [rad], Fundamental voltage [V] and SRF axes voltage [V]

sequence components, ensuring accurate detection of the phase angle even under unbalanced voltages. However, the DDSRF-PLL is still sensitive to harmonics in the grid voltage, which can affect its performance. Therefore, for applications where the grid conditions are expected to be highly distorted, more advanced PLL techniques should be considered.

2.4 Second Order General Integrator PLL

2.4.1 SOGI-PLL concept

SOGI-PLL is proposed for use as phase detectors [3] and positive-sequence voltage extractors in single-phase grid-connected systems [4].

SOGI structures are mainly composed of two filter types. First, a band-pass filter with no

phase delay at the fundamental frequency is used for the estimation of the phase voltage v' . Secondly, a low-pass filter is used to obtain the in-quadrature component qv' , which is 90° phase delayed from the input signal. Therefore, SOGI structures have the attractive benefit of providing simultaneous access to both the filtered output as well as a quadrature-shifted version of the same output, which represent the α and β components. As such, they allow for an easy implementation that can fit that of conventional SRF-PLL mentioned before.

The general principle of the SOGI-based PLL is given in Figure 2.14.

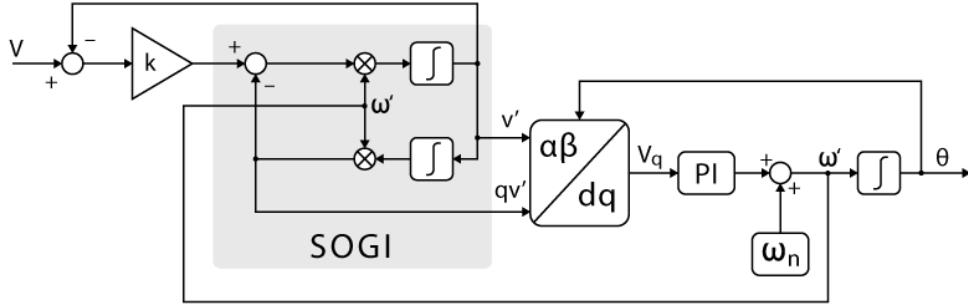


Figure 2.14: Block diagram of SOGI-PLL

Based on the preceding diagram, the subsequent transfer functions can be derived as follows:

$$D(s) = \frac{v'}{v}(s) = \frac{k\omega' s}{s^2 + k\omega' s + \omega'^2} \quad (2.13)$$

and the quadrature component is given by:

$$Q(s) = \frac{qv'}{v}(s) = \frac{k\omega'^2}{s^2 + k\omega' s + \omega'^2} \quad (2.14)$$

where ω' is the estimated angular frequency of the grid voltage, and k is the damping factor of the SOGI.

The effect of the damping factor k on the frequency response of the SOGI is shown in Figure 2.15.

An examination of the above transfer functions reveals that the parameter ω' centers the transfer function of the filters, while the parameter k plays a significant role in adjusting the filter's bandwidth.

It is also worth noting that the damping factor k does not alter the behavior of the SOGI at the frequency ω' . Consequently, a lower k value enhances frequency selectivity but slows down the response to voltage changes. Therefore, a trade-off between transient response and attenuation of distortions must be made. A commonly adopted tuning is $k = \sqrt{2}$, which is equivalent to $k = 2\zeta = 2\frac{1}{\sqrt{2}}$, with ζ representing the damping ratio for a second-order system.

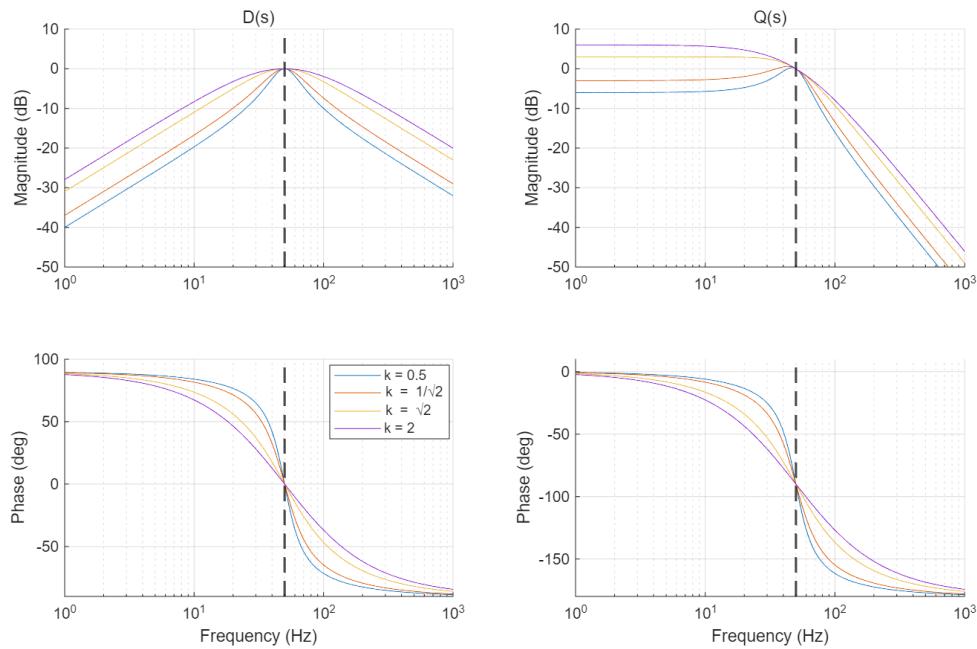


Figure 2.15: Effect of damping factor k on frequency response of SOGI

2.4.2 Different discrete methods for SOGI

When implementing the SOGI-PLL in a digital control system, it is essential to discretize the continuous-time transfer functions. Several discretization methods can be employed, each with its own advantages and disadvantages. The most commonly used methods include:

2.4.3 SOGI-PLL with DC offset rejection

In practical applications, the grid voltage may contain a DC offset component due to various reasons, such as sensor errors or power quality issues. If a DC offset is present in the measured voltage, it is not filtered by $Q(s)$ since the latter is of low-pass type. Consequently, the offset is also transferred to the quadrature signal and enters the SRF-PLL. This continuous term is then shifted to 2ω through the Park transformation, resulting in an oscillating term at twice the grid frequency in V_q . Given that the PI controller is unable to fully attenuate a non-continuous term, this oscillation is further propagated to the frequency and phase estimations.

To address this issue, a DC offset rejection technique can be implemented in the SOGI-PLL. SOGI block can be modified so that the low-pass filter generating the quadrature signal, $Q(s)$, is replaced with a band-pass filter with the same characteristics at the fundamental frequency. The block diagram of the SOGI-PLL with DC offset rejection is shown in Figure 2.16.

The transfer function of the band-pass filter can be expressed as:

$$D(s) = \frac{v'}{v}(s) = \frac{k_{dc}\omega s^2}{s^3 + (k + k_{dc})\omega s^2 + \omega^2 s + k\omega^3} \quad (2.15)$$

$$Q(s) = \frac{qv'}{v}(s) = \frac{k_{dc}\omega^2 s}{s^3 + (k + k_{dc})\omega s^2 + \omega^2 s + k\omega^3} \quad (2.16)$$

The Bode diagram of the SOGI with DC offset rejection is shown in Figure 2.17.

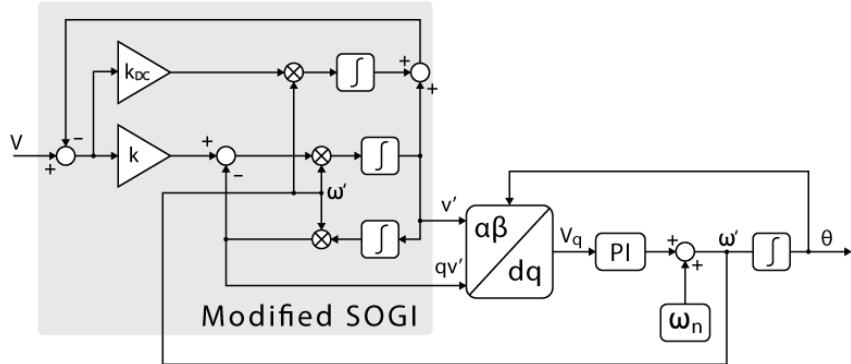


Figure 2.16: Block diagram of SOGI-PLL with DC offset rejection

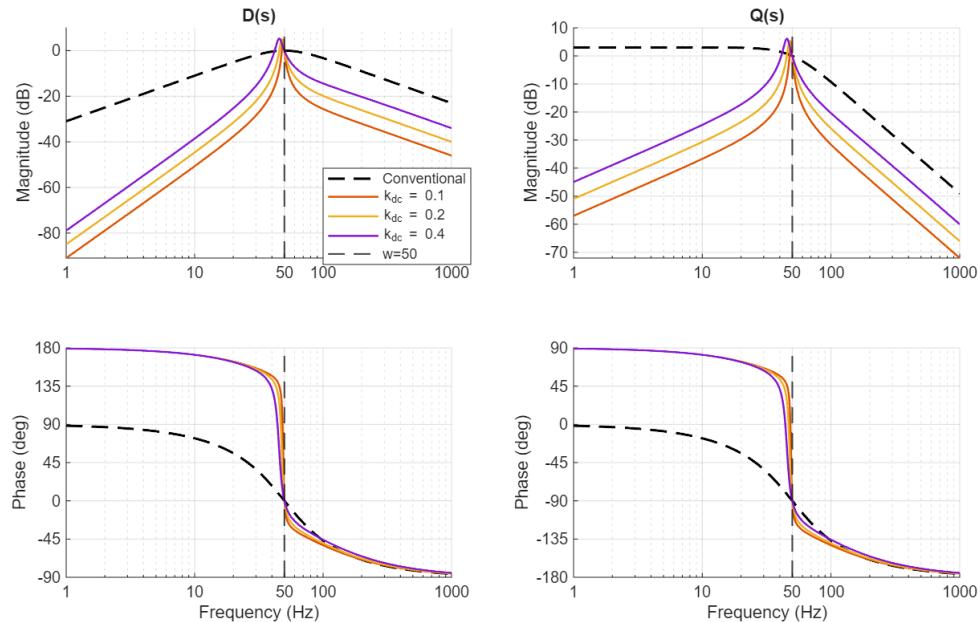


Figure 2.17: Bode diagram of SOGI with DC offset rejection

2.4.4 SOGI-PLL under different grid conditions

To simply test the performance of the SOGI-PLL under different grid conditions, a simulation is carried out in MATLAB/Simulink. The parameters of the SOGI-PLL are chosen with a natural frequency of $\omega_n = 50\text{Hz}$ and a damping ratio of $\zeta = 0.707$. The cut-off frequency of the low pass filter is chosen to be $\omega_c = 30\text{rad/s}$. The damping factor of the SOGI is chosen to be $k = \sqrt{2}$.

The result of SOGI-PLL without DC offset and harmonics with a phase shift of 180° at $t = 0.1\text{s}$ is shown in Figure 2.18. It can be observed that the SOGI-PLL can track the phase angle of the grid voltage, however the dynamic response is slower compared to the SRF-PLL and DDSRF-PLL.

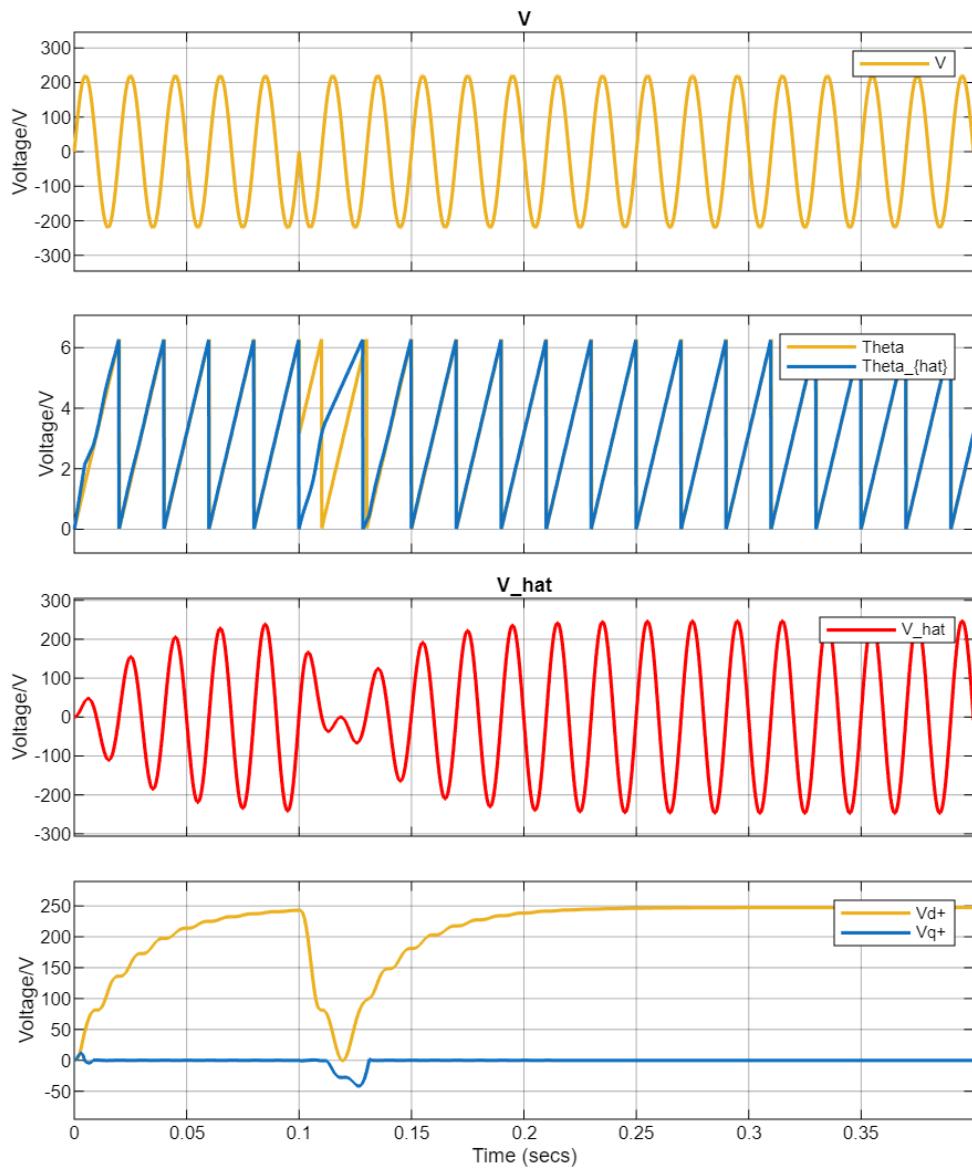


Figure 2.18: Response of the SOGI-PLL with a phase shift at $t=0.1s$ without DC offset and harmonics. Utility voltage [V], Detected phase angle [rad], Fundamental voltage [V] and SRF axes voltage [V]

The result of SOGI-PLL with 66V DC offset and no harmonics with a phase shift of 180° at $t = 0.1s$ is shown in Figure 2.19. It can be observed that there is a slight oscillation in the detected phase angle due to the presence of DC offset in the grid voltage and a 2ω ripple in the d axis voltage. To solve this issue, the SOGI-PLL with DC offset rejection can be used as mentioned before.

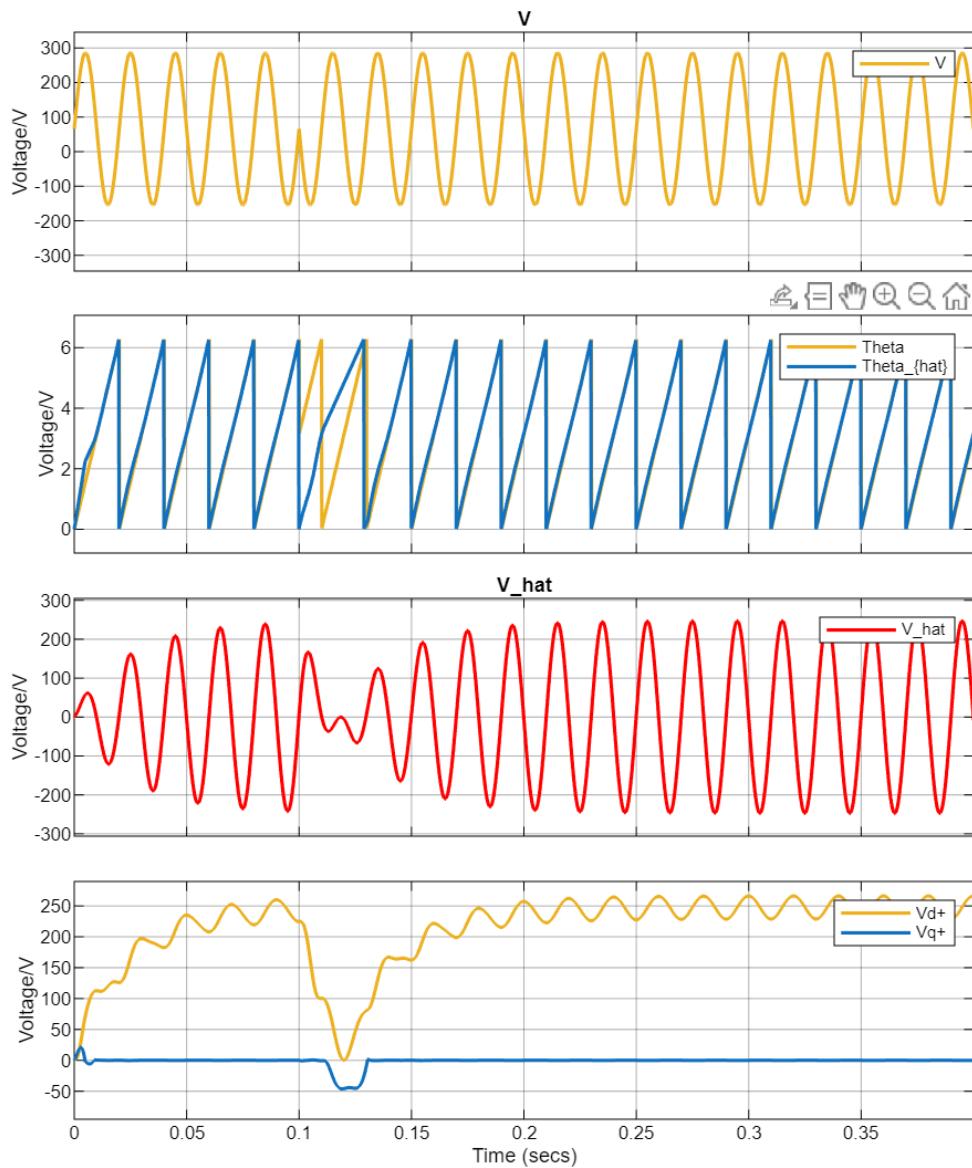


Figure 2.19: Response of the SOGI-PLL with a phase shift at $t=0.1s$ with 66V DC offset and no harmonics. Utility voltage [V], Detected phase angle [rad], Fundamental voltage [V] and SRF axes voltage [V]

The result of SOGI-PLL with 30% of the 5th harmonics and no DC offset with a phase shift of 180° at $t = 0.1s$ is shown in Figure 2.20. It can be observed that the SOGI-PLL can still track the phase angle of the grid voltage without any oscillations in the detected phase angle, thanks to the SOGI structure that effectively filters out the harmonics. The d and q axis voltages show little oscillations at the harmonic frequencies, which indicates that the PLL is robust against harmonics in the grid voltage.

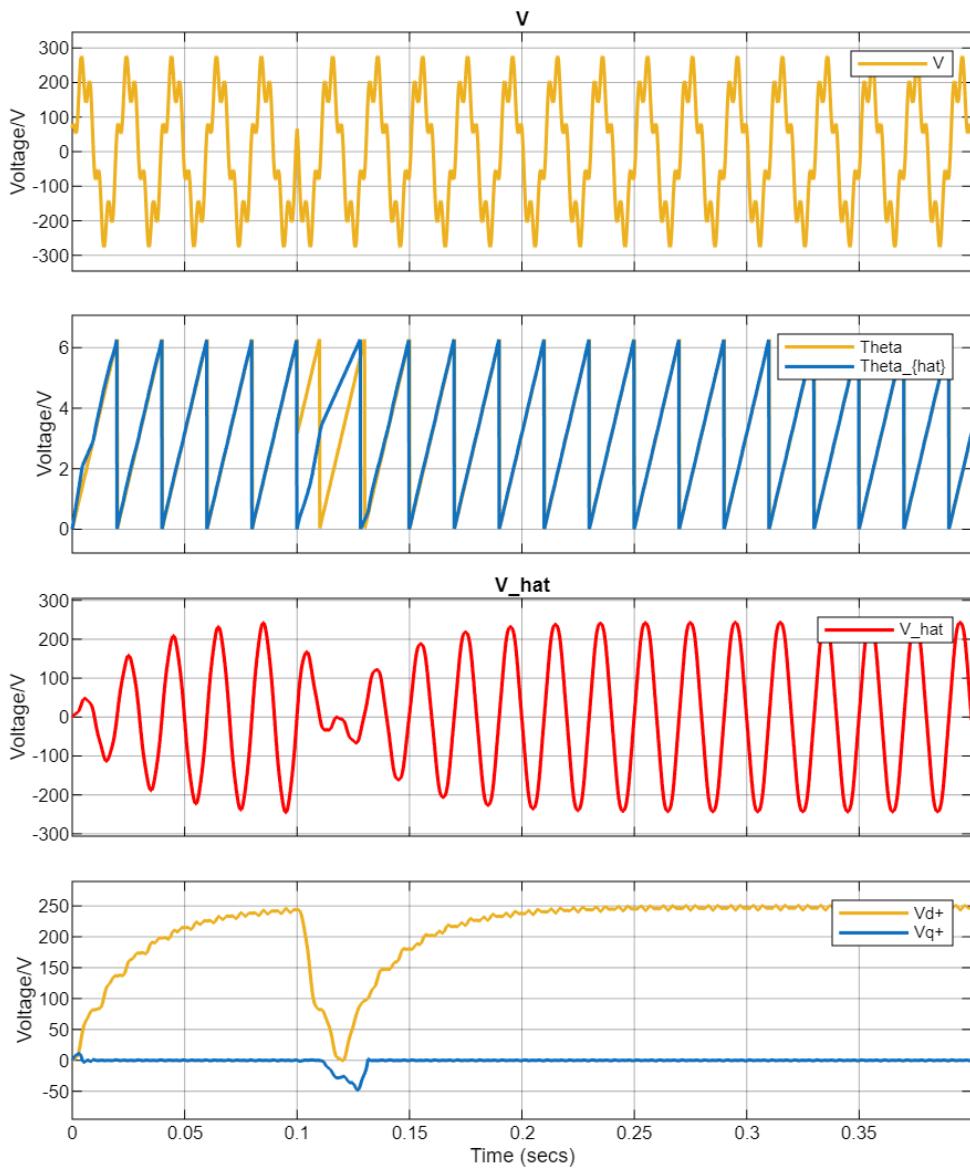


Figure 2.20: Response of the SOGI-PLL with a phase shift at $t=0.1s$ with 30% of the 5th harmonics and no DC offset. Utility voltage [V], Detected phase angle [rad], Fundamental voltage [V] and SRF axes voltage [V]

2.4.5 Performance of SOGI-PLL with DC offset rejection

To simply test the performance of the SOGI-PLL with DC offset rejection under different grid conditions, a simulation is carried out in MATLAB/Simulink. The parameters of the SOGI-PLL with DC offset rejection are chosen with a natural frequency of $\omega_n = 50\text{Hz}$ and a damping ratio of $\zeta = 0.707$. The cut-off frequency of the low pass filter is chosen to be $\omega_c = 30\text{rad/s}$. The damping factor of the SOGI is chosen to be $k = \sqrt{2}$ and $k_{dc} = \sqrt{2}$.

The result of SOGI-PLL with DC offset rejection with 66V DC offset and no harmonics with a phase shift of 180° at $t = 0.1s$ is shown in Figure 2.21. It can be observed that the SOGI-PLL with DC offset rejection can track the phase angle of the grid voltage without any oscillations

in the detected phase angle, thanks to the band-pass filter that effectively filters out the DC offset. The d and q axis voltages show no oscillations at twice the fundamental frequency, which indicates that the PLL is robust against DC offset in the grid voltage. However, the dynamic response is still slower compared to conventional SOGI-PLL.

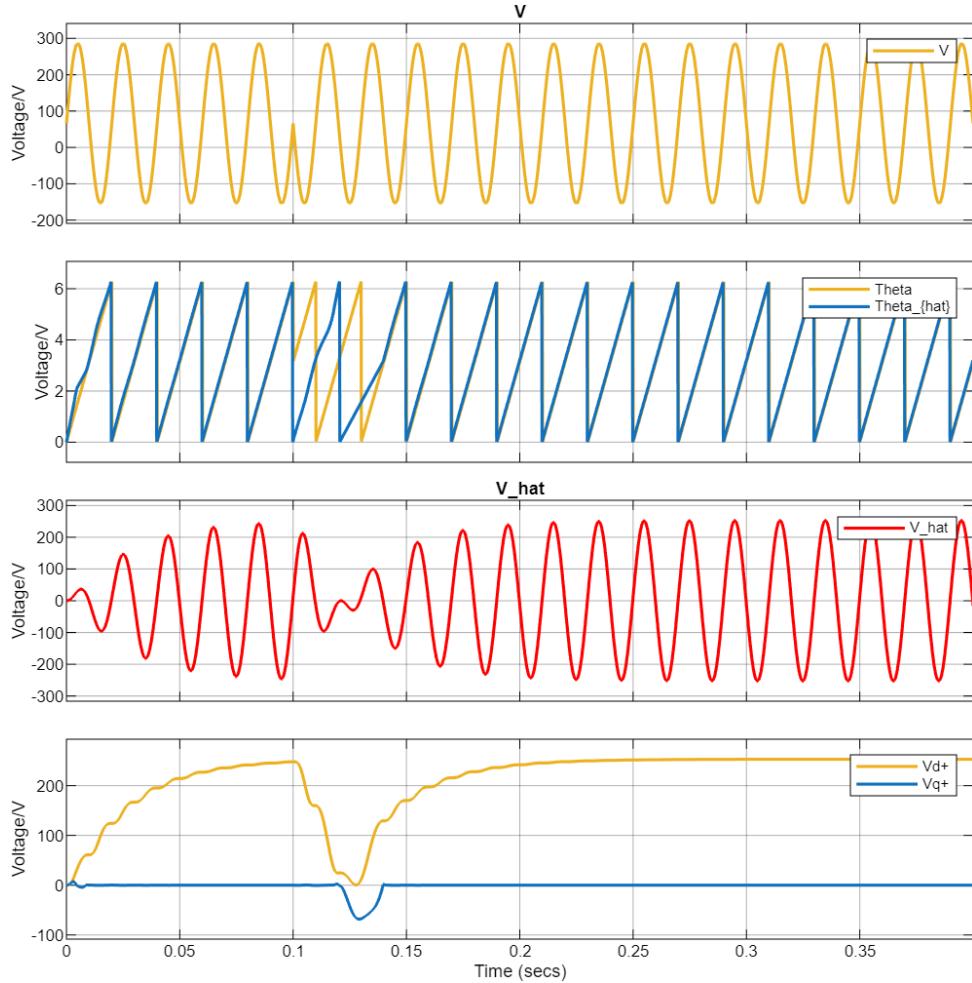


Figure 2.21: Response of the SOGI-PLL with DC offset rejection with a phase shift at $t=0.1s$ with 66V DC offset and no harmonics. Utility voltage [V], Detected phase angle [rad], Fundamental voltage [V] and SRF axes voltage [V]

In conclusion, the SOGI-PLL is an effective method for single phase grid synchronization under distorted grid conditions. The SOGI structure effectively filters out harmonics in the grid voltage, ensuring accurate detection of the phase angle even under distorted voltages. However, the SOGI-PLL is sensitive to DC offset in the grid voltage, which can affect its performance. Therefore, for applications where the grid conditions are expected to have DC offset, the SOGI-PLL with DC offset rejection should be considered.

2.5 Dual Second Order General Integrator PLL

2.5.1 DSOGI-PLL concept

For three-phase synchronization systems, the DSOGI structure is common, since it not only attenuates low-order voltage harmonics but also allows ready estimation of symmetrical components by passing its output through a positive/negative sequence calculator (PSC) prior to feeding into the SRF-PLL. However, the estimated frequency from the SRF-PLL needs to be fed back into the SOGI to make it frequency adaptive, and thus provide accurate voltage magnitude and phase estimation as the grid frequency varies [5]. This feedback path limits the dynamic performance of the SRF-PLL, increases the complexity of tuning the PLL gains and reduces its stability margin [6].

The block diagram of the DSOGI-PLL is shown in Figure 2.22.

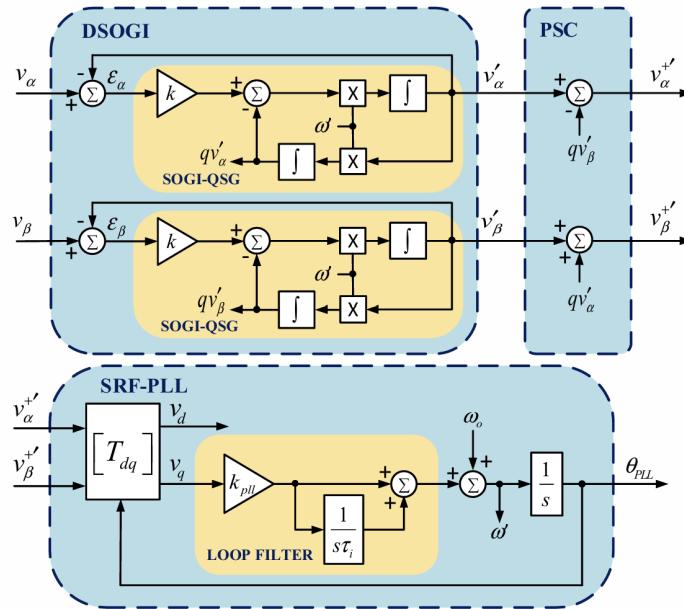


Figure 2.22: Block diagram of DSOGI-PLL

The DSOGI consists of two SOGIs, one for the α axis and one for the β axis. The transfer functions of the DSOGI can be expressed as:

$$\begin{aligned} \begin{bmatrix} v_{\alpha}'(s) \\ v_{\beta}'(s) \end{bmatrix} &= \frac{1}{2} \begin{bmatrix} D(s) & -Q(s) \\ Q(s) & D(s) \end{bmatrix} \begin{bmatrix} v_{\alpha}(s) \\ v_{\beta}(s) \end{bmatrix} \\ &= \frac{1}{2} \frac{k\omega}{s^2 + k\omega' + \omega'^2} \begin{bmatrix} s & -\omega' \\ \omega' & s \end{bmatrix} \begin{bmatrix} v_{\alpha}(s) \\ v_{\beta}(s) \end{bmatrix} \end{aligned} \quad (2.17)$$

The equation above shows how the combination of the DSOGI and the PSC form a low-pass filter that both filters out harmonic voltages and extracts the positive sequence only, from a distorted and unbalanced input voltage set. Consequently the positive sequence stationary frame

quadrature output signals $v_{\alpha}^{+'}$ and $v_{\beta}^{+'}(s)$ will have equal amplitudes, which will eliminate any unbalanced double frequency voltage oscillations prior to feeding the voltages into the SRF-PLL for phase angle and frequency estimation.

2.5.2 DSOGI-PLL under different grid conditions

To simply test the performance of the DSOGI-PLL under different grid conditions, a simulation is carried out in MATLAB/Simulink. The parameters of the DSOGI-PLL are chosen with a natural frequency of $\omega_n = 50Hz$ and a damping ratio of $\zeta = 0.707$. The cut-off frequency of the low pass filter is chosen to be $\omega_c = 30rad/s$. The damping factor of the SOGI is chosen to be $k = \sqrt{2}$.

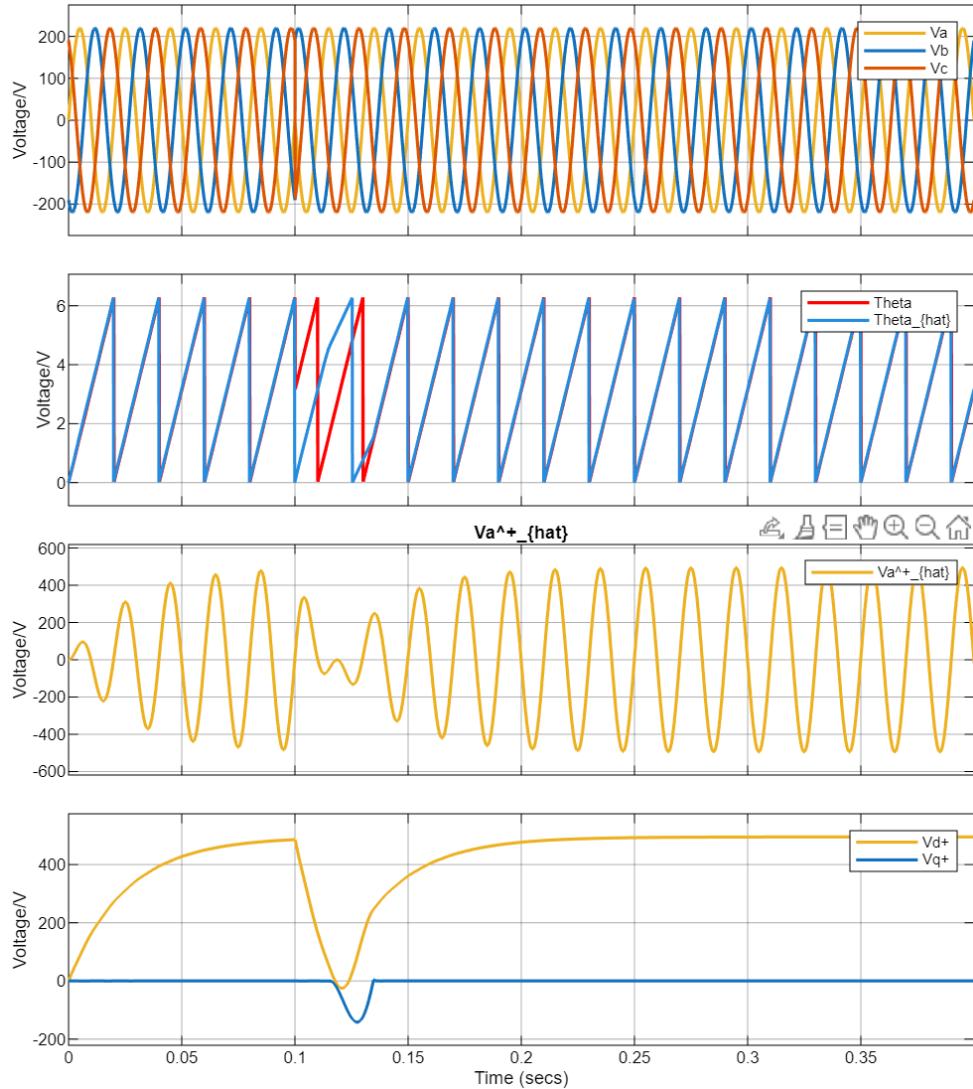


Figure 2.23: Response of the DSOGI-PLL with a phase shift at $t=0.1s$ under balanced conditions. Utility voltage [V], Detected phase angle [rad], Fundamental voltage [V] and SRF axes voltage [V]

The result of DSOGI-PLL under balanced grid conditions with a phase shift of 180° at $t = 0.1s$ is shown in Figure 2.23. It can be observed that the DSOGI-PLL can quickly track the phase angle of the grid voltage.

The result of DSOGI-PLL under unbalanced grid conditions with a negative sequence component of 30% and a phase shift of 180° at $t = 0.1s$ is shown in Figure 2.24. It can be observed that the DSOGI-PLL can still track the phase angle of the grid voltage without any oscillations in the detected phase angle, thanks to the DSOGI structure that effectively filters out the negative sequence component. The d and q axis voltages also show no oscillations at twice the fundamental frequency, which indicates that the PLL is robust against unbalanced grid conditions.

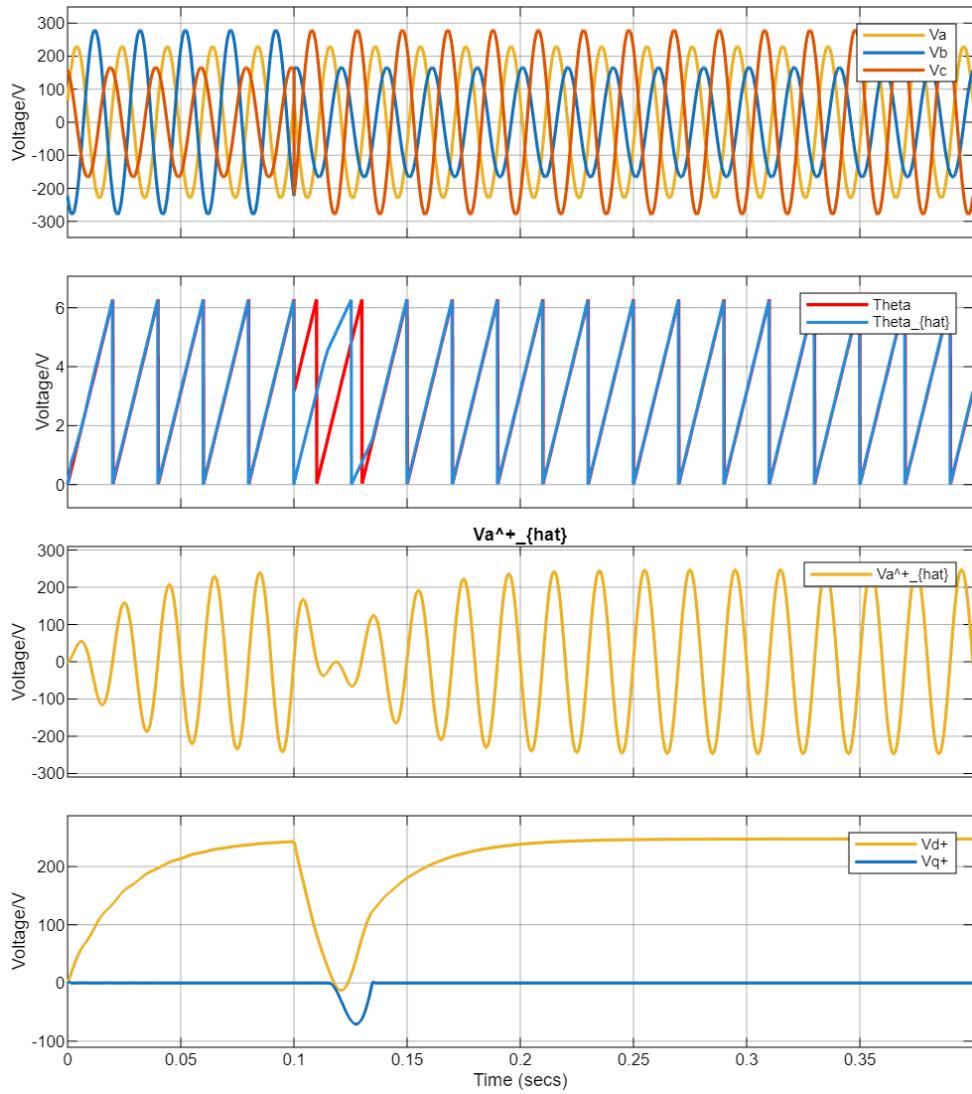


Figure 2.24: Response of the DSOGI-PLL with a phase shift at $t=0.1s$ under unbalanced conditions. Utility voltage [V], Detected phase angle [rad], Fundamental voltage [V] and SRF axes voltage [V]

The result of DSOGI-PLL under grid conditions with 30% of the 5th harmonics and a phase

shift of 180° at $t = 0.1\text{s}$ is shown in Figure 2.25. It can be observed that the DSOGI-PLL can still track the phase angle of the grid voltage without any oscillations in the detected phase angle, thanks to the DSOGI structure that effectively filters out the harmonics. The d and q axis voltages show little oscillations at the harmonic frequencies, which indicates that the PLL is robust against harmonics in the grid voltage.

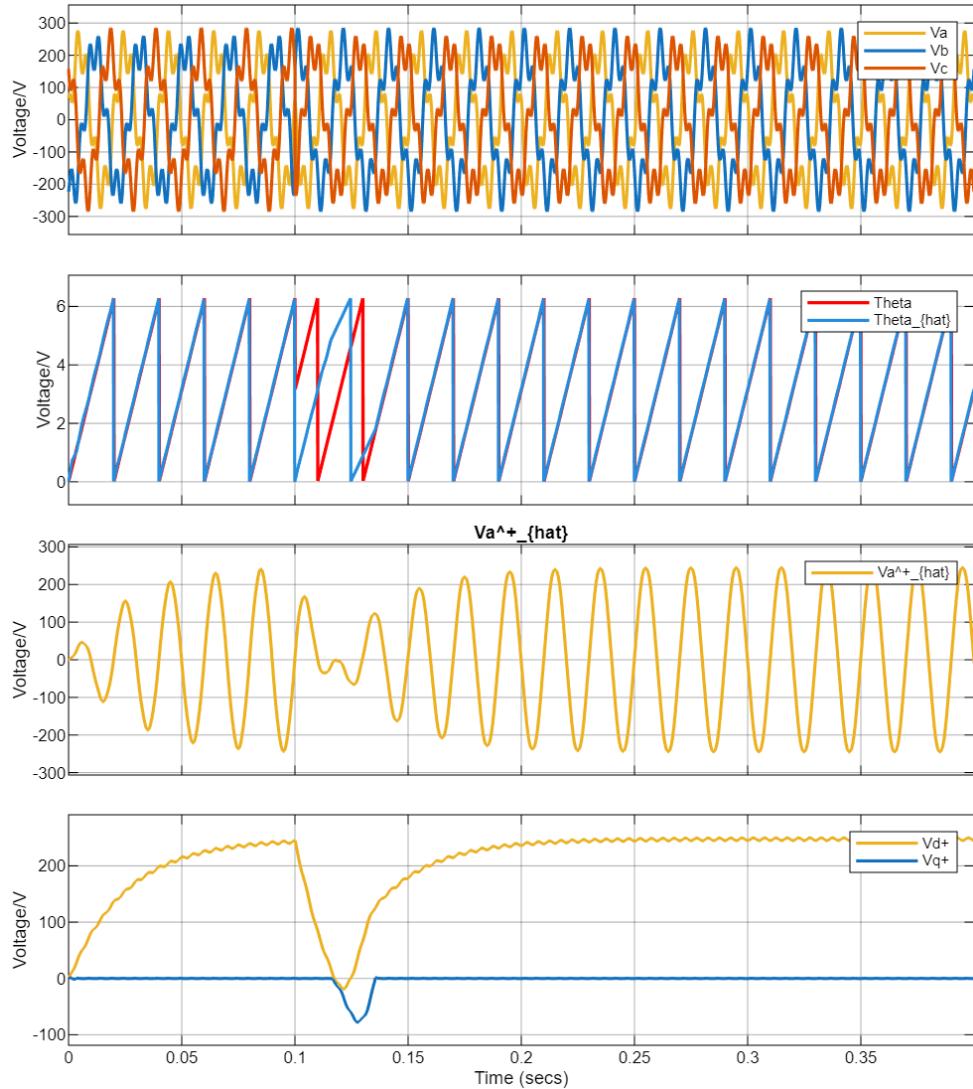


Figure 2.25: Response of the DSOGI-PLL with a phase shift at $t=0.1\text{s}$ under grid conditions with 30% of the 5th harmonics. Utility voltage [V], Detected phase angle [rad], Fundamental voltage [V] and SRF axes voltage [V]

In conclusion, the DSOGI-PLL is an effective method for three phase grid synchronization under unbalanced and distorted grid conditions. The DSOGI structure effectively filters out negative sequence components and harmonics in the grid voltage, ensuring accurate detection of the phase angle even under unbalanced and distorted voltages.

2.6 Multiple Second Order General Integrator PLL

2.6.1 MSOGI-PLL concept

In a SOGI block, the attenuation of low-order harmonic distortions typically ranges between -10dB and -20dB for harmonics of order less than 10th when $k = \sqrt{2}$. However, in certain applications, this level of attenuation may prove insufficient. In order to selectively attenuate certain harmonics, a cross-feedback network composed of multiple SOGIs can be introduced, each tuned to the selected frequencies. This solution is referred to as the MSOGI-PLL. It is very effective for estimating the positive sequence component under disturbed conditions [7].

The block diagram of the MSOGI-PLL is shown in Figure 2.26.

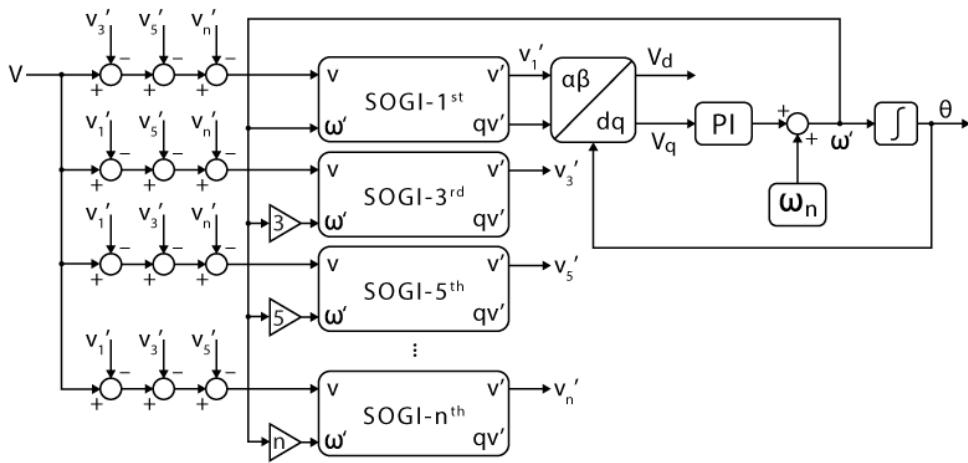


Figure 2.26: Block diagram of MSOGI-PLL

The parallel structure shown in Figure 2.26 forms a cross-feedback architecture often known as a Harmonic Decoupling Network (HDN). The key benefit of this network is that it creates sharp notches in the system's frequency response precisely at the frequencies where the individual SOGIs are tuned. As a consequence, the selective filtering characteristic of each SOGI is significantly improved. This enhancement allows the MSOGI-PLL to maintain a robust performance even in the presence of high distortion levels in the input signal.

The MSOGI consists of several SOGIs connected in parallel, each tuned to a specific harmonic frequency. The transfer function of the MSOGI can be expressed as:

$$v'_i = \left[D_i(s) \prod_{\substack{j=1 \\ (j \neq i)}}^n \left(\frac{1 - D_j(s)}{1 - D_i(s)D_j(s)} \right) \right] v \quad (2.18)$$

where $D_i(s)$ represents the transfer function of the SOGI block tuned to the i -th harmonic frequency of interest.

2.6.2 MSOGI-PLL under different grid conditions

To simply test the performance of the MSOGI-PLL under different grid conditions, a simulation is carried out in MATLAB/Simulink. The parameters of the MSOGI-PLL are chosen with a

natural frequency of $\omega_n = 50\text{Hz}$ and a damping ratio of $\zeta = 0.707$. The cut-off frequency of the low pass filter is chosen to be $\omega_c = 30\text{rad/s}$. The damping factor of the SOGI is chosen to be $k = \sqrt{2}$. The MSOGI is designed to attenuate the 5th and 7th harmonics.

The result of MSOGI-PLL with 30% of the 5th and 7th harmonics and no DC offset with a phase shift of 180° at $t = 0.1\text{s}$ is shown in Figure 2.27. It can be observed that the MSOGI-PLL can track the phase angle of the grid voltage without any oscillations in the detected phase angle, thanks to the MSOGI structure that effectively filters out the 5th and 7th harmonics. The d and q axis voltages show little oscillations at the harmonic frequencies, which indicates that the PLL is robust against harmonics in the grid voltage.

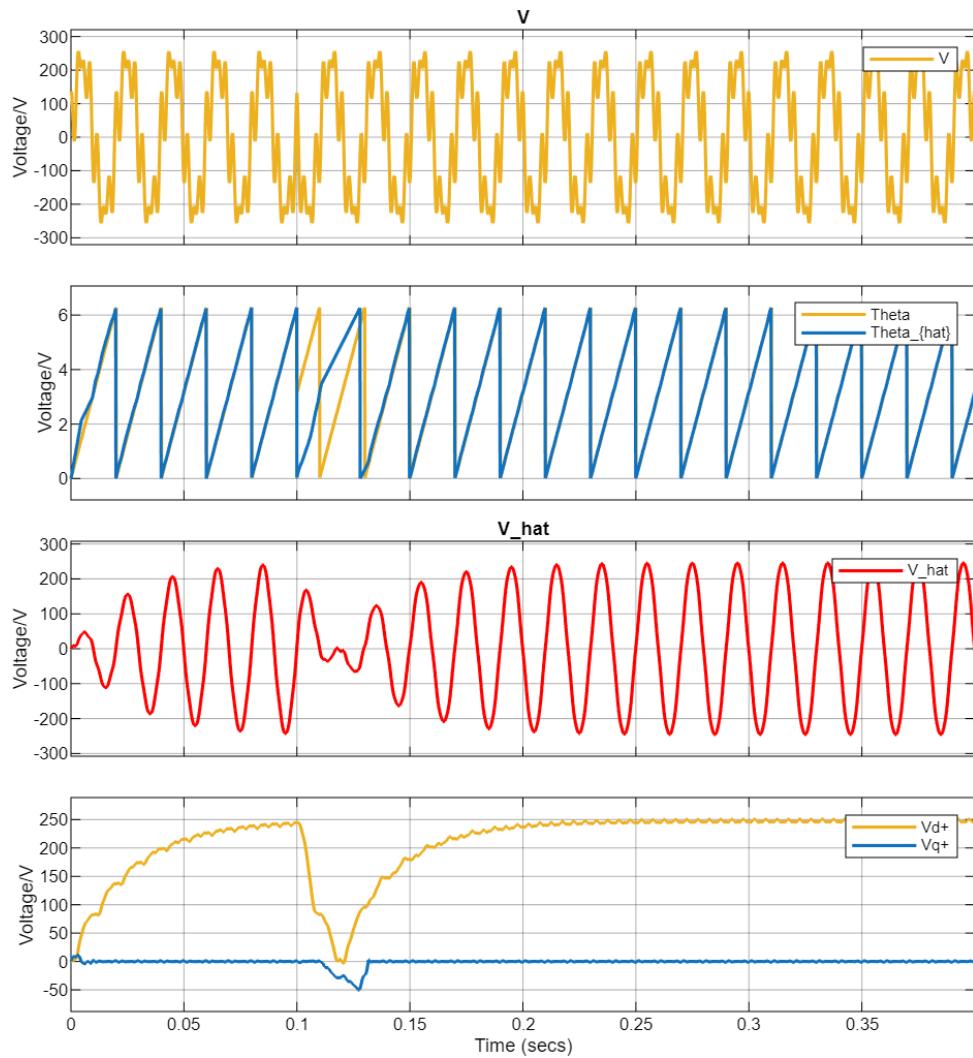


Figure 2.27: Response of the MSOGI-PLL with a phase shift at $t=0.1\text{s}$ with 30% of the 5th and 7th harmonics and no DC offset. Utility voltage [V], Detected phase angle [rad], Fundamental voltage [V] and SRF axes voltage [V]

2.7 Comparison of PLLs

The following is a summarized description of the five different types of PLLs:

- SRF-PLL: Uses Park transformation to convert three-phase signals to d-q frame and locks the phase using PI control.
- DDSRF-PLL: An improved SRF-PLL that decouples positive and negative sequence components for better unbalance handling.
- SOGI: A second-order filter structure generating orthogonal signals from a single-phase input, used to extract fundamental frequency.
- DSOGI: Extension of SOGI for dual orthogonal outputs, positive and negative sequences in $\alpha - \beta$ frame.
- MSOGI: A bank of multiple SOGIs tuned to different harmonics; useful in harmonic estimation and multi-frequency systems.

For disturbances like unbalance, harmonics, and DC offset, the PLLs can be described in table 2.1.

Table 2.1: Comparison of Signal Disturbance Handling Capabilities

Technique	Unbalance Handling	Harmonics Immunity	DC Offset Immunity	Frequency Deviation Handling
SRF-PLL	Poor	Moderate	Poor	Good
DDSRF-PLL	Excellent	Moderate	Poor	Good
SOGI	Poor	Poor	Moderate	Moderate
DSOGI	Good	Moderate	Moderate	Good
MSOGI	Excellent	Excellent	Moderate	Excellent

Additionally, the dynamic response of the PLLs can be compared in table 2.2.

Table 2.2: Comparison of Dynamic Response

Technique	Dynamic Response
SRF-PLL	Fast
DDSRF-PLL	Moderate
SOGI	Slow
DSOGI	Moderate
MSOGI	Slow

The calculation time of the PLL is also an important factor to consider, especially in real-time applications. The computational complexity of each PLL can be summarized in table 2.3.

In summary, the choice of PLL technique depends on the specific application requirements, including the nature of the disturbances expected in the grid, the desired dynamic response, and the available computational resources. Each PLL has its strengths and weaknesses, and a careful evaluation is necessary to select the most suitable one for a given scenario.

Table 2.3: Comparison of Computational Complexity

Technique	Number of Operations	Memory Usage	Implementation Complexity
SRF-PLL	Low	Low	Low
DDSRF-PLL	High	Low	Moderate
SOGI	Moderate	Moderate	Moderate
DSOGI	High	Moderate	Moderate
MSOGI	High	High	High

CHAPTER 3

Algorithm Development for MPPT

3.1 Overview of MPPT and its Applications

Maximum Power Point Tracking (MPPT) is a family of control algorithms that aims at optimizing the use of a power source that possesses a fluctuating power profile.

Indeed, some power sources, like solar panels, present power characteristics that strongly depend on the operating conditions. For instance, the cloud coverage significantly impacts the capability of a panel to deliver electricity. As such, maximizing the extracted power requires identifying and tracking the operating point that provides the highest power level as a function of the operating conditions.

Therefore, MPPT is often applied in renewable energy systems, e.g. photovoltaic plants or wind turbines, as their power delivery capability varies significantly and in an unpredictable manner. Other special operating points may be interesting to track, such as the maximum efficiency point tracking (MEPT), or other optimum, e.g. related to operating costs.

3.2 Mathematical Model of PV Array

The PV array is the largest building block of the PV system which consists of PV panels, then PV modules. The PV modules are consisting of several PV cells connected in series and parallel to produce the required voltage and current from the module. So, the PV cell is the basic unit of the PV systems. The PV cell is consisting of two semiconductor materials from types P and N. The PN junction absorbs the light from the Sun which adds energy to the electrons in this junction enabling it to have enough energy to cross the junction and produce voltage difference between their terminals.

There are several research works that have been done to model the PV cell [8]. The one-diode model is the most common model used to represent the electrical characteristics of the PV cell. The equivalent circuit of the one-diode model is shown in Fig.3.1.

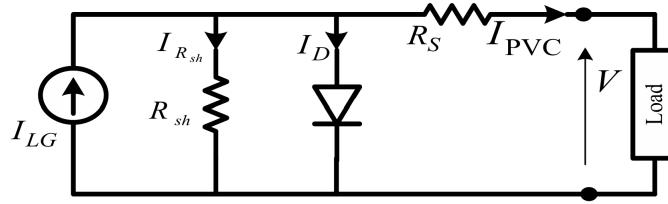


Figure 3.1: The equivalent circuit of the one-diode model of a PV cell.

Moreover, the one-diode model parameters can be easily determined experimentally [9]. Some other models like the two-diode model [10] and the three-diode model [11] have been proposed to represent the PV cell more accurately, but they are more complex. Therefore, we just discuss the one-diode model in this report.

The output current generated from the PV cell is given by the following equation:

$$I_{\text{PVC}} = I_{\text{LG}} - I_{\text{sat}} * \left[e^{\left(\frac{q}{K T} (V_{\text{PVC}} + R_s I_{\text{PVC}}) \right)} - 1 \right] - \frac{V_{\text{PVC}} + R_s I_{\text{PVC}}}{R_{\text{sh}}} \quad (3.1)$$

where:

- I_{LG} : Light-generated current (A)
- I_{sat} : Reverse saturation current (A)
- q : Charge of an electron (C)
- K : Boltzmann constant (J/K)
- T : Absolute temperature (K)
- V_{PVC} : Output voltage of the PV cell (V)
- R_s : Series resistance (Ω)
- R_{sh} : Shunt resistance (Ω)

The light-generated current for given radiation and temperature can be calculated as follows:

$$I_{\text{LG}} = (I_{\text{STC}} + K_I(T_c - T_r)) \frac{G}{G_o} \quad (3.2)$$

where:

- I_{STC} : PV cell current at standard test conditions (A)
- K_I : Temperature coefficient of current (A/K)
- T_c : PV cell temperature (K)
- T_r : Rated temperature (K)

- G : The current solar irradiance (W/m^2)
- G_o : Reference solar irradiance (kW/m^2)

The module voltage can be obtained by multiplying the cell voltage by the number of cells connected in series N_{SC} in the module.

$$V_M = N_{SC} * V_{PVC} \quad (3.3)$$

The module current can be obtained by multiplying the cell current by the number of cells connected in parallel N_{PC} in the module.

$$I_M = N_{PC} * I_{PVC} \quad (3.4)$$

Multiplying the terminal voltage by the output current determines the generated power from the PV array. The relation between the terminal voltage and current in uniform condition for different irradiances, and the relation between the terminal voltage and output power are shown in Fig.3.2.

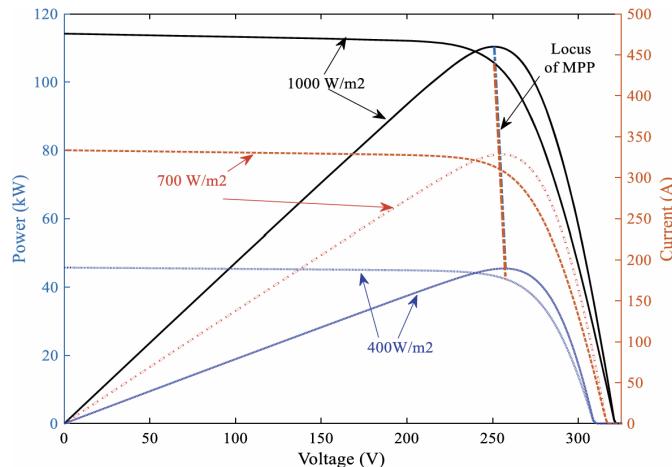


Figure 3.2: The characteristics of a PV module under different irradiance levels.

It's clear that the PV module has a nonlinear characteristic, and there is a unique point on each curve where the power is maximum. This point is called the Maximum Power Point (MPP), and the goal of the MPPT algorithms is to track this point under different operating conditions.

3.3 Perturb and Observe Algorithm

The Perturb and Observe (P&O) algorithm is one of the most widely used MPPT techniques due to its simplicity and ease of implementation. The basic idea behind the P&O algorithm is to perturb the operating voltage of the PV module and observe the resulting change in power output. If the power increases, the perturbation is continued in the same direction; if the power decreases, the perturbation direction is reversed. This process is repeated continuously to track the MPP [12].

The flowchart of the P&O algorithm is shown in Fig.3.3.

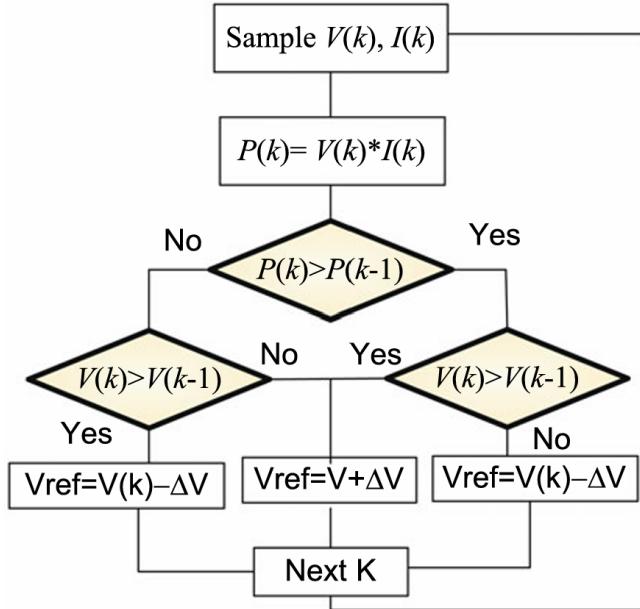


Figure 3.3: The flowchart of the Perturb and Observe algorithm.

There are many P&O techniques that have been proposed to improve the performance of the basic P&O algorithm. Some of these techniques include adaptive step size and variable perturbation frequency [13].

3.3.1 Response of PV Module to Irradiance Variation

When the irradiance level changes suddenly, the output power of the PV module also changes. The response of the PV module to a sudden change in irradiance from 1000 W/m² to 500 W/m² is shown in Fig.3.4.

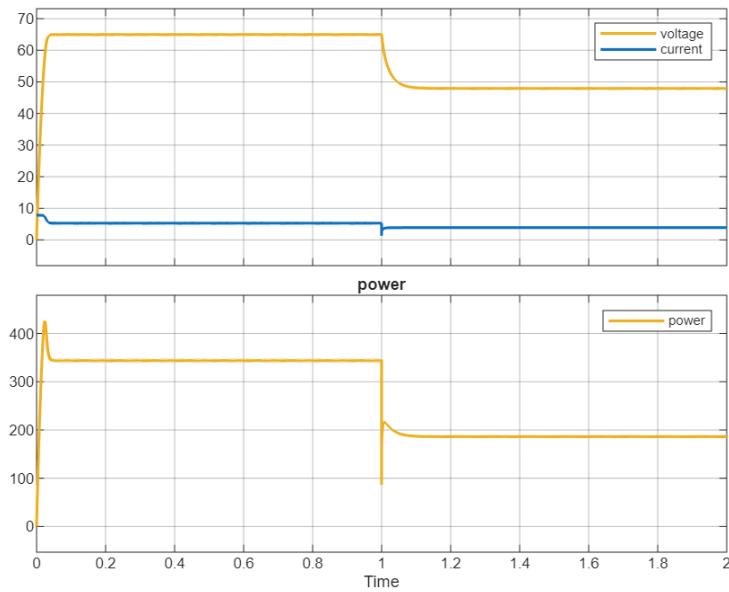


Figure 3.4: The response of a PV module to a sudden change in irradiance with MPPT

3.4 Incremental Conductance Algorithm

The Incremental Conductance (IncCond) algorithm is another popular MPPT technique that is based on the principle that the derivative of power with respect to voltage is zero at the MPP. The IncCond algorithm calculates the incremental conductance (dI/dV) and compares it to the instantaneous conductance (I/V) to determine the direction of perturbation. If $dI/dV > -I/V$, the operating voltage is increased; if $dI/dV < -I/V$, the operating voltage is decreased. This process is repeated continuously to track the MPP [14].

The flowchart of the IncCond algorithm is shown in Fig.3.5.

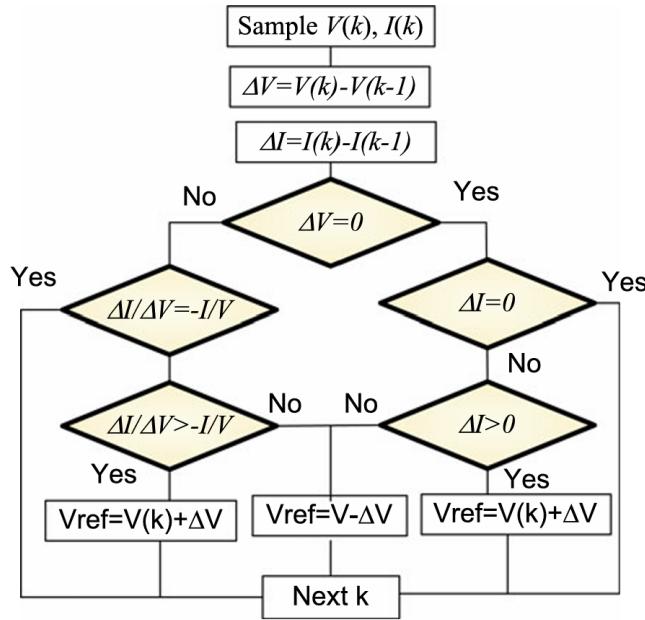


Figure 3.5: The flowchart of the Incremental Conductance algorithm.

3.4.1 Response of PV Module to Irradiance Variation

When the irradiance level changes suddenly, the output power of the PV module also changes. The response of the PV module to a sudden change in irradiance from 1000 W/m² to 500 W/m² is shown in Fig.3.6.

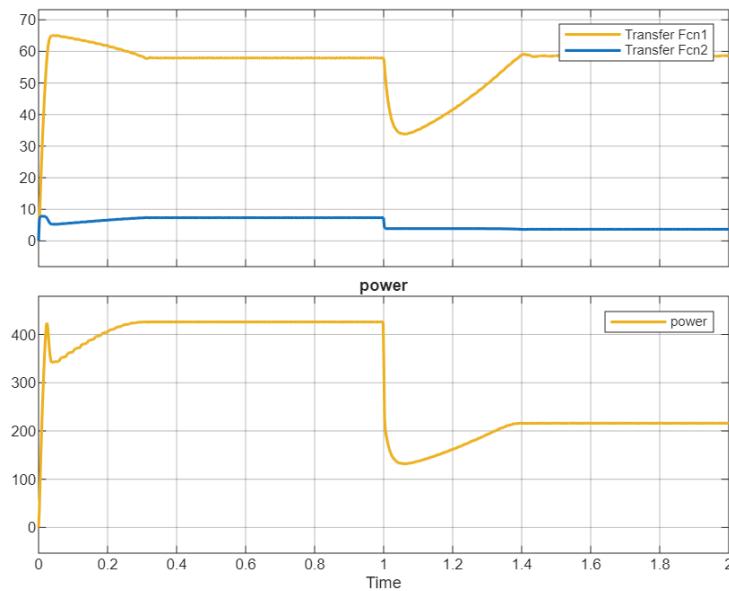


Figure 3.6: The response of a PV module to a sudden change in irradiance with MPPT using Incremental Conductance algorithm.

3.5 Comparison between P&O and IncCond Algorithms

- P&O: A simple MPPT algorithm that perturbs the operating voltage slightly and observes the effect on output power. If power increases, it continues in that direction; if it decreases, it reverses.
- IncCond: A more advanced method that calculates the derivative of power with respect to voltage (dP/dV) to predict whether the system is approaching or moving away from the MPP.

The main differences between the two algorithms are summarized in Table 3.1.

Table 3.1: Comparison between P&O and IncCond Algorithms

Feature	P&O	IncCond
Complexity	Simple and easy to implement	More complex (needs derivative calculations)
Cost	Low computational cost	Higher computational cost
Tracking Accuracy	Less accurate, especially under fast-changing irradiance	More accurate, especially in dynamic conditions
Oscillations at MPP	Yes – tends to oscillate around MPP	Minimal – can settle exactly at MPP
Speed of Convergence	Moderate	Faster in dynamic conditions
Response to Irradiance Change	Can be confused by rapid changes – may mistake irradiance shifts for MPP shifts	Handles irradiance changes more accurately
Implementation	Widely used in small-scale systems due to simplicity	Preferred in systems where accuracy and efficiency are more critical
Sensitivity to Noise	Low	Can be more sensitive due to derivative calculations

CHAPTER 4

Design and Implementation

To implement the Model Based Design (MBD) for the PLL algorithms, MATLAB/Simulink is used as the simulation platform.

4.1 Modeling in MATLAB/Simulink for PLL

The following subsections describe the different PLL models developed in MATLAB/Simulink.

4.1.1 Test Signal Generation Block

The test signal generation block is used to generate the three-phase voltage signals with adjustable frequency, amplitude, phase angle, negative sequence, and harmonic distortion. The fundamental waveform generation block is shown in Fig. 4.1.

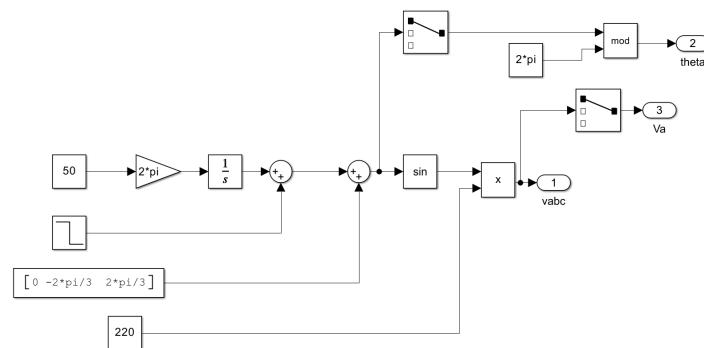


Figure 4.1: Fundamental Waveform Generation Block

The harmonic waveform generation block is shown in Fig. 4.2.

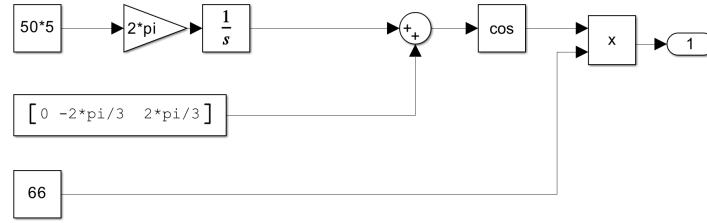


Figure 4.2: Harmonic Waveform Generation Block

The negative sequence waveform generation block is shown in Fig. 4.3.

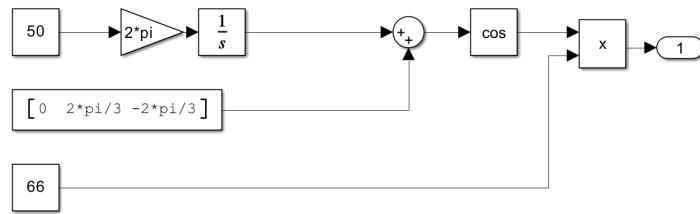


Figure 4.3: Negative Sequence Waveform Generation Block

4.1.2 SRF-PLL Model

The SRF-PLL model developed in MATLAB/Simulink is shown in Fig. 4.4.

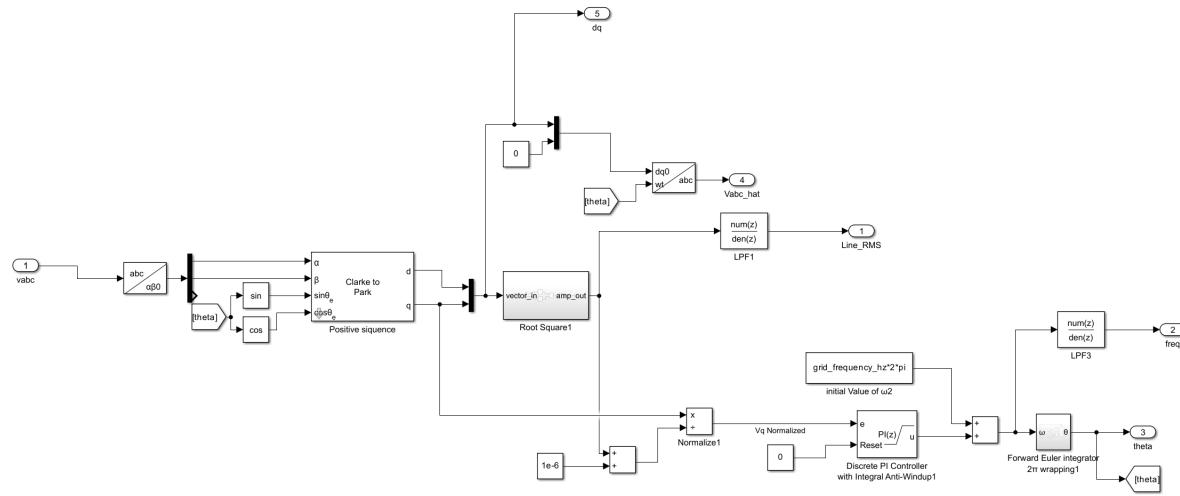


Figure 4.4: SRF-PLL Model

The SRF-PLL model consists of the blocks such as Clarke Transformation, Park Transformation, PI Controller with saturation limits and a foward Euler integrator to obtain the phase angle. The model is then used to implement MBD and generate C code for real-time implementation.

4.1.3 DDSRF-PLL Model

The double decoupled block is shown in Fig. 4.5. It extracts the positive and negative sequence components and subtracts them from the original signal to provide a decoupled signal for the SRF-PLL. The block implements the Equation 2.11 mentioned in Chapter 2.

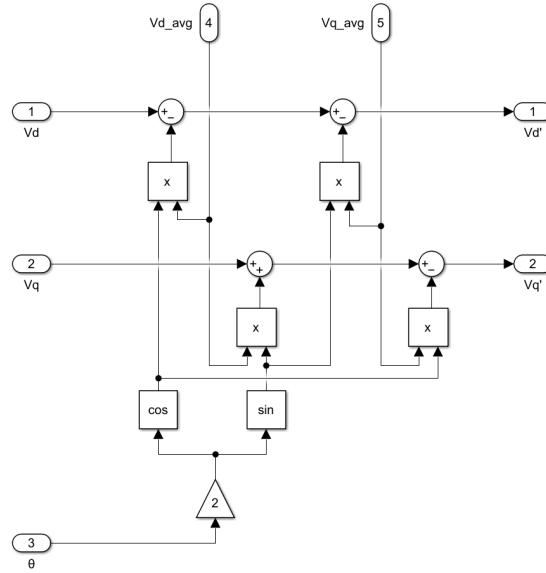


Figure 4.5: Double Decoupled Block

The complete DDSRF-PLL model developed is shown in Fig. 4.6.

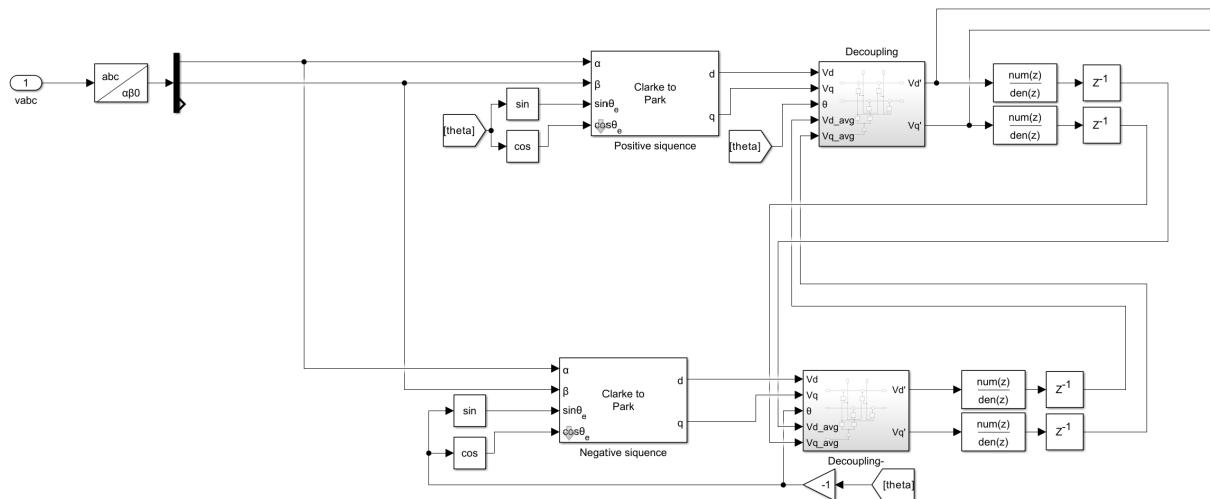


Figure 4.6: DDSRF-PLL Model

After the block is a SRF-PLL block similar to the one shown in Fig. 4.4.

4.1.4 SOGI-PLL Model

We use Tustin discretization method for the SOGI integrator implementation in the SOGI-PLL model. The Tustin method provides a good balance between accuracy and stability for the integrator in this application, and its block diagram is shown in Fig. 4.7.

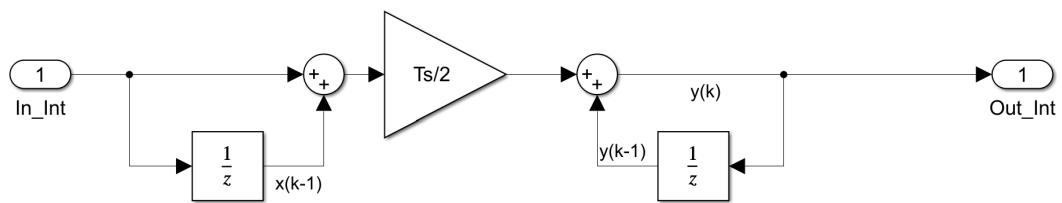


Figure 4.7: Tustin Integrator Block

The SOGI block used in the SOGI-PLL model is shown in Fig. 4.8.

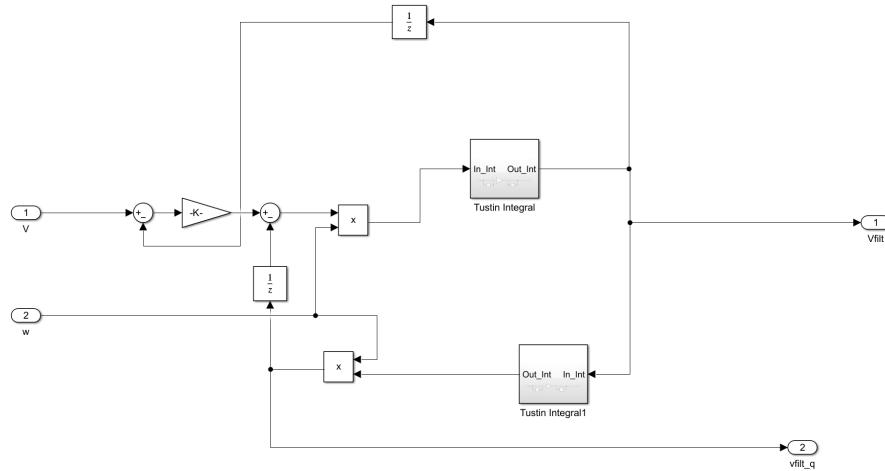


Figure 4.8: SOGI Block

If the DC offset rejection is required, an additional integrator is needed in the SOGI block as shown in Fig. 4.9.

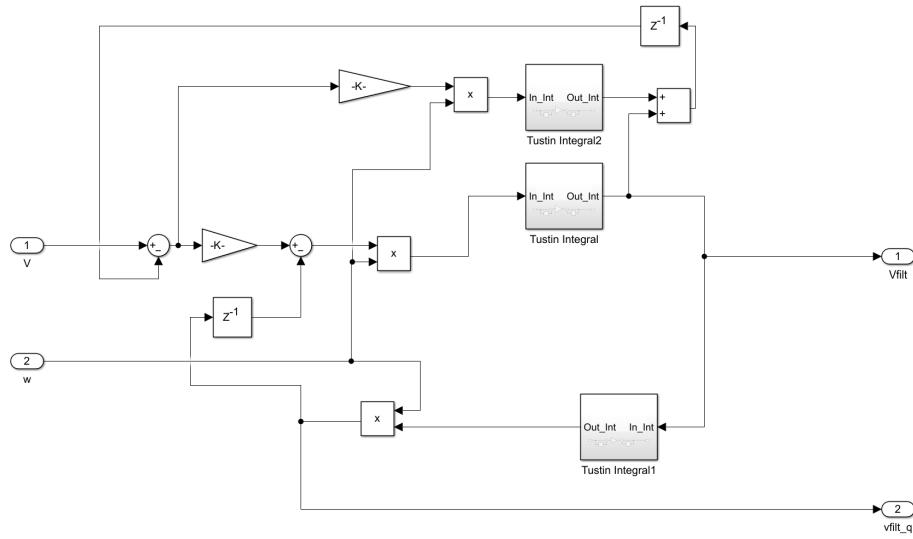


Figure 4.9: SOGI Block with DC Offset Rejection

4.1.5 DSOGI-PLL Model

DSOGI uses two SOGI blocks to extract the positive and negative sequence components separately. The block diagram of the DSOGI is shown in Fig. 4.10.

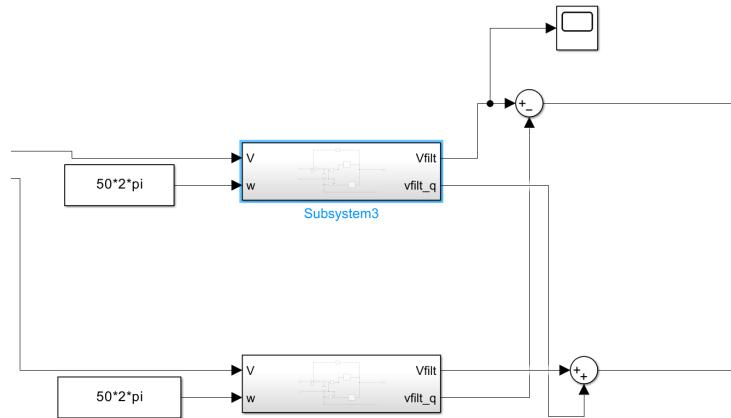


Figure 4.10: DSOGI Block

The rest of the DSOGI-PLL model is similar to the SRF-PLL model.

4.1.6 MSOGI-PLL Model

MSOGI uses multiple SOGI blocks to extract the harmonic components separately. The block diagram of the MSOGI is shown in Fig. 4.11.

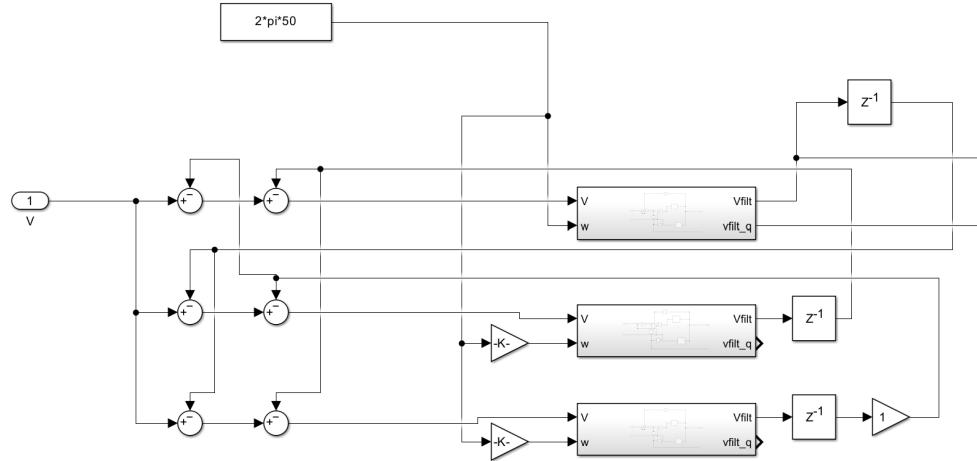


Figure 4.11: MSOGI Block

The rest of the MSOGI-PLL model is similar to the SRF-PLL model.

4.2 Modeling in MATLAB/Simulink for MPPT

The following subsections describe the different MPPT models developed in MATLAB/Simulink.

4.2.1 MPPT P&O Model

The MPPT P&O model developed in MATLAB/Simulink is shown in Fig. 4.12.

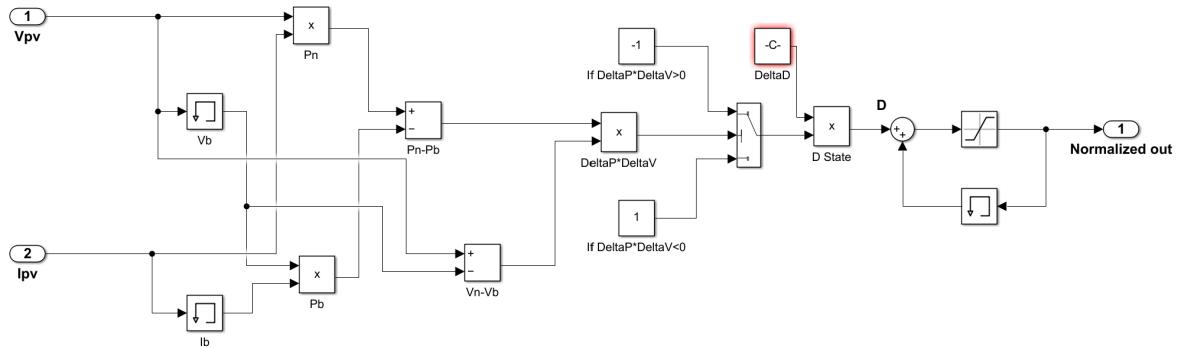


Figure 4.12: MPPT P&O Model

4.2.2 MPPT IncCond Model

The MPPT IncCond model developed in MATLAB/Simulink is shown in Fig. 4.13.

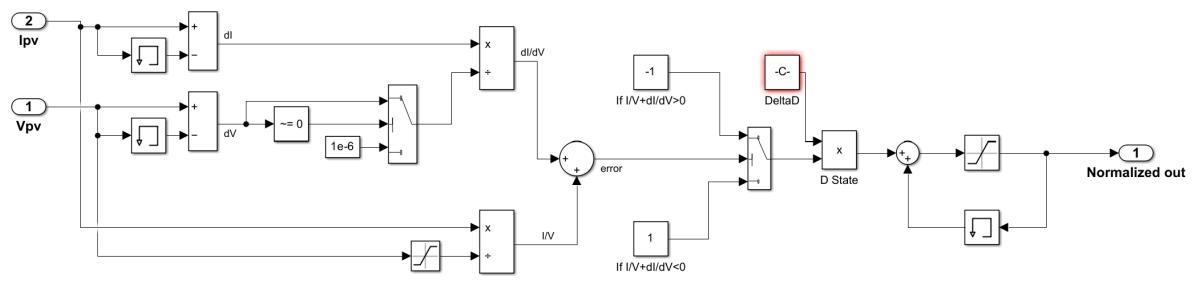


Figure 4.13: MPPT IncCond Model

CHAPTER 5

Conclusion

5.1 Summary of Work

5.2 Recommendations for Future Work

APPENDIX A

List of symbols and abbreviations

A.1 List of symbols

General remark:

The following convention was used for variables:

Scalars are italic letters:	x
Vectors are bold lower case letters:	\boldsymbol{x}
Matrices are bold upper case letters:	\boldsymbol{X}
References are marked with a star superscript:	x^*

Used symbols:

In the following the most important symbols are listed which are used within this work.

General symbols:

\boldsymbol{x}	State vector
\boldsymbol{u}	Input vector
\boldsymbol{y}	Output vector
\boldsymbol{A}	State matrix
\boldsymbol{B}	Input matrix
\boldsymbol{C}	Output matrix
\boldsymbol{D}	Feedthrough matrix
t	Time (continuous)
k	Time (discrete, current sample)
$\frac{d}{dt}$	Time derivation
T_s	Sampling time
t_{sw}	Variable switching time point (VSP)
Δ	Difference
J	Inertia

General electrical variables:

a, b, c	Phases
α, β	Equivalent two-phase coordinates
j	$\sqrt{-1}$
v	Voltage
i	Current
R	Resistor
C	Capacitor
L	Inductor

Induction machine parameters:

v_s, v_r	Stator and rotor voltage
i_s, i_r	Stator and rotor current
ψ_s, ψ_r	Stator and rotor flux
ω_m	Mechanical machine speed
ω_{el}	Electrical machine speed
T_m	Mechanical machine torque
T_l	Mechanical load torque
P	Machine power
p	Number of pole pairs
R_s, R_r	Stator and rotor resistance
L_s, L_r	Stator and rotor inductance
L_m	Mutual inductance

Further variables and parameters:

S_{xi}	Switch i in phase x
s_{xi}	Gating signal for switch i in phase x
j	Cost function value
w	Weighting factor
v_o, i_o	Inverter output voltage and current (UPS)
v_l, i_l	LC lowpass-filter output voltage and current (UPS)

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