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Research on Control and Modulation Optimization for MMC-SST

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Declaration

The work in this thesis is based on research carried out at the Chair of High-Power Converter Systems, Technical University of Munich (TUM) supervised by Dr. Gean Maia de Sousa. No part of this thesis has been submitted elsewhere for any other academic degree or qualification and it is all my own work unless referenced to the contrary in the text.

Place, Date, Signature

Abstract

Acknowledgments

. . . if you would like to thank someone. In a thesis, acknowledgements are usually put on one of the first pages.

Munich, in September 2022
Max Mustermann

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CHAPTER 1

Introduction

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CHAPTER 2

Modeling and Control of MMC-SST

The chapter presents the modeling and control strategies for MMC-SST. It covers the topology, modeling, and control methods for both the MMC and the DAB converter used in the SST system.

2.1 Topology of MMC and its working principle

2.1.1 Topology of three-phase MMC

The topology of a three-phase MMC is illustrated in Figure 2.1.

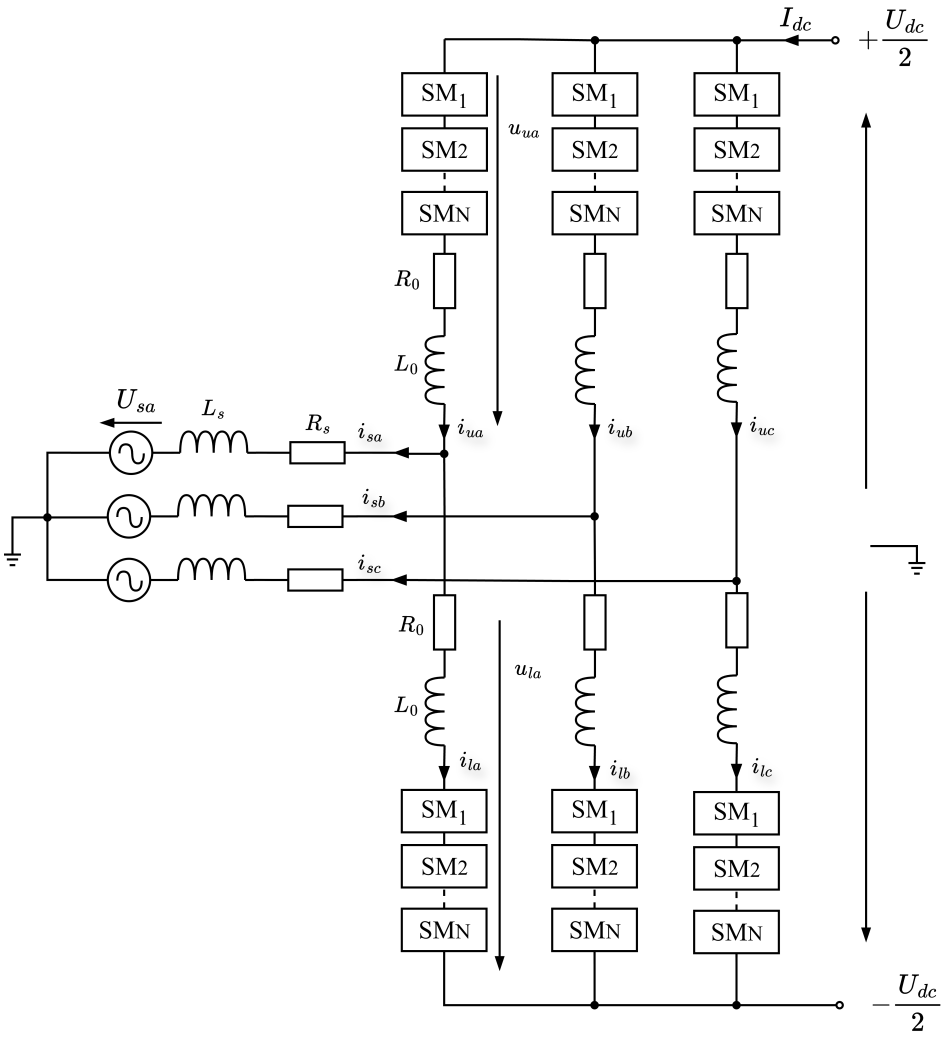


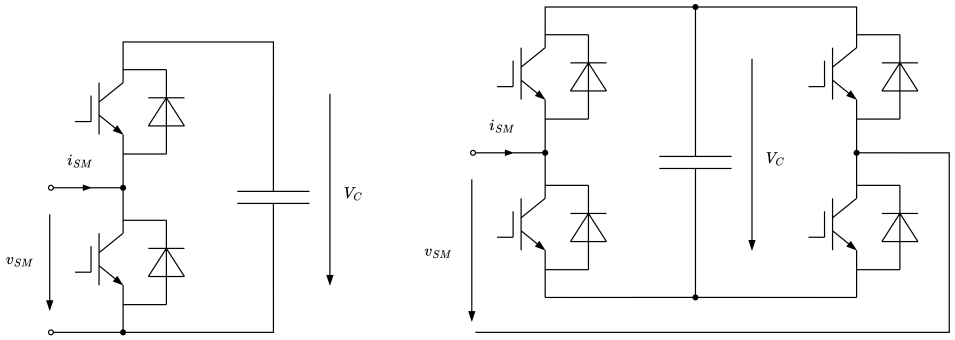
Figure 2.1: Topology of Three-Phase MMC

In the Figure 2.1, $u_{sj}(j = a, b, c)$ represents the AC side phase voltages, and i_{sj} represents the AC side phase currents. u_{uj} and u_{lj} represent the upper and lower arm voltages of phase j, respectively. i_{uj} and i_{lj} represent the upper and lower arm currents of phase j, respectively.L_s and R_s represent the AC side filter inductance and resistance, respectively. L_0 and R_0 represent the arm inductance and resistance, respectively. I_{dc} represents the DC side current, and U_{dc} represents the DC side voltage.

Each phase of the MMC consists of upper and lower arms, each containing multiple submodules (SMs) connected in series. Each arm also includes an arm inductor L_0 and an arm resistor R_0. L_0 helps to limit the change rate of arm current when faults occur, and helps to suppress circulating current ripples. The arms are connected to the AC side through inductors L_s and its equavilant resistance R_s.

2.1.2 Topology of SMs of MMC

SMs are the minimal blocks of MMC, and its performance directly affects the performance of MMC. Different types of SMs have diffetent characteristics. The most commonly used SM types are half-bridge SM and full-bridge SM. The topology of half-bridge SM and full-bridge SM are illustrated in Figure 2.2.



a) Half-bridge b) Full-bridge

Figure 2.2: Topology of SMs: (a) Half-Bridge SM (HB-SM); (b) Full-Bridge SM (FB-SM)

Different SM types have different characteristics in terms of number of switches, voltage levels, fault handling capability, control complexity, and losses. A comparison of the characteristics of half-bridge SM and full-bridge SM is provided in Table 2.1.

Table 2.1: Comparison of MMC Submodule Topological Characteristics

Submodule Type	Switches	Levels	Fault Handling	Control Complexity	Losses
HB-SM	2	2	No	Simple	Low
FB-SM	4	3	Yes	Simple	High

2.1.3 Working principle of SMs

HB-SM is most commonly used in MMC due to its simple structure and low losses. HB-SM can only insert or bypass the capacitor voltage, thus it can only generate two voltage levels: 0 and U_c. The working principle of HB-SM is illustrated in Figure 2.3.

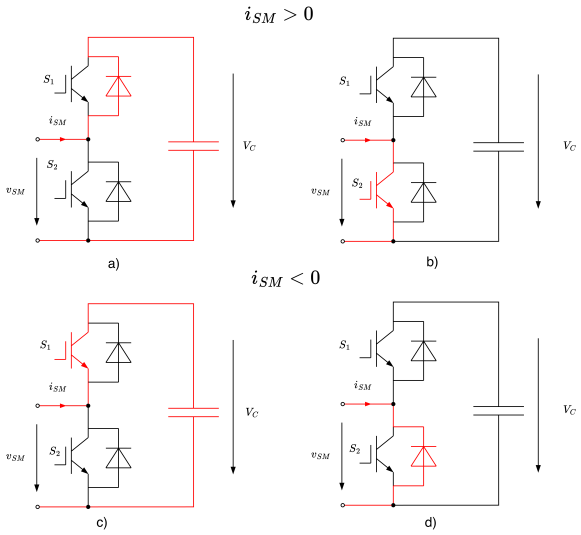


Figure 2.3: Working Principle of HB-SM

When the switch S1 is closed and S2 is open, the capacitor voltage V_c is inserted into the circuit, resulting in an output voltage of V_c. When S1 is open and S2 is closed, the capacitor is bypassed, resulting in an output voltage of 0. The red arrows indicate the current flow direction in each state.

For FB-SM, it can generate three voltage levels: U_c, 0, and $-U_c$. The working principle of FB-SM is illustrated in Figure 2.4.

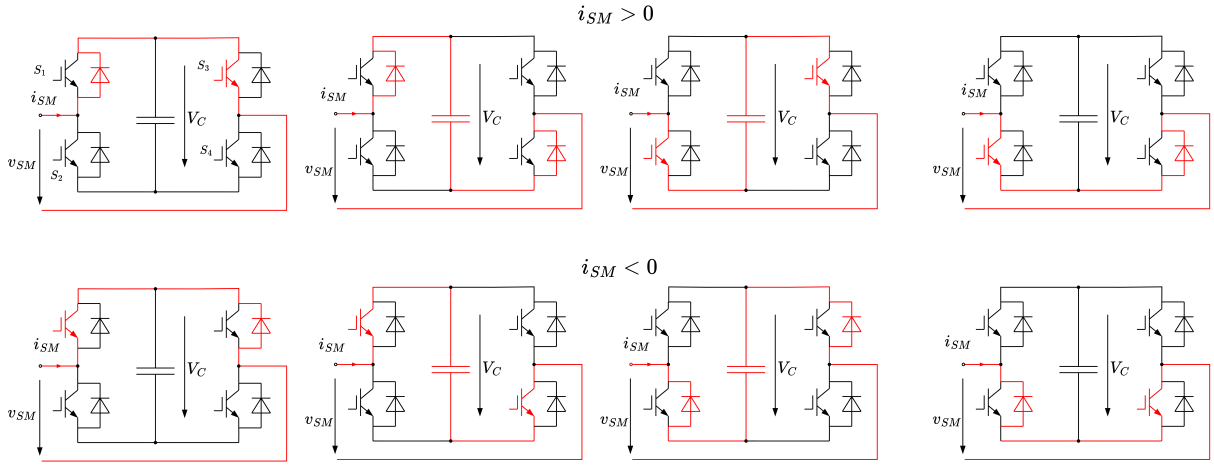


Figure 2.4: Working Principle of FB-SM

The switches of FB-SM have four working states. When S1 and S4 are closed while S2 and S3 are open, the capacitor voltage V_c is inserted into the circuit, resulting in an output voltage of V_c. When S2 and S3 are closed while S1 and S4 are open, the negative capacitor voltage $-V_c$ is inserted into the circuit, resulting in an output voltage of $-V_c$. When S1 and S3 are closed while S2 and S4 are open and vice versa, the capacitor is bypassed, resulting in an output voltage of 0. The red arrows indicate the current flow direction in each state.

2.1.4 Working principle of 3-phase MMC

The topology of the three-phase MMC is illustrated in Figure 2.1. During normal steady-state operation, the MMC control system generates trigger pulses based on specific control objectives to manage the switching devices in each arm, thereby regulating the operating states of SMs. By superimposing the SM voltages and controlling the number of SMs inserted into the upper and lower arms at any given time, a multi-level stepped waveform approximating a sine wave is produced on the AC side, while a stable DC voltage U_{dc} is maintained on the DC side.

To analyze the operating principle of the three-phase MMC, the voltage drops across the arm inductors and resistors, as well as SM redundancy, are initially neglected. This implies that the arm inductors and resistors are considered short-circuited, and the insertion or bypass states of the SMs are distributed between the upper and lower arms. If each arm contains N submodules, the total number of SMs per phase is $2N$. Since the DC bus voltage is supported by the capacitors of the inserted SMs across the three phases, maintaining a constant DC bus voltage U_{dc} requires the number of inserted submodules N_{in} in each phase to remain fixed or nearly constant, such that $N_{in} = N$. Under the assumption of no redundancy, the SMs in the upper and lower arms of each phase are typically operated complementarily, satisfying the condition:

$$n_{uj} + n_{lj} = N \tag{2.1}$$

where n_{uj} and n_{lj} are the number of inserted submodules in the upper and lower arms of phase j, respectively. Since the number of submodules in each phase is equal to N, the bus voltage is maintained by the series structure of the arm submodules. The relationship for the average operating voltage of the submodules should satisfy:

$$U_c = \frac{U_{dc}}{n_{uj} + n_{lj}} = \frac{U_{dc}}{N} \tag{2.2}$$

where U_c is the average capacitor voltage of the submodules.

Since the three phase units are structurally symmetrical, the DC side current should be equally divided among the phases. Therefore, the DC current contained in each phase is $1/3$ of the DC side current. Furthermore, because the upper and lower arm structures are symmetrical and have identical parameters, the AC current is equally divided between the upper and lower arms. Thus, the currents in the upper and lower arms should satisfy:

$$i_{uj} = \frac{I_{dc}}{3} + \frac{i_{sj}}{2} \tag{2.3}$$

$$i_{lj} = \frac{I_{dc}}{3} - \frac{i_{sj}}{2} \tag{2.4}$$

where i_{uj} and i_{lj} are the upper and lower arm currents of phase j, respectively; I_{dc} is the DC bus side current; and i_{sj} is the AC side current of phase j.

Taking the case where the number of submodules in each arm is $N = 4$ as an example, a 5-level voltage output is achieved by inserting different numbers of submodules into the upper and lower arms at different times, as shown in Table 2.2.

Table 2.2: Working States and Operating Modes of 5-Level MMC Output Modules

Time Period	1	2	3	4	5	6	7	8
AC Output Voltage	0	$U_{dc}/4$	$U_{dc}/2$	$U_{dc}/4$	0	$-U_{dc}/4$	$-U_{dc}/2$	$-U_{dc}/4$
Upper Arm SMs	2	1	0	1	2	3	4	3
Lower Arm SMs	2	3	4	3	2	1	0	1
Total SMs per Phase	4	4	4	4	4	4	4	4
DC Voltage	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc}

The more submodules are used in each arm, the more voltage levels can be generated, resulting in a waveform that more closely approximates a sine wave. This reduces the harmonic content in the output voltage and current, improving power quality.

2.2 Mathmatical modle of MMC

2.3 Control of MMC

2.4 Modeling of DAB

2.5 Control of DAB

CHAPTER 3

Research on Modulation and Control Optimization of MMC-SST

3.1 Modeling of Single Stage AC-AC MMC

3.2 Control of Single Stage AC-AC MMC

3.3 Pulse Amplitude Control (PAC) for MMC-SST

3.4 Proposed Modulation and Control Optimization Methods for MMC-SST

CHAPTER 4

Simulation and Verification

CHAPTER 5

Conclusion

An example for conclusion chapter.

5.1 Summary

The goals of this work were

1. to find solutions to reduce the calculation effort for FS-MPC methods,
2. to increase the time resolution of FS-MPC methods in order to reduce ripples on the controlled variables and
3. a combination of the two last points, i.e. to find methods to reduce ripples on the controlled variables with less calculation effort.

Within this work solutions for all three items have been proposed and were proven experimentally.

It was also verified that FS-MPC methods offer several advantages over conventional PID controllers:

1. Multivariable control is easily possible (control of two currents, both flux and torque, and also the voltage balancing can be performed by one single FS-MPC controller).
2. Constraints can be considered without problems and nonlinearities can also be included.
3. FS-MPC controllers can easily operate the system at its physical limits. Conventional controllers mostly need additional (adaptive) schemes and feed forward controllers to achieve the same or similar dynamics.
4. FS-MPC controllers do normally not produce an overshoot which is usual for conventional controllers.

5.2 Final evaluation

As already mentioned, the applicability of direct switching strategies is highly dependent on the power range of the system: For medium- and high-voltage systems the system losses are dominated by the inverter switching losses. In this case switching frequencies of only a few hundred Hz per device are desired. For that reason industrial applications of FS-MPC methods have been reported mainly for high-power systems (MPDTC which was developed by ABB). Compared to classical DTC, MPDTC can lead to a further reduction of the switching frequency while maintaining at the same time the same quality of the control result. Sophisticated FS-MPC methods can partly even outperform Optimized Pulse Patterns for these types of drive systems [1].

In contrast to this, the presented work deals with low-voltage and smaller systems which are in the range of a few kW. For these applications a good quality of the controlled variables is usually much more important than a low switching frequency as in this case the inverter losses are less dominant. For these applications switching frequencies of 10–$20\,\mathrm{kHz}$ per device can be easily handled. The conventional FS-MPC approach only allows to change an inverter switching state at the *beginning* of a sample which is the reason for undesired high ripples. Another very important drawback of FS-MPC is the high calculation effort which rises exponentially with the prediction horizon. Thus, in this work several extensions to FS-MPC in order to reduce the calculation effort and to reduce ripples on the controlled variables were presented. As the shown experimental results clearly verify, the proposed extensions can effectively reduce these two drawbacks of FS-MPC methods. These extensions could even be successfully implemented for more sophisticated inverter topologies (three-level NPC and FC) where several tasks have to be performed by one single FS-MPC (e.g. control of two currents and three FC voltages). Even despite the high number of possible switching states (27 for an NPC and 64 for an FC inverter), up to three prediction steps could be realized in real-time with sampling rates up to $16\,\mathrm{kHz}$. For the proposed methods only one or two weighting factors have to be tuned (if any at all). Compared to linear controllers where parameter tuning is a work-intensive and crucial task, the proposed algorithms just need to be implemented and the weighting factors can be tuned quickly.

Although the methods presented within this work can enable FS-MPC strategies to become more attractive also for smaller and low-power (drive) systems, it is still questionable whether FS-MPC can outperform PWM-based MPC methods: For continuous-valued optimization tasks and linear systems the optimization problem can be solved analytically (e.g. with the MPT toolbox) which drastically reduces the calculation effort. PWM distributes the switching time points over the whole sample which leads to excellent control results in terms of ripples. Compared to the calculation of a VSP or to the implementation of an oversampled FS-MPC in hardware, the basic idea of PWM is ingeniously simple and has been proven to work well within the last decades. For multilevel inverters it is also possible to include a voltage balancing algorithm into the PWM which means that the overlaying controller only needs to calculate the voltages which should be applied—then it is not necessary to handle the voltage balancing within the control algorithm itself. Another drawback of FS-MPC is the varying switching frequency: Compared to PWM, FS-MPC methods produce an undesired audible noise which is much more annoying than the sound of PWM. Of course, it is also possible to modify the cost function such that a more or less constant switching frequency per device can be obtained. However, this can only be achieved at the expense of a deteriorated result regarding the main control objective (to mini-

mize the control deviation). Thus, in order to achieve the same control result in terms of ripples as without forcing a constant switching frequency, the sampling frequency and with it the time resolution of FS-MPC has to be drastically increased.

5.3 Outlook

There are several possibilities to extend and to modify the strategies which were presented in this work: One promising extension could be a method to calculate not only one but two or even more VSPs. If e.g. only one IGBT is allowed to switch at a time and if two VSPs are calculated within one sample, "online optimized" pulse patterns and a constant switching frequency could be obtained. Such an FS-MPC method would then be fully comparable to PWM in terms of ripples on the controlled variables. Another possibility would also be to increase the prediction horizon for VSP methods.

Another very promising application for (FS-)MPC is to perform direct speed or even position control for electrical drives. In this way all disadvantages which result from cascaded control loops could be overcome. Furthermore, it would then also be possible to operate the drive at its physical limits while still keeping all controlled variables within their allowed range.

APPENDIX A

List of symbols and abbreviations

A.1 List of symbols

General remark:
The following convention was used for variables:

Scalars are italic letters:	x
Vectors are bold lower case letters:	$\boldsymbol{x}$
Matrices are bold upper case letters:	$\boldsymbol{X}$
References are marked with a star superscript:	x^*

Used symbols:
In the following the most important symbols are listed which are used within this work.

General symbols:

$\boldsymbol{x}$	State vector
$\boldsymbol{u}$	Input vector
$\boldsymbol{y}$	Output vector
$\boldsymbol{A}$	State matrix
$\boldsymbol{B}$	Input matrix
$\boldsymbol{C}$	Output matrix
$\boldsymbol{D}$	Feedthrough matrix
t	Time (continuous)
k	Time (discrete, current sample)
$\frac{\mathrm{d}}{\mathrm{d}t}$	Time derivation
T_s	Sampling time
t_sw	Variable switching time point (VSP)
Δ	Difference
J	Inertia

General electrical variables:

a, b, c	Phases
α, β	Equivalent two-phase coordinates
j	$\sqrt{-1}$
v	Voltage
i	Current
R	Resistor
C	Capacitor
L	Inductor

Induction machine parameters:

$\boldsymbol{v}_\mathrm{s}$, $\boldsymbol{v}_\mathrm{r}$	Stator and rotor voltage
$\boldsymbol{i}_\mathrm{s}$, $\boldsymbol{i}_\mathrm{r}$	Stator and rotor current
$\boldsymbol{\psi}_\mathrm{s}$, $\boldsymbol{\psi}_\mathrm{r}$	Stator and rotor flux
ω_m	Mechanical machine speed
ω_el	Electrical machine speed
T_m	Mechanical machine torque
T_l	Mechanical load torque
P	Machine power
p	Number of pole pairs
R_s, R_r	Stator and rotor resistance
L_s, L_r	Stator and rotor inductance
L_m	Mutual inductance

Further variables and parameters:

S_{xi}	Switch i in phase x
s_{xi}	Gating signal for switch i in phase x
j	Cost function value
w	Weighting factor
v_o, i_o	Inverter output voltage and current (UPS)
v_l, i_l	LC lowpass-filter output voltage and current (UPS)

A.2 List of abbreviations

AC	Alternating Current
AD	Analog to Digital (converter)
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
DA	Digital to Analog (converter)
DC	Direct Current
DMTC	Direct Mean Torque Control
DSC	Direct Self Control
DSP	Digital Signal Processor
DTC	Direct Torque Control
EMI	Electromagnetic Interference
FC	Flying Capacitor
FIFO	First In First Out (buffer)
FOC	Field Oriented Control
FPGA	Field Programmable Gate Array
FS	Finite-Set
FS-MPC	Finite-Set Model Predictive Control
GPC	Generalized Predictive Control
HDL	Hardware Description Language
IGBT	Insulated Gate Bipolar Transistor
IM	Induction Machine, Induction Motor
ISA	Industry Standard Architecture (bus)
LCD	Liquid Crystal Display
LP	Linear Program
LTI	Linear Time-Invariant
MILP	Mixed Integer Linear Program
MIQP	Mixed Integer Quadratic Program
MPC	Model Predictive Control
MPDTC	Model Predictive Direct Torque Control
mpLP	Multiparametric Linear Program
mpQP	Multiparametric Quadratic Program
MPT	Multiparametric Toolbox
NP	Neutral Point
NPC	Neutral Point Clamped
PCC	Predictive Current Control
PTC	Predictive Torque Control
PWM	Pulse Width Modulation
QP	Quadratic Program
RAM	Random Access Memory
RMS	Root Mean Square
RPM	Revolutions Per Minute
RTAI	Real-Time Application Interface

SI	International System of Units
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VSP	Variable Switching Point
VSP2CC	Variable Switching Point Predictive Current Control
VSP2TC	Variable Switching Point Predictive Torque Control

APPENDIX B

Test bench data

B.1 Two-level inverter test bench

A quick overview of the two-level inverter test bench has already been given in chapter X. The complete test bench consists of a real-time computer system, two squirrel-cage induction motors, two two-level inverters and measurement devices. It is to be noted that for this test bench no DC link voltage measurement is possible.

B.1.1 Real-time computer system

The real-time computer system consists of a PC104 module with a 1.4 GHz Pentium M CPU, 1 GB RAM and a 60 GB hard disk. All components are mounted into a 19 inch rack. The system is running an Arch Linux distribution with an RTAI (real-time application interface) kernel patch. This RTAI kernel patch allows to program kernel modules which can be executed in real-time. The real-time control algorithm can be conveniently programmed in *C*.

The necessary peripheral hardware for analog and digital in- and outputs is connected via the 16 bit ISA bus. The used 19 inch rack has space for up to twelve extension boards. In order to measure the signal from the current transducers, an AD card with two channels is used. The encoder signal can be read via a special encoder board. The most important extension card is responsible for the inverter gating (PWM) signals: In order to synchronize the generation of these gating signals with the control algorithm which is running on the real-time computer, this card also generates an interrupt for the real-time computer. Every time when such an interrupt occurs, the control algorithm is executed. Thus, the whole control algorithm is triggered by this extension card. As this board contains an FPGA, it is possible to modify the existing implementations for the generation of the gating signals according to the user's needs. The current implementation allows of course the generation of PWM signals but direct switching and switching at a VSP is also possible. Furthermore, the interrupt for the control algorithm also triggers the measurements of the AD converters such that it is possible to trigger the measure-

ments at the beginning of a sample. In order to conveniently output measured values, DA cards can be inserted into the system as well: Then, variables can be easily visualized and recorded with an oscilloscope. Another extension board with a four digit hexadecimal (16 bit) display and four hexadecimal switches can be used for status notifications and user interaction (start and stop of the control algorithm, reference value changes etc.). Further information about this system can be found in [2].

B.1.2 Inverters

As already mentioned, the test bench consists of two inverters. Both inverters are supplied from a three-phase voltage source with an RMS phase to phase voltage of $400\,\mathrm{V}$. Since the inverters cannot feed back energy to the three-phase grid, the DC link voltage will rise if a connected machine is operated in generator mode. In order to avoid damages of the system, a break chopper resistor can be connected to discharge the DC link such that the voltage level does not become critical. Since both machines are connected to each other, one drive is normally operated as motor while the other one works as generator. Thus, in order to avoid a frequent use of the break chopper resistor, the DC links of both drives are coupled together.

The controlled inverter is a modified Seidel/Kollmorgen Servostar 600 $14\,\mathrm{kVA}$ inverter. It allows the user to directly command the IGBT gating signals from the real-time computer system. This inverter is connected to the working machine which is also controlled by the user. Consequently, the load inverter (Danfoss VLT FC-302 $3.0\,\mathrm{kW}$) is connected to the load machine. This inverter allows to perform speed and torque control of different machines. Furthermore, it can also be used to measure machine parameters.

B.1.3 Induction machines

Table B.1: Parameters for the working machine of the two-level inverter test bench

Parameter	Value
Nominal power P_{nom}	$2.2\,\mathrm{kW}$
Synchronous frequency f_{syn}	$50\,\mathrm{Hz}$
Nominal current $\lvert\boldsymbol{i}_{\mathrm{s,\,nom}}\rvert$	$8.02\,\mathrm{A}$
Power factor $\cos(\varphi)$	0.85
Nominal speed ω_{nom}	$2772\,\mathrm{rpm}$
Number of pole pairs p	1
Stator resistance R_{s}	$2.6827\,\Omega$
Rotor resistance R_{r}	$2.1290\,\Omega$
Stator inductance L_{s}	$283.4\,\mathrm{mH}$
Rotor inductance L_{r}	$283.4\,\mathrm{mH}$
Mutual inductance L_{m}	$275.1\,\mathrm{mH}$
Inertia J	$0.005\,\mathrm{kg\,m^2}$

The two-level inverter test bench consists of two $2.2\,\mathrm{kW}$ squirrel-cage induction machines which are coupled to each other. The parameters of the working machine (driven by the controlled inverter) are given in Table B.1. The load machine is completeley operated by the load inverter and hence, its parameters are not shown. The parameters were measured with the Danfoss load inverter. On both machines incremental encoders with 1024 points are mounted.

B.2 FPGA-based test bench

In chapter X a quick overview of the FPGA-based test bench has already been given. It consists of the FPGA board which is shown in Figure X. The FPGA board is connected to an optics board which allows to transmit the IGBT gating signals optically to the inverter. Furthermore, one current measurement board and one board for voltage measurements are connected to the FPGA board. The two-phase three-level inverter just consists of two phase legs.

B.2.1 FPGA board

The FPGA board which is shown in Figure X is used for the real-time computer system for the three-level inverter test bench. As the board uses an Altera Cyclone III FPGA with $40{,}000$ logic elements, it is also possible to directly implement control algorithms on the FPGA which is clocked with $20\,\mathrm{MHz}$. The board also has a very fast 12 bit AD converter. It allows to measure all eight different channels simultaneously with up to 65 megasamples per second. Because of this it is also possible to implement highly oversampled control algorithms and safety routines. The measurement boards can be connected to the FPGA board with RJ45 plugs. In order to deliver good measurement results and in order to have less EMI sensitivity, analog differential signalling is used for the measurements.

B.2.2 Two-leg three-level inverter

As already mentioned, the two-leg three-level inverter uses the same design as the version with three phase legs. Another difference is that in this case the complete DC link capacitance is $500\,\mu\mathrm{F}$ and the two flying capacitors both have a size of $500\,\mu\mathrm{F}$, too. For this inverter also a $12\,\mathrm{V}$ power supply is used for the optical interface for the gating signals and to provide auxiliary voltages for the gate drivers.

B.2.3 Loads

As mentioned in chapter X, experimental results were conducted with a resistive-inductive load and for a UPS application. The loads were simply made of discrete components (resistors, inductors, capacitors and diodes for the nonlinear load in UPS configuration).

List of Figures

List of Tables

Bibliography

[1] T. Geyer, "A comparison of control and modulation schemes for medium-voltage drives: Emerging predictive control concepts versus PWM-based schemes," *IEEE Transactions on Industry Applications*, vol. 47, no. 3, pp. 1380–1389, May 2011.

[2] N. A. Ameen, A. A. Naassani, and R. Kennel, "Design of a digital system dedicated for electrical drive applications," *EPE Journal*, vol. 20, no. 4, pp. 37–44, Dec. 2010.