lab4实验报告

截图

```
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Test m_trap [OK]
Privileged test finished.
Exit with code = 0
```

流水线改动

harzard:新增mreW，检测w阶段产生的异常、终端、mret。刷新流水线。
异常改变ireq：在core中新增寄存器存储新地址，在i_wait结束后，新地址从寄存器进入pcreg。
指令地址未对齐：在ireq处进行判断，在fetch模块中增加异常信号的输入。
在每阶段data中增加csr_ctl，存储异常中断相关数据：code，类型，zimm， rs1寄存器数据等。
异常和中断的检测：fetch阶段pc地址未对齐，memory阶段内存地址未对齐，decode阶段ecall、mret和csr指令，writeback阶段中断。
异常和中断的执行：writeback阶段：维护mode寄存器。csr.sv中分情况写入csr寄存器。
中断的异步：csr.sv中，根据流水线是否有阻塞的输入信号，选择是否将中断写入相关的数据写到另外的寄存器中保存，等到inter_valid为1后再执行中断操作。