Exercise 6:

a) Generation Of Synchronisation Pulses For The Monitor

Driving a monitor with synchronisation pulses originates from the time when cathode-ray-tube (CRT) displays were the standard display type for computers. In these monitors an electron beam forces the phosphorous coating on the inside of the front of the screen to emit visible light.

This electron beam moves from left to right and top to bottom. When the beam reaches the right or bottom end of the screen, the corresponding synchronisation impulse (horizontal or vertical) forces the monitor to retrace the electron beam to its starting position as shown in figure 1.

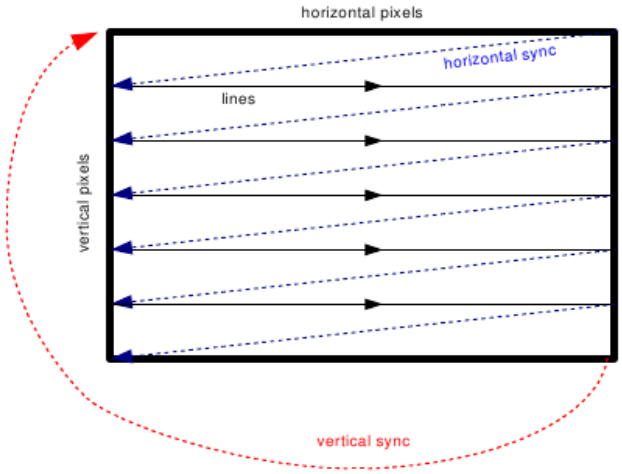

Figure 1: Vertical and horizontal synchronization pulse

During the time the beam requires to move back, no image data can be displayed. All other signals required by the monitor are derived from these two synchronisation signals, so it is important that their timing is correct (although modern monitors tend to be more flexible in handling non-standard timings than older ones).
The timing conditions and the generics for the sync pulse are given in the waveform in figure 2. As you can see, a front and a back porch have to be considered along with the sync pulse and the visible area (for the horizontal and for the vertical sync pulse).

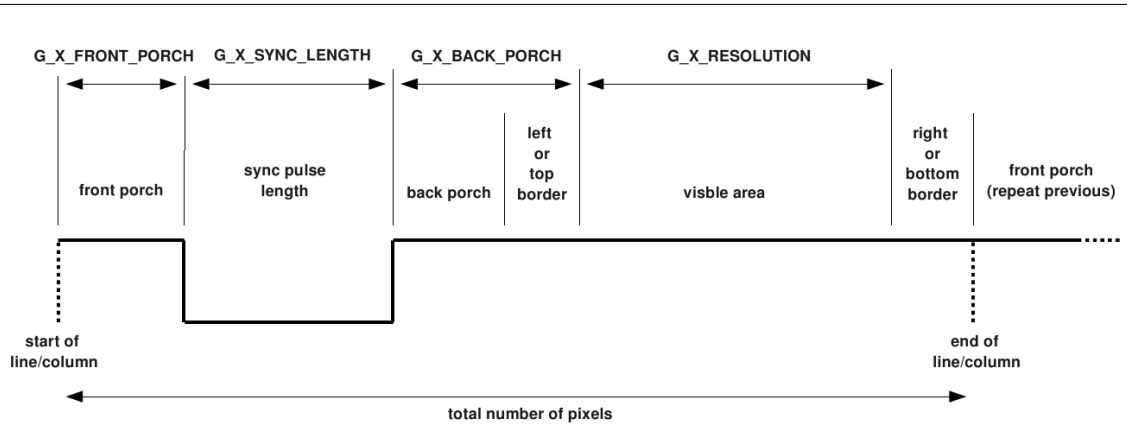

Figure 2: Timing conditions for the vertical and horizontal sync pulse

Your task will be to implement a synchronisation pulse generator in VHDL that functions properly for for different resolutions and refresh frequencies (although only 640x480 at a 60 Hz refresh rate will be used in the final project).

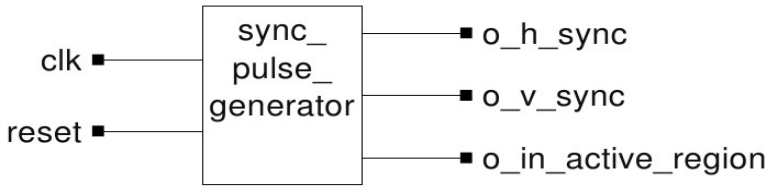

Figure 3: sync_pulse_generator

Port declaration:

- *clk* : in std_logic
- *reset* : in std_logic
- *o_h_sync* : out std_logic
- *o_v_sync* : out std_logic
- *o_in_active_region* : out std_logic

To realize a sync pulse generator which works for different resolutions and refresh frequencies, we will use generics. Generics are used to parametrize modules and can be written hierarchically (using a generic map described in Exercise 2). Therefore, you will perform calculations using only these generics instead of the values we need for our specific monitor. Afterwards, these generics will be defined in another module. Nevertheless, you can find the values required on the next page.

List of generics:

- *G_H_PIXEL_NUMBER* : horizontal pixel number (incl. non visible)
- *G_H_RESOLUTION* : visible horizontal resolution
- *G_H_FRONT_PORCH* : horizontal front porch length in pixels
- *G_H_BACK_PORCH* : horizontal back porch length in pixels
- *G_H_SYNC_LENGTH* : horizontal sync pulse length in pixels
- *G_H_SYNC_ACTIVE* : horizontal sync pulse polarity (1 = pos, 0 = neg)
- each of the above generics exist with a leading '*G_V*' instead of '*G_H*' for their vertical counterparts, too.

Generic declaration:
All generics are of type integer, except *G_H_SYNC_ACTIVE* and *G_V_SYNC_ACTIVE*, which are of type std_logic.

The output for horizontal synchronisation pulses is *o_h_sync*, *o_v_sync* for the vertical pulses. Additionally, the output *o_in_active_region* should be active ('1') when the electron beam is in the area where the picture is displayed on the screen.
In order to make the time between two impulses measurable, the synchronisation pulse generator (and the whole block *graphic_output*) is fed with a different clock signal than the rest of the circuit. It has a cycle length that represents the time required by the electron beam to display one pixel on the screen. All times needed are multiples of this pixel clock cycle length and and can thus be measured by a simple counter.

To ensure that all PC monitors work with all computers the VESA (Video Electronics Standards Association[1]) specifies the signal timings. In this lab the display should run at a 640x480 resolution with a refresh frequency of 60 Hz. The detailed timing data for this resolution is given in the manual[2] of the FPGA evaluation board used in this lab (a detailed list for most standard video modes can be found here[3]).

"VGA industry standard" 640x480 pixel mode

General characteristics

```
Clock frequency 25.175 MHz
Line  frequency 31469 Hz
Field frequency 59.94 Hz
```

One line

```
  8 pixels front porch
 96 pixels horizontal sync
 40 pixels back porch
  8 pixels left border
640 pixels video
  8 pixels right border
---
800 pixels total per line
```

One field

```
  2 lines front porch
  2 lines vertical sync
 25 lines back porch
  8 lines top border
480 lines video
  8 lines bottom border
---
525 lines total per field
```

Other details

```
Sync polarity: H negative, V negative
Scan type: non interlaced.
```

1 http://www.vesa.org
2 http://www.digilentinc.com/Data/Products/S3BOARD/S3BOARD-rm.pdf
3 http://www.epanorama.net/documents/pc/vga_timing.html